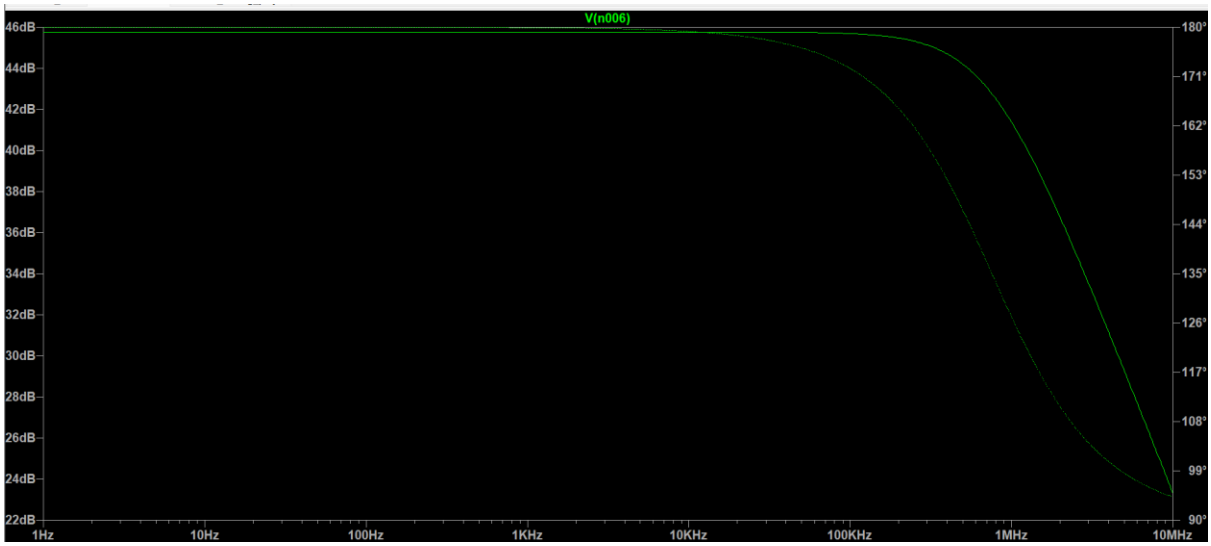
Objective: Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

Observations & Results:

- Design of Cascode Amplifier and Current Mirror in 180nm Technology (supply 1.8V):

  Gain: 45.8 dB

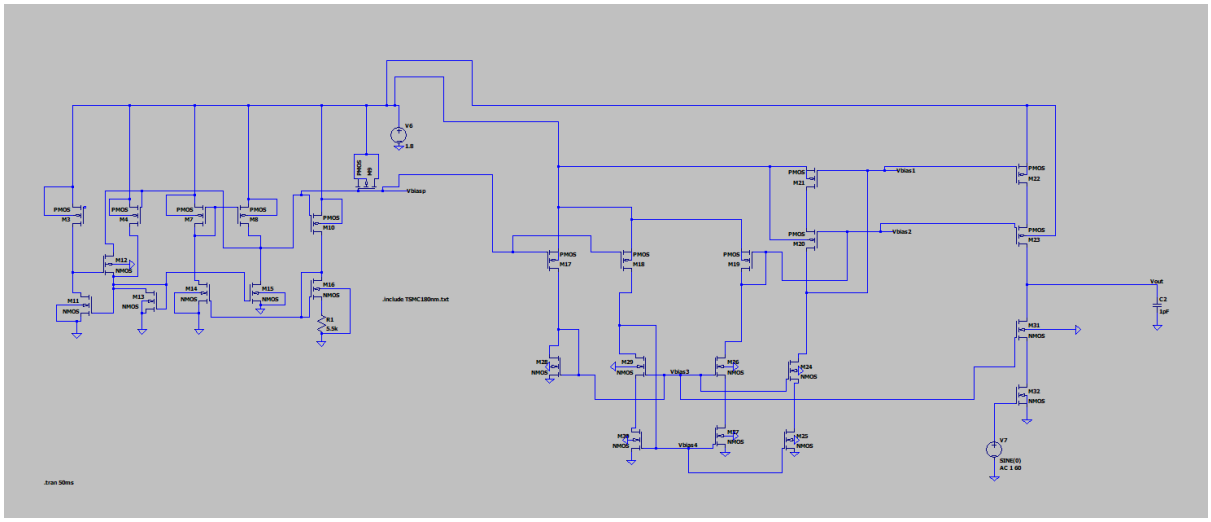


Id in the cascode amplifier= 191.2uA

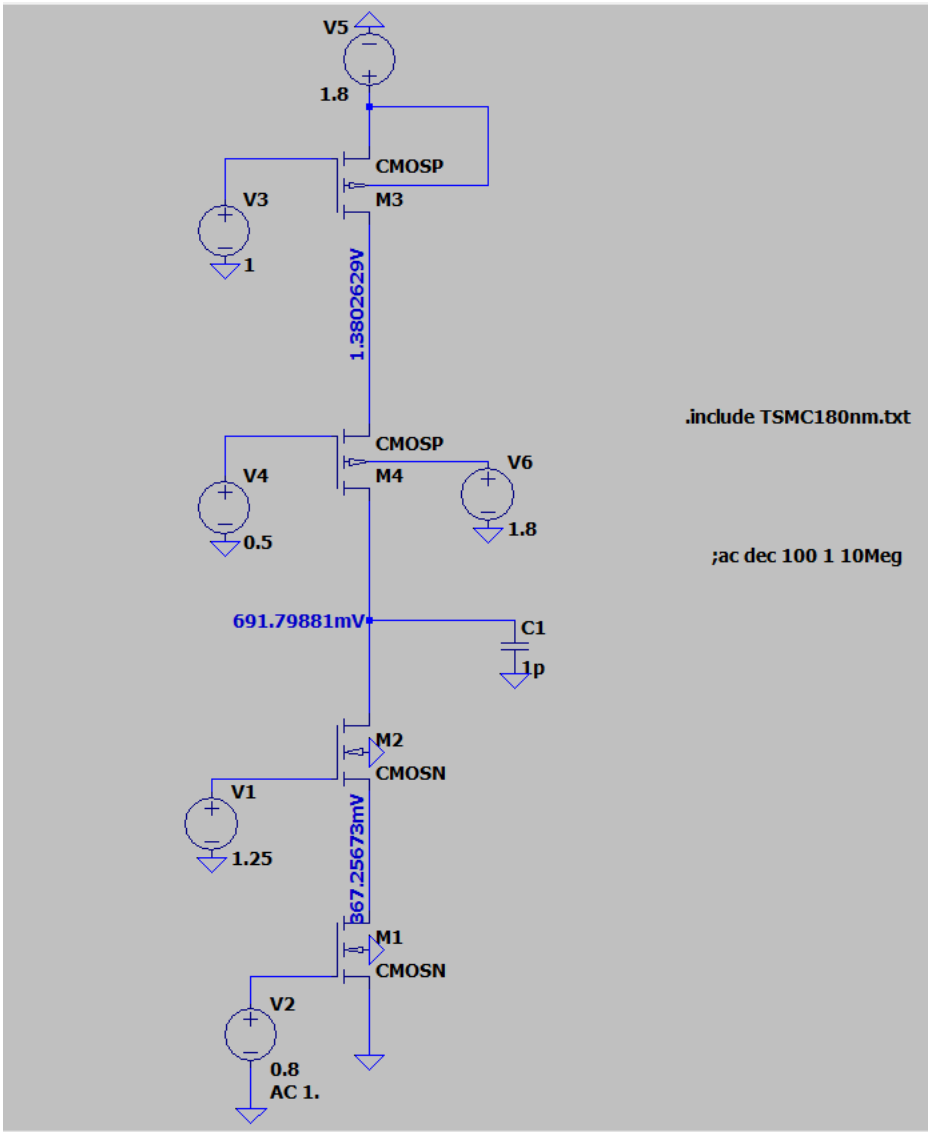
Power consumption in the circuit=0.344mW

Unity gain bandwidth>500kHz

Following is the simulation of the complete circuit in the LT Spice:



Following is the circuit diagram of the single stage Cascode Amplifer simulated in LT Spice:



Dimensions of the MOSFETs are :

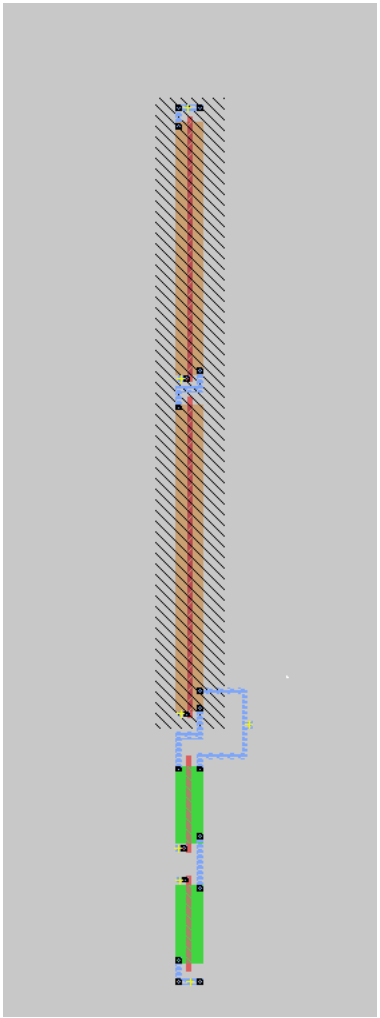
Bias Voltage for the MOSFETs:

MOSFET	Width	Length
M1:	5.04u	0.36u
M2:	5.4u	0.36u
M4:	21.6u	0.36u
M3:	17.82u	0.36u

To verify the MOSEFTs if they are in saturation or not following data was considered:

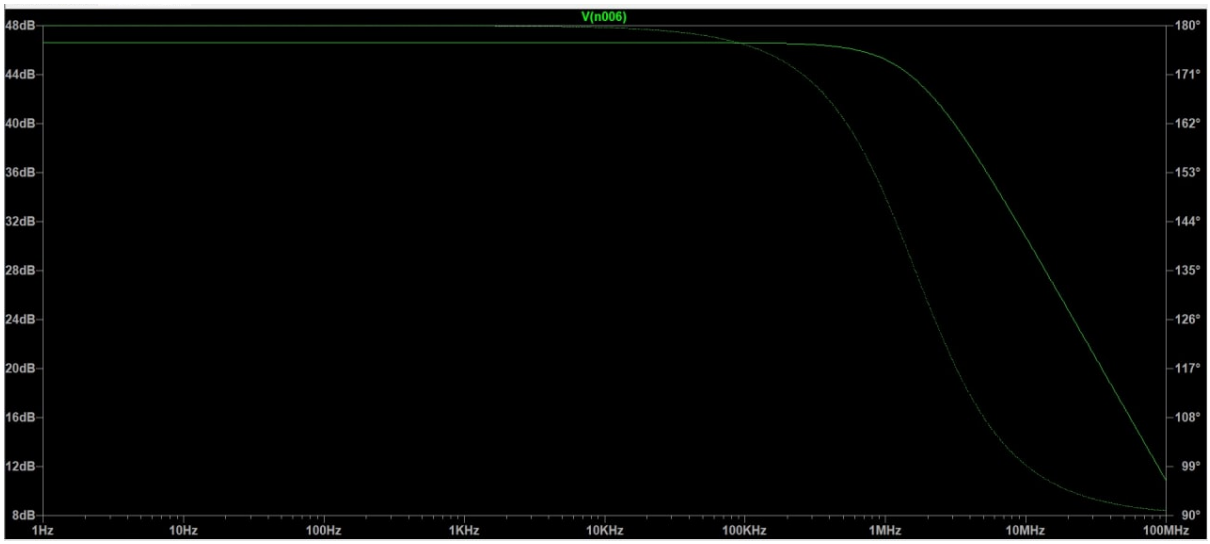
Model:	cmosp	cmosp	cmosn	cmosn
Id:	-1.91e-04	-1.91e-04	1.91e-04	1.91e-04
Vgs:	-8.80e-01	-8.00e-01	8.83e-01	8.00e-01
Vds:	-6.88e-01	-4.20e-01	3.25e-01	3.67e-01
Vbs:	4.20e-01	0.00e+00	-3.67e-01	0.00e+00
Vth:	-5.75e-01	-4.55e-01	5.66e-01	4.64e-01
Vdsat:	-2.56e-01	-2.69e-01	2.21e-01	2.20e-01

Circuit implemented in Magic:



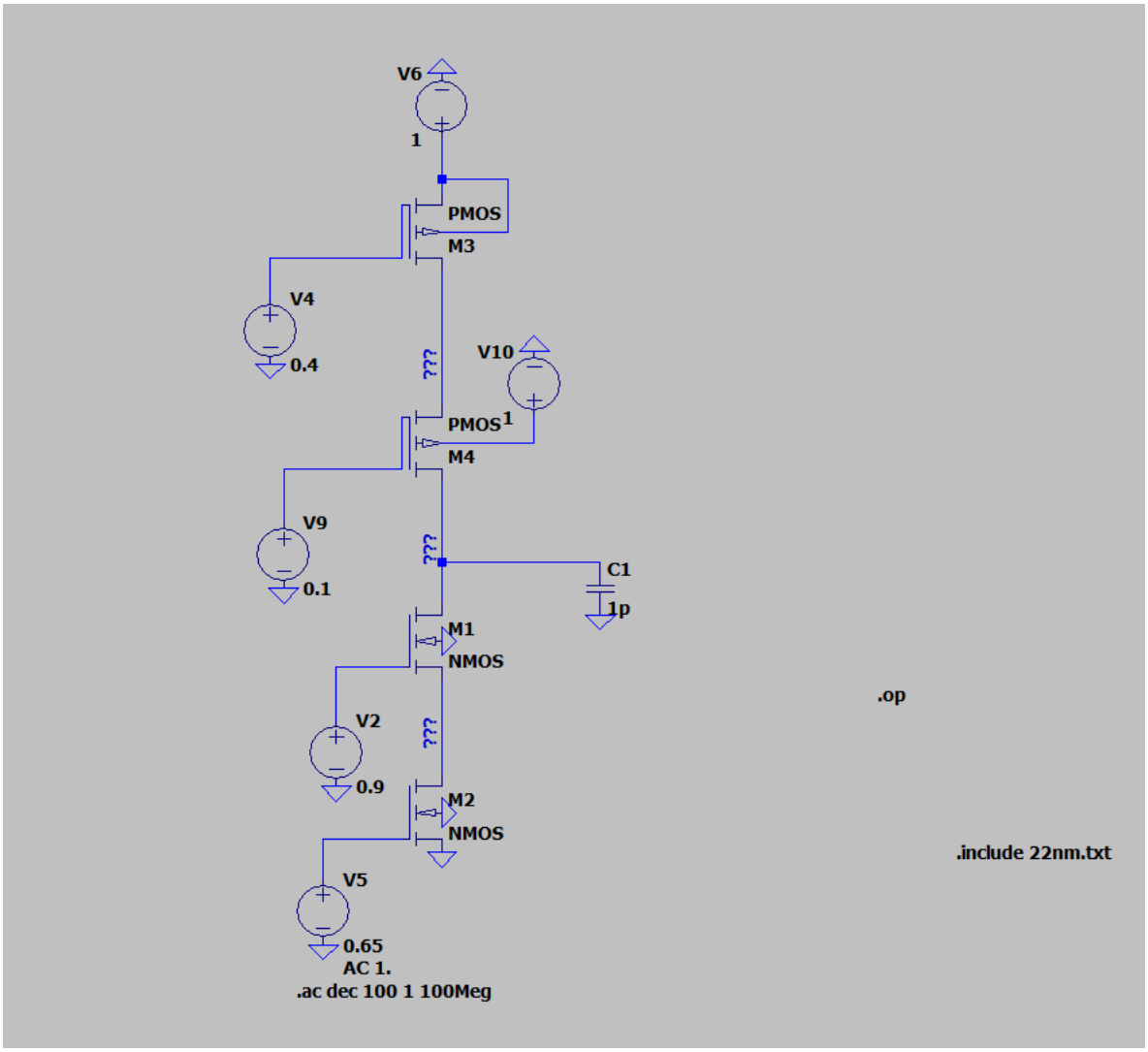
- Design of Cascode Amplifier in 22nm Technology (supply 1V):

Gain: 46 dB



Id in the Cascode amplifier = 262 uA.
Power Consumption in the circuit = 0.262 mW
Unity Gain Bandwidth > 500 KHz

Following is the circuit diagram of the single stage Cascode Amplifer simulated in LT Spice:



Conclusion:

We concluded that the Cascode Amplifier is a **low pass filter.**