**Course: ELL 782**

**Assignment: Design and Verification of SimpleRisc Processor**

**Submitted by: Akshat Mathur (2023EEN2223)**

1. **Reference Documents:**

Sarangi, S.R., 2021. *Basic Computer Architecture*. 1st ed. White Falcon Publishing. ISBN: 1636403034.

1. **Basic Overview**

This implementation of SimpleRisc processor is

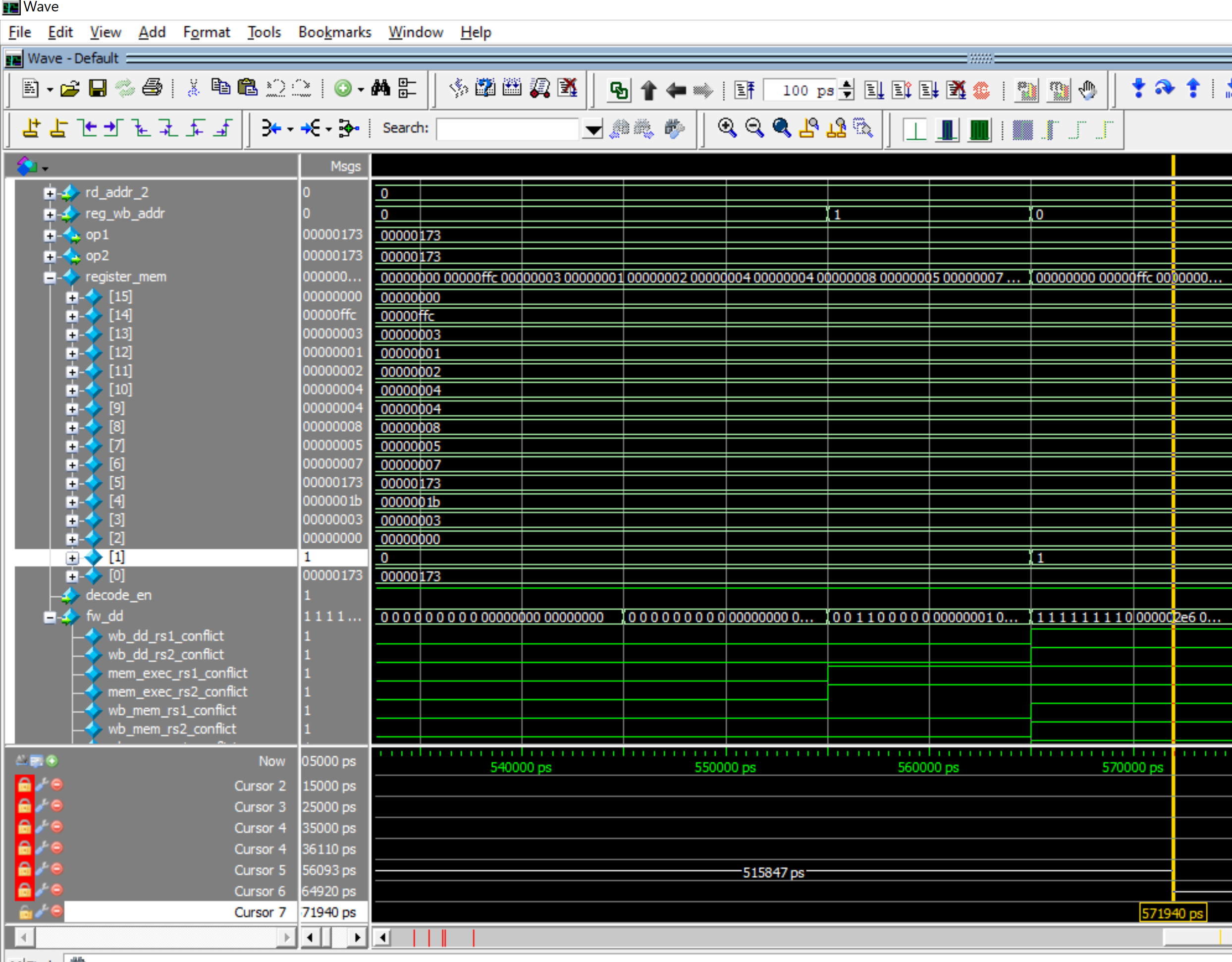
1. fully pipelined
2. interlocks
3. Forwarding.
4. Synthesized on Xilinx Virtex 7 technology using Xilinx Vivado.
5. **Modules**
   1. riscv\_params\_pkg.sv
   2. fetch\_unit.sv
   3. decode\_unit.sv
   4. control\_unit.sv
   5. register\_access.sv
   6. execute\_unit.sv
   7. memory\_access\_unit.sv
   8. register\_wb.sv
   9. forwarding\_unit.sv
   10. risc\_proc\_top.sv
   11. tb\_fde\_memory\_unit.sv
6. **Result screenshots**

Fig: Amrstrong.asm working with correct values in registers

A screenshot of a computer

Description automatically generated

Fig: factorial-rec.asm working with correct values

A screenshot of a computer

Description automatically generated

Fig: factorial.asm working with correct values

A screenshot of a computer

Description automatically generated

Fig: Post compile schematic

A screenshot of a computer

Description automatically generated

Fig: Post synth schematic