CS221: Digital Design

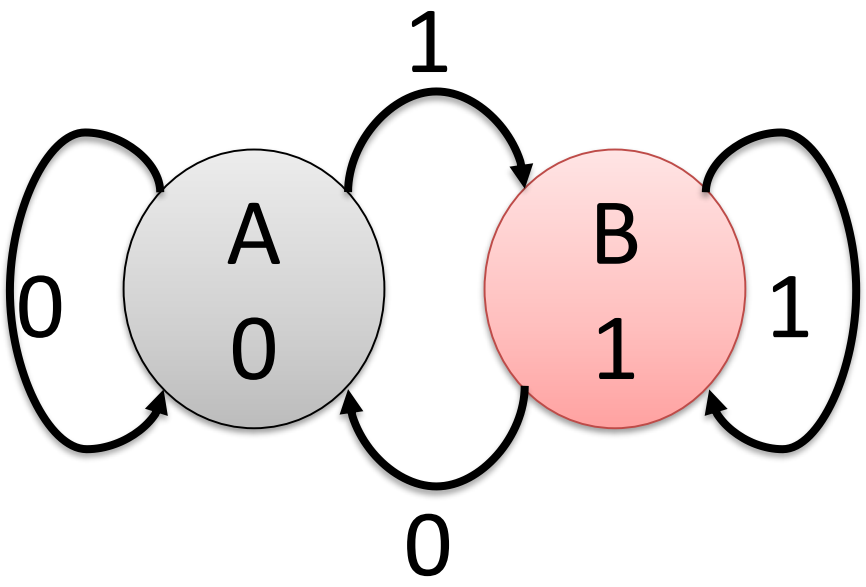
ASM/ FSMD/ RTL Design

A. Sahu

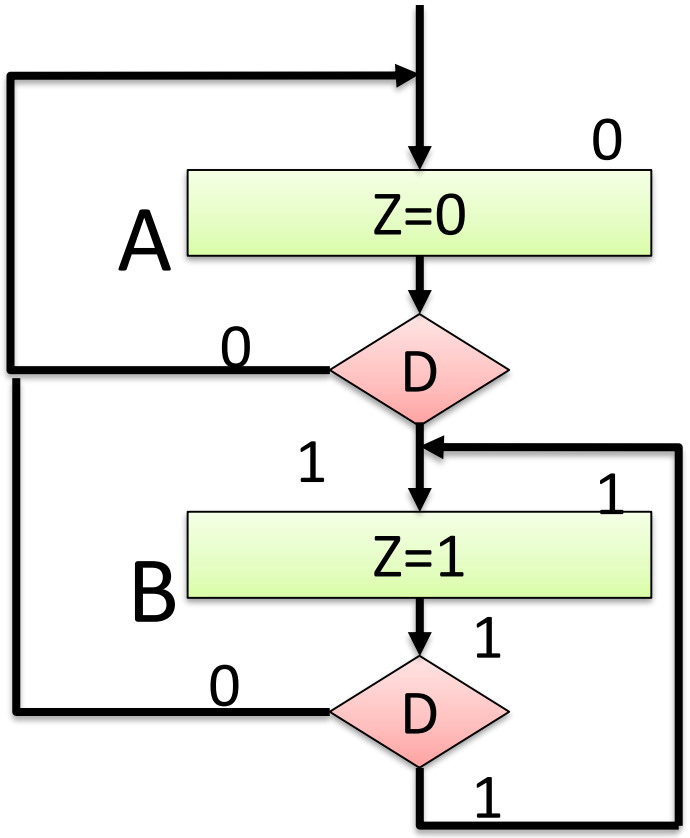
Dept of Comp. Sc. & Engg.

Indian Institute of Technology Guwahati

Example 1: Draw ASM of D-FF

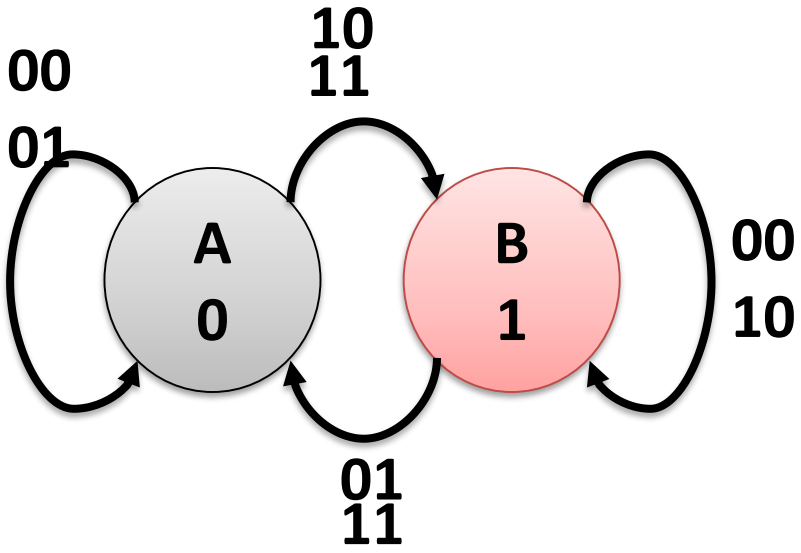


FSM

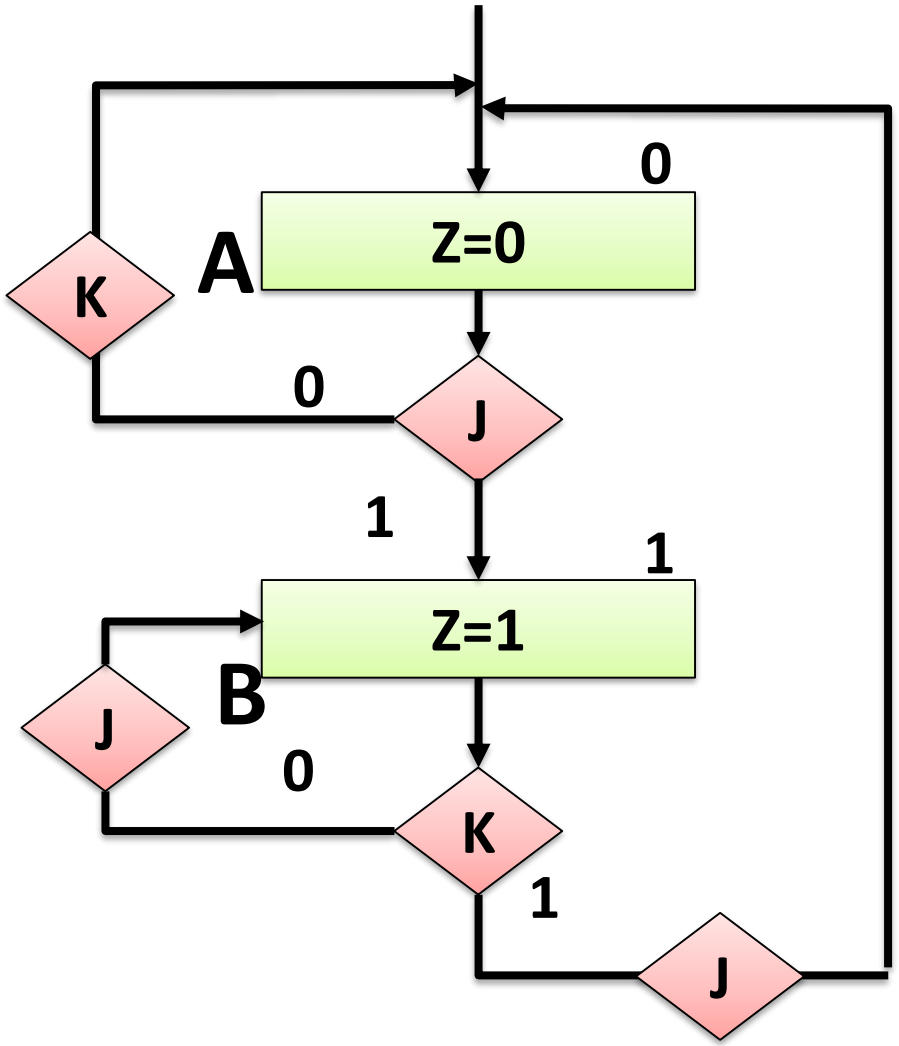


ASM

Example 2: Draw ASM of JK-FF



FSM



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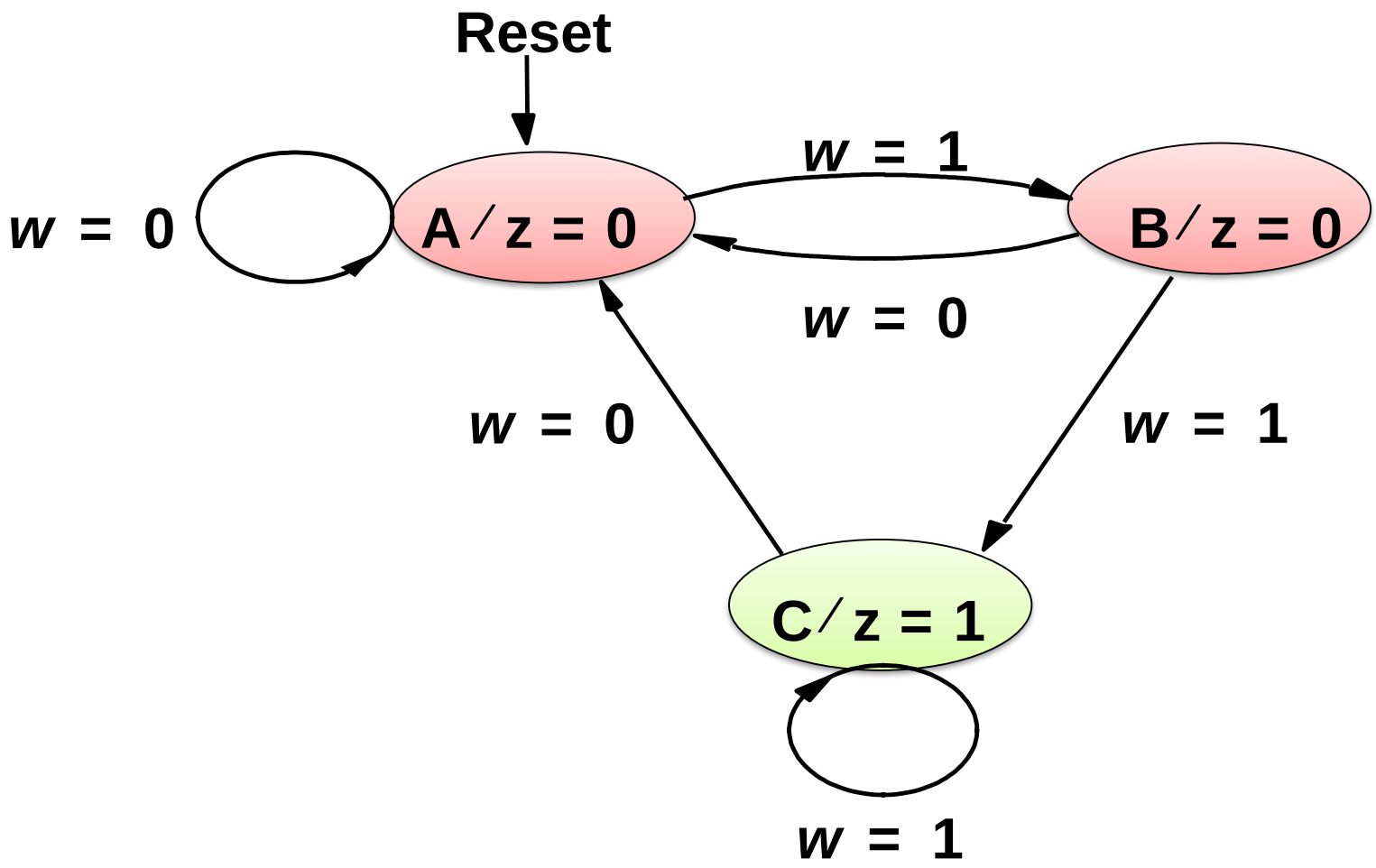
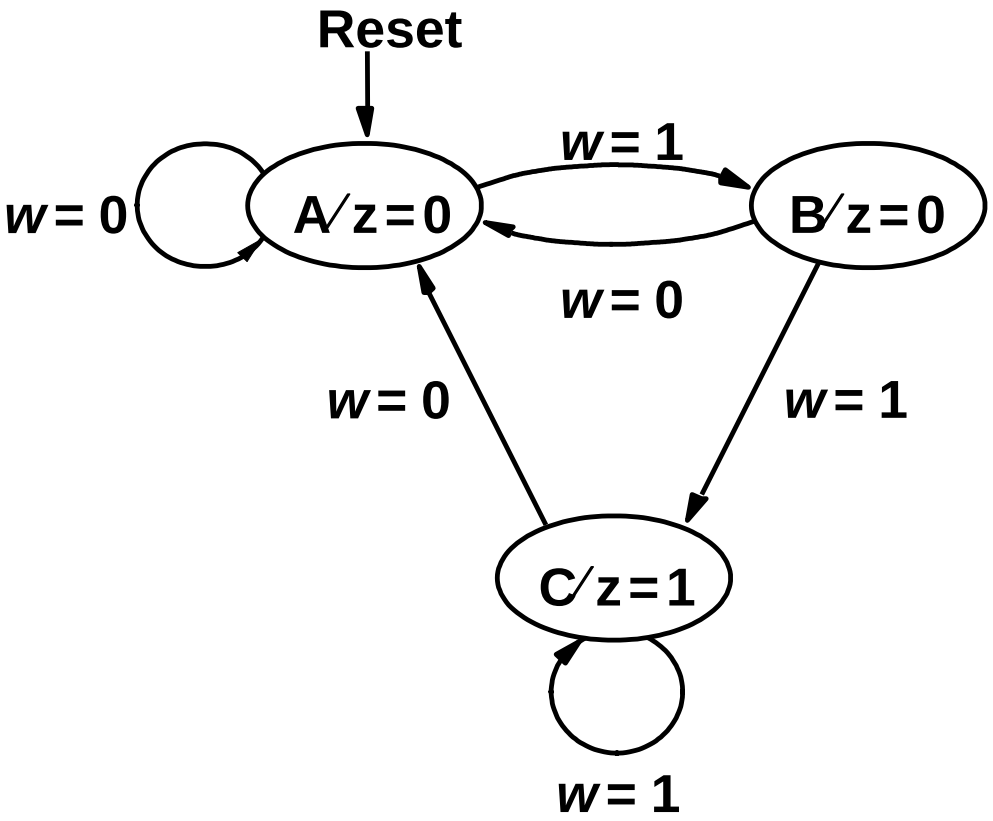
Moore FSM – Example 3: Sequence of two 1's



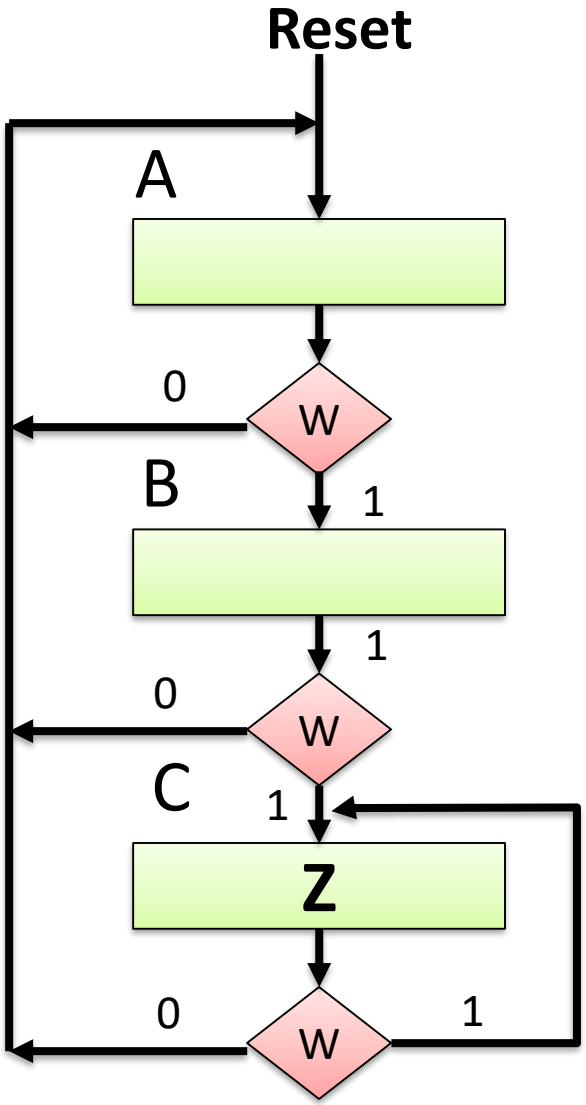
Moore FSM – Example 3: Sequence of two 1's

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	A	B	0
B	A	C	0
C	A	C	1

Example 3: ASM Chart for Moore FSM



FSM



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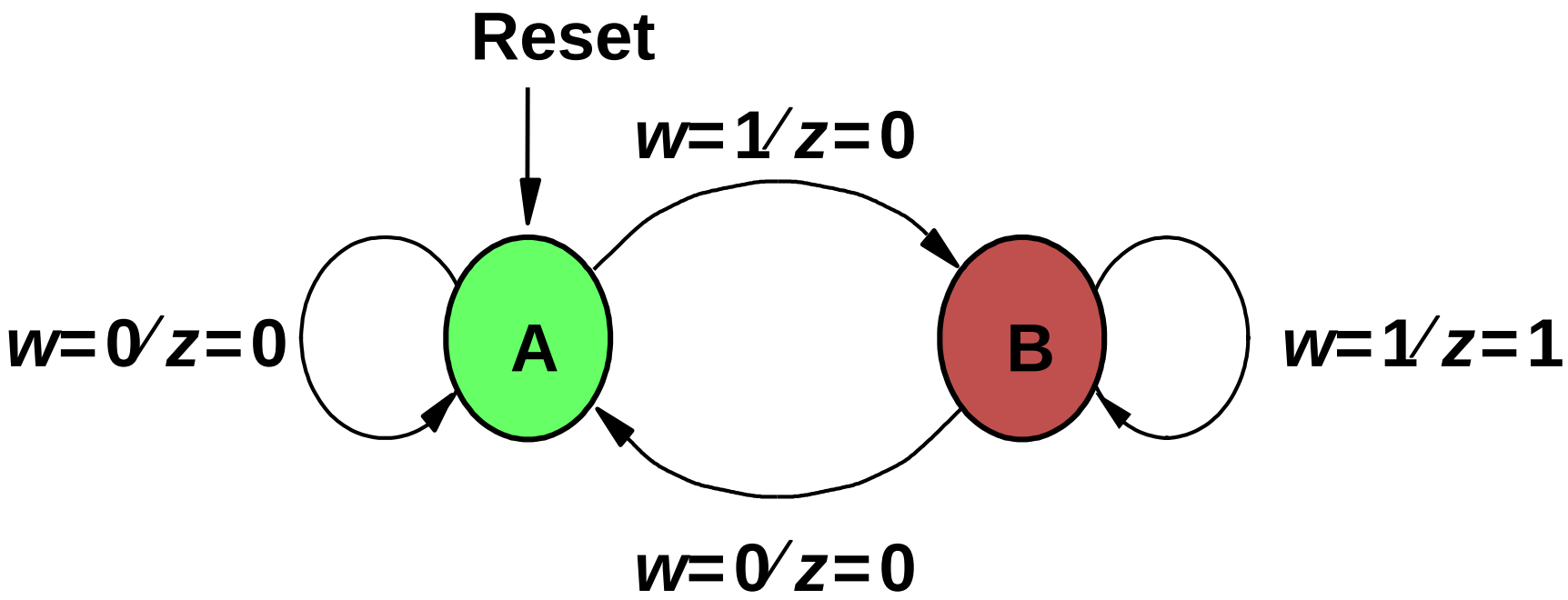
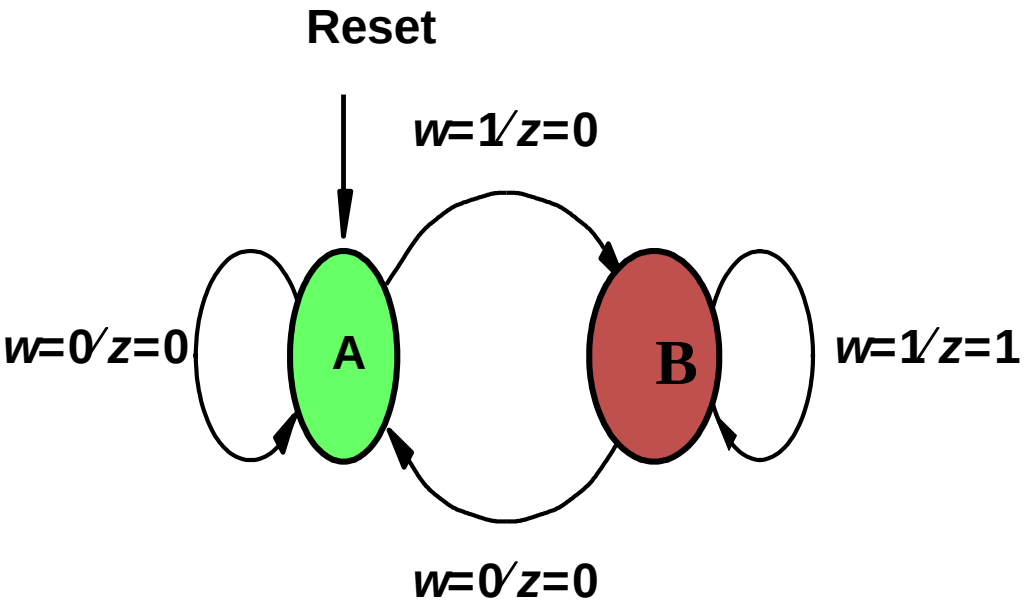
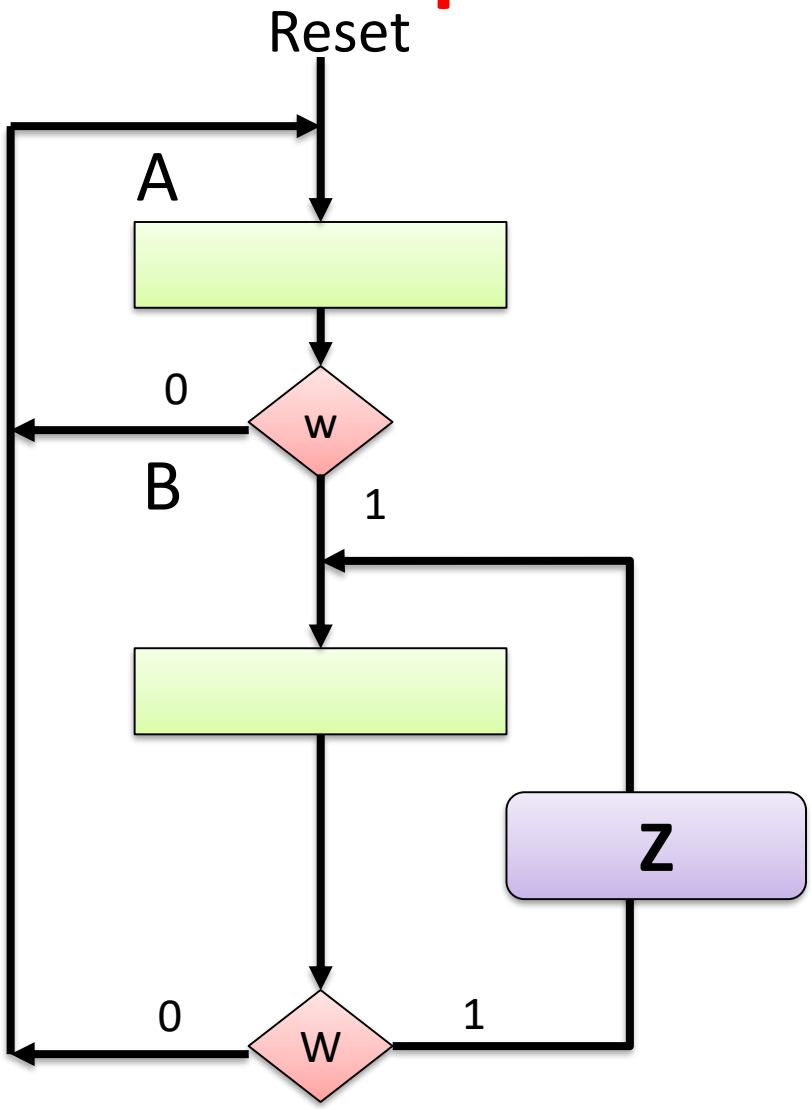
Mealy FSM –Example 4: Sequence of two 1's



ASM Chart for Mealy FSM – Example 4



FSM



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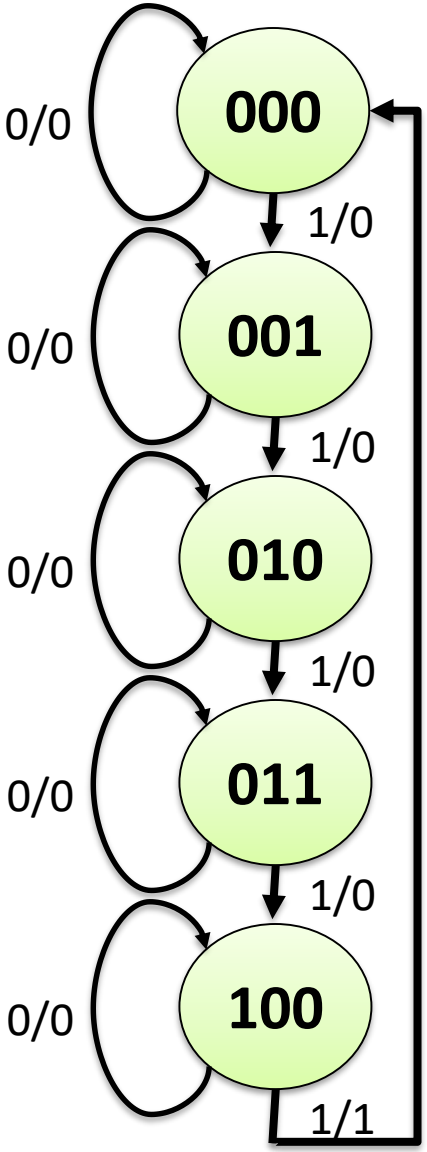
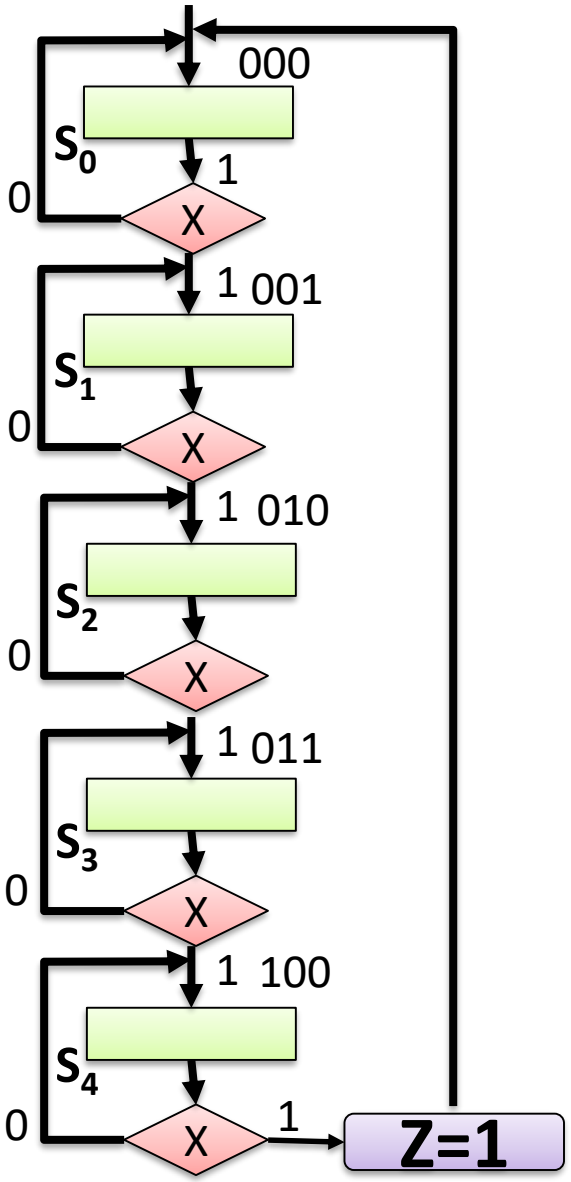
ASM Chart : Example 5, mod 5 counter



FSM



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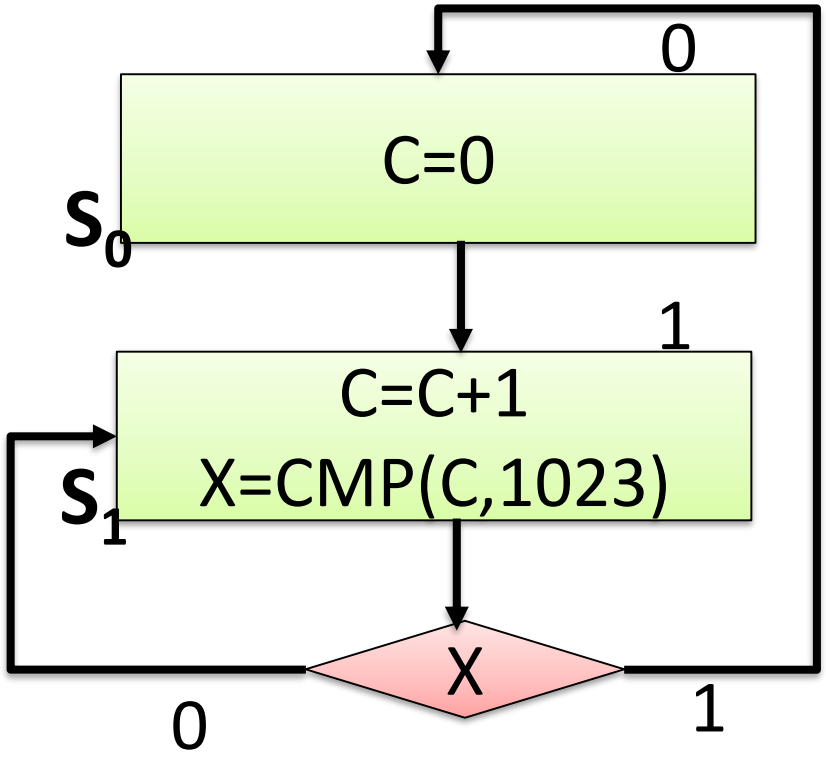
ASM Chart : Example 6: 10 bit counter



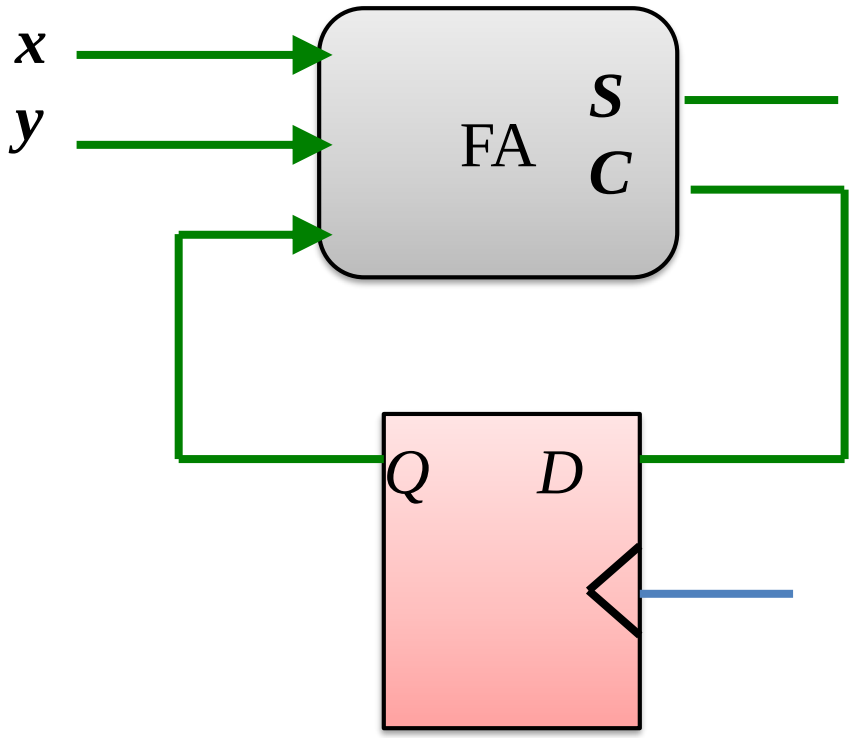
Require : addition, comparison data path

In state : We can put RTL like statement

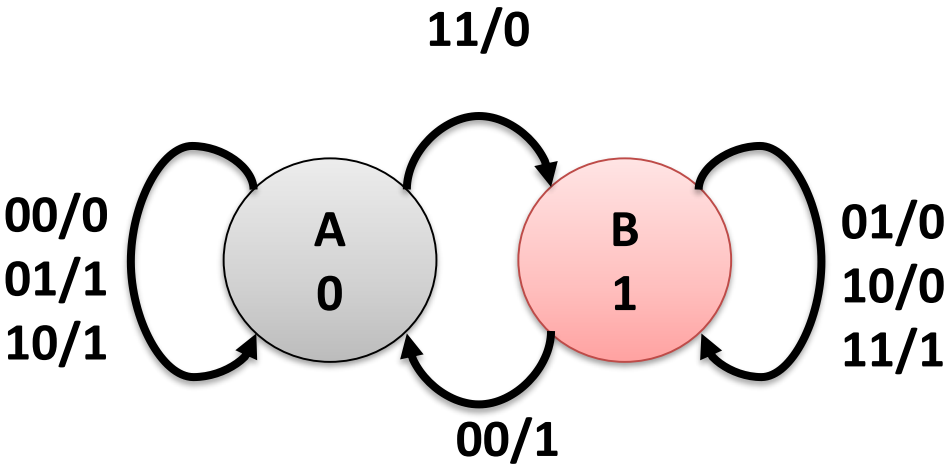
C=C+1, X=CMP(C,1023)

Remember : Serial Addition

- Model S in terms of X, Y and Q (State)

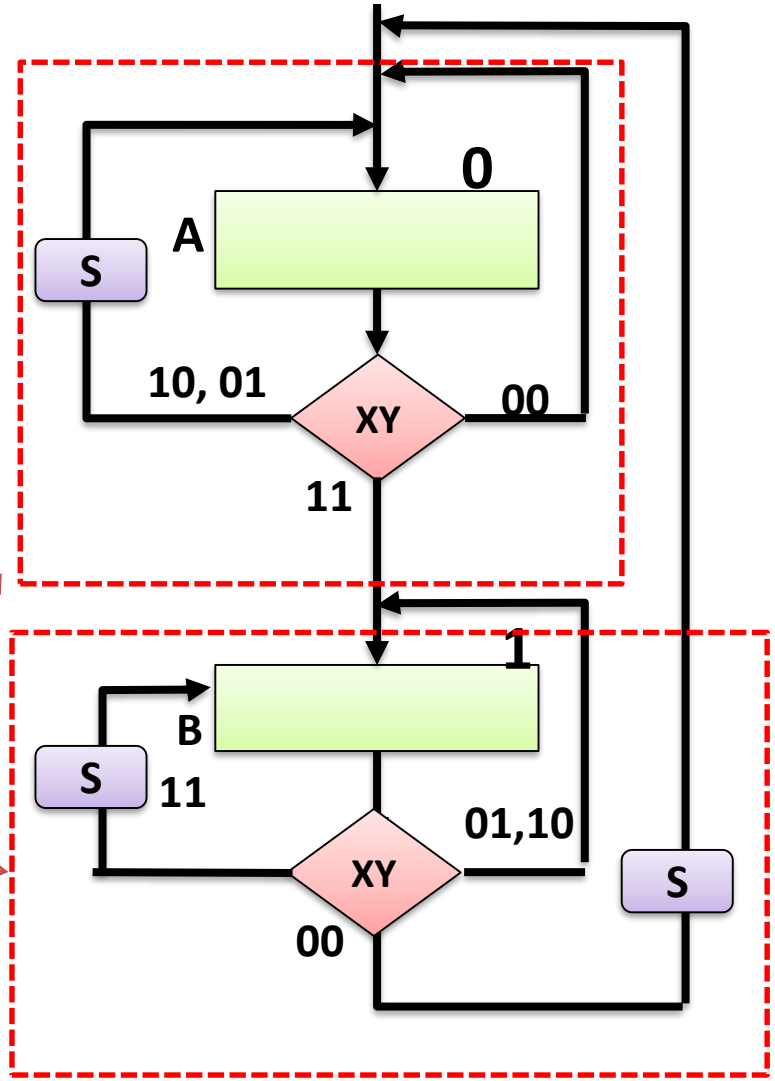


Mealy FSM for Binary Adder



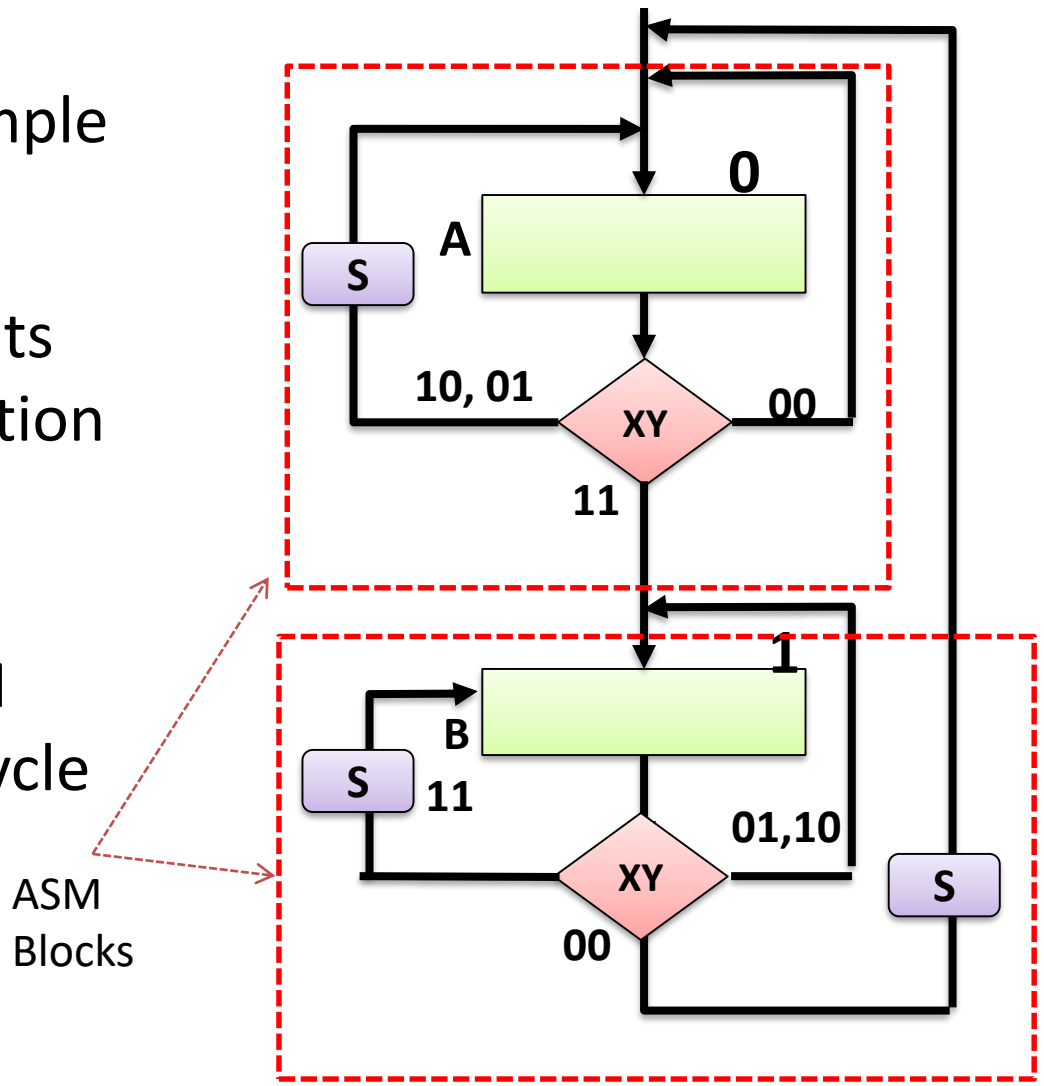
FSM

ASM Blocks



Mealy FSM for Binary Adder

- ASM Blocks
  - Two blocks in this example
- An ASM Block
  - Include a state and all its out going edges, condition boxes and conditional state boxes
  - All the parts of an ASM block execute in one cycle



Mealy FSM for Binary Adder