CS 223 Computer Architecture & Organization

Computer Fundamentals

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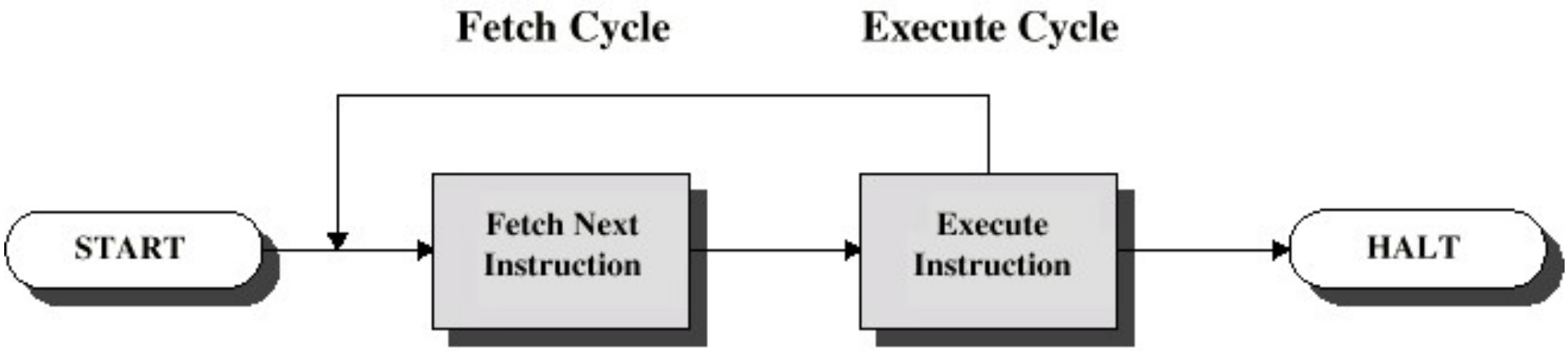
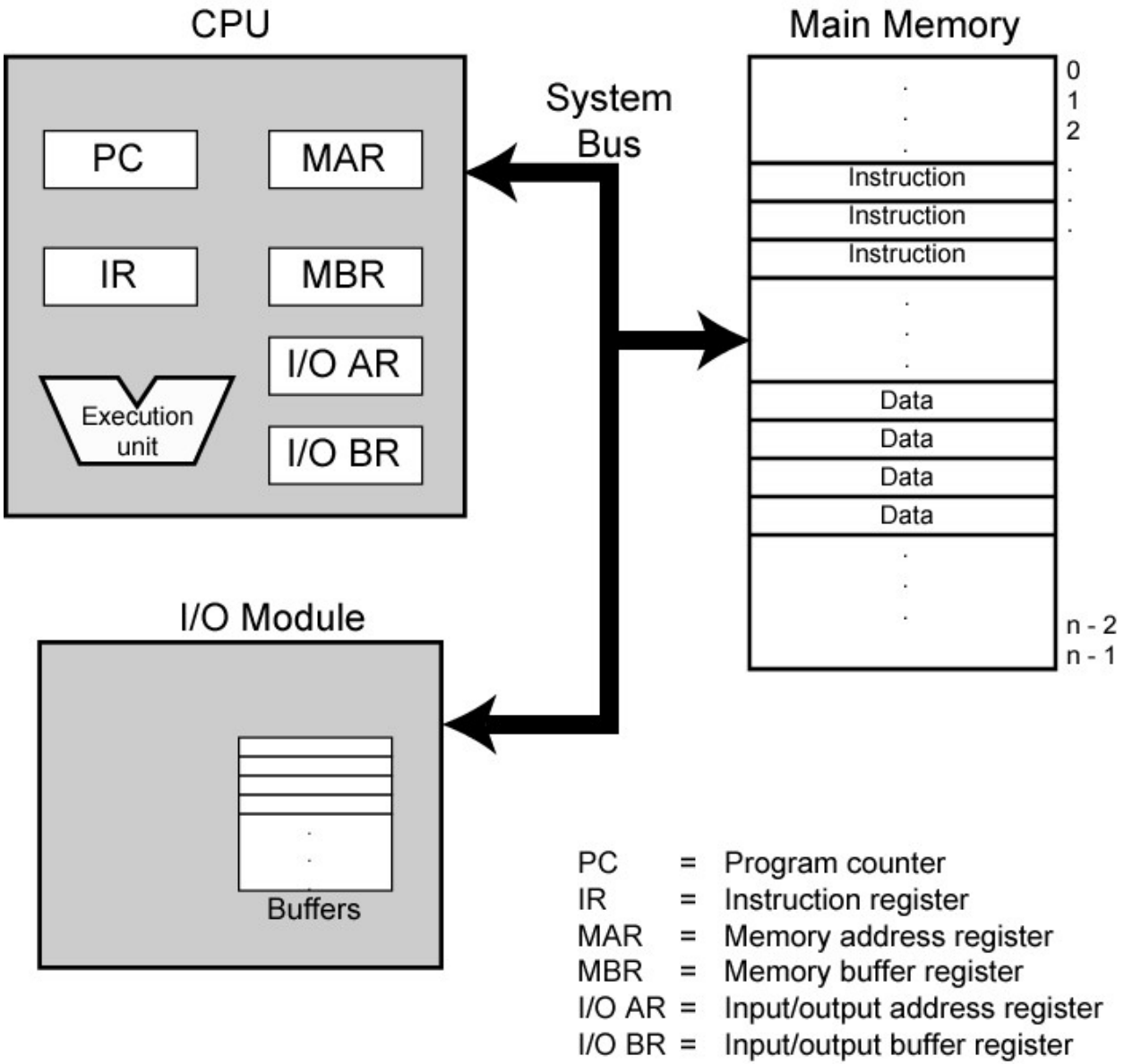
Instruction Cycle

- Two steps:
  - Fetch
  - Execute



Computer Components: Top Level View



Data Bus and Address Bus

- Size of Address Bus:

SIZE	BINARY	DEC	HEXA	
8	0000 0000	0	00	
8	1111 1111	255	FF	
8	0101 0111	87	57	
8	0000 0110	6	06	
10	11 1111 1111	1023	3FF	
12	1111 1111 1111	4095	FFF	
16	1111 1111 1111 1111	2^{16} -1	FFFF	
20	1111 1111 1111 1111 1111	2^{20} -1	FFFFF	
30	11 …… 1111	2^{30} -1	3FFFFFFF	
32	1111 …… 1111	2^{32} -1	FFFFFFFF	

Data Bus and Address Bus

- Size of Address Bus and Memory Capacity:

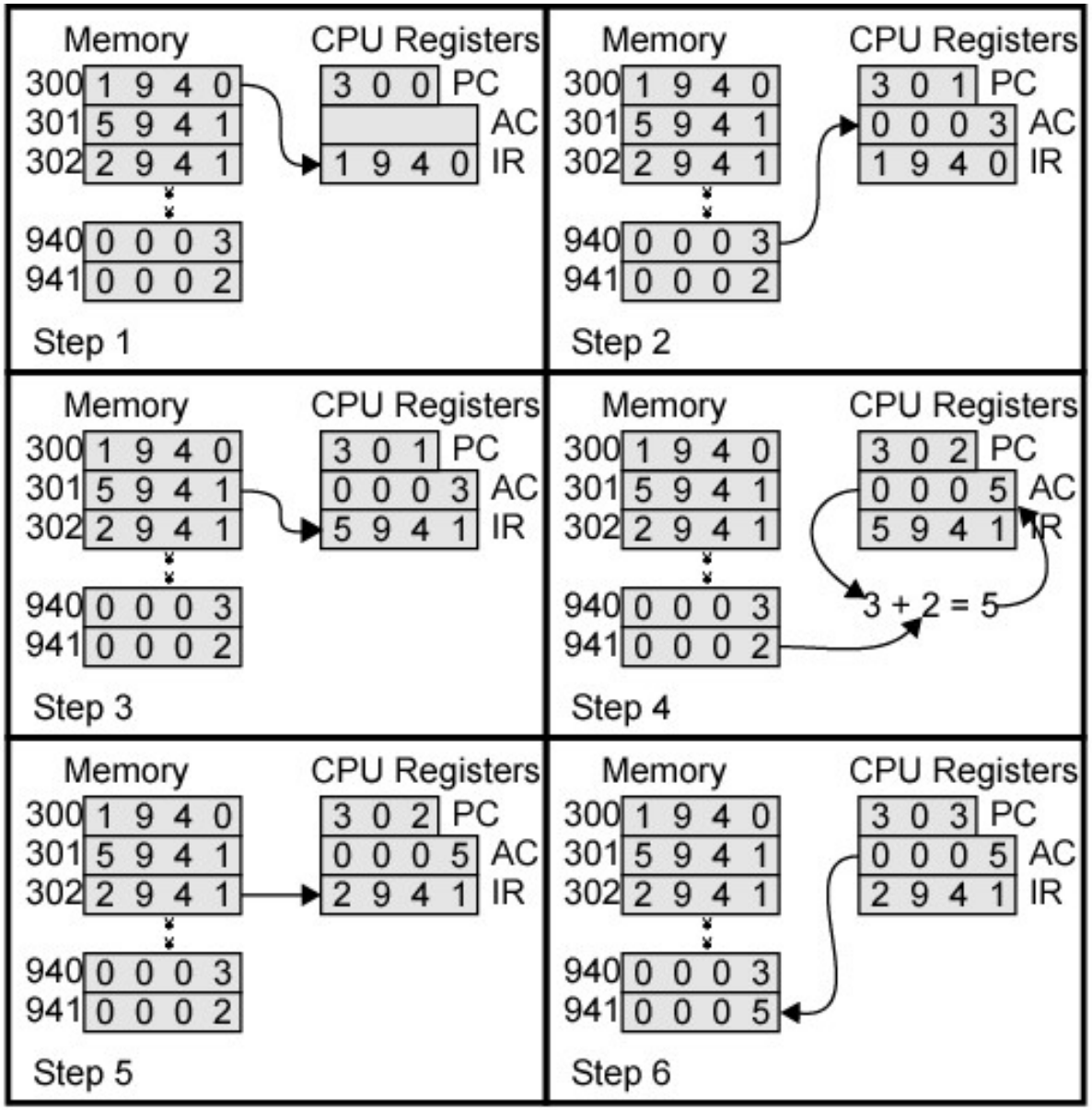
SIZE	BINARY	DEC	HEXA	Size
8	0000 0000	0	00	
8	1111 1111	255	FF	256
10	11 1111 1111	1023	3FF	1K
12	1111 1111 1111	4095	FFF	4K
16	1111 1111 1111 1111	2^{16} -1	FFFF	64K
20	1111 1111 1111 1111 1111	2^{20} -1	FFFFF	1M
30	11 …….. 1111	2^{30} -1	3FFFFFFF	1G
32	1111 …….. 1111	2^{32} -1	FFFFFFFF	4G

Data Bus and Address Bus

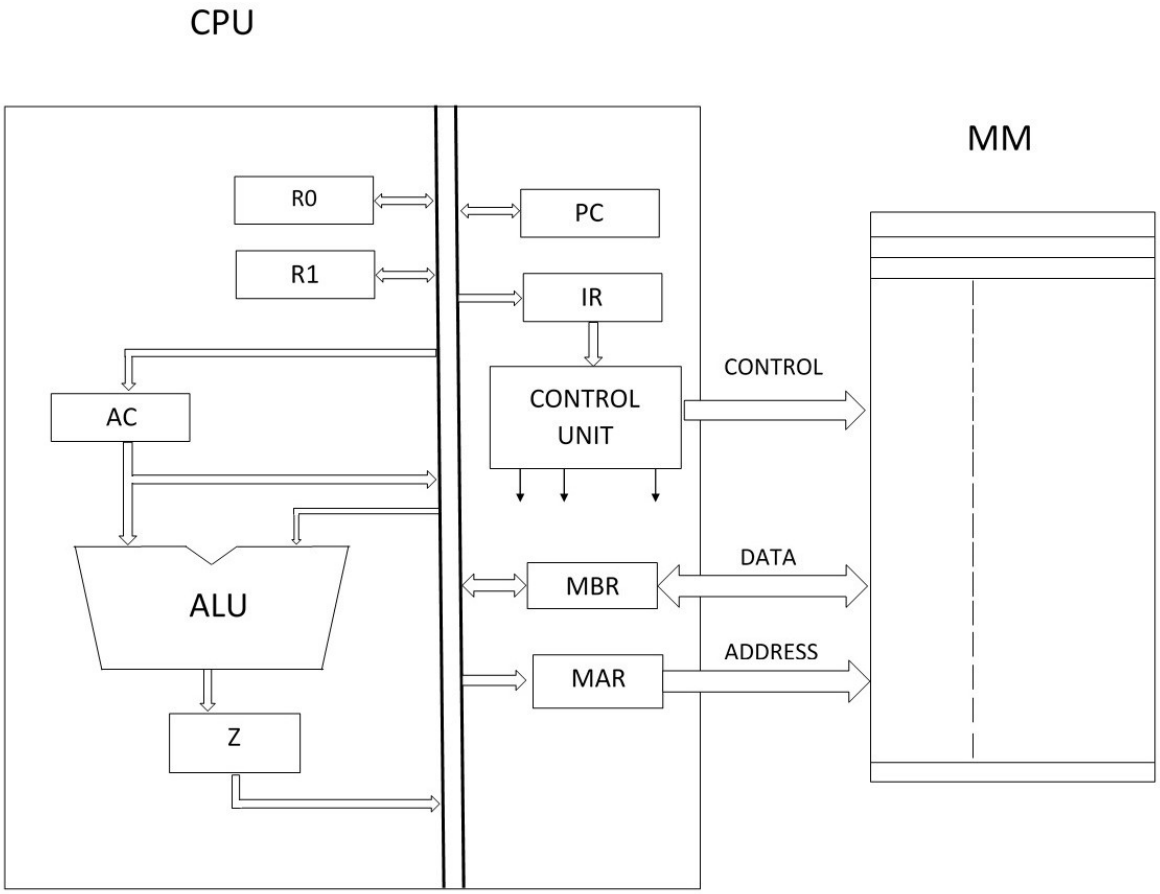
- Size of Data Bus/Memory Location:

SIZE	BINARY	DEC	HEXA
8	1111 1111 0111 1111	-127 +127	00 - FF
12	1111 1111 1111 0111 1111 1111	-2047 +2047	000 - FFF
16	1111 1111 1111 1111 0111 1111 1111 1111	$-(2^{15} - 1)$ $+(2^{15} - 1)$	0000- FFFF
20	1111 1111 1111 1111 1111 0111 1111 1111 1111 1111	$-(2^{19} -1)$ $+(2^{19} -1)$	00000 - FFFFF
32	1111 ……1111 0111 ……1111	$-(2^{31} -1)$ $+(2^{31} -1)$	00000000 – FFFFFFFF

Example of Program Execution



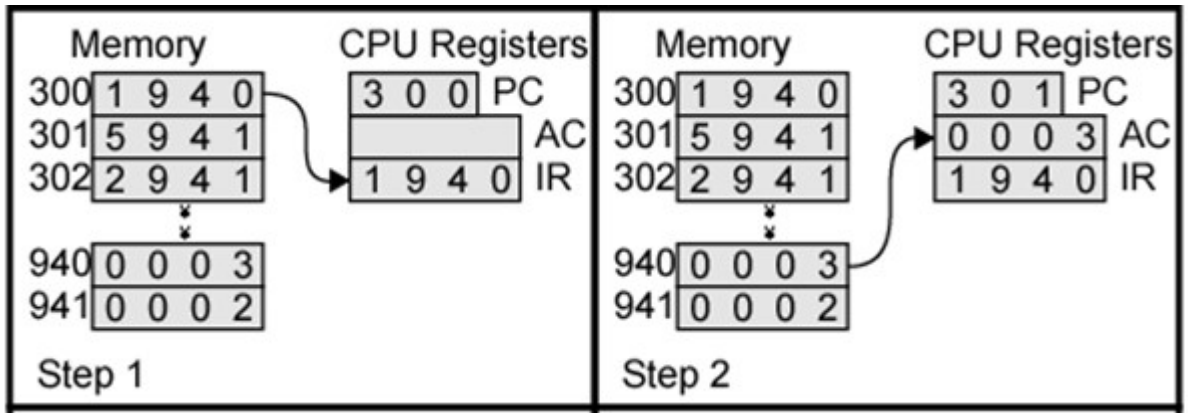
CPU Organization



Fetch Cycle:

MAR <- PC
Read
PC <- PC+1
IR <- MBR

Instruction Execution



Fetch Cycle:

MAR <- PC
Read
PC <- PC+1
IR <- MBR

Format of Instruction:

4 bits: Operation
12 bits: Address

Execute Cycle:

MAR <- $IR_{Address}$
Read
AC <- MBR

(Data Movement)

Machine Instruction

Machine	Instruction Format				Assembly
Instruction	Operation	Address			Code
1940	0001	1001	0100	0000	LDA M
5941	0101	1001	0100	0001	ADD M
2941	0010	1001	0100	0001	STA M

(LDA M) LOAD AC: Load the accumulator by the contents of memory location specified in the instruction

(ADD M) ADD AC: Add the contents of memory location specified in the instruction to accumulator and store the result in accumulator

(STA M) STORE AC: Store the contents of accumulator the memory location specified in the instruction

Computer Program

High Level Code	Assembly Code	Machine Code (HEX)
Y = X + Y	LDA X ADD Y STA Y	1940 5941 2941

Size of Operation Code (Op Code): 4 bits

16 possible instructions Used: 1: LDA M, 5: ADD M, 2: STA M

Size of Address Bus: 12 bits

Addressable Memory Location: $2^{12} = 4096 = 4$ K

Size of Data Bus: 16 bits

Size of each location of memory: 16 bits

Size of Memory Module: 4096 x 16 = 4096 x 2 x 8 = 8 KB (Kilo Byte)

Reference

Computer Organization and Architecture –
Designing for Performance
William Stallings

Chapter 3: Page no. 59 – 64 (Seventh Edition)
Page No.: 68 – 73 (Eighth Edition)