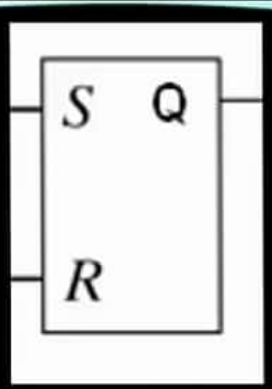
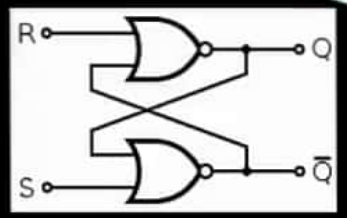
CS101-2021
INTRODUCTION TO COMPUTING
LEC – 6

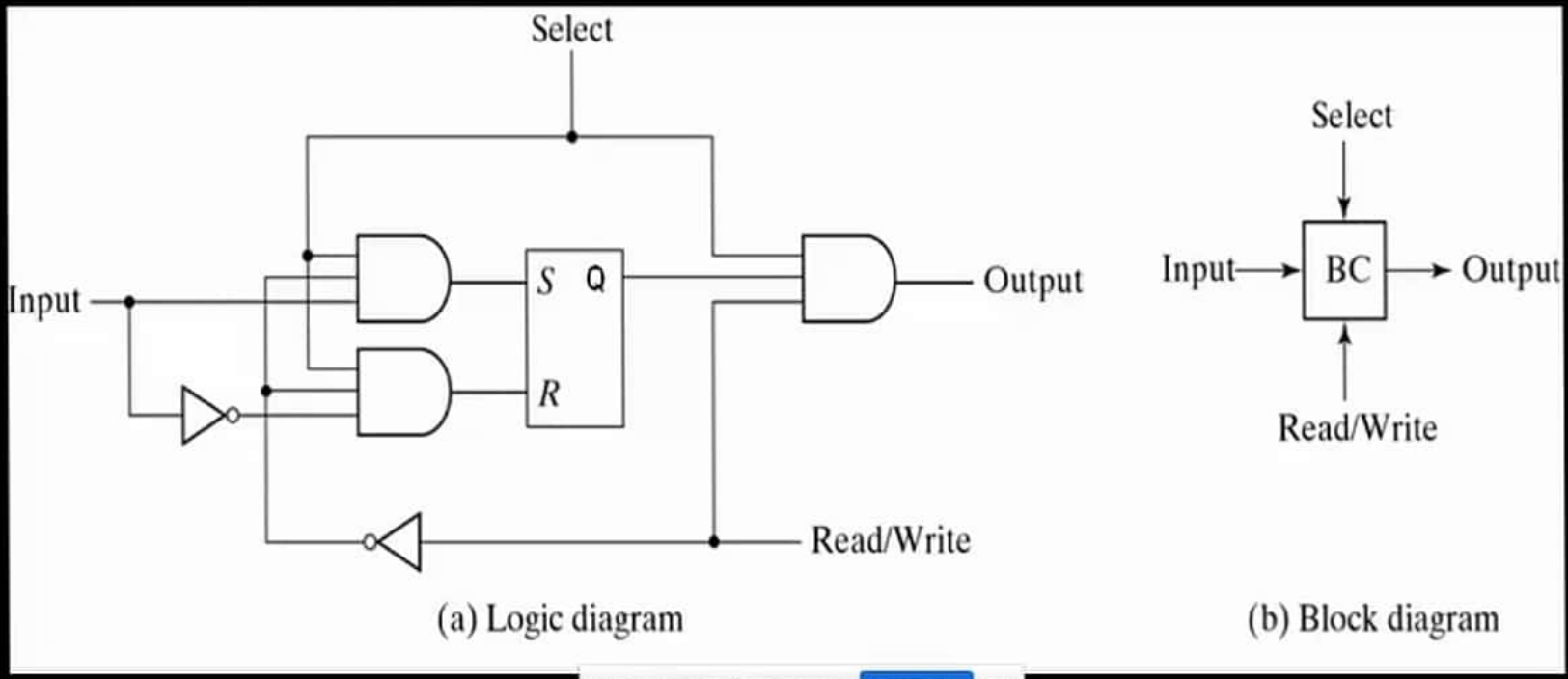
MEMORY MEMORABILIA (CONTD.)

RAM: ONE BIT

- Basis of each RAM cell is an S-R latch
- Note that data goes to both S and R
- Select enables operation
- Read/write enables read OR write, but not both







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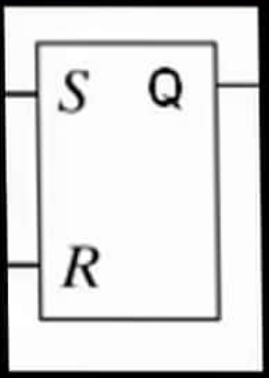

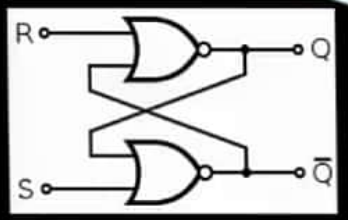

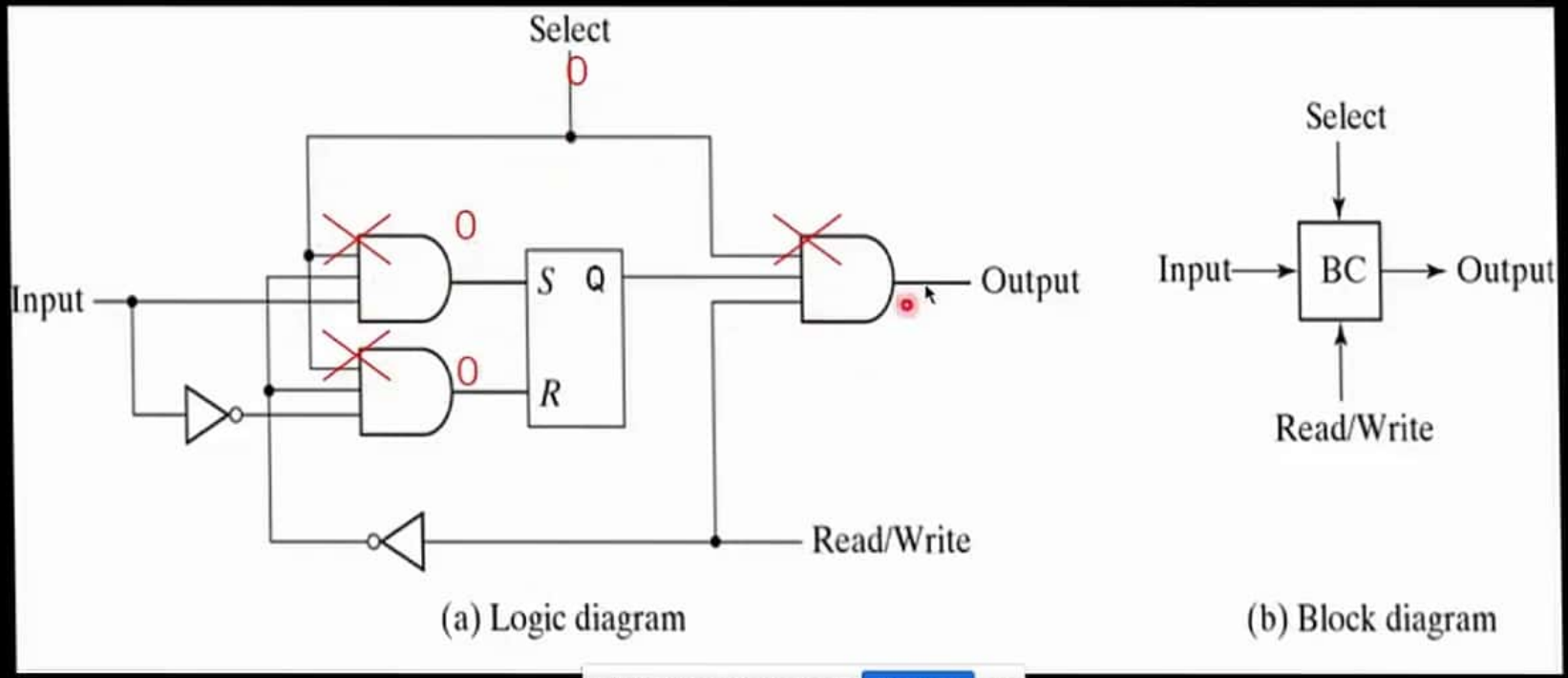

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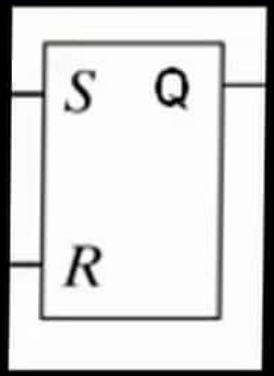

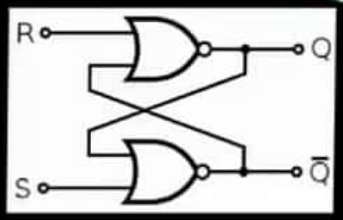

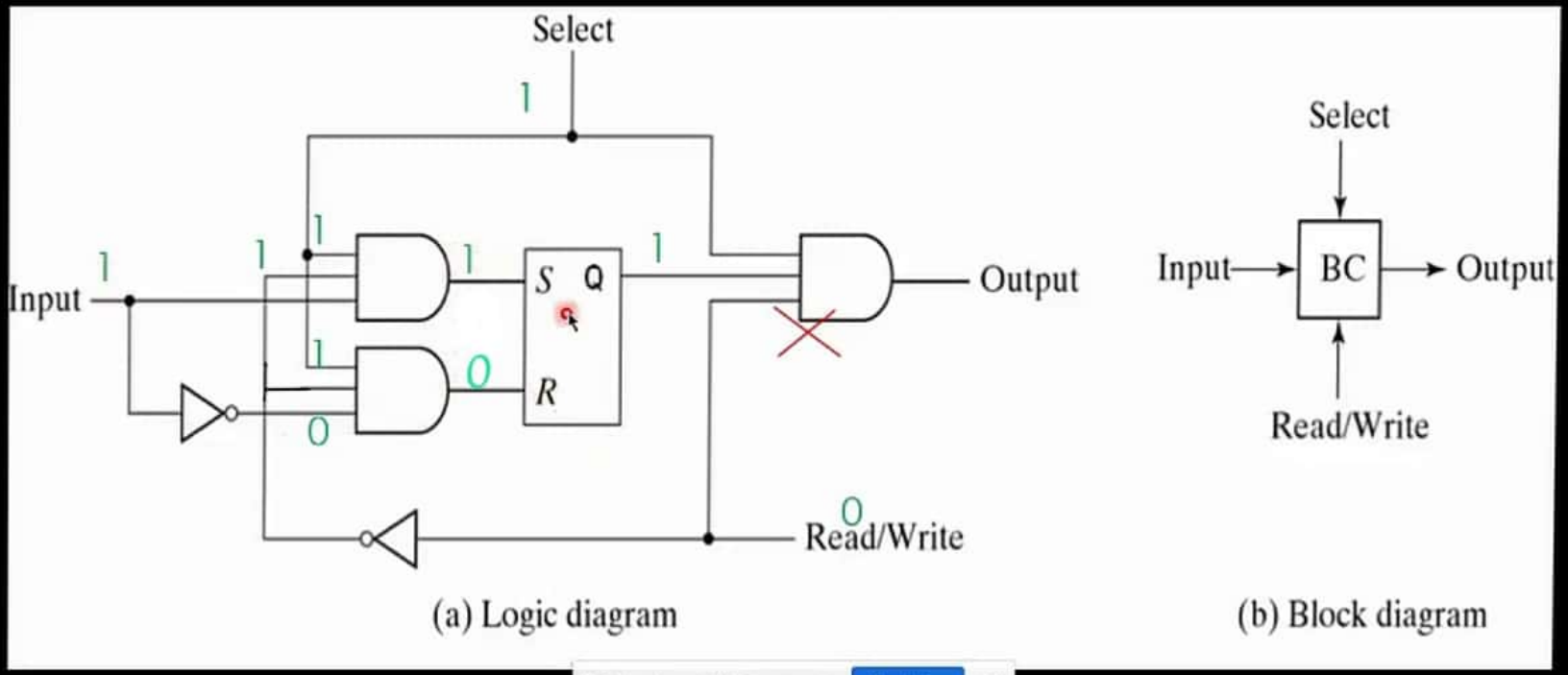

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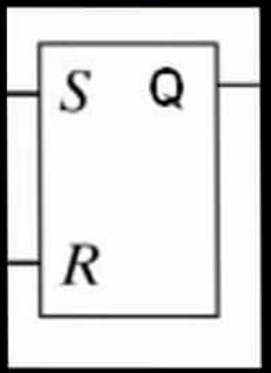

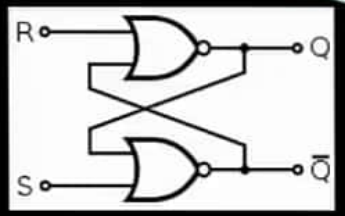

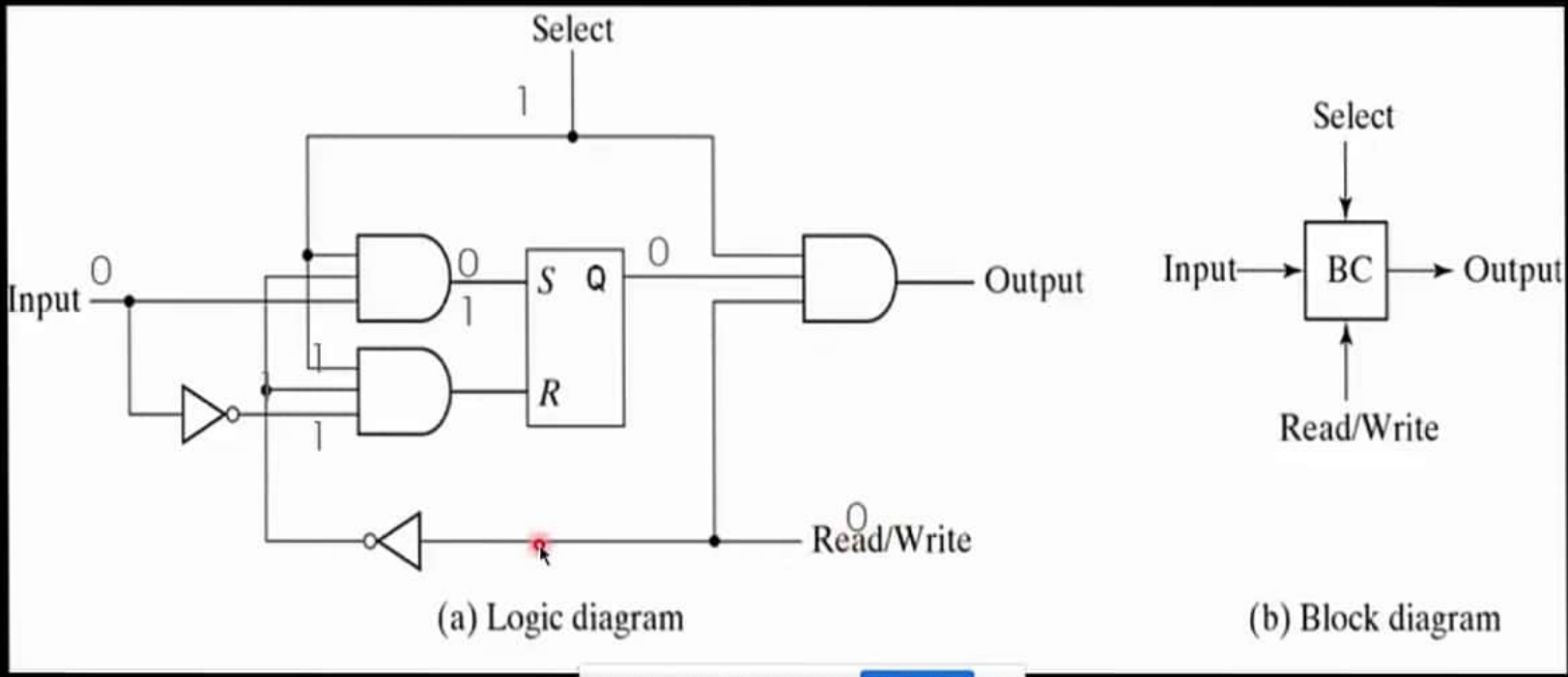

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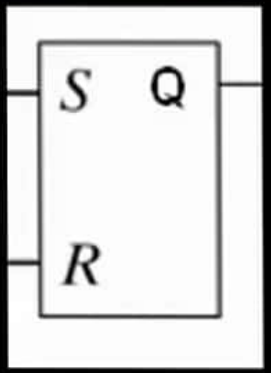
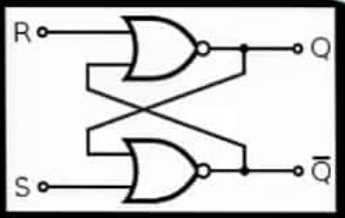
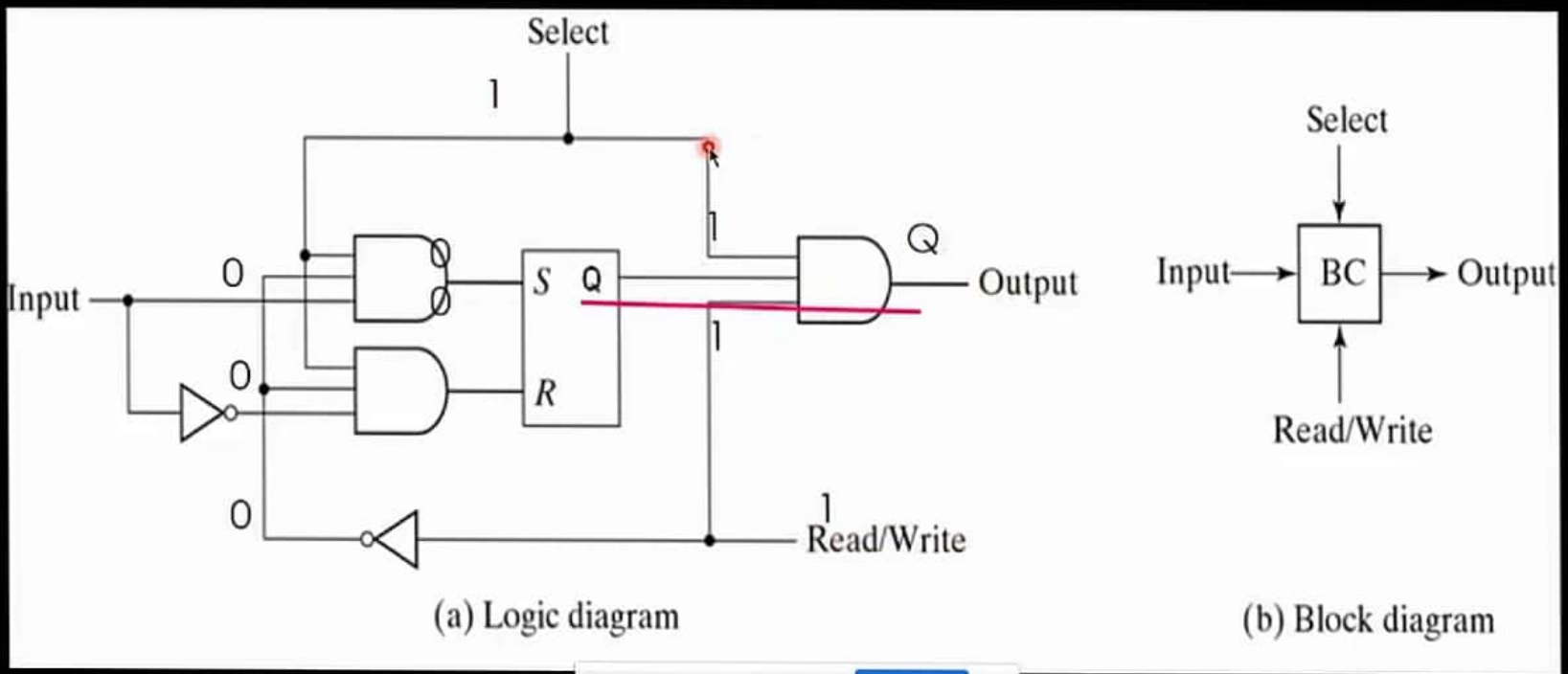


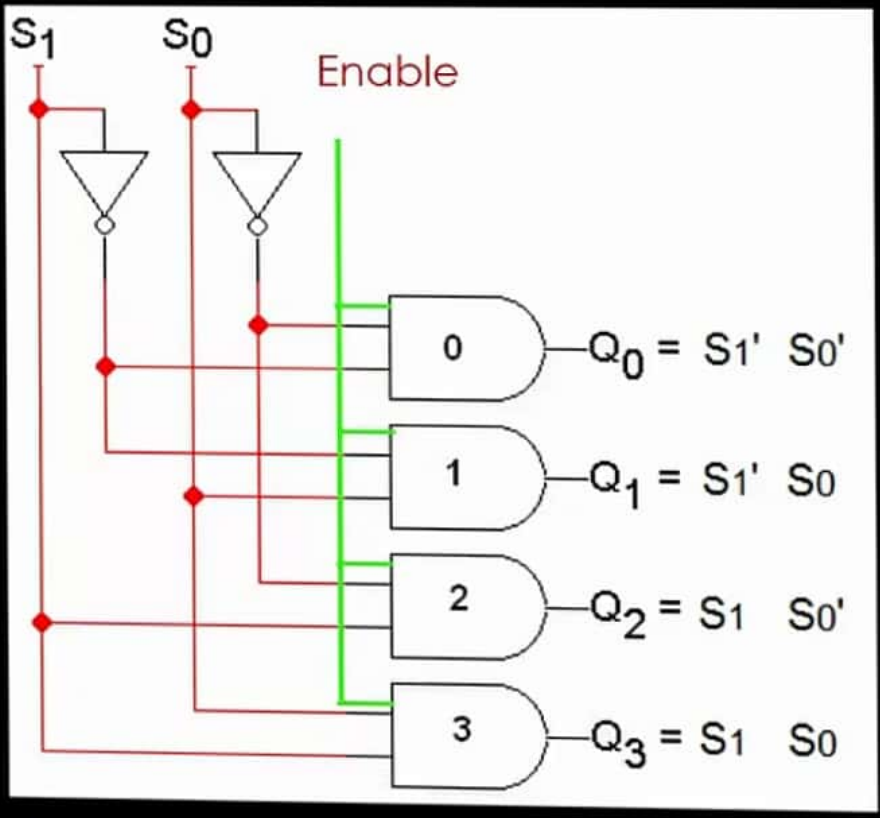




2-to-4 decoder RECAP

2 inputs and 2^2 *outputs*

S1	S0		Q_3	Q_2	Q_1	Q_0
0	0		0	0	0	1
0	1		0	0	1	0
1	0		0	1	0	0
1	1		1	0	0	0



When Enable = 0 all outputs are 0 irrespective of S0 and S1.
The circuit behaves as a decoder only when Enable =1
Enable can be used to switch ON or switch OFF decoding.

RAM (R/W MEMORY)

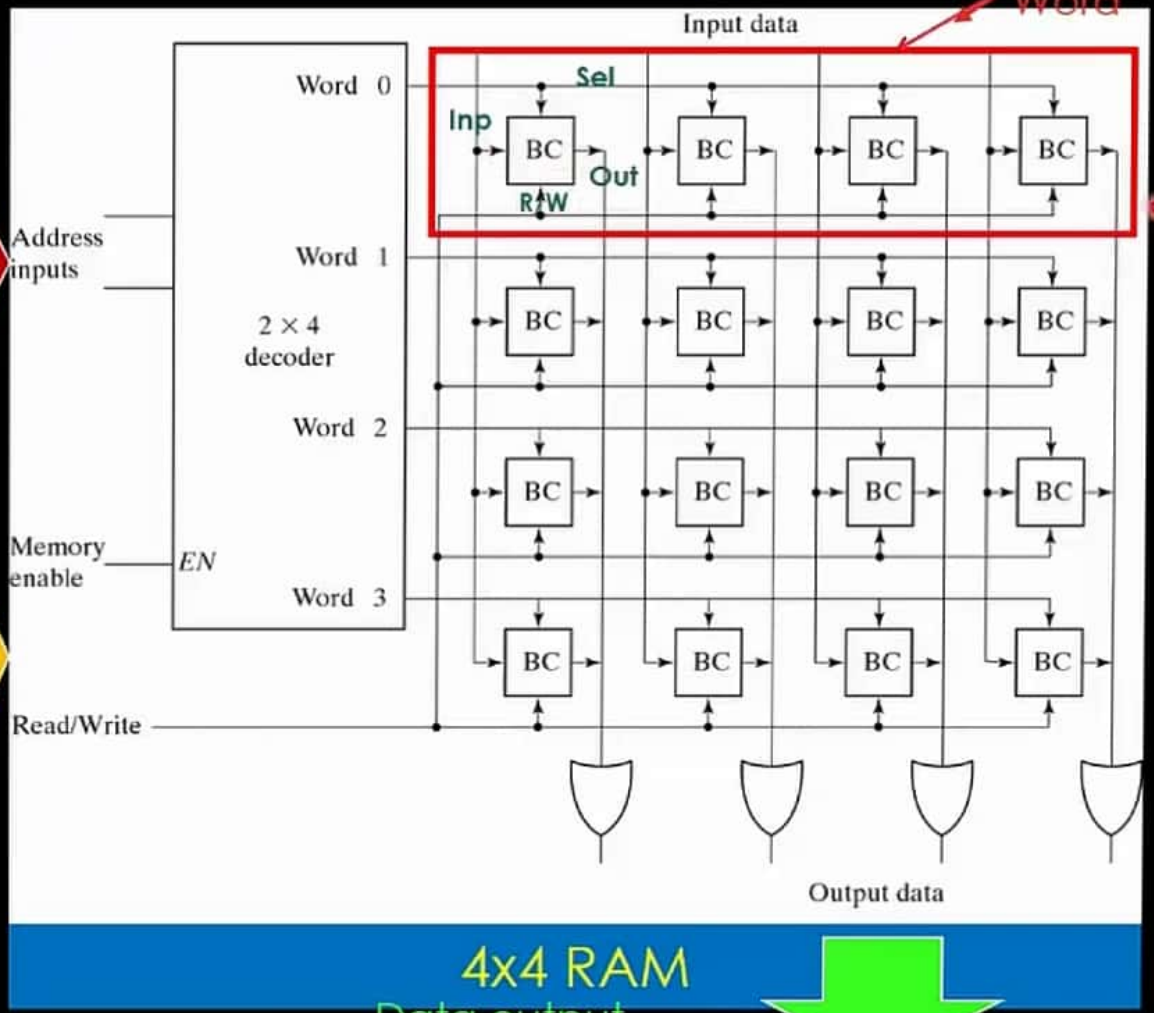
Data input

One Word

Word

Address Bus

Control Bus

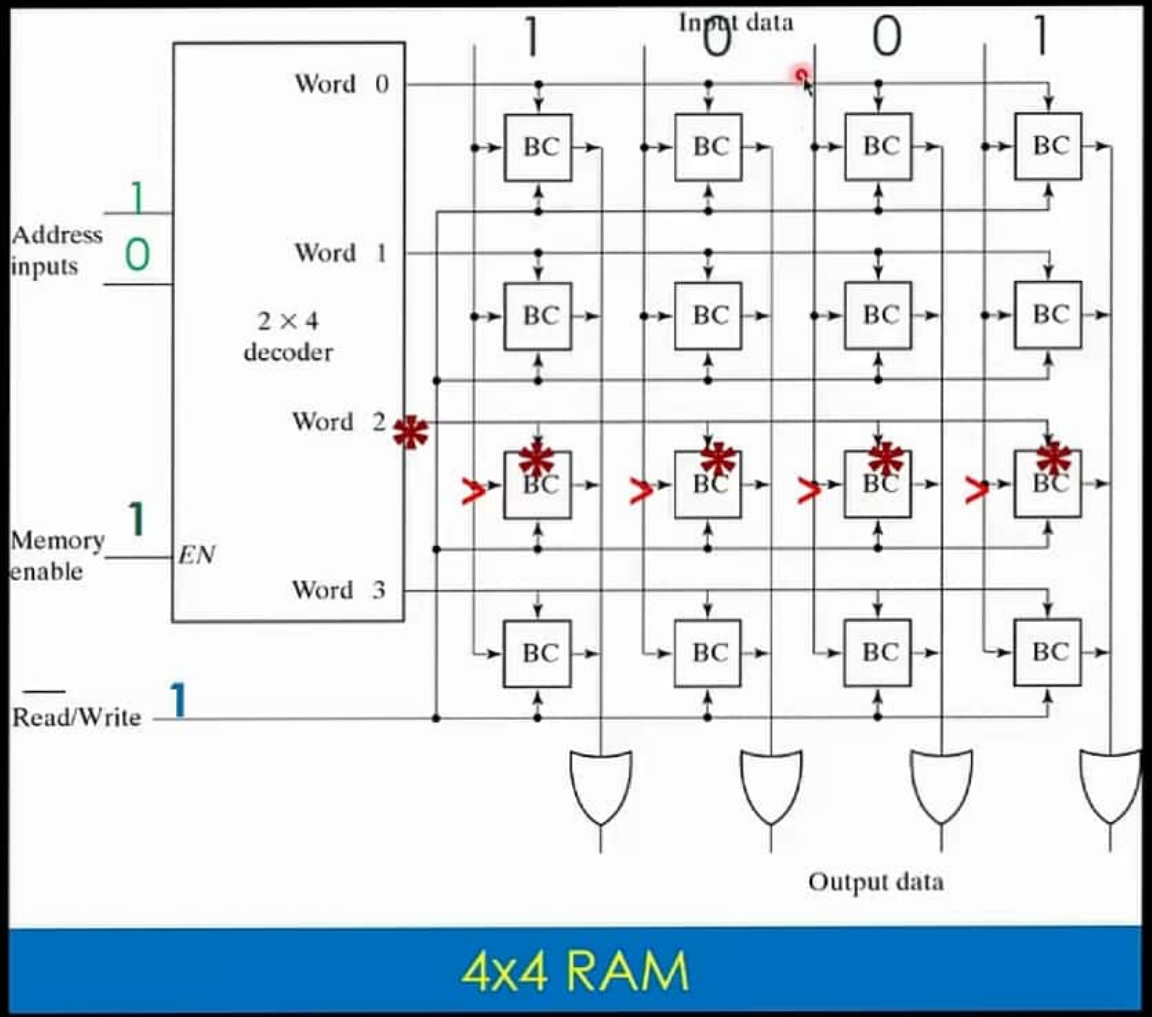


4x4 RAM

Data output

RAM

- Address inputs go into decoder
  - Only one output active
- Word line selects a row of bits (word)
- Data passes through OR gate
- Each binary cell (BC) stores one bit
- Input data stored if Read/Write is 0
- Output data driven if Read/Write is 1



4x4 RAM

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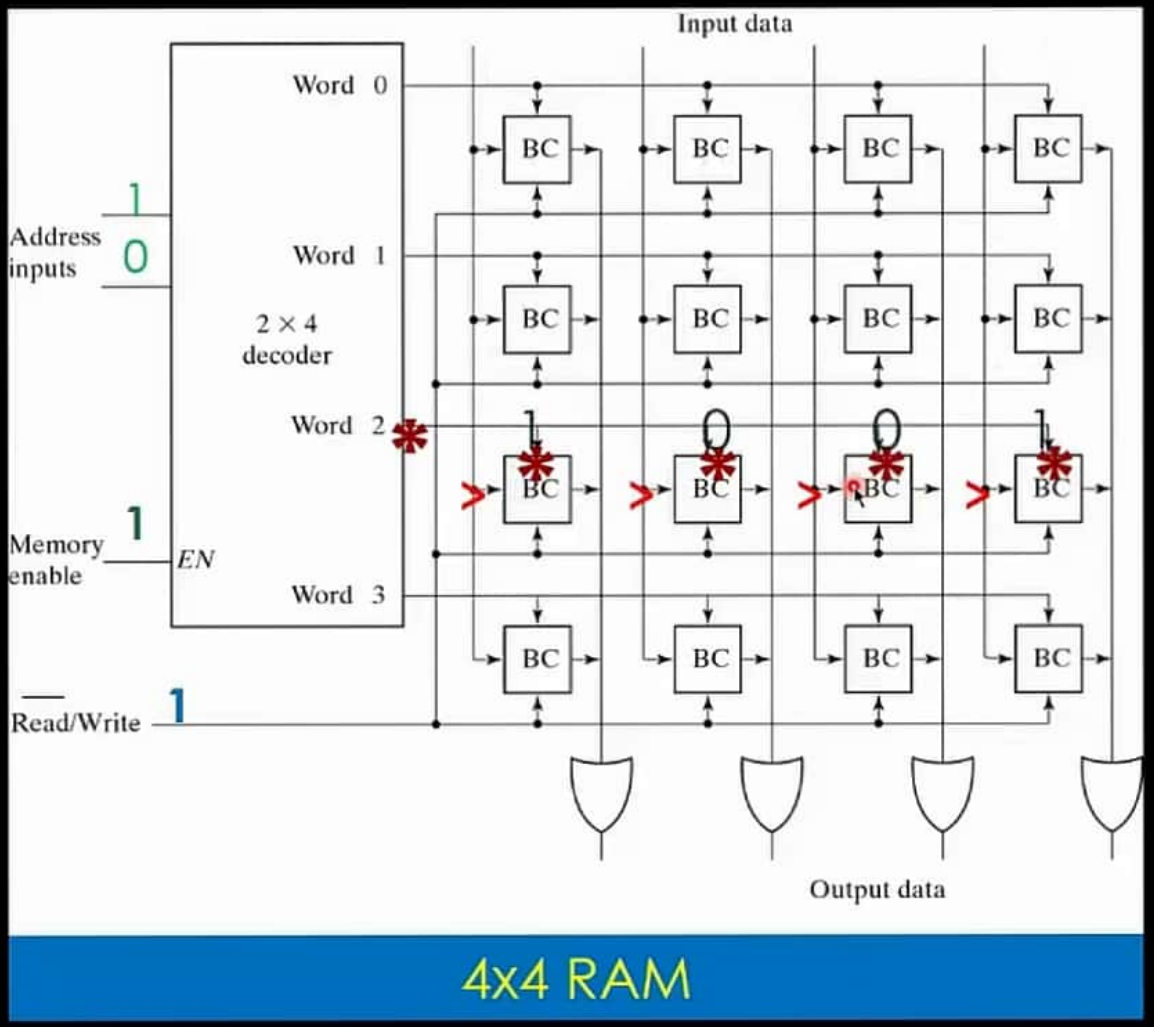
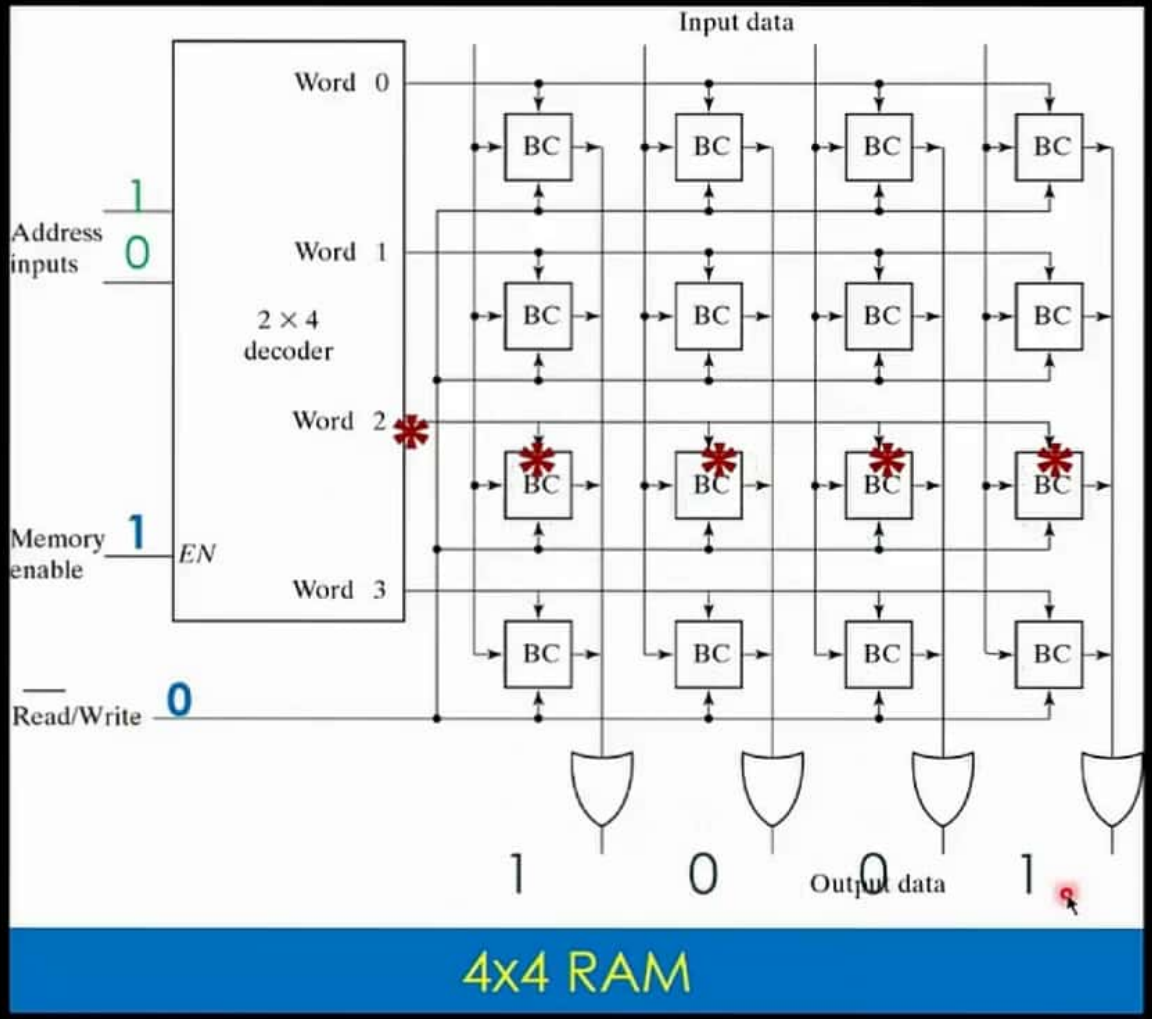


4x4 RAM

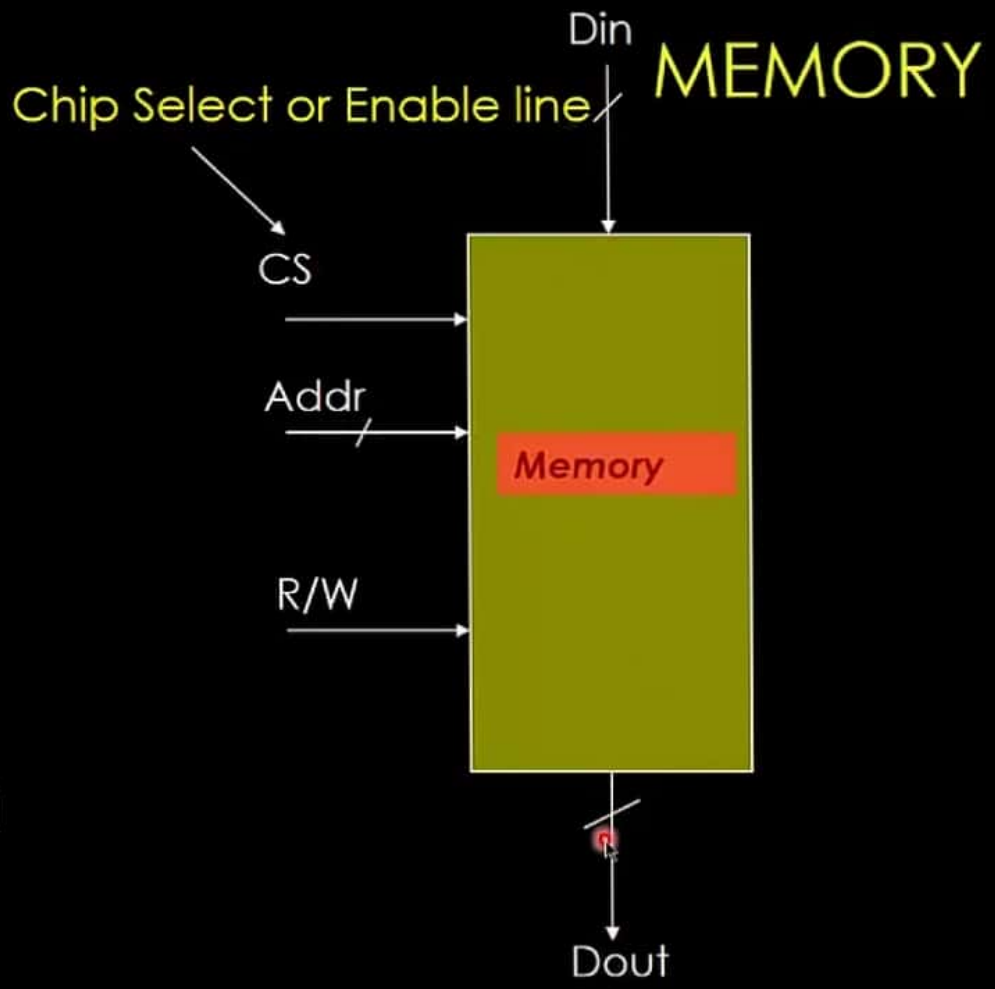
RAM READING



- Typical →
  - Data input bus
  - Data output bus
  - Address
  - Read/Write control
  - Chip Select

Size: m x n

where m = no. of words & n = bits/word



ORGANIZING LEVELS OF MEMORY (STORAGE)

Storage	Almirah	Rack	Study Table
Capacity (books stored)	High	Medium	Small
Speed of Access	Slow	Medium	Fast
Transfers done in one stroke	Several Books	One book	Page

LEVELS OF THE MEMORY HIERARCHY