

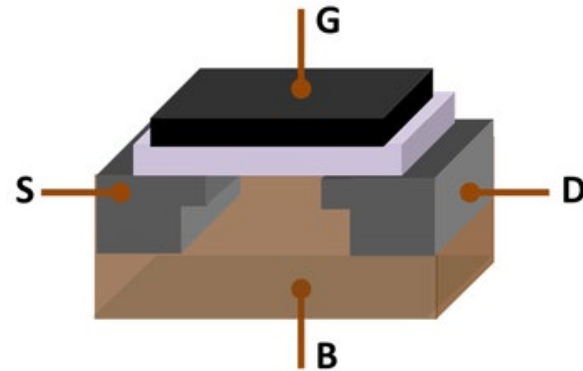
CMOS transistors and gates

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- **Metal-oxide semiconductor (MOS) transistors and gates**
 - Chapter 5, Kohavi's book

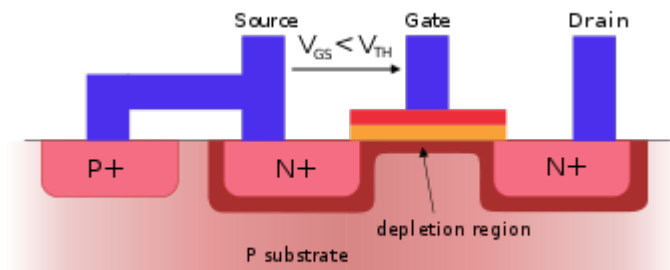
MOSFET

- The **metal–oxide–semiconductor field-effect transistor (MOSFET)**, also known as the **metal–oxide–silicon transistor (MOS transistor, or MOS)** is a type of insulated-gate field-effect transistor that is fabricated by the controlled oxidation of a semiconductor, typically silicon.

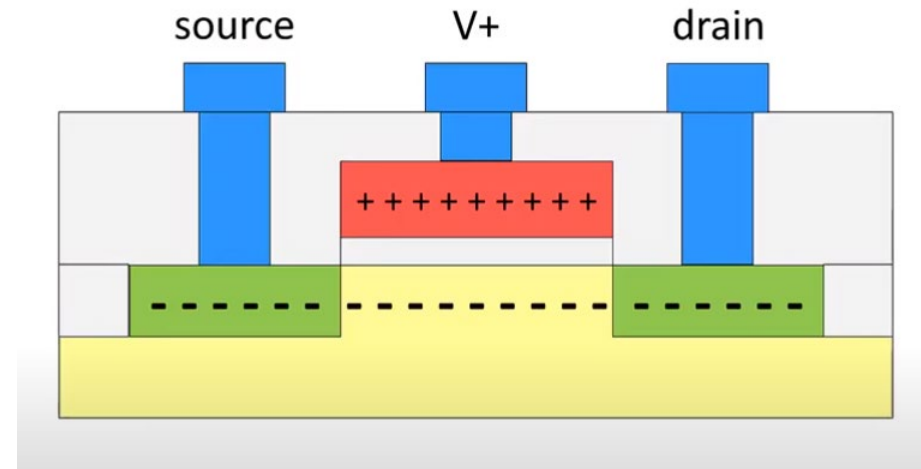
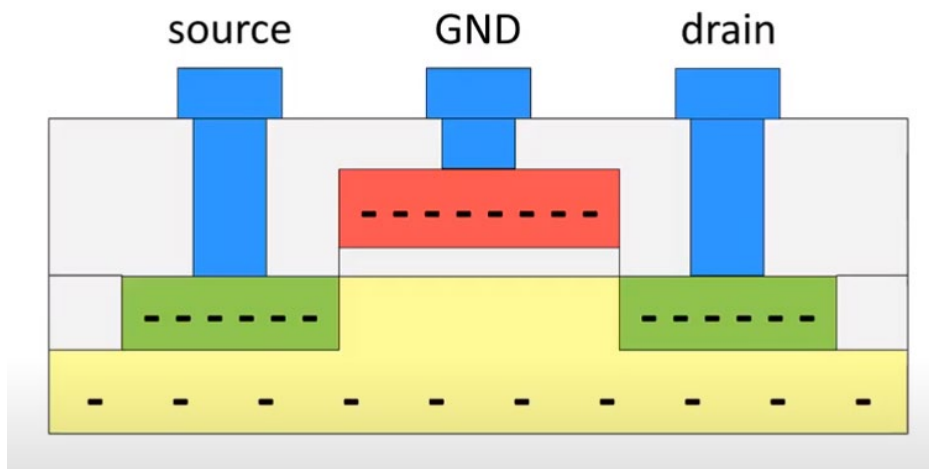


MOSFET

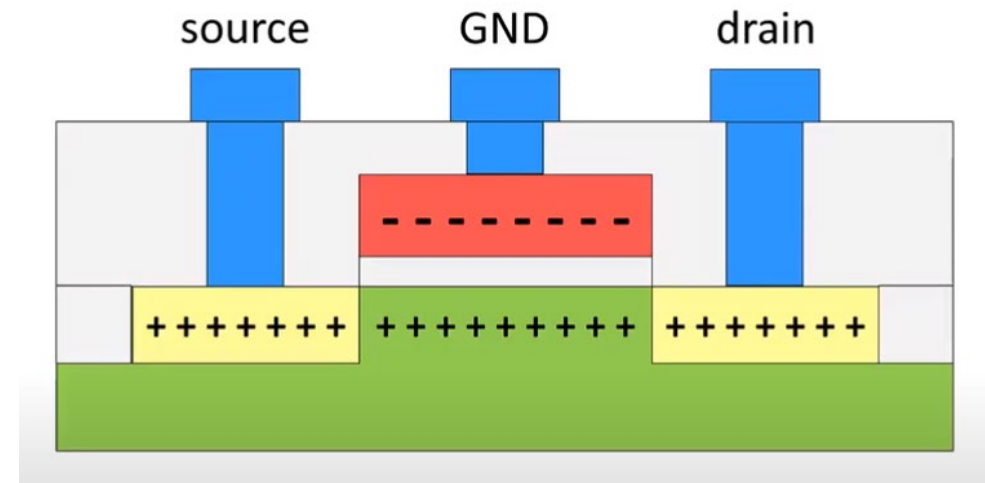
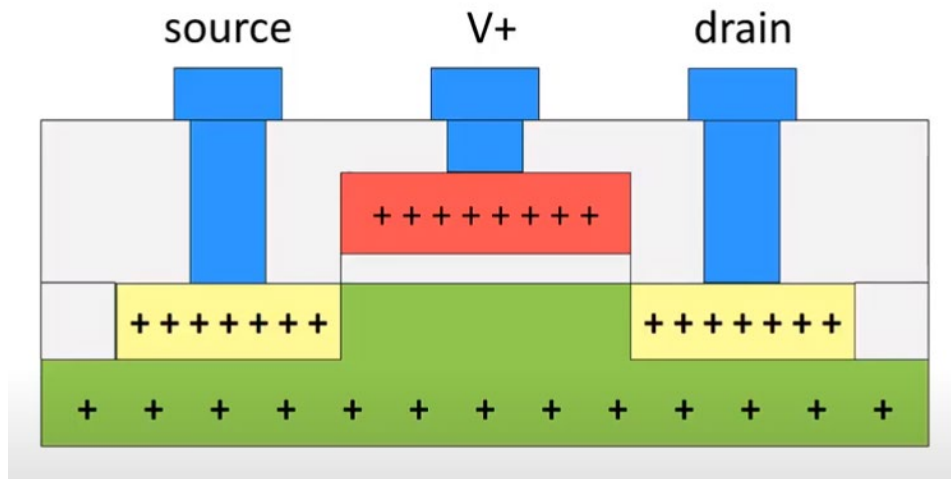
- The traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide on top of a silicon substrate, commonly by thermal oxidation and depositing a layer of metal or polycrystalline silicon. As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor.
- When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor.



NMOS

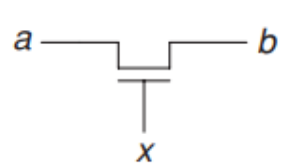


PMOS

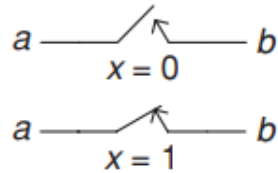


METAL-OXIDE SEMICONDUCTOR GATES AND TRANSISTORS

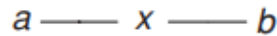
- Complementary metal-oxide semiconductor (CMOS) is the dominant technology for implementing chips.



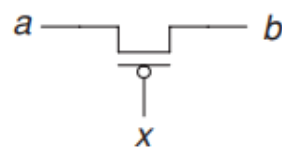
(a) nMOS transistor



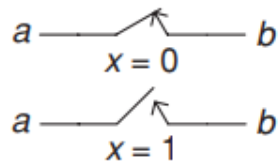
(b) nMOS operation



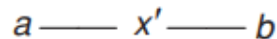
(c) nMOS model



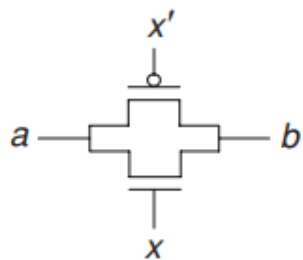
(d) pMOS transistor



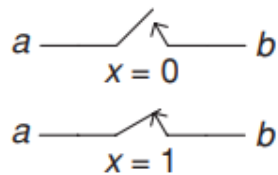
(e) pMOS operation



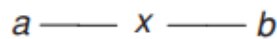
(f) pMOS model



(g) Complementary switch



(h) Complementary switch operation

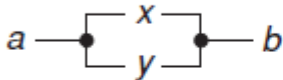

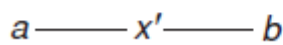


(i) Complementary switch model

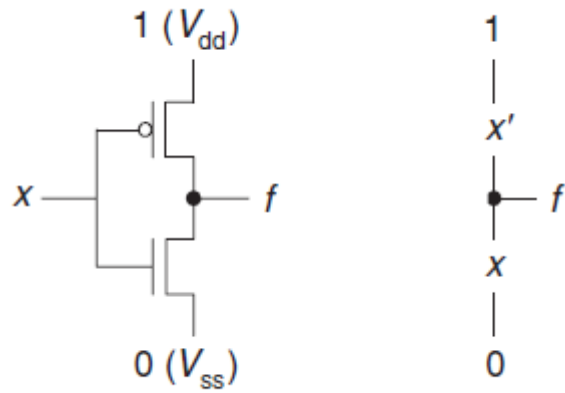
MOS CONTD.

- nMOS Transistor: The switch is open when $x=0$ and closed when $x=1$
- pMOS Transistor: The switch is open when $x=1$ and closed when $x=0$
- An nMOS transistor passes a 0 perfectly, but a 1 imperfectly.
- pMOS transistor is good at propagating a 1, but bad at propagating a 0.
- To overcome this drawback of nMOS and pMOS transistors they can be connected in parallel.
- It is called a complementary switch. This switch is closed when $x = 1$ since both its transistors are closed for this value.

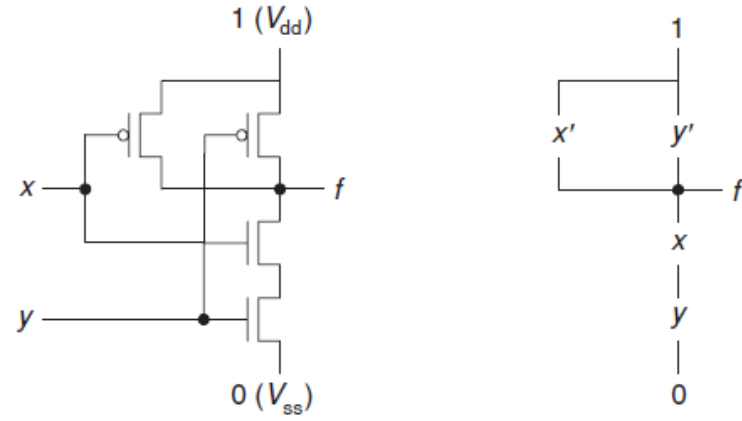
- Any switching expression can be realized by an appropriate connection of such transistors

Network	Transmission function
	$T_{ab} = x + y$
	$T_{ab} = xy$
	$T_{ab} = x'$

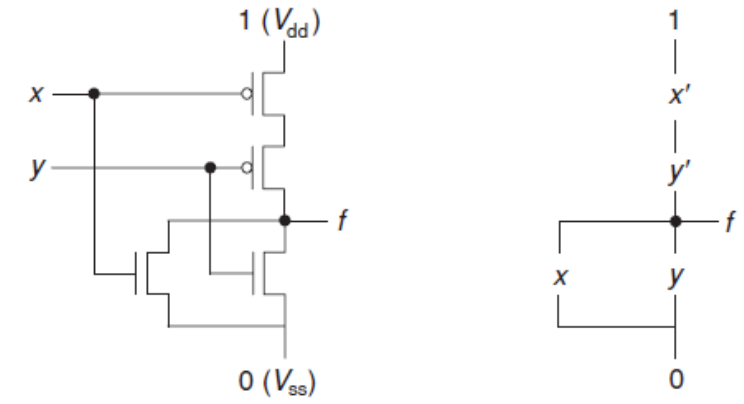
Gate realization using transistors



NOT GATE



(a) CMOS NAND gate and its transmission functions.



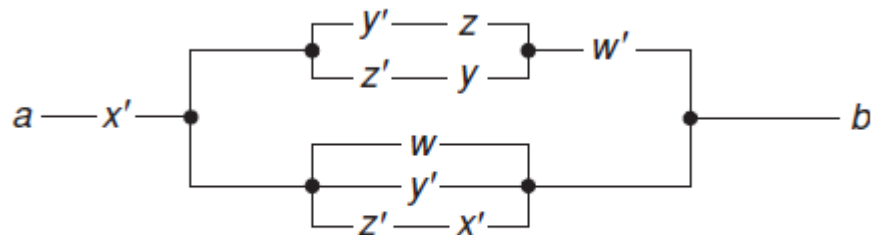
(b) CMOS NOR gate and its transmission functions.

Analysis of series–parallel networks

- Two MOS transistors with transmission functions x and y , connected in parallel, is $x + y$.
- the transmission function of a network consisting of two MOS transistors connected in series is xy .
- Since the algebra of MOS networks is isomorphic to switching algebra, the transmission function of two networks, $T1$ and $T2$, connected in series is $T1T2$ and the transmission function of a parallel connection of these two networks is $T1 + T2$.
- Utilizing these properties, we can determine the transmission function of any series–parallel network.

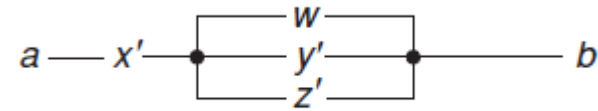
Analysis of series–parallel networks

$$T_{ab}(w, x, y, z) = x'[(y'z + yz')w' + w + y' + x'z'].$$



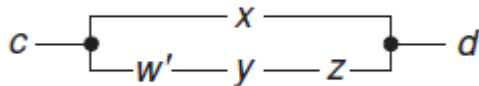
(a) $T_{ab} = x'[(y'z + z'y)w' + w + y' + x'z'].$

$$T_{ab}(w, x, y, z) = x'(w + y' + z').$$



(b) $T_{ab} = x'(w + y' + z').$

Simplified expression

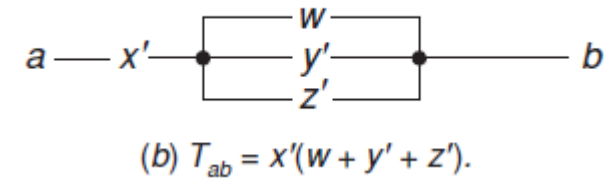
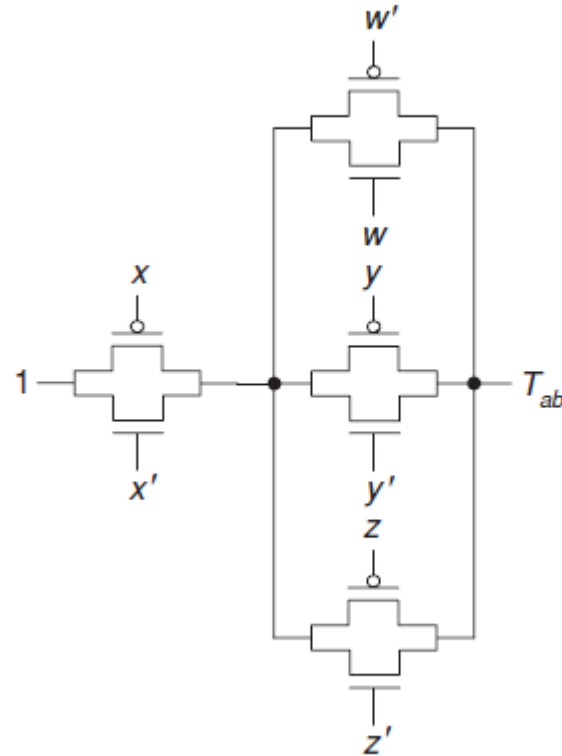


(c) $T_{cd} = T'_{ab} = x + w'yz.$

Complement

Complementary-switch-based CMOS implementation

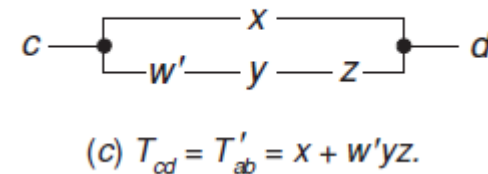
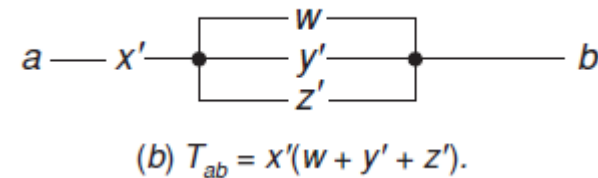
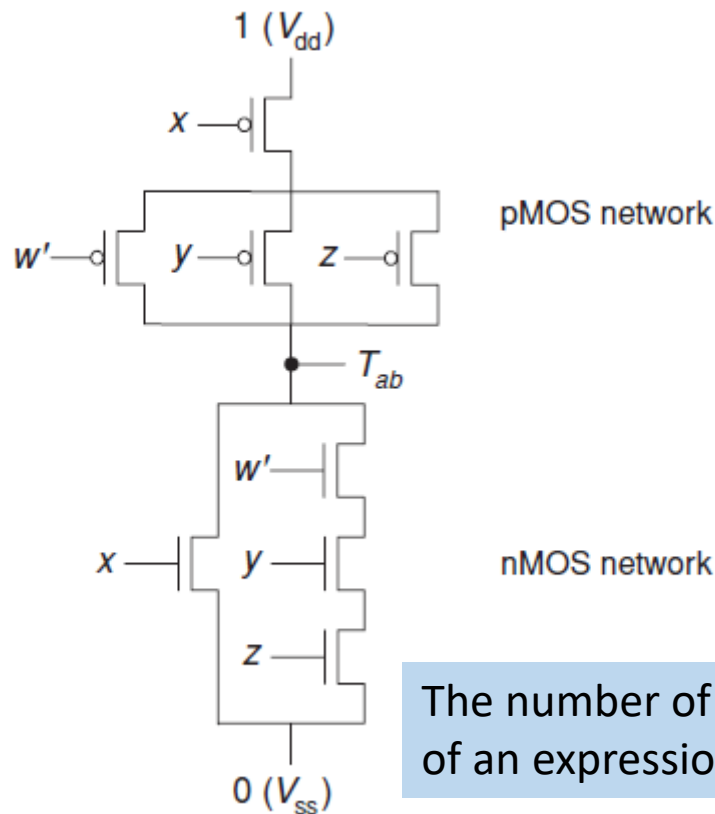
$$T_{ab}(w, x, y, z) = x'(w + y' + z)$$



simply involves a one-to-one mapping from the network

Complex CMOS-gate implementation

- A CMOS gate is said to be complex if it does not implement a primitive function such as a NOT, NAND or NOR gate.



The number of transistors in complex CMOS-gate implementation of an expression is **TWICE** of its literal count

Synthesis of MOS networks

- Obtain the switching expression of the function
- Obtain the minimal/simplified expression
- Implement the simplified function using series-parallel network
- Simplify the network if possible (if some parallel sub-paths can be merged without changing the functionality).

