CS221: Digital Design

Register and Memory

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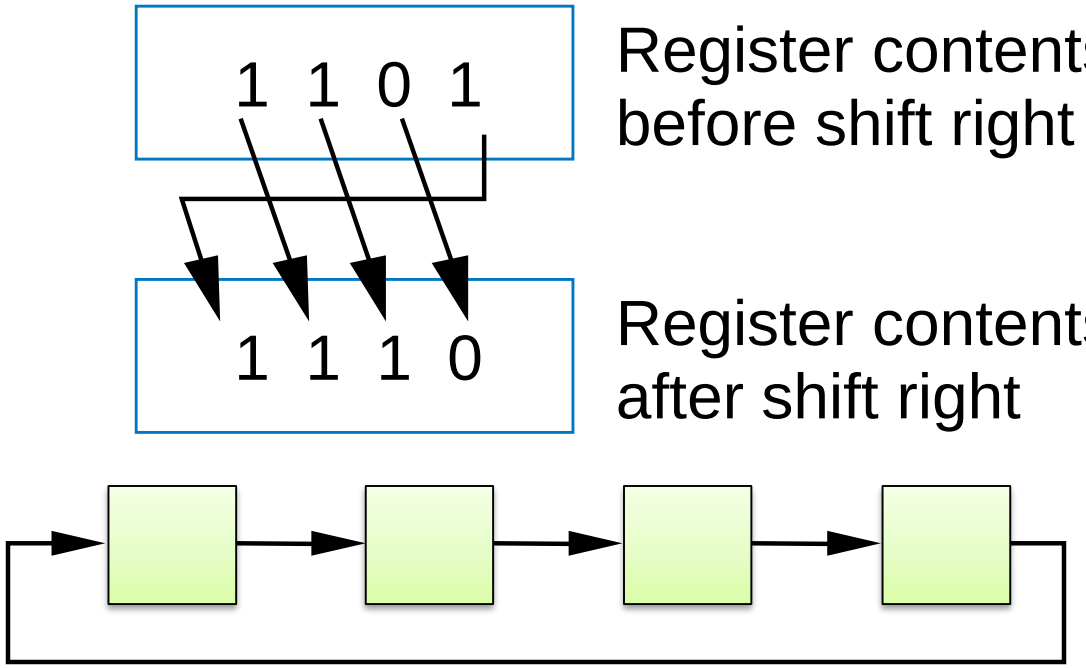
Outline

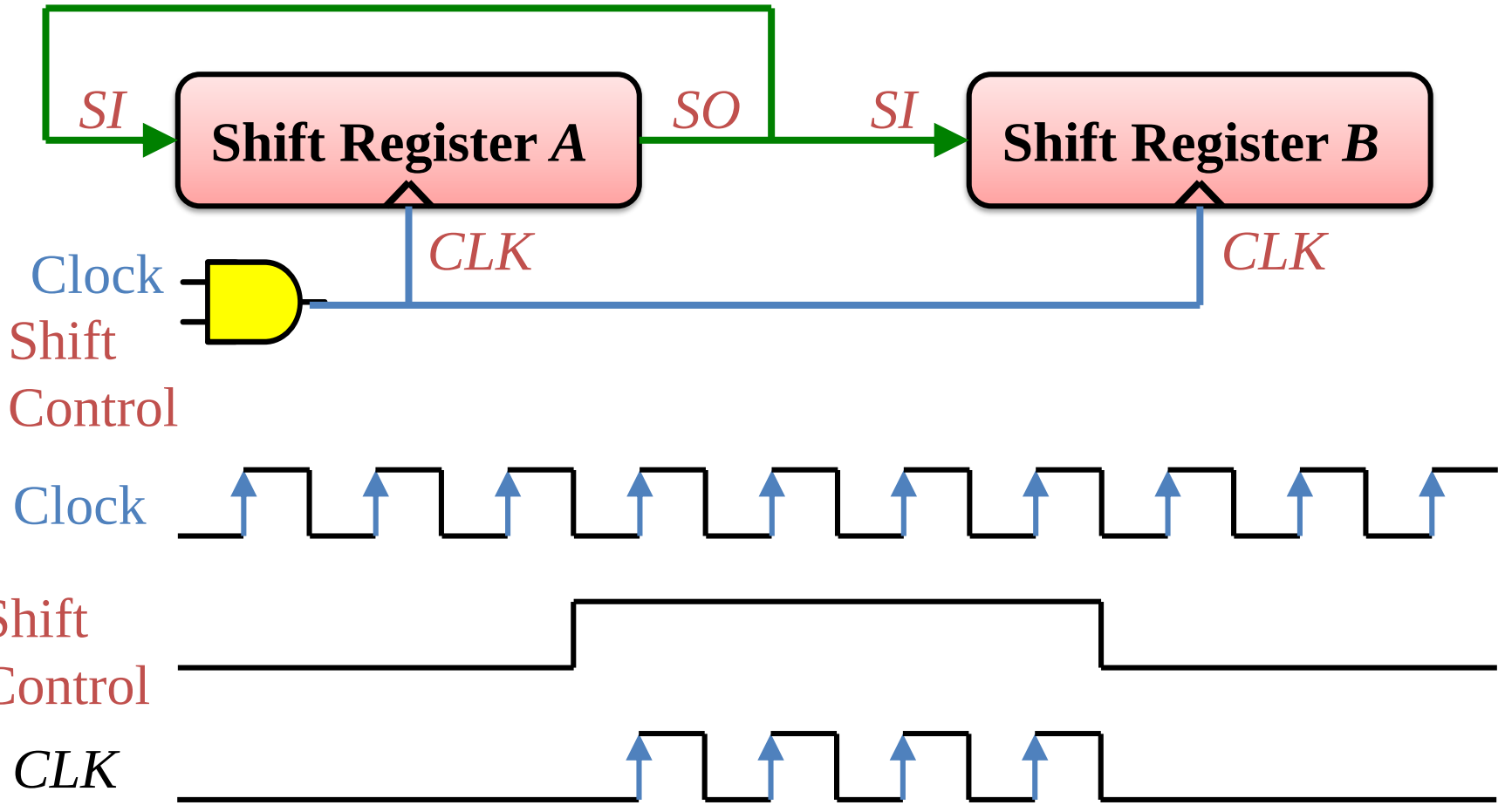
- Register
  - Parallel Load, Parallel out : (PIPO)
  - Serial Load, Wrap around load, Serial out (SISO)
  - PISO, SIPO Register
- Multifunction Register : How to design?
- Memory Design using array of PIPO registers
  - RAM: Random Access Memory

Rotate Register

- Rotate right: Like shift right, but leftmost bit comes from rightmost bit

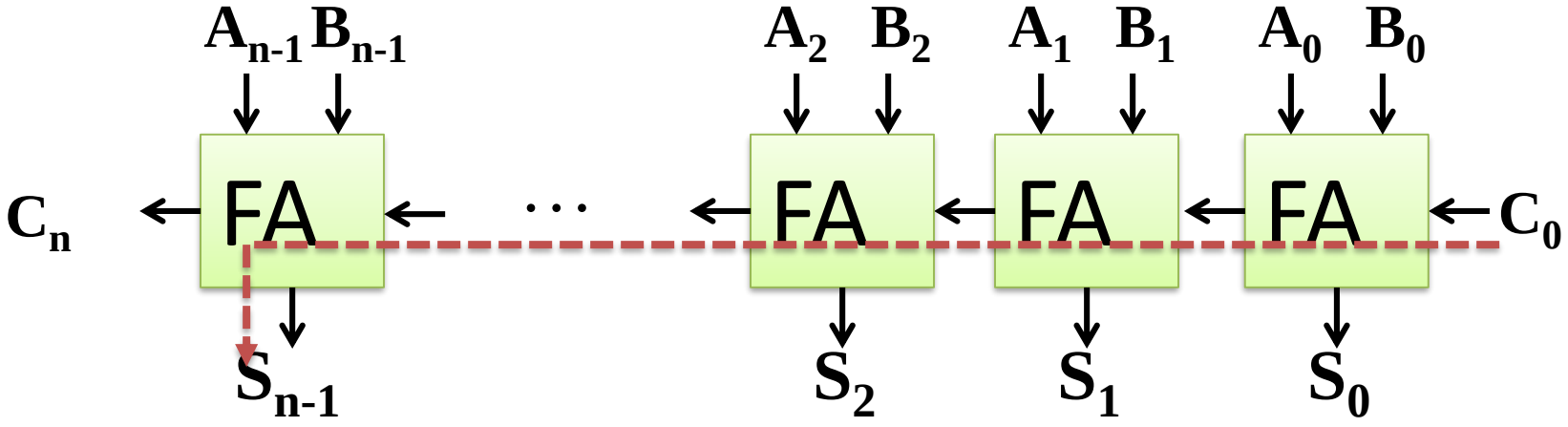


Serial Transfer

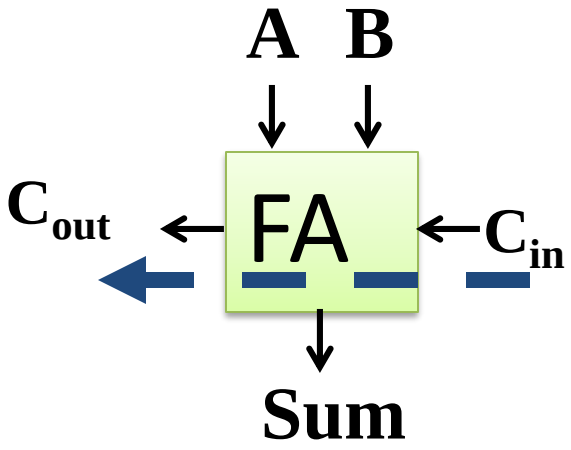


N-Bit RCA: Series of FA Cells

- To add two n-bit numbers

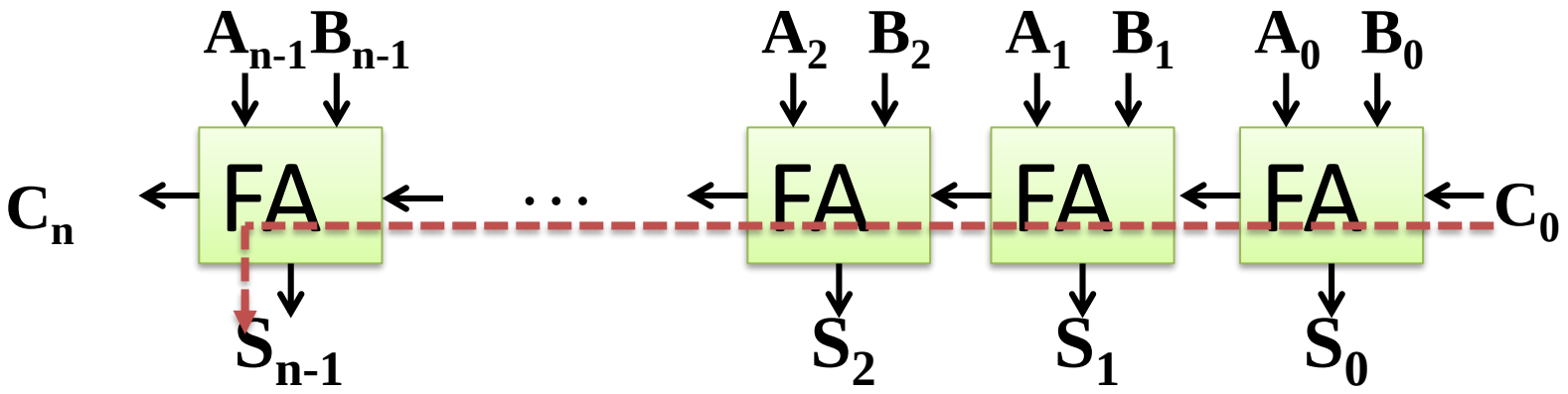


- Adder delay = Tc * n
- Tc = (C_{in} to C_{out} delay) of a FA



N-Bit Ripple-Carry Adder

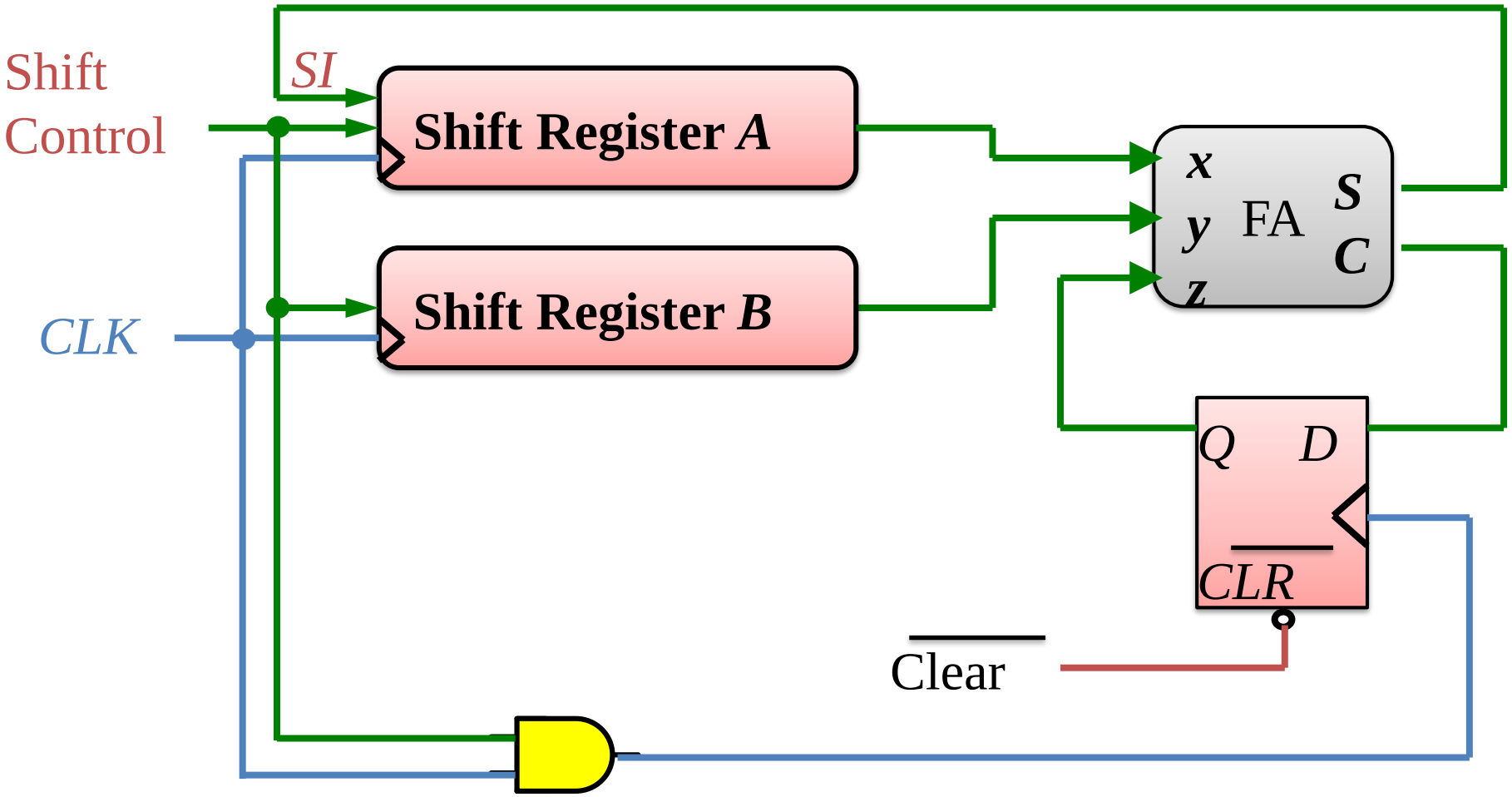
- To add two n-bit numbers



- Any point of time: only one FA is active

Do we require N Full Adder?

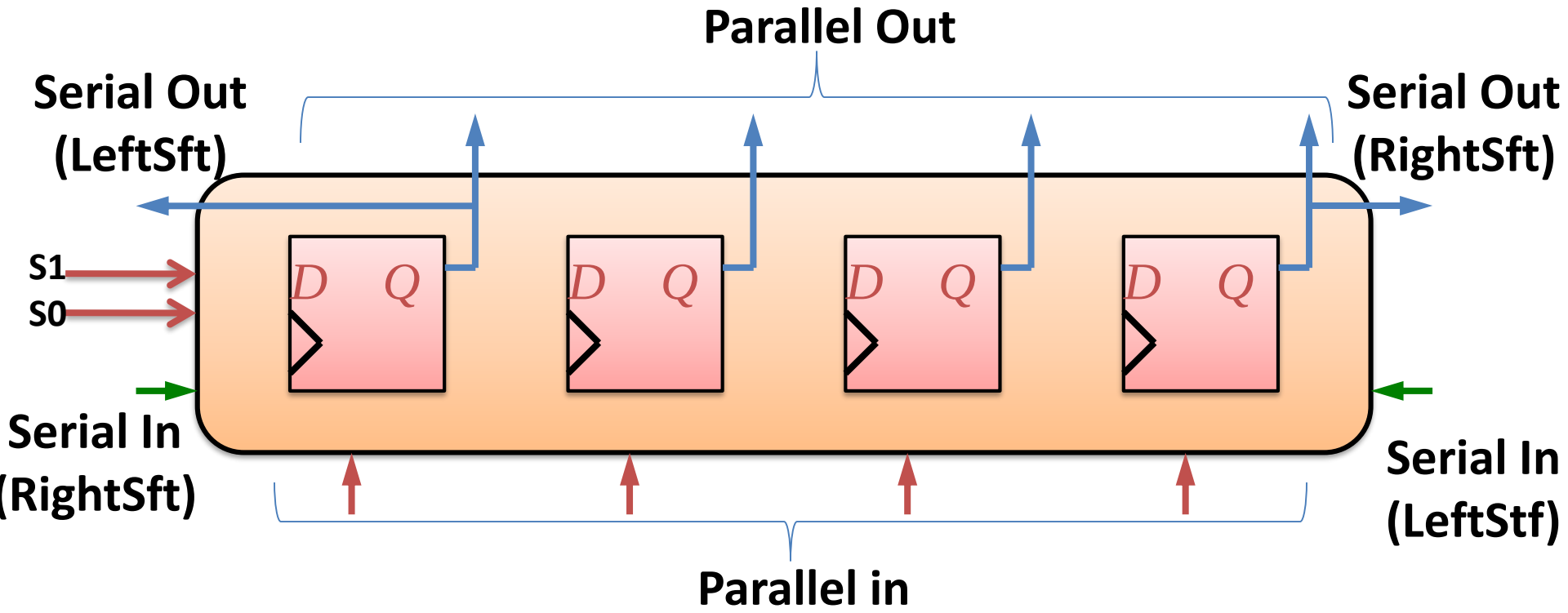
Serial Addition



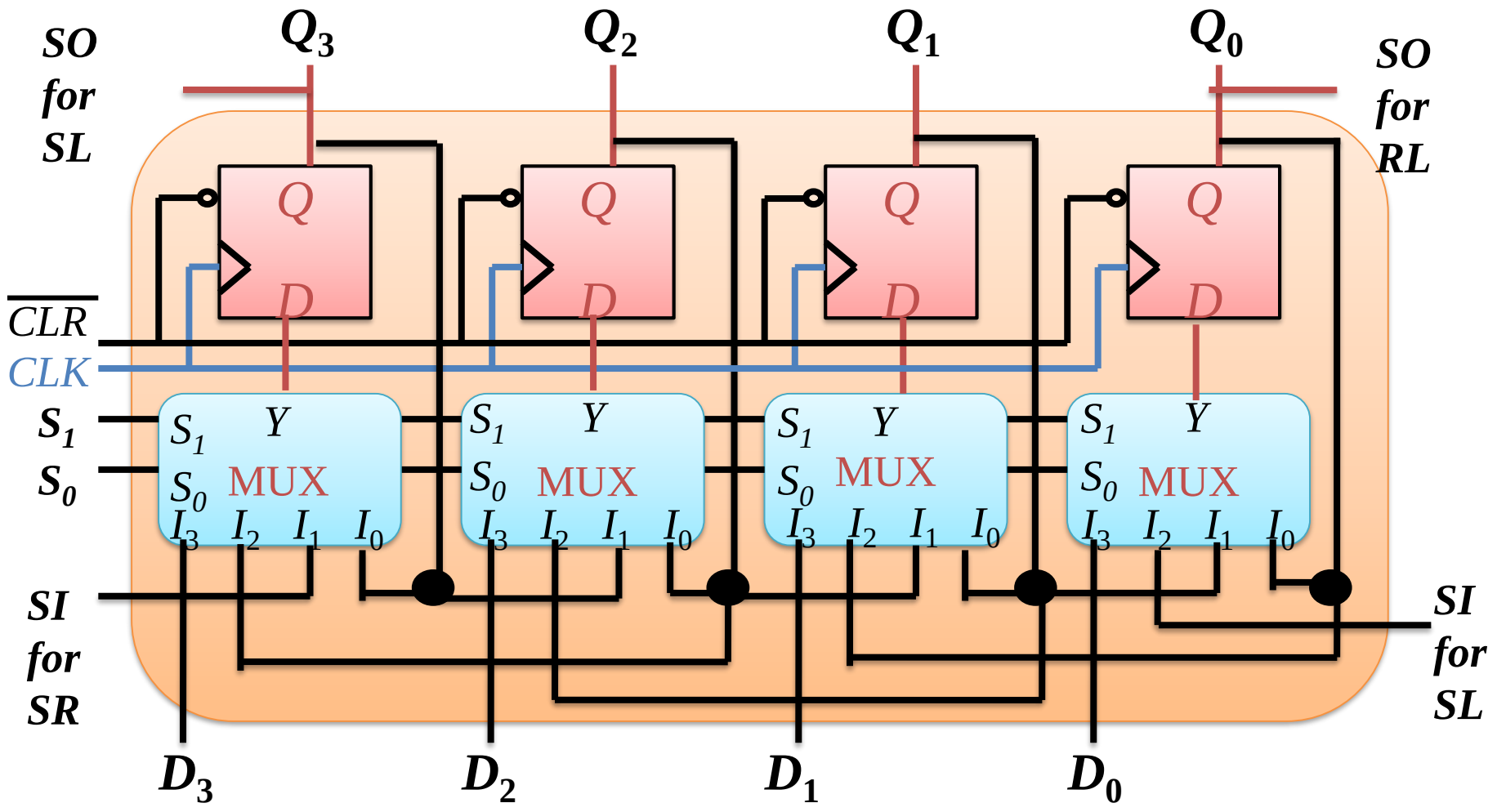
Universal Shift Register

- Parallel-in Parallel-out (PIPO)
- Serial-in Serial-out (SISO)
- Serial-in Parallel-out (SIPO)
- Parallel-in Serial-out (PISO)

Universal Shift Register



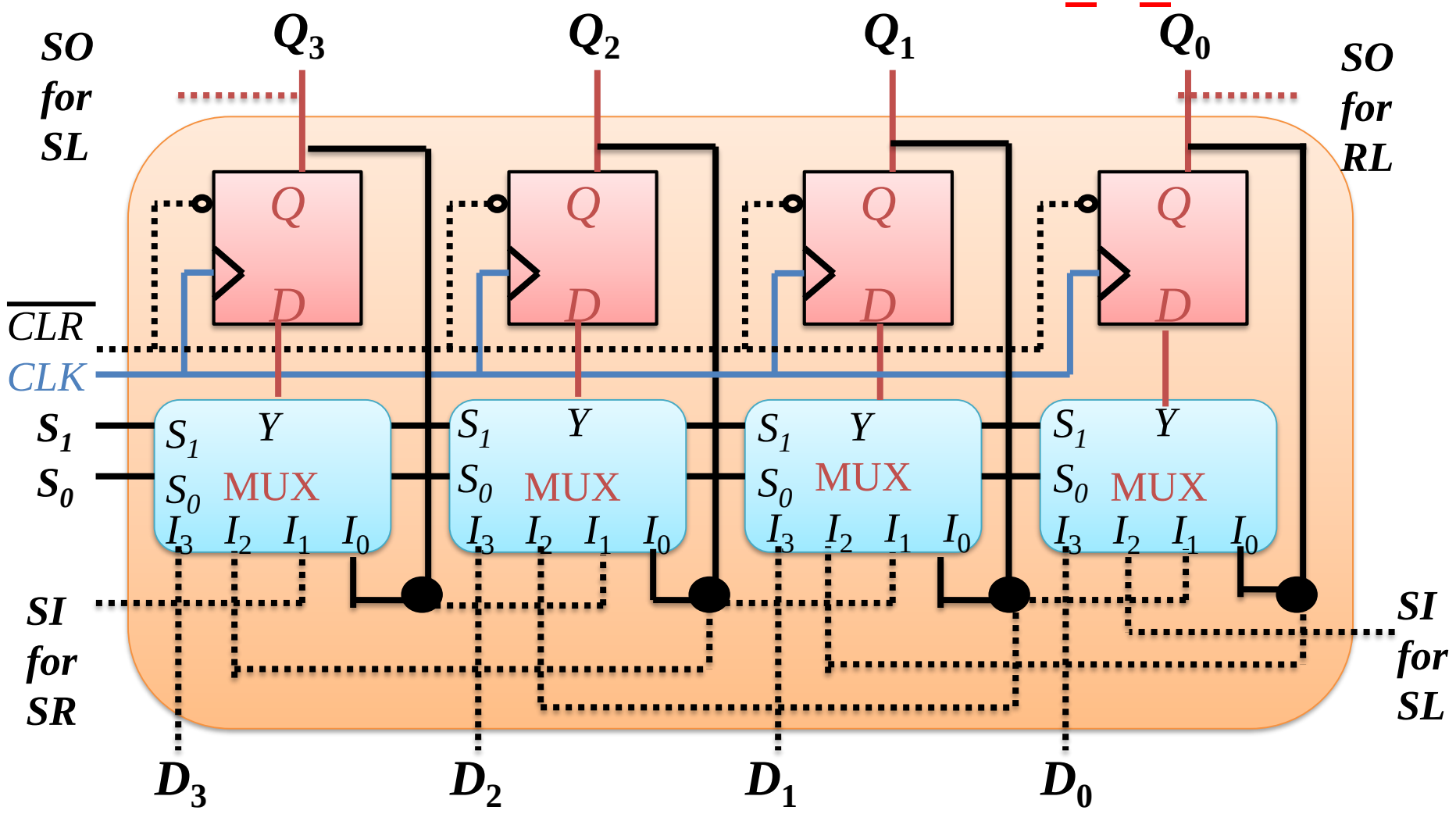
Universal Shift Register



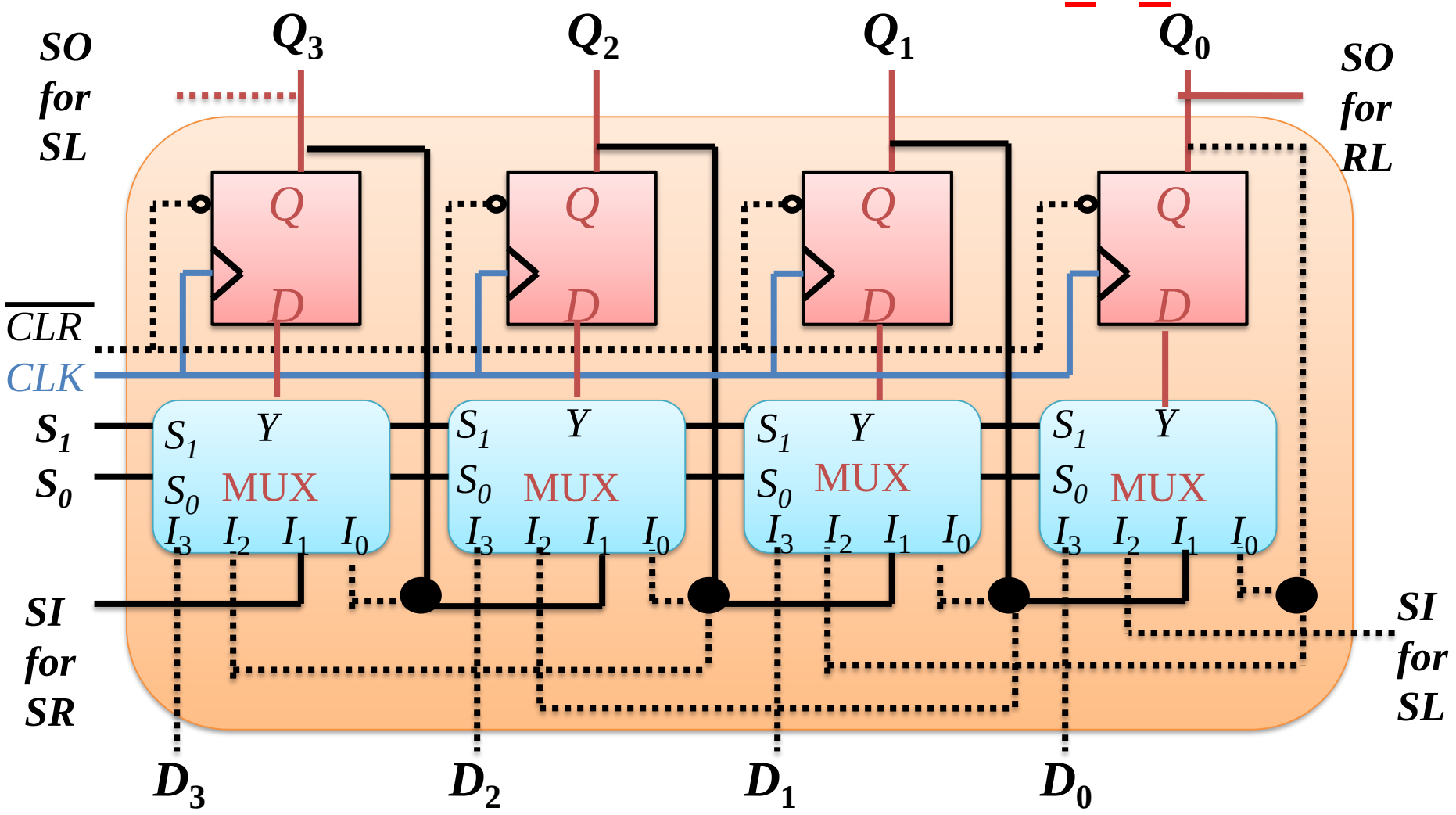
Operation Table for USR

S1	S0	Register Operation
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

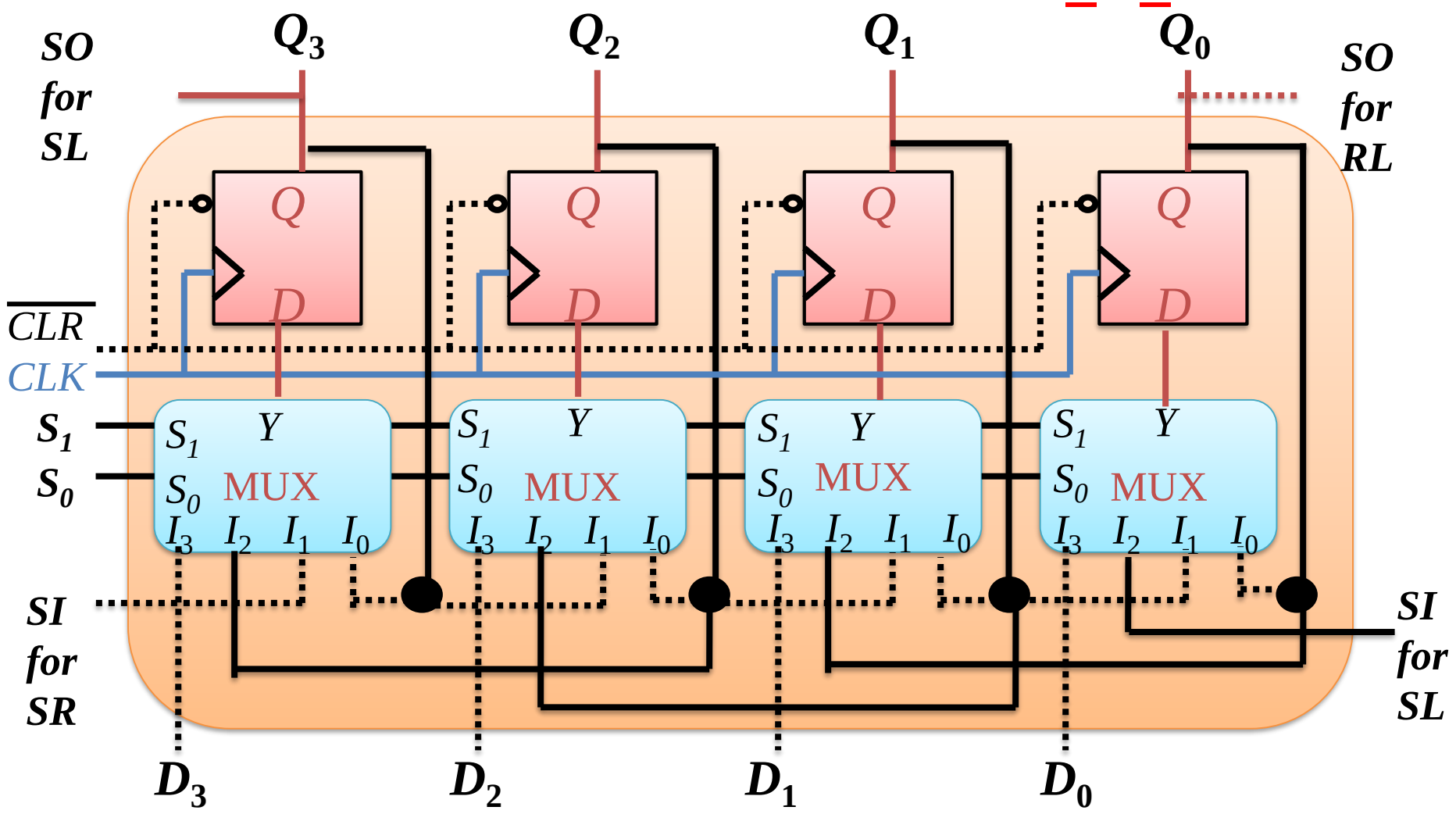
Universal Shift Register: S_1S_0=00



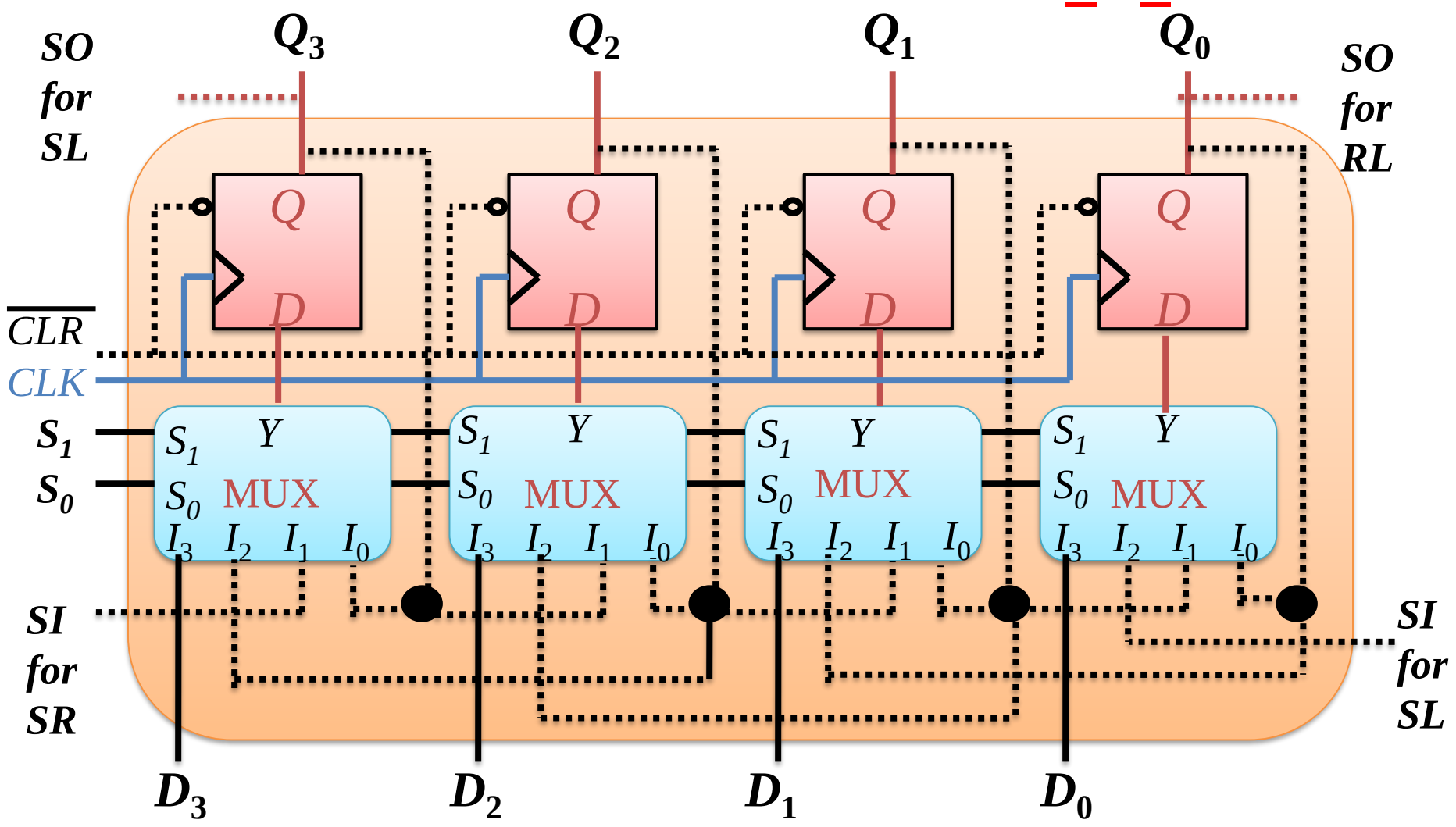
Universal Shift Register: S_1S_0=01



Universal Shift Register: $S_1S_0=10$



Universal Shift Register: $S_1S_0=11$



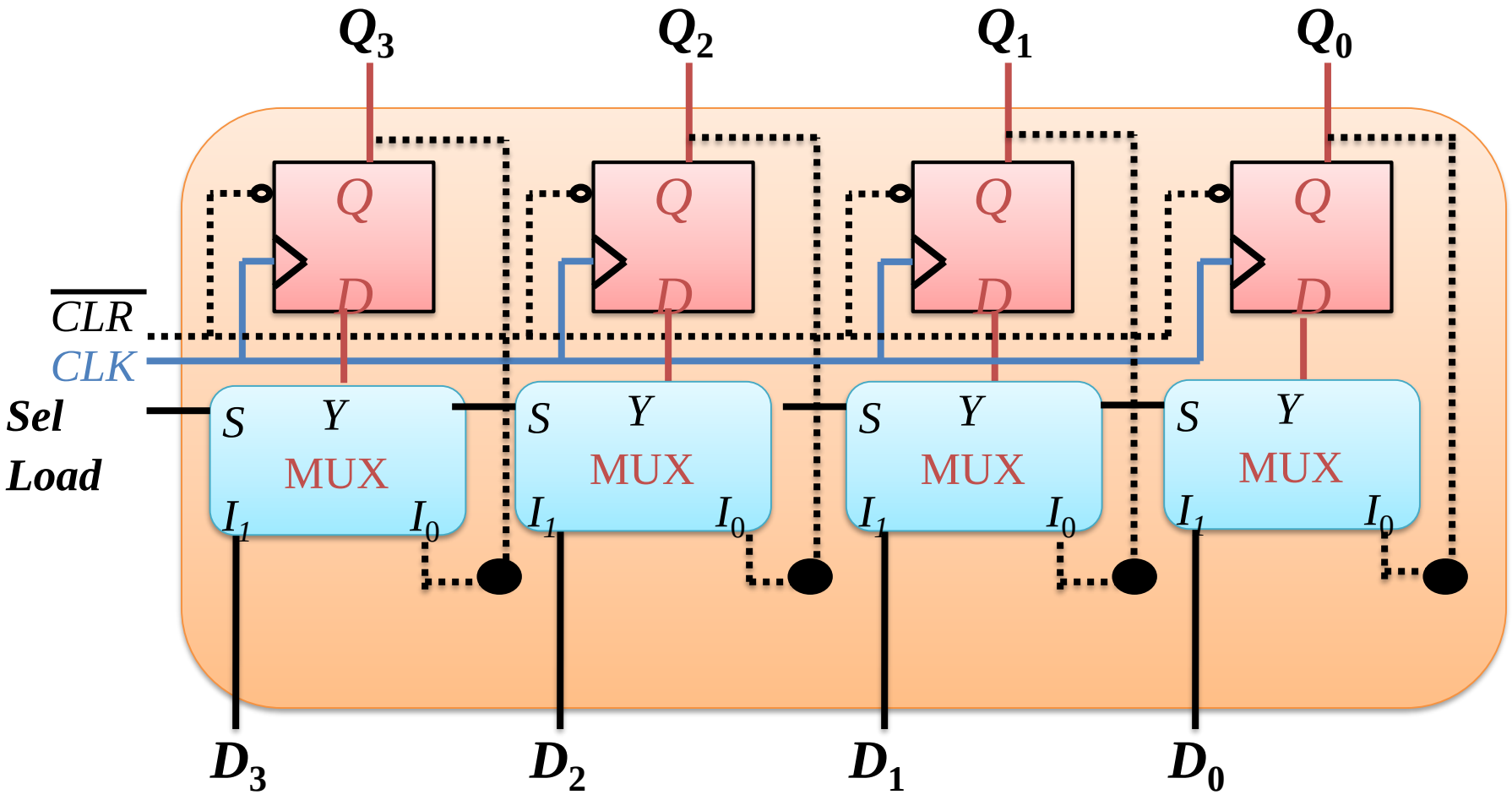
Design of Multifunction Register

- M function N bit Register
  - Last example : 4 functions and 4 bits register
- N number of $ceil[Log_2M]x2^{ceil[Log2M]}$ size Multiplexor (Mux)
  - For 4 function 2x4 Mux (**4 to 1 Mux**), 2 select line
  - For 5 function 3x8 Mux (**8 to 1 Mux**), 3 select line
- Extra functions of Mux need to shunted (ignored) to do no work
  - For 5 function need a 3x8 Mux, we need to shunt 8-5=3 lines shunted (ignored) to do no work

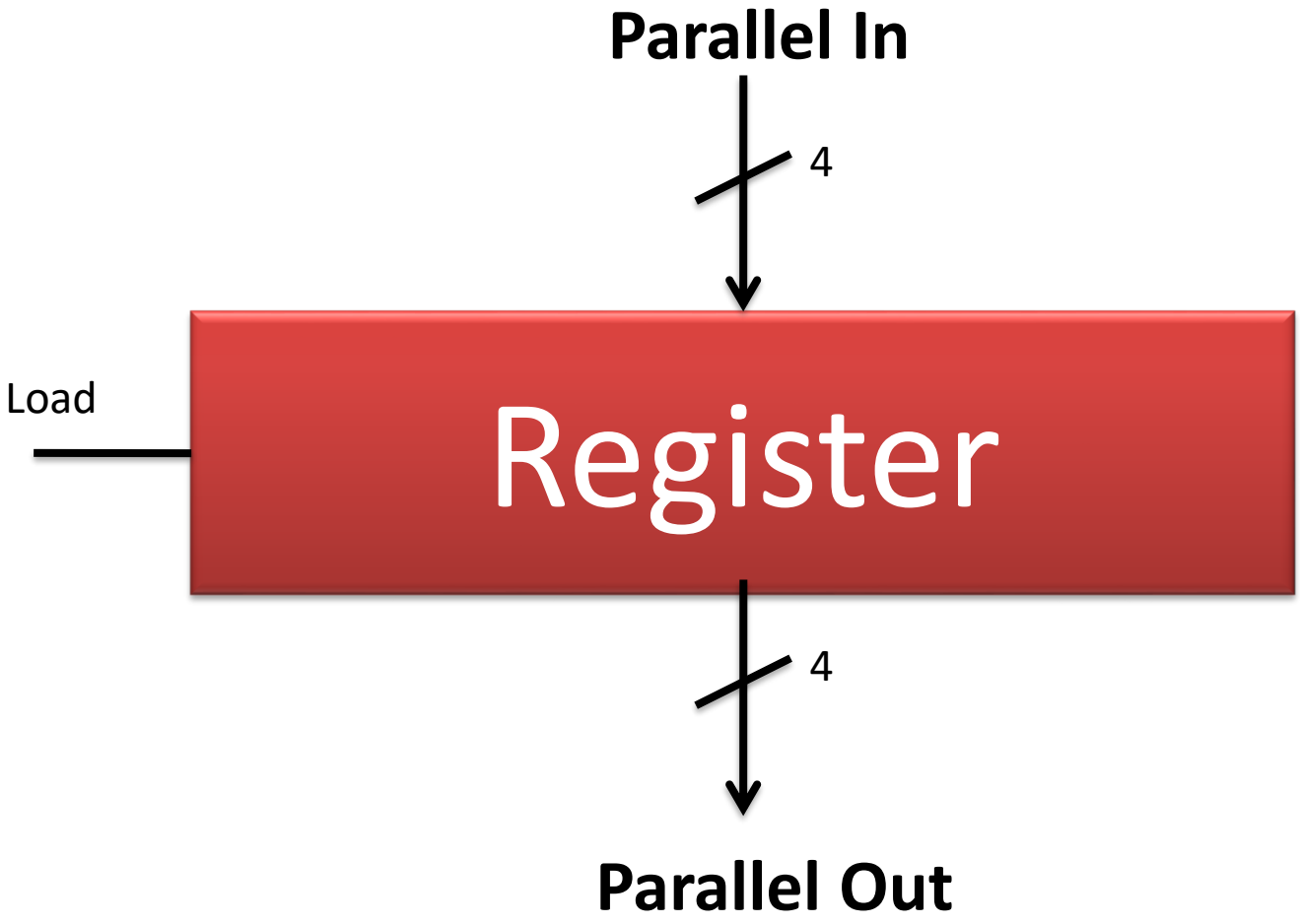
Memory

- Universal register : One register with many functionality
- Many registers clubbed with less functionality
  - No Shift
- Parallel load (In) or Parallel Out to a specific register
- Multiplexors used for selection of resisters

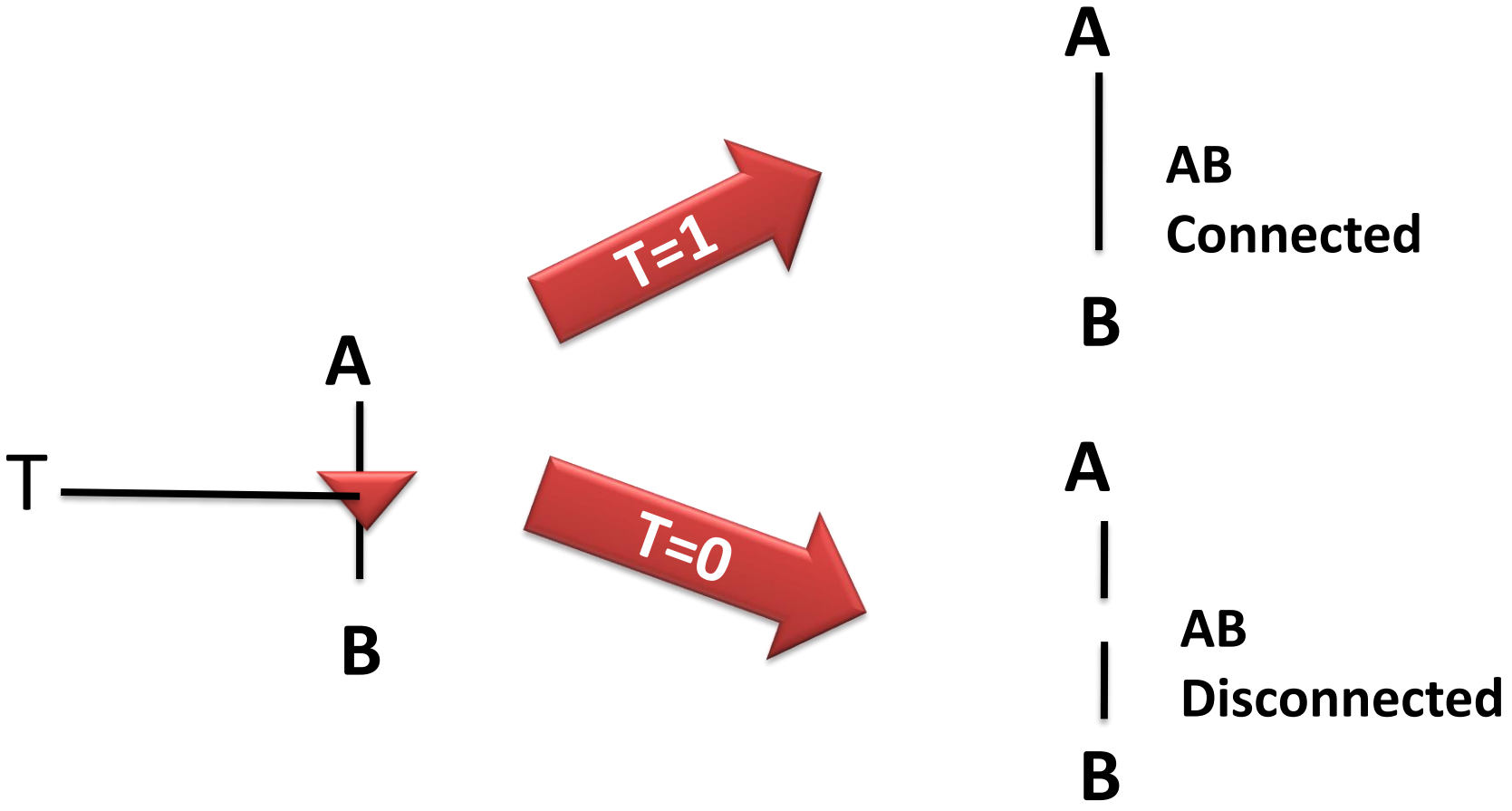
Register(PIPO)



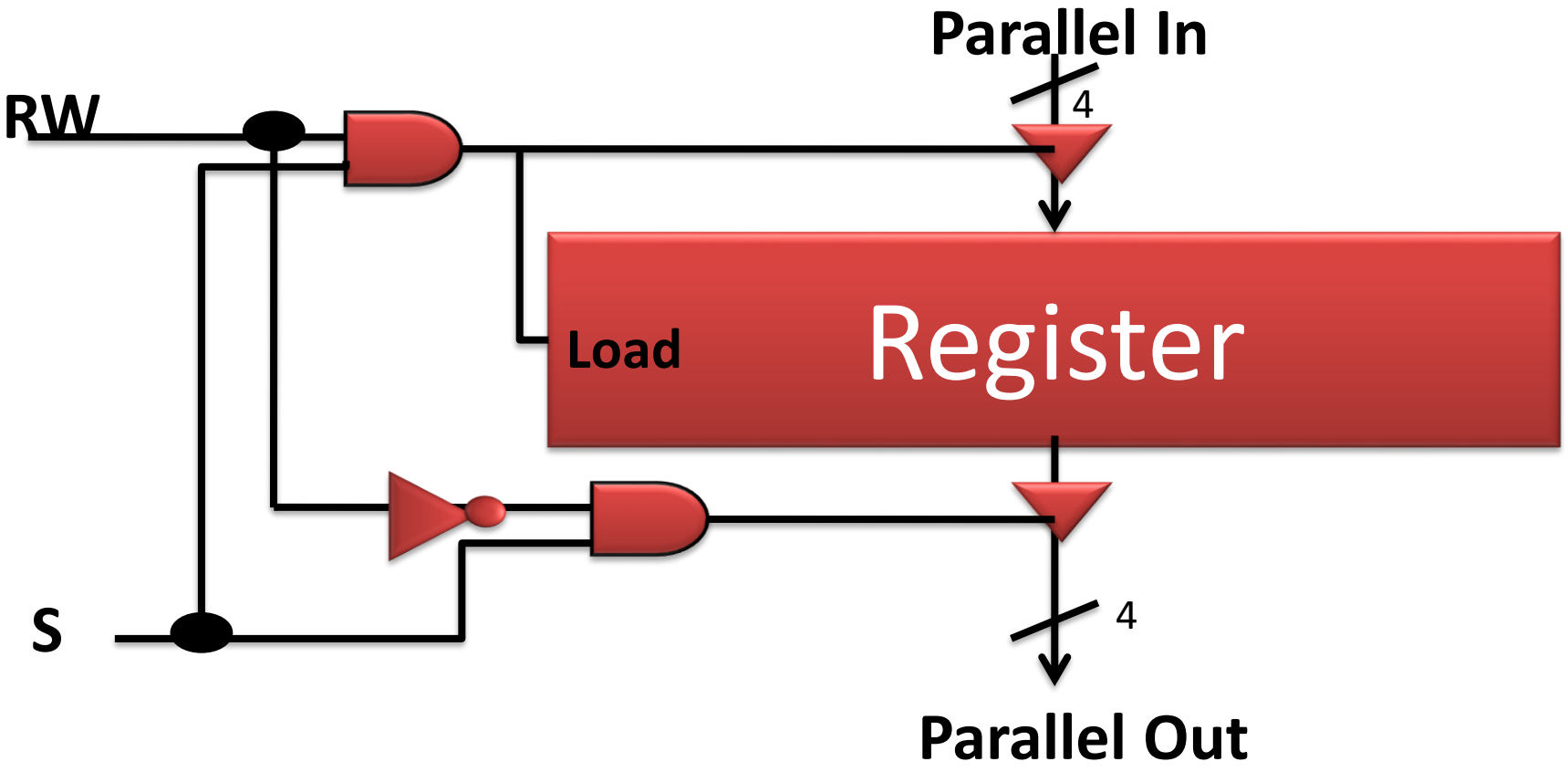
Register(PIPO)



Tri-state Buffer



Register with Read and write control

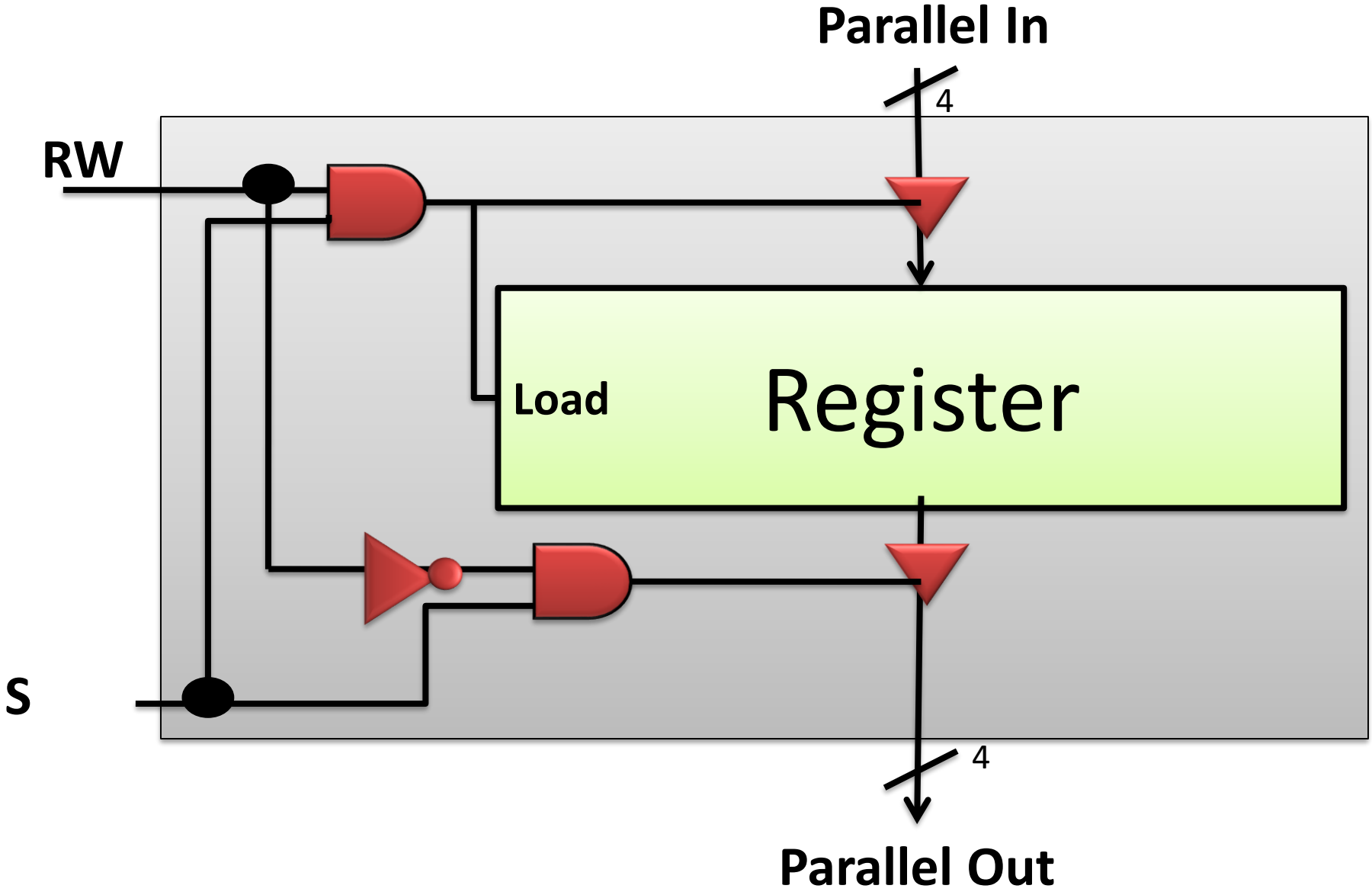


If S =0, TS1 and TS2 will be open

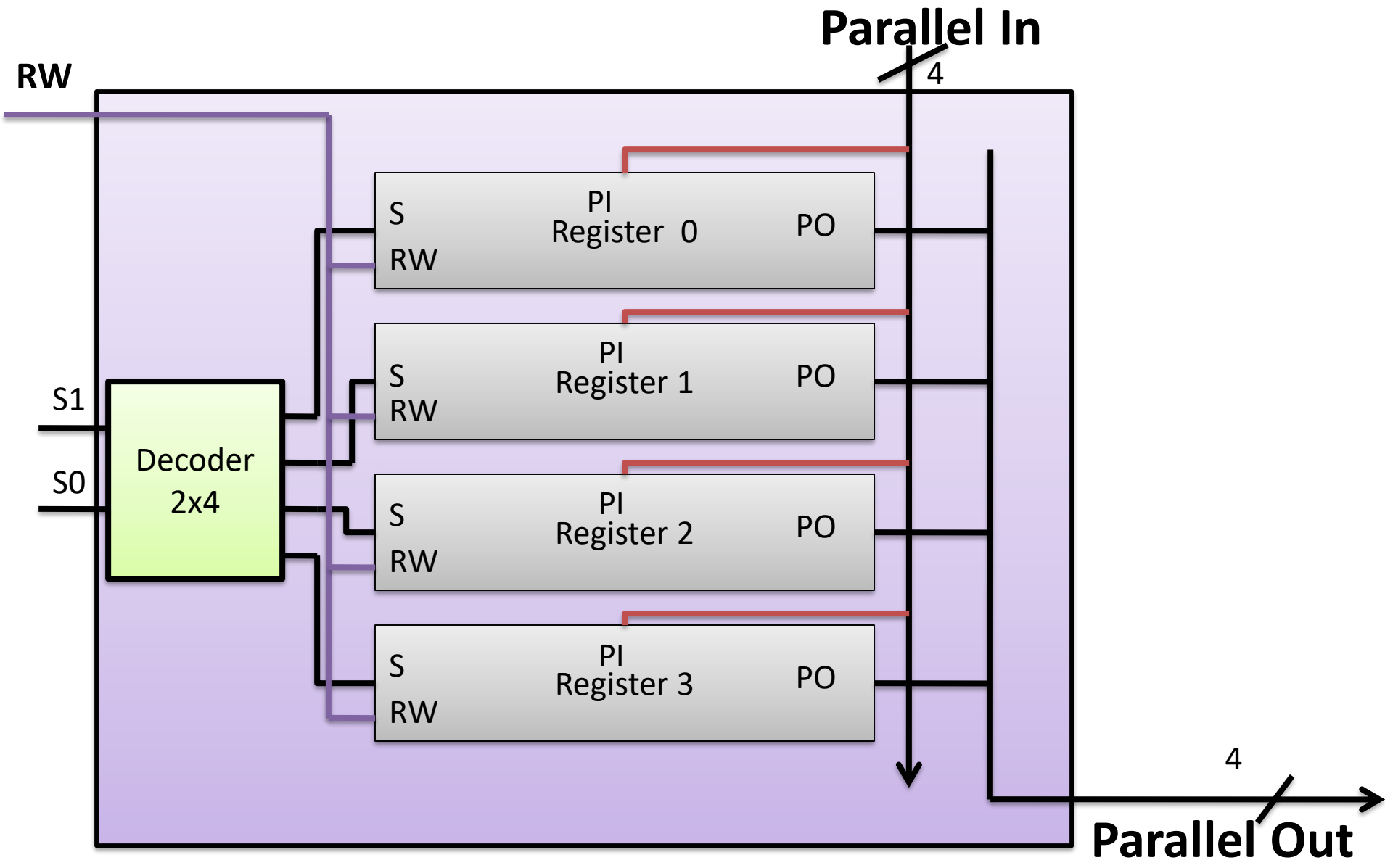
S=1, RW=1 , Write to Register 4 bit of data

S=1, RW=0, Read data from Register

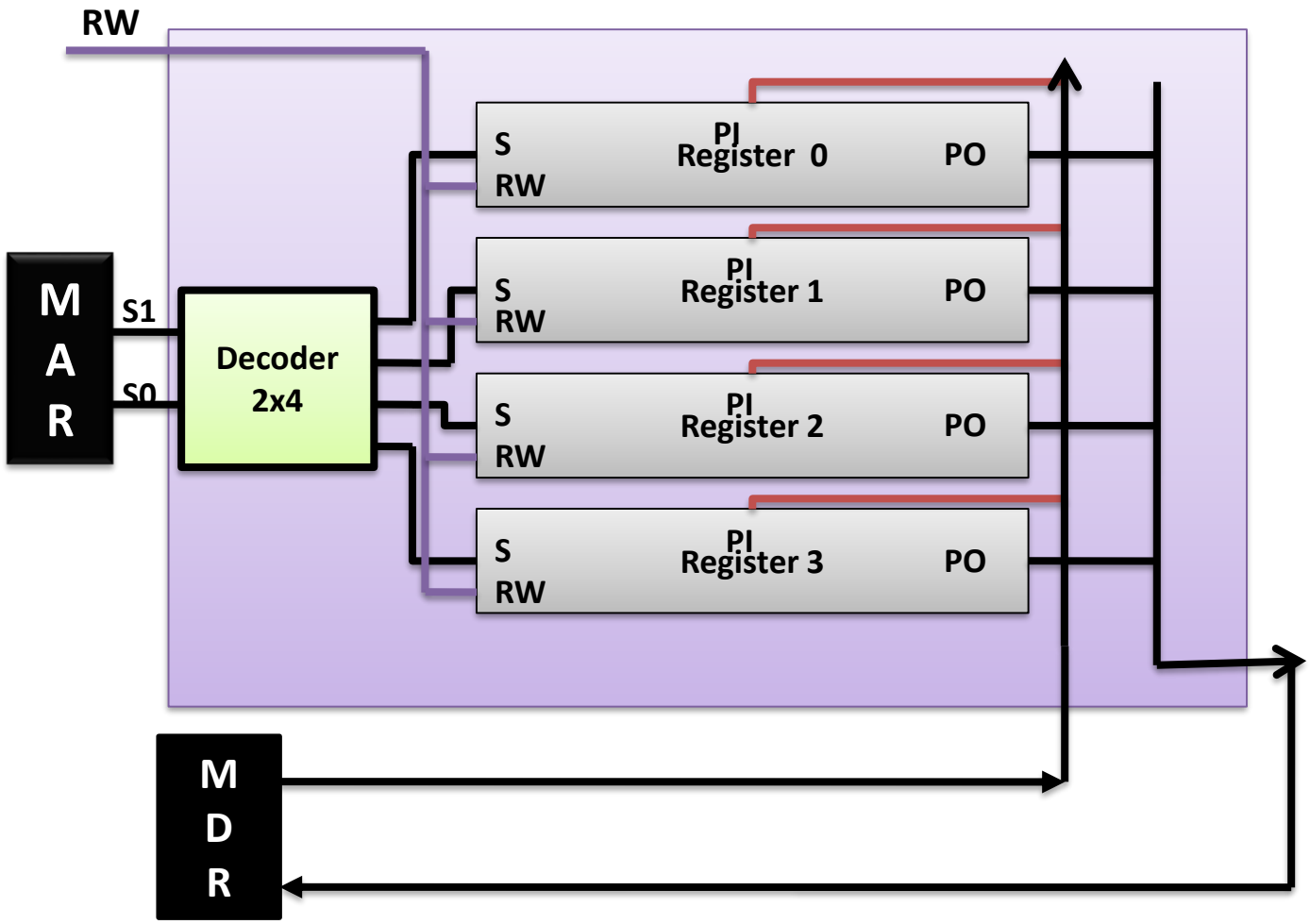
Register with Read and write control



Many Register with RW control



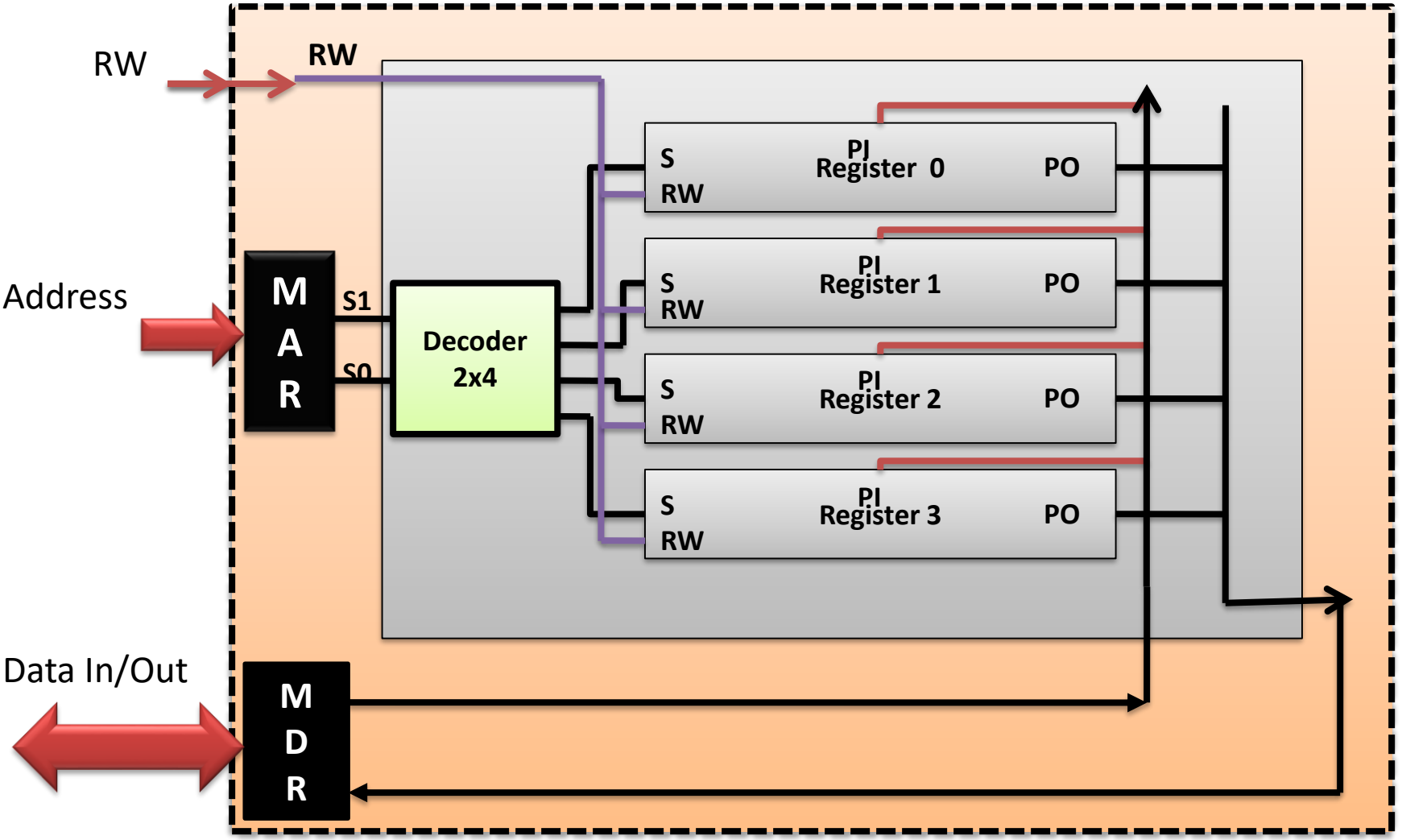
Memory with MAR and MDR



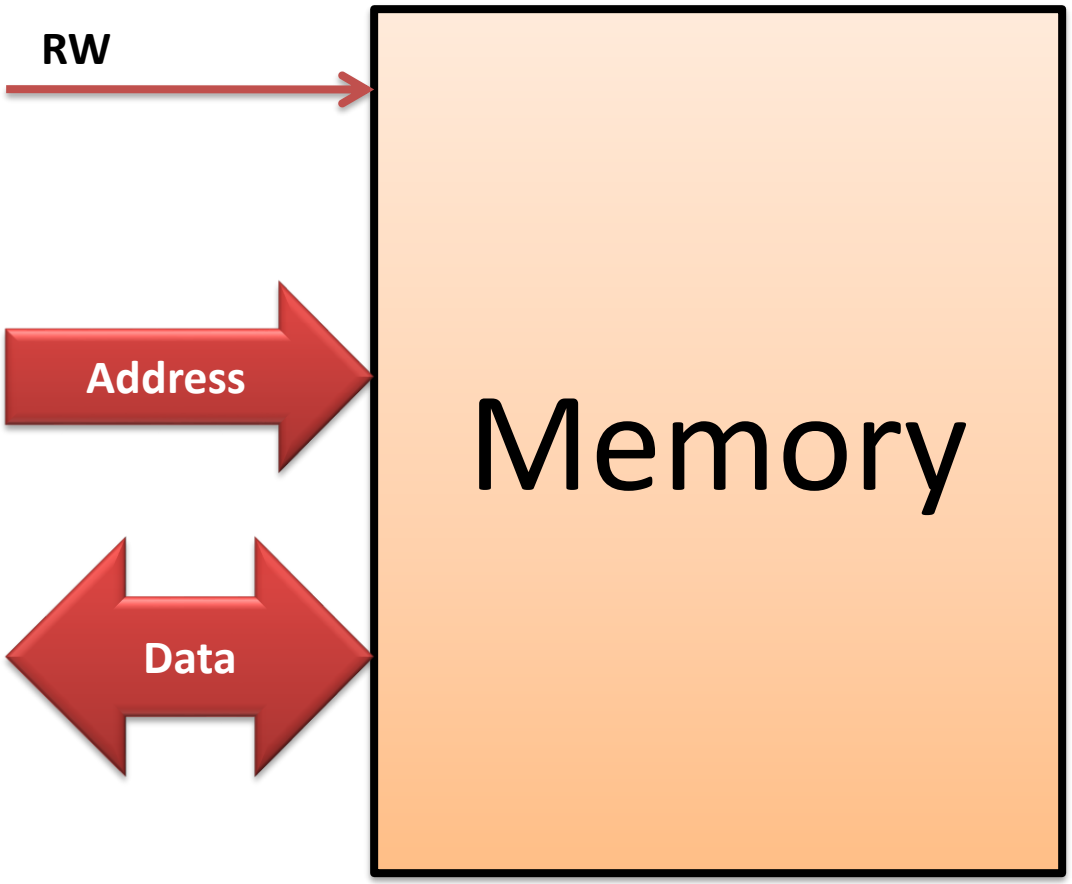
MAR: memory Address Register

MDR: Memory Data Register

Many Register with RW control: 4 four bit word Memory



General Memory



Memory : Locations & Word size

- ADDRESS decides the number of memory location
- MDR size : decides the WordSize
- Number of registers : 2+NumLocations
  - $2 + 2^{\text{AddressSize}}$
  - 1 for MBR, 1 for MAR
- NumFF= MARsize+MDRsize+NumLoc*MDRSize

Designing 1KB Mem using two 1KN Mem