CS 223 Computer Architecture & Organization

Computer Fundamentals

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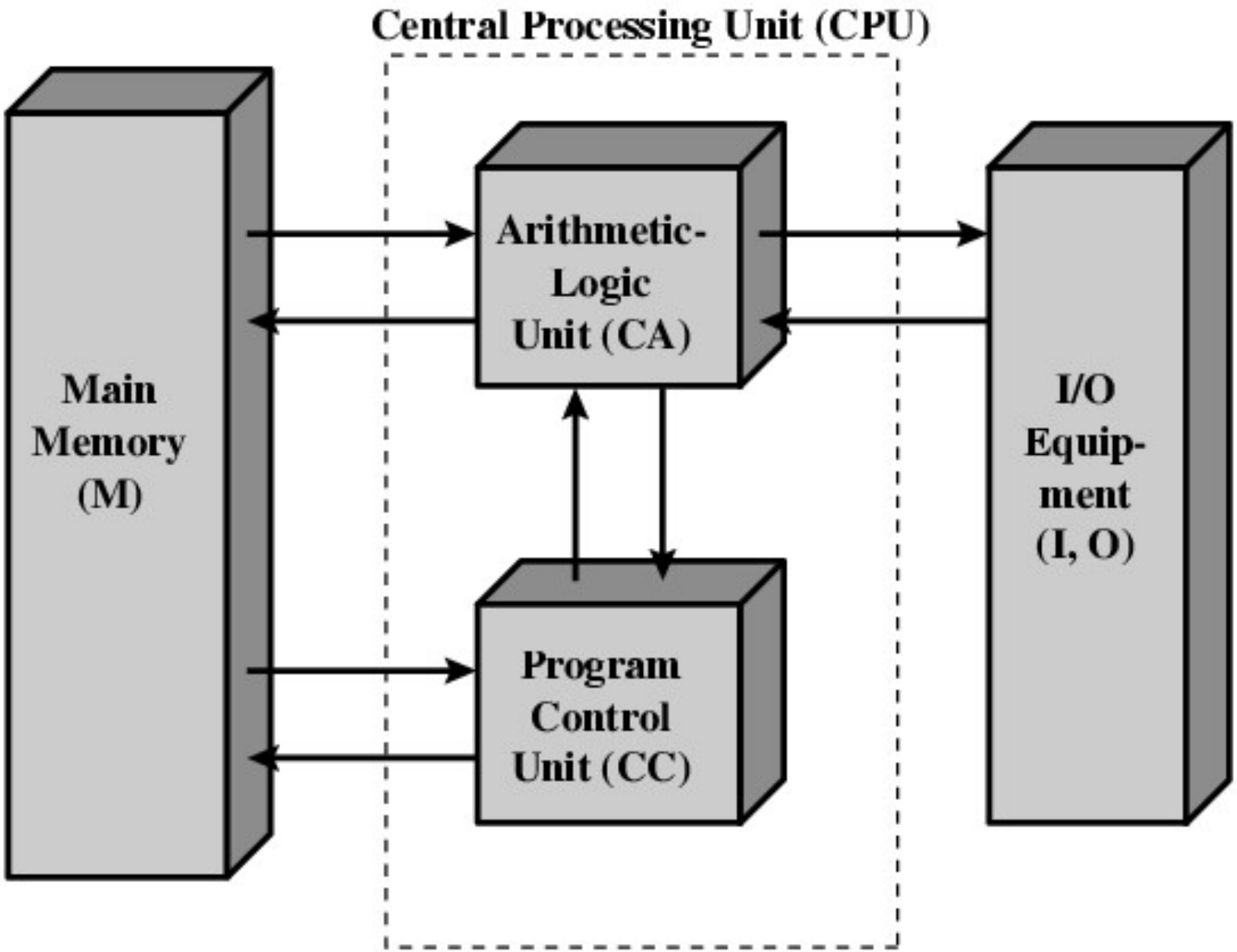
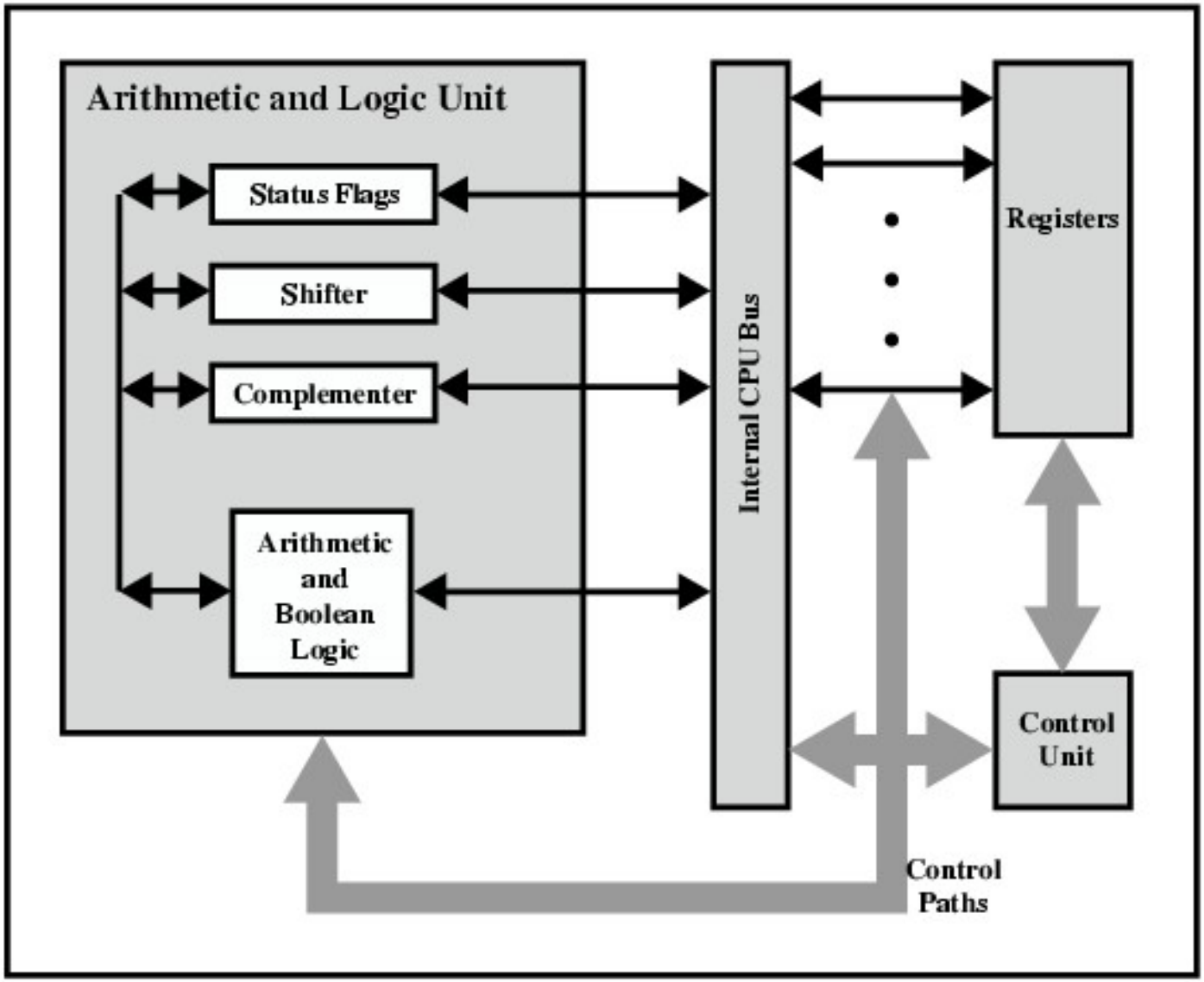
Von Neumann Principle

- Stored Program concept
- **Main memory** storing programs and data
- **ALU** operating on binary data
- **Control unit** interpreting instructions from memory and executing
- **Input and output equipment** operated by control unit
- Princeton Institute for Advanced Studies
  - IAS
- Completed 1952

Structure of Von Neumann machine



CPU Internal Structure

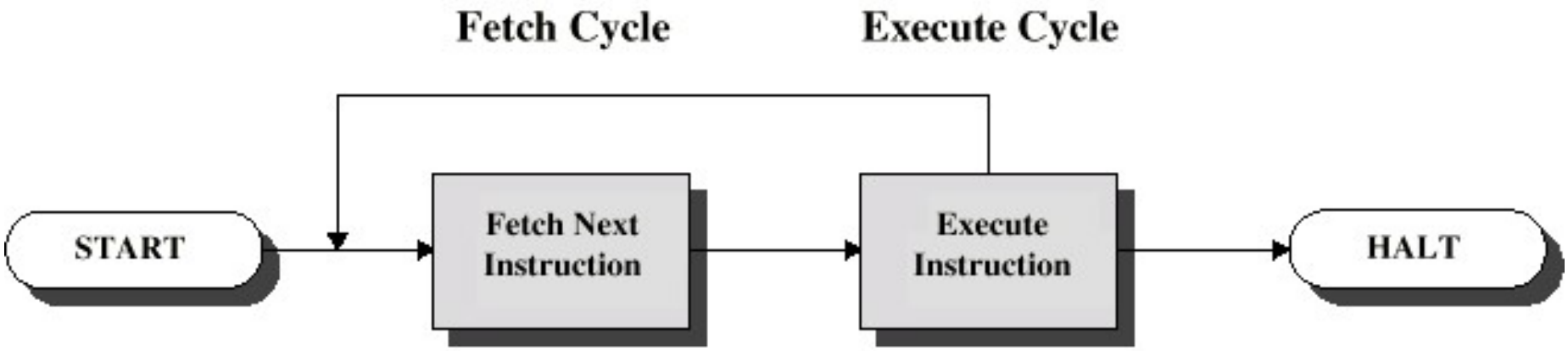


What is a program?

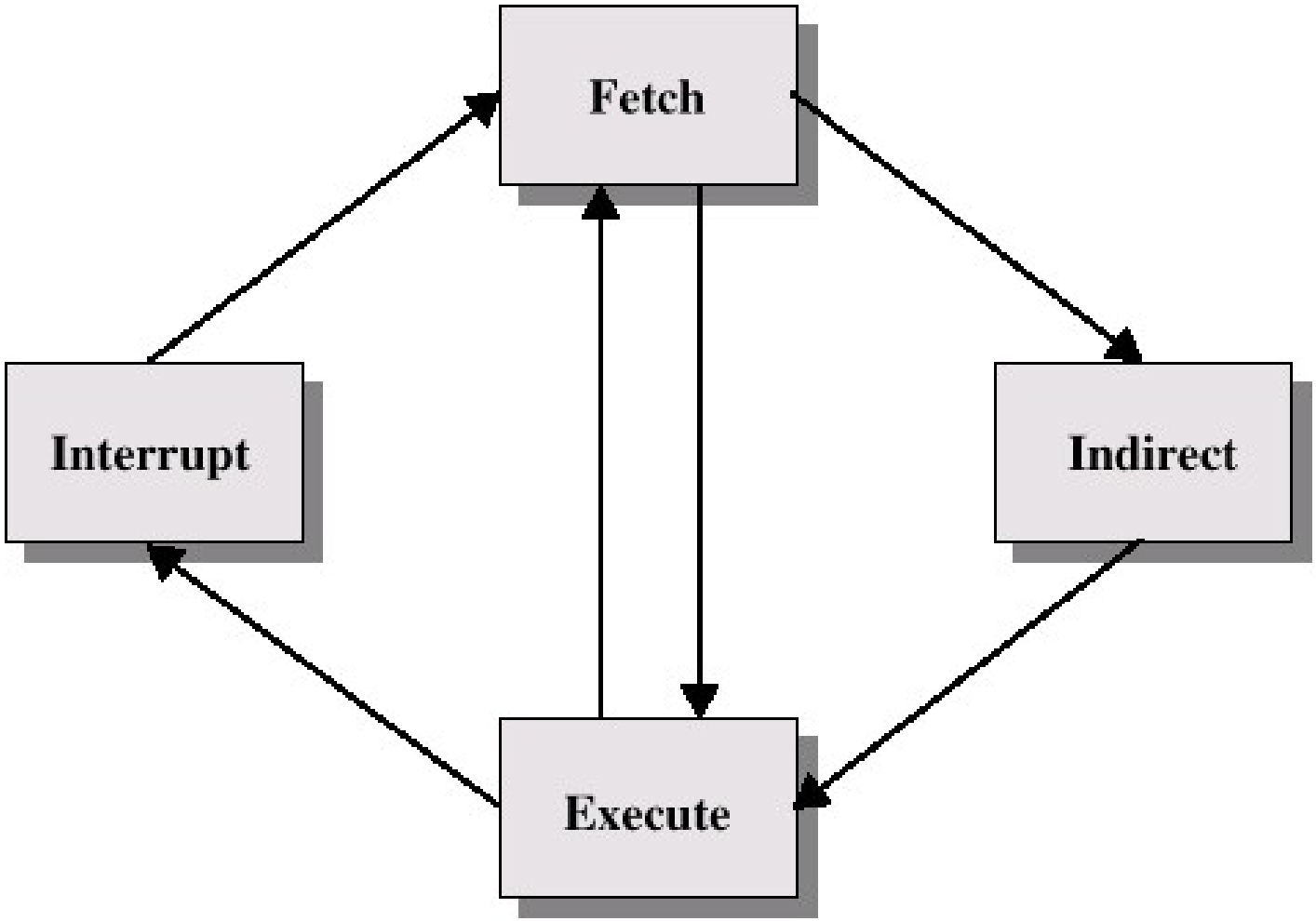
- A sequence of steps (instructions)
- For each step, an arithmetic or logical operation is done
- For each operation, a different set of control signals is needed

Instruction Cycle

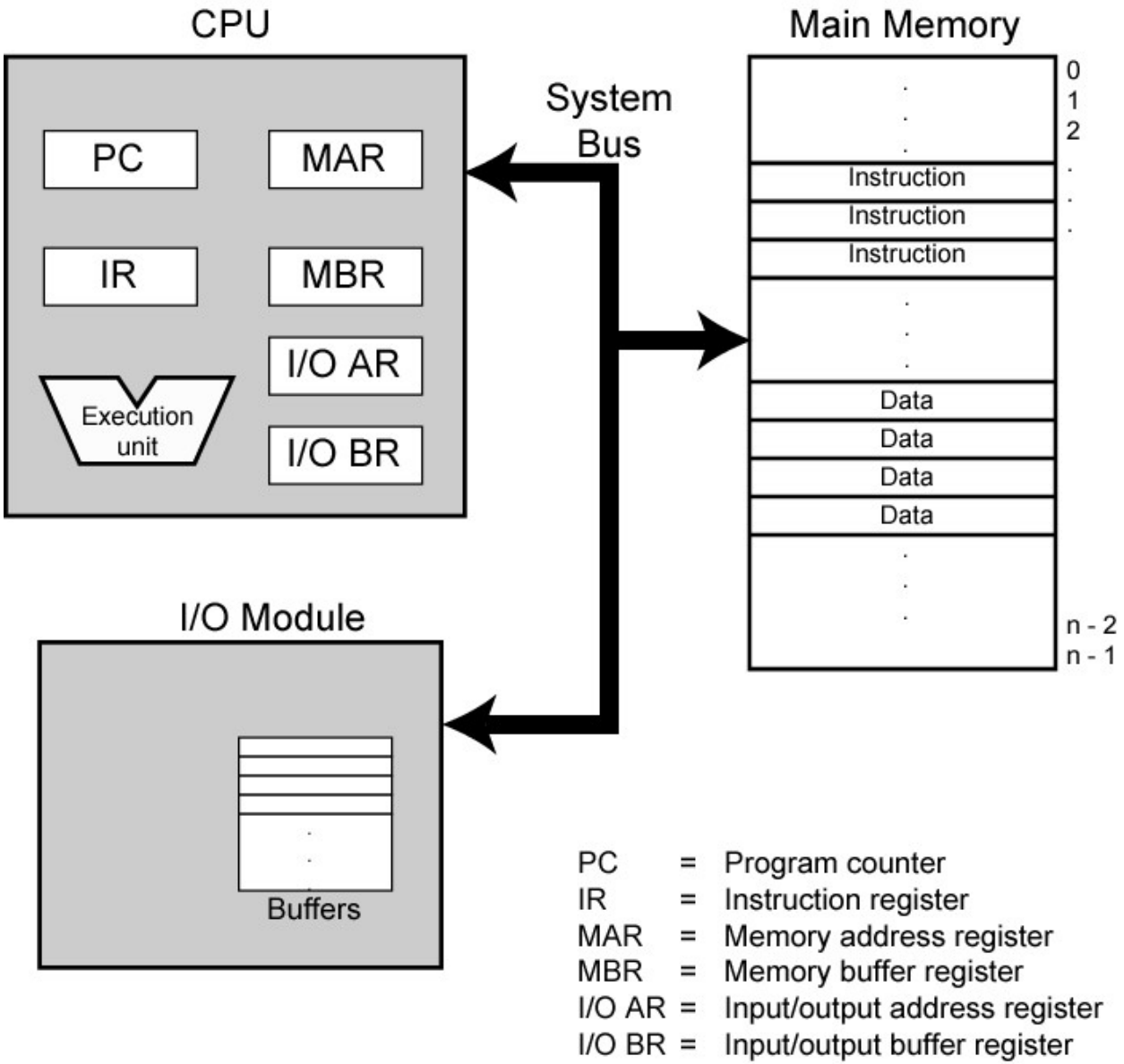
- Two steps:
  - Fetch
  - Execute



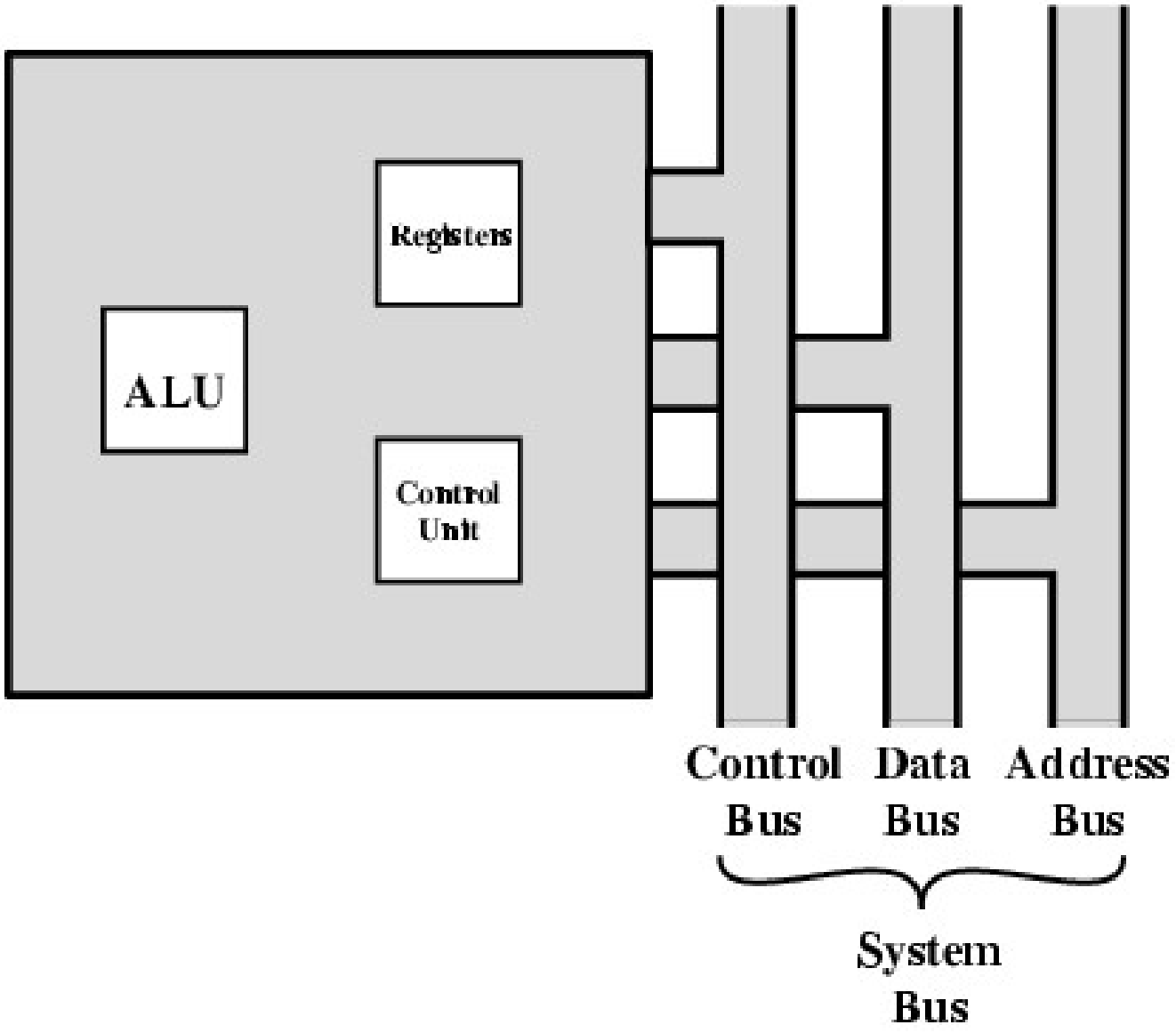
Instruction Cycle with Indirect



Computer Components: Top Level View



CPU With System Bus



What is a Bus?

- A communication pathway connecting two or more devices
- Usually broadcast
- Often grouped
  - A number of channels in one bus
  - e.g. 32 bit data bus is 32 separate single bit channels

Advantage of Bus System

- Multiple devices may be connected to a bus
- Transfer data between devices through bus

Data Bus

- Carries data
  - Remember that there is no difference between “data” and “instruction” at this level
- Width is a key determinant of performance
  - 8, 16, 32, 64 bit

Address bus

- Identify the source or destination of data
- e.g. CPU needs to read an instruction (data) from a given location in memory

Address bus

- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space

Control Bus

- Control and timing information
  - Memory read/write signal
  - Interrupt request
  - Clock signals

Address and Data of a Memory Location

Address of a Memory Location
Data of a memory Location

Interface between CPU and Memory

MAR: Memory Address Register
MBR: Memory Buffer Register

Data movement: Memory and CPU register

Interface between CPU and Memory

IR: Instruction Register
PC: Program Counter

Data movement: Between CPU registers

Fetch Cycle

- Program Counter (PC) holds address of next instruction to fetch
- Processor fetches instruction from memory location pointed to by PC
- Increment PC
  - Unless told otherwise
- Instruction loaded into Instruction Register (IR)
- Processor interprets instruction and performs required actions

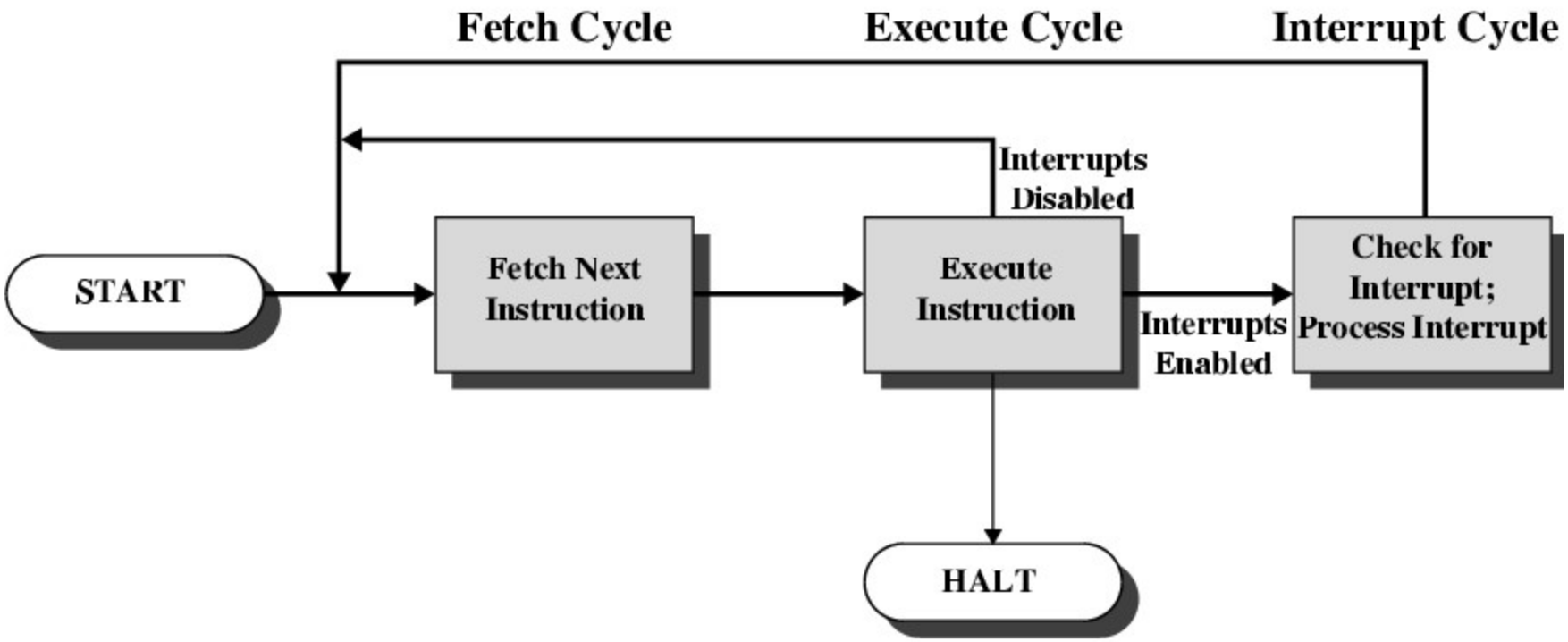
Indirect Cycle

- May require memory access to fetch operands
- Indirect addressing requires more memory accesses
- Can be thought of as additional instruction subcycle

Execute Cycle

- Processor-memory
  - data transfer between CPU and main memory
- Processor I/O
  - Data transfer between CPU and I/O module
- Data processing
  - Some arithmetic or logical operation on data
- Control
  - Alteration of sequence of operations
  - e.g. jump
- Combination of above

Instruction Cycle with Interrupts



Reference

Computer Organization and Architecture –
Designing for Performance
William Stallings

Chapter 3: Page no. 56 – 79 (Seventh Edition)
Page No.: 66 – 93 (Eighth Edition)