1.1 Implementation of AND gate

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity andGate is
   Port ( a : in  STD_LOGIC;
          b : in  STD_LOGIC;
          c : out  STD_LOGIC);
end andGate;

architecture Behavioral of andGate is

begin
          c <= a and b;
end Behavioral;
```