Phase Lock Loop

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1 Introduction

Phase Locked Loop is used to synchronize the converter to the grid. The grid frequency varies throughout the day. This is an example from North East Region Load Dispatch center. The reason that the VSC must be in same phase is that the current output $I_1 + I_2$ develop error with time.

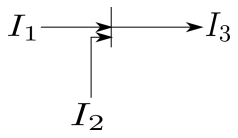


Figure 1: Current injection in bus

Example

$$I_3 = I_1 + I_2 \tag{1}$$

Say, I_1, is the grid current given as

$$I_1 = \omega_0 t \tag{2}$$

and I_2, is the current injected by VSC given as

$$I_2 = \omega_0 t \tag{3}$$

Now if the freq. changed, the I_2 changed as

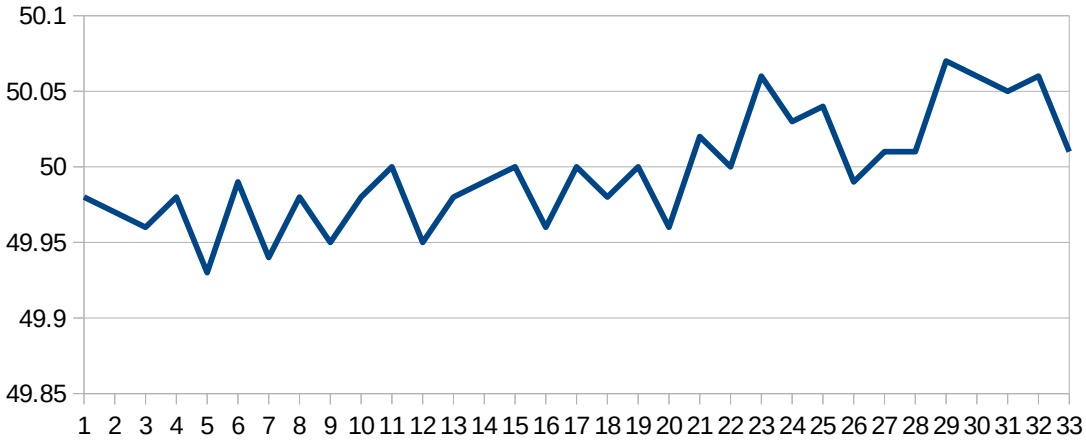
$$I_{2,new} = (\omega_0 - 0.2\pi)t \tag{4}$$

If the freq. output is not changed the error increases with time.

Frequency (1 Aug 2021)

North East Region Load Dispatch Center

12 am to 8 am



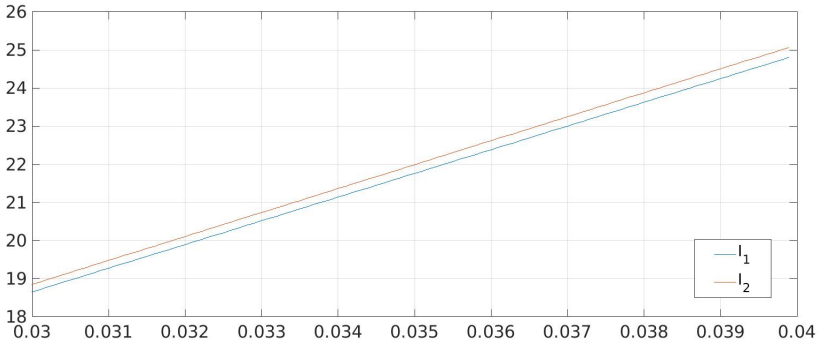


Figure 2: Error with time

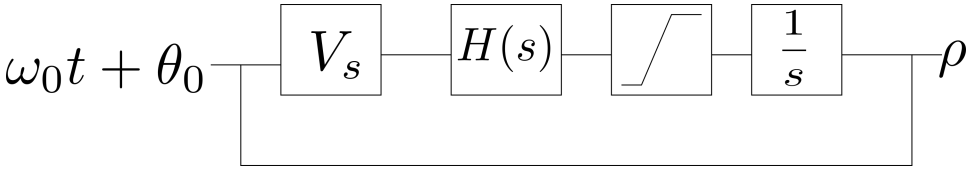


Figure 3: Control Block Diagram for PLL

2 Theory

PLL tracks the phase angle of grid.

$$V_{sd} = V_s cos(\omega_0 t + \theta_0 - \rho) \tag{5}$$

$$V_{sq} = V_s sin(\omega_0 t + \theta_0 - \rho) \tag{6}$$

If $\rho = \omega_0 t + \theta_0$, V_{sq} corresponds to 0. Thus, regulating V_{sq} to zero, phase angle can be tracked.

$$\frac{d\rho}{dt} = \omega(t) \tag{7}$$

$$\omega(t) = H(p)V_{sq} \tag{8}$$

$$\frac{d\rho}{dt} = H(p)V_s sin(\omega_0 t + \theta_0 - \rho) \tag{9}$$

If PLL, tracks ρ, then $sin(\omega_0 t + \theta_0 - \rho)$ can be approximated as $\omega_0 t + \theta_0 - \rho$. The equation (10), becomes

$$\frac{d\rho}{dt} = H(p)V_s(\omega_0 t + \theta_0 - \rho) \tag{10}$$

Here $\omega_0 t + \theta_0$, can be seen as input, ρ as output. The control block diagram is given as Fig.3.

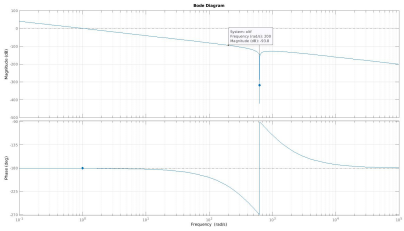


Figure 4: Bode for open loop no compensator

3 Compensator H(s) design

Input can be seen as two signals. First signal, $theta_0$ is a constant DC value. ρ tracks the constant component of the reference signal with zero steady-state error. To address steady state error due to ramp signal $\omega_0 t$ a pole is added at origin.

$$E_{steadystate} = \lim_{s \to 0} \frac{sR(s)}{1 + G(s)H(s)} \tag{11}$$

To avoid double frequency harmonics in V_sq which occurs due to negative sequence and 5^{th} harmonic in the grid voltages zeros are added at $s = \pm j2\omega_0$.
Design Parameters

- Phase margin = 60^o.
- Gain crossover freq. = 200 rad/s.
- $\omega_0 = 100\pi$

Now from above comments the transfer function is

$$H(s) = \frac{K(s^2 + (2\omega_0)^2)}{s} F(s) \tag{12}$$

Here F(s), is the lead compensator for satisfying design parameters. Before that we consider -40 db/dec slope of magnitude bode plot for frequencies more than double frequency to attenuate higher frequencies. Thus two poles are added at s= $\pm 2\omega_0$.

$$H(s) = \frac{K(s^2 + (2\omega_0)^2)}{s(s + \omega_0)^2} F(s) \tag{13}$$

Assuming KF(s)=1 , bode plot for open loop gain (Fig. 3) H(s)/s is given as The gain at 200 rad/s is -93.8 db , for cross over at 200 rad/s we take gain as K= 48977.88. Then the open loop gain has crossover at 200 rad/s. Next we look at the phase margin of the current plot. We get phase margin of -35.3 ^{o}. Thus, actual phase of loop is -215.3 ^{o} which is 144.7^o. To get phase margin of 60^o we need to add $60^o + 35.3^o$ at crossover frequency. Since phase to be compensated is large (95.3). F(s) can be cascaded with each compensator providing phase

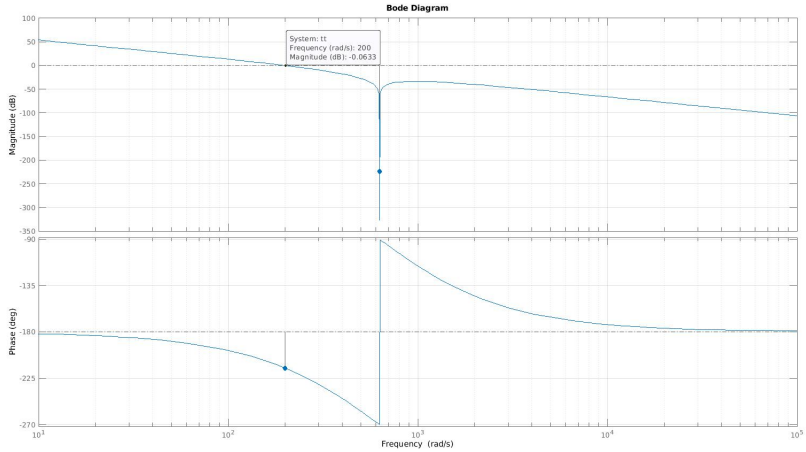


Figure 5: Bode for open loop with K= 48977.88

lead of (47.65^o).
F(s) is then given as

$$F(s) = \frac{s + p/\alpha}{s + p} \frac{s + p/\alpha}{s + p} \tag{14}$$

$$p = \omega_c \sqrt{\alpha} \tag{15}$$

$$\alpha = \frac{1 + sin(\delta_m)}{1 - sin(\delta_m)} \tag{16}$$

$$\delta_m = 47.65 \tag{17}$$

Thus F(s) is

$$F(s) = \frac{(s + 77.474)}{(s + 516.3)} \frac{(s + 77.474)}{(s + 516.3)} \tag{18}$$

Fig. 5 shows that we have satisfied all the parameters. Now we will track the frequency change using PLL in next section.

4 PLL Simulation

Using above design, model made by Muhammad N Qureshi (2021). Compensator Design for the PLL (https://www.mathworks.com/matlabcentral/fileexchange/60193-compensator-design-for-the-pll), MATLAB Central File Exchange is modified.
The deviation in frequency is presented as follows

- From time = 0.15 sec to 0.5 sec, a step change of +5 is added.
- Then from 0.5 to 0.7 sec it is changed to 50 Hz.

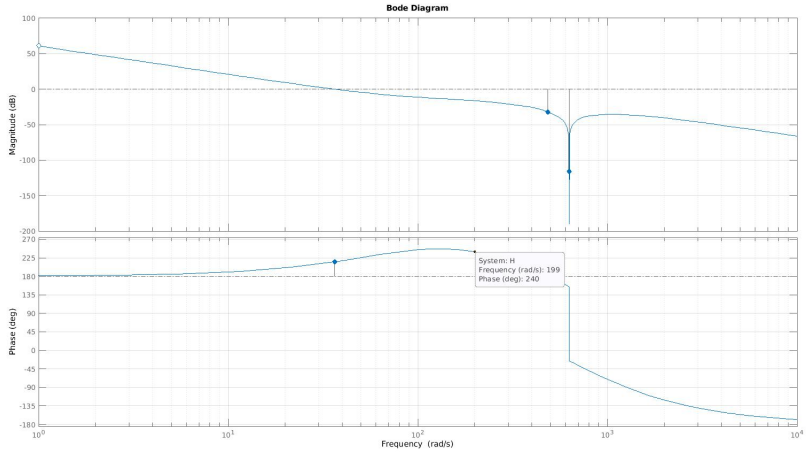


Figure 6: Bode for compensated open loop

- From 0.7 sec to 1.5, the step change in frequency from 50 to 45 is introduced.
- Then from 1.5 to 2 sec the frequency is again retained to 50 Hz.

5 Conclusion

The PLL successfully tracks the frequency deviations. However the settling time is an issue. The faster settling time is appreciated. The above design is taking about 0.25 sec to settle down. As the PLL value is taken up for further calculation this time must be minimized. **Please Refer to section 8.3.5 page 213 of A. Yazdani and R. Iravani, "Voltage-Sourced Converters in Power Systems: Modelling, Control, and Applications," 460 pages, ISBN: 978-0-470-52156-4, Wiley/IEEE.**

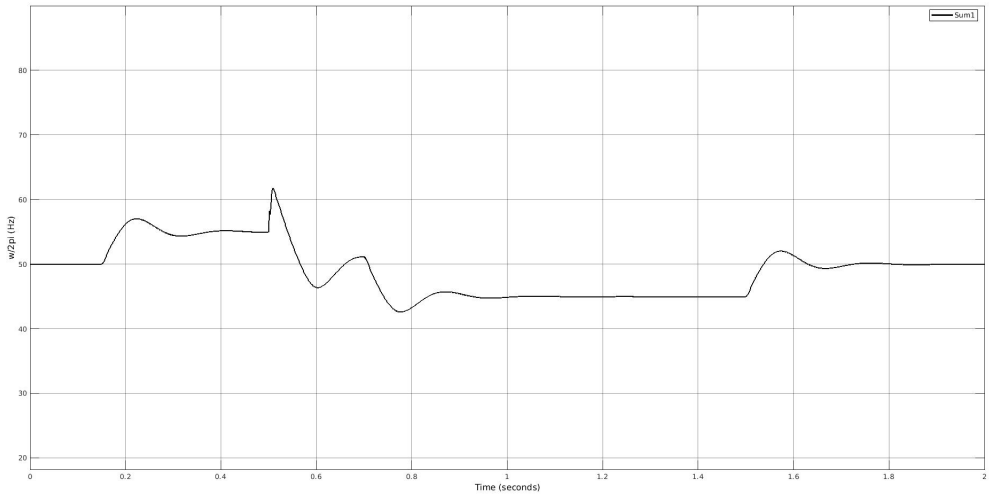


Figure 7: PLL tracking frequency

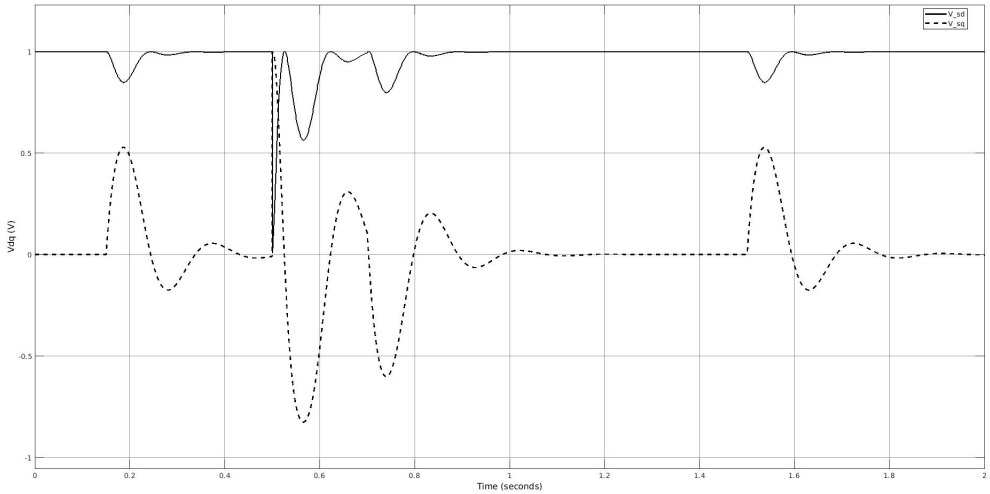


Figure 8: PLL tracking frequency