Memory Management

Non Contiguous Allocation Methods

Virtual Memory

- If the size of the program is greater than the available memory size, then the concept of virtual memory is used.
- Two most common method of implementing virtual storage are paging & segmentation.
- The addresses developed by the running programs are not necessarily those addresses available in primary memory.

Non Contiguous Allocation

Paging

- Memory Management scheme that permits the physical address space of a process to be non continuous.
- Avoids External Fragmentation.
- No need for compaction and coalescing.

Paging

- An address generated by the CPU is commonly referred to as **logical address**.
- An address in the memory unit ie. actual memory locations are referred to as **physical address**.
- The set of all logical addresses are called **logical address space**.
- The set of all physical addresses are called **physical address space**.

Paging

- Physical memory is broken into fixed sized blocks called **Page Frames.**
- Logical memory is divided into blocks of same size called **Pages.**
- **Page size is equal to Frame size.**
- The page/Frame size will be always given as powers of 2 (2, 4 8, 16, 32, 64, 128,….)

Paging

- When a process is to be executed, its pages are loaded into any available memory frames from the backing store.

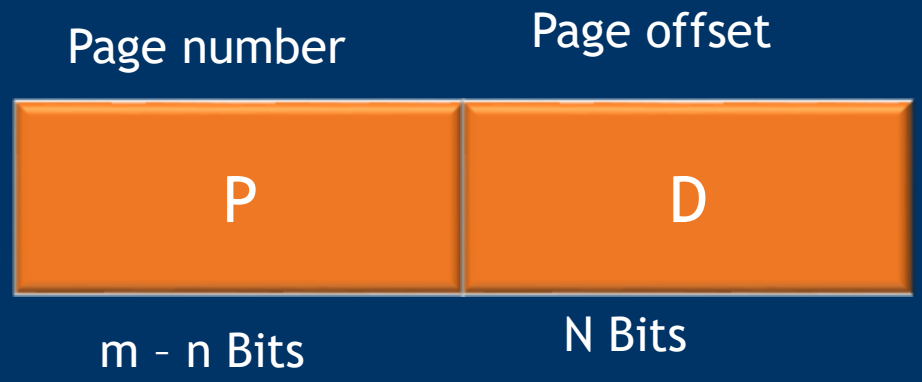
- The backing store is divided into fixed sized blocks that are of the same size as the memory frames

Paging

- **Every address generated by the CPU is divided into two parts**
  - *Page number (P)*
  - *Page offset / Displacement (D)*

Paging

If the total size of the logical address space is 2^m and the page size is 2^n bytes , then



Paging

- Consider there are 4 pages of size 16 bytes.

Page With size 16 Bytes

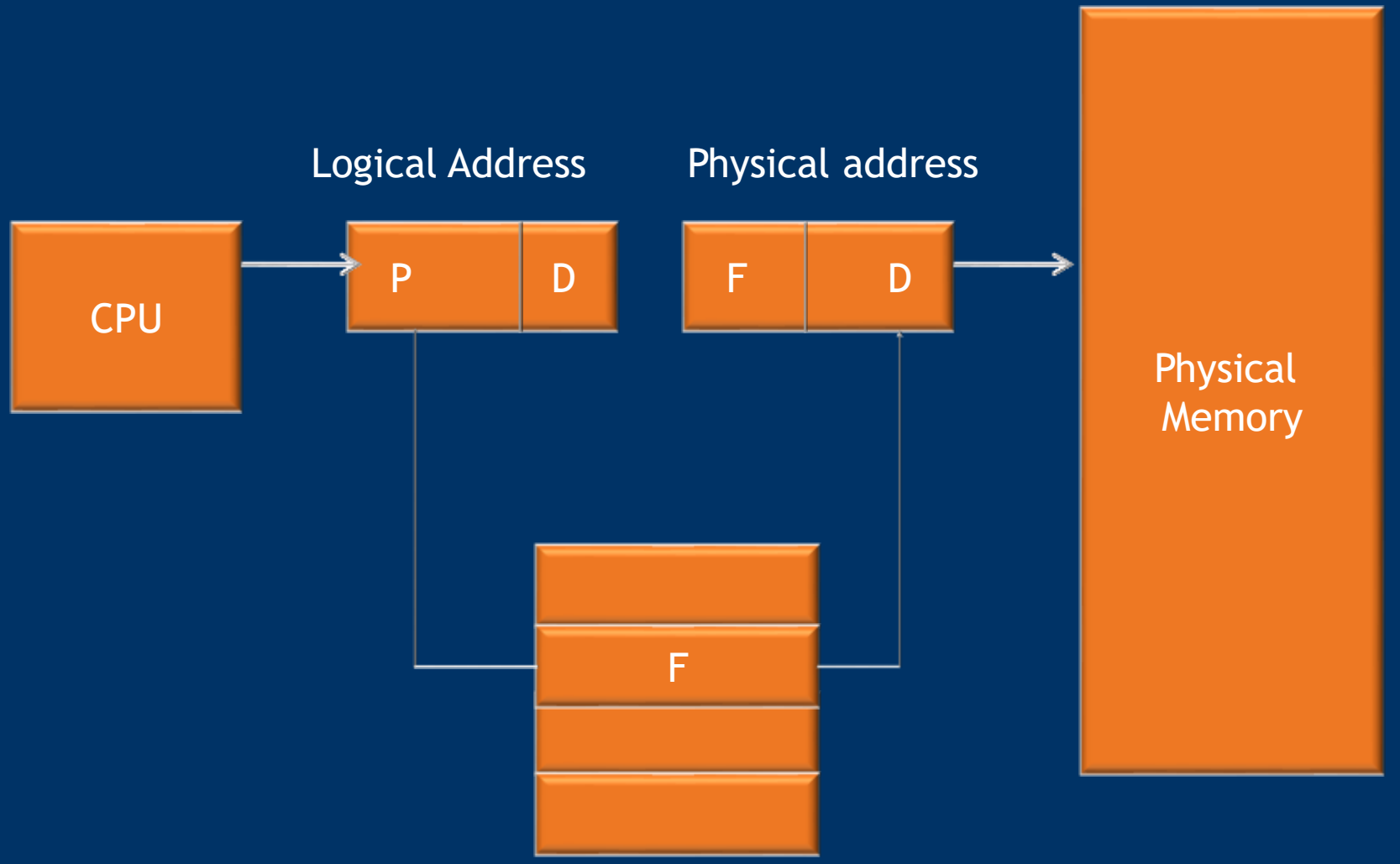
Paging

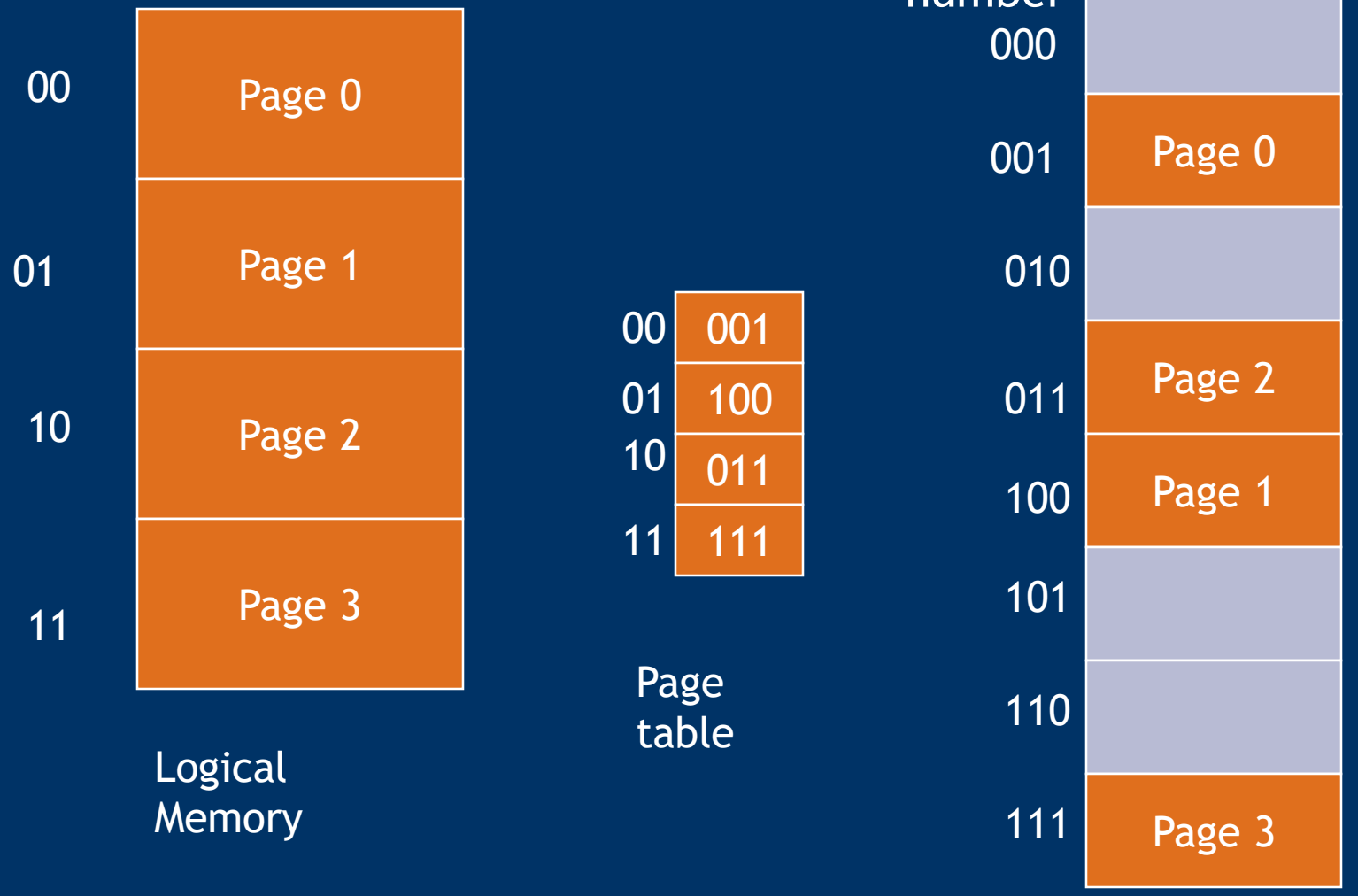
- How many bits are there to represent the Page Number ?
  - 2 Bits (2^2 = 4 Pages)
- How many bits are there to represent the Page Offset / Displacement ?
  - 4 Bits (2^4=16)
- How many bits will be there in the Logical Address?
  - Page number + Offset (2 + 4 = 6 bits)

Paging

- The page number is used as an index to the page table.
- Page table contains the base address of main memory frames.
- This base address is combined with the page offset to define the physical memory address that is sent to the memory unit.

Paging- Basic Method




00
Page 0
01
Page 1
10
Page 2
11
Page 3
Logical Memory
00
001
01
100
10
011
11
111
Page table
Frame number
000
001
Page 0
010
011
Page 2
100
Page 1
101
110
111
Page 3

Page Map Table (PMT)

- Data structure used by a virtual memory system to store the mapping between Logical Addresses and Physical Addresses.

- For each page there will be an entry in the Page Map Table for each process.

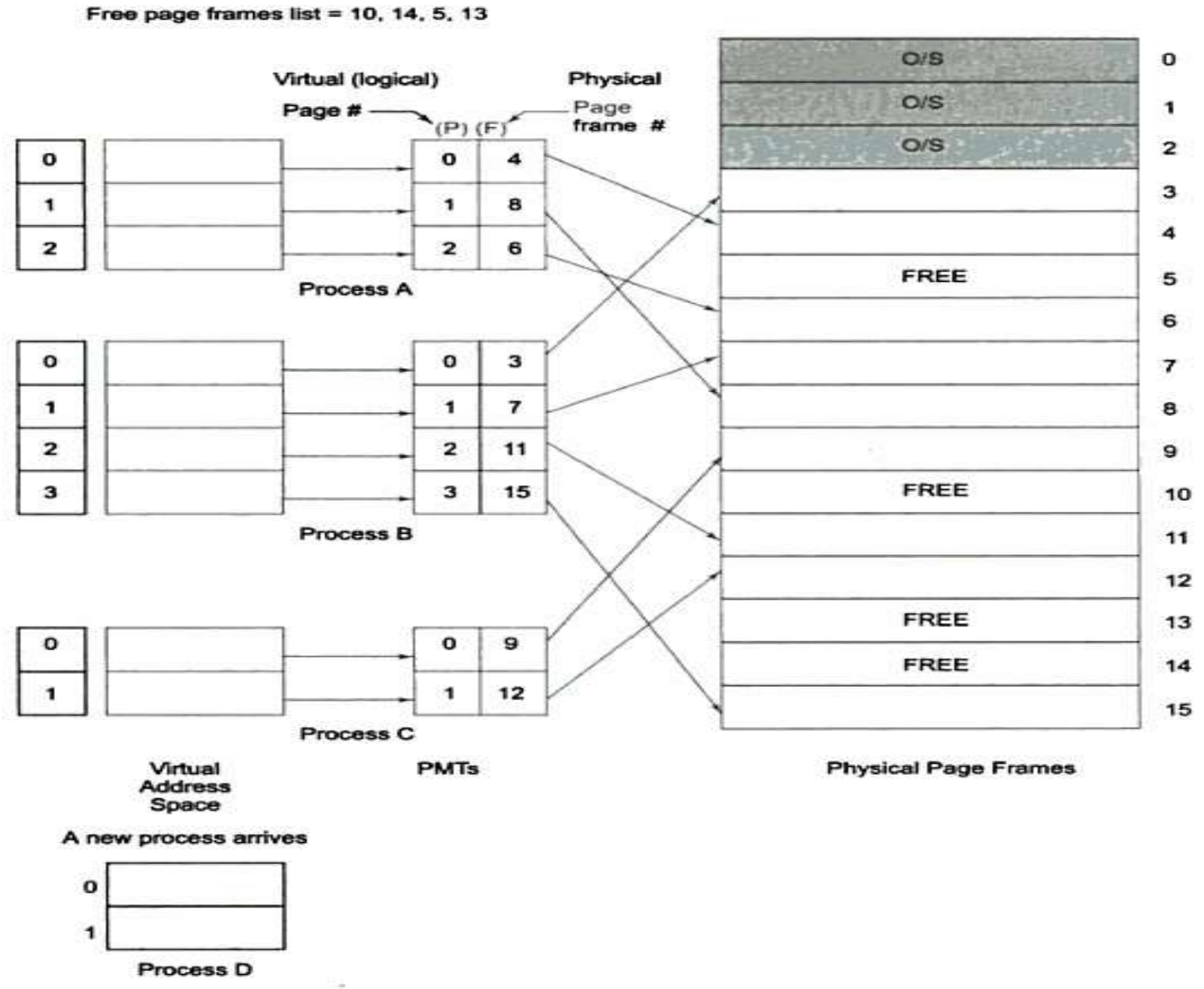


Fig. 8.19 Memory allocation for processes A, B and C before allocation for newly arrived process D is done

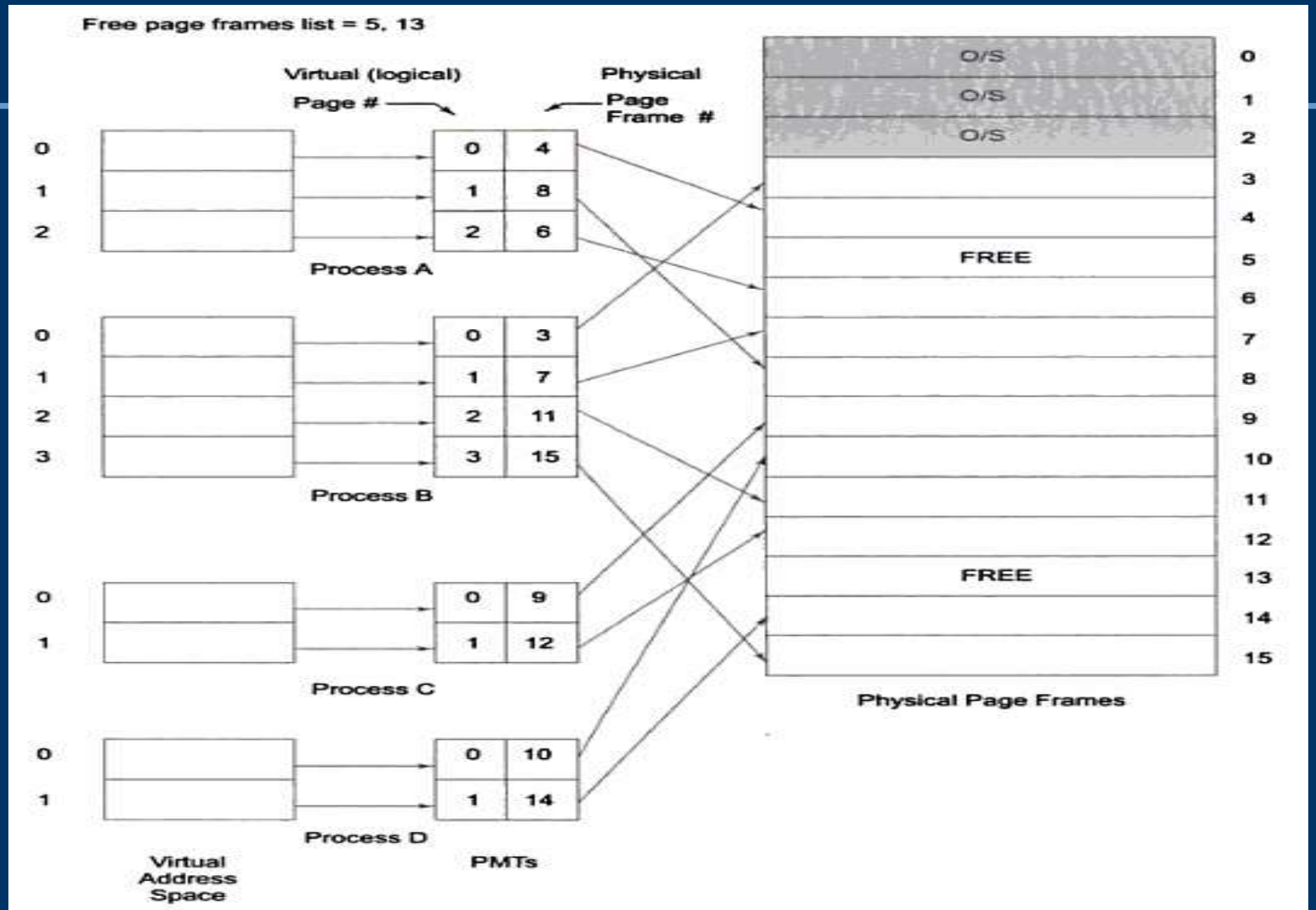
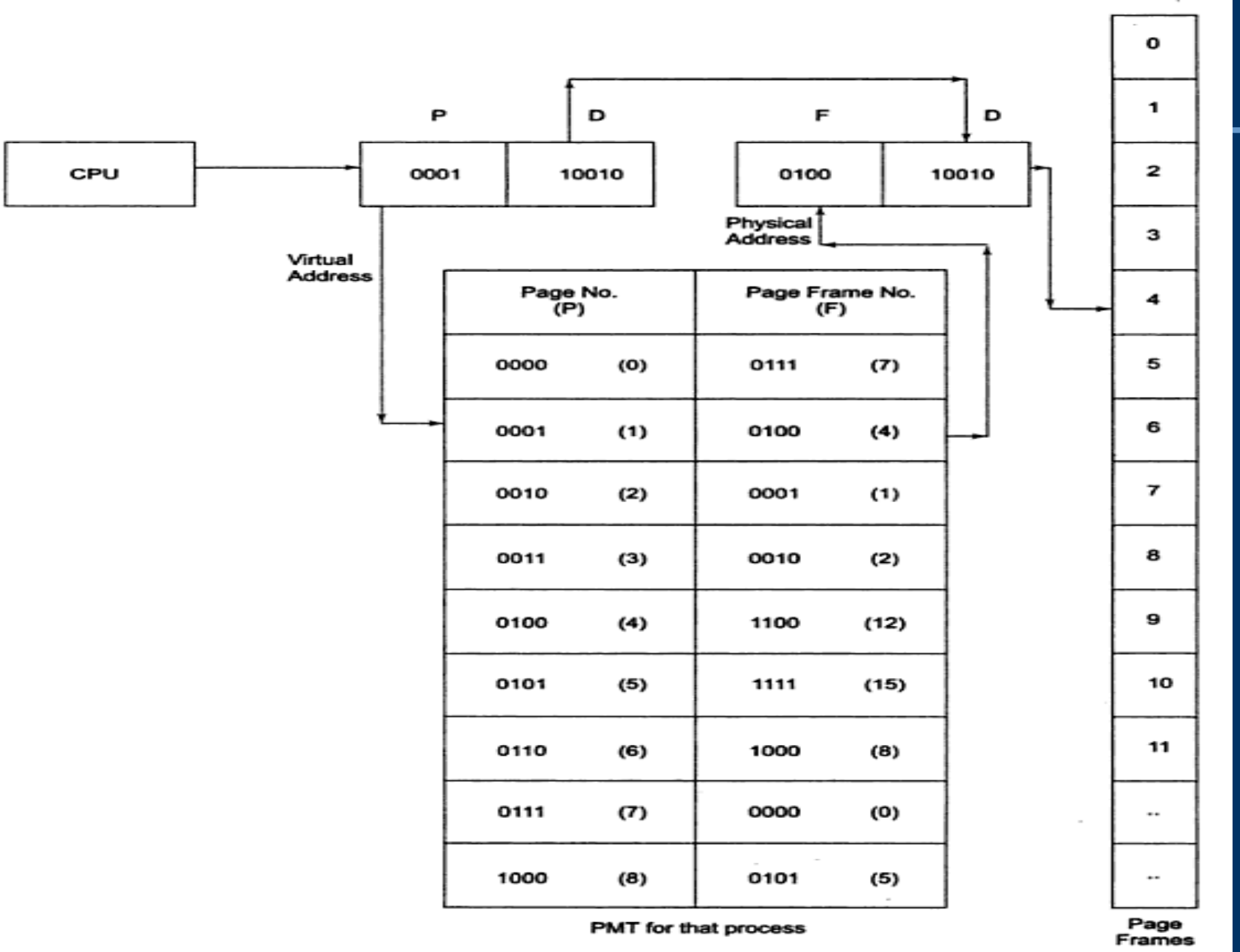


Fig. 8.20 After allocation of memory to process D


CPU
P
D
0001
10010
F
D
0100
10010
Physical Address
Virtual Address
Page No. (P)
Page Frame No. (F)
0000 (0) 0111 (7)
0001 (1) 0100 (4)
0010 (2) 0001 (1)
0011 (3) 0010 (2)
0100 (4) 1100 (12)
0101 (5) 1111 (15)
0110 (6) 1000 (8)
0111 (7) 0000 (0)
1000 (8) 0101 (5)
PMT for that process
0
1
2
3
4
5
6
7
8
9
10
11
..
..
Page Frames

Page Map Table Implementation

Implementation affects the performance.

Maximum size of the page map table.

Maximum program size and page size

Size of Address Bus

Page Map Table Limit Register

- PMTLR contains the number of pages contained in a process.
- One PMTLR for each PMT
- PMTLR entry in PCB corresponding to a process.
- Can be used for protection purpose.

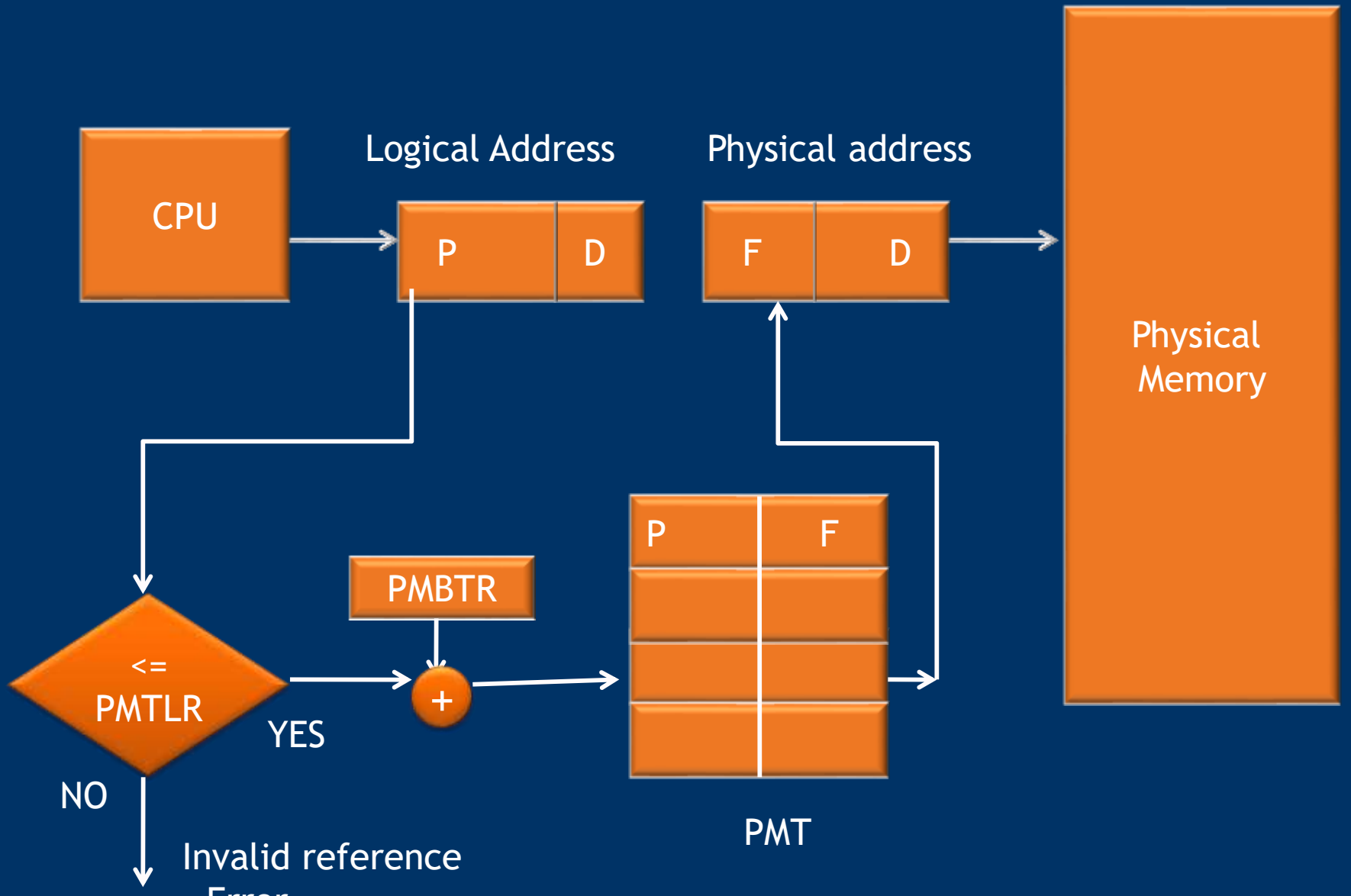
Page Map Table Implementation

- Software Method
- Hardware Method
- Hybrid Method

Software Method

- OS Keeps all PMTs in Main Memory.
- The starting address of PMT is stored in PMTBR(Page Map Table Base Register)
- Also stored in PCB.
- Two Memory access required - PMT then Instruction.

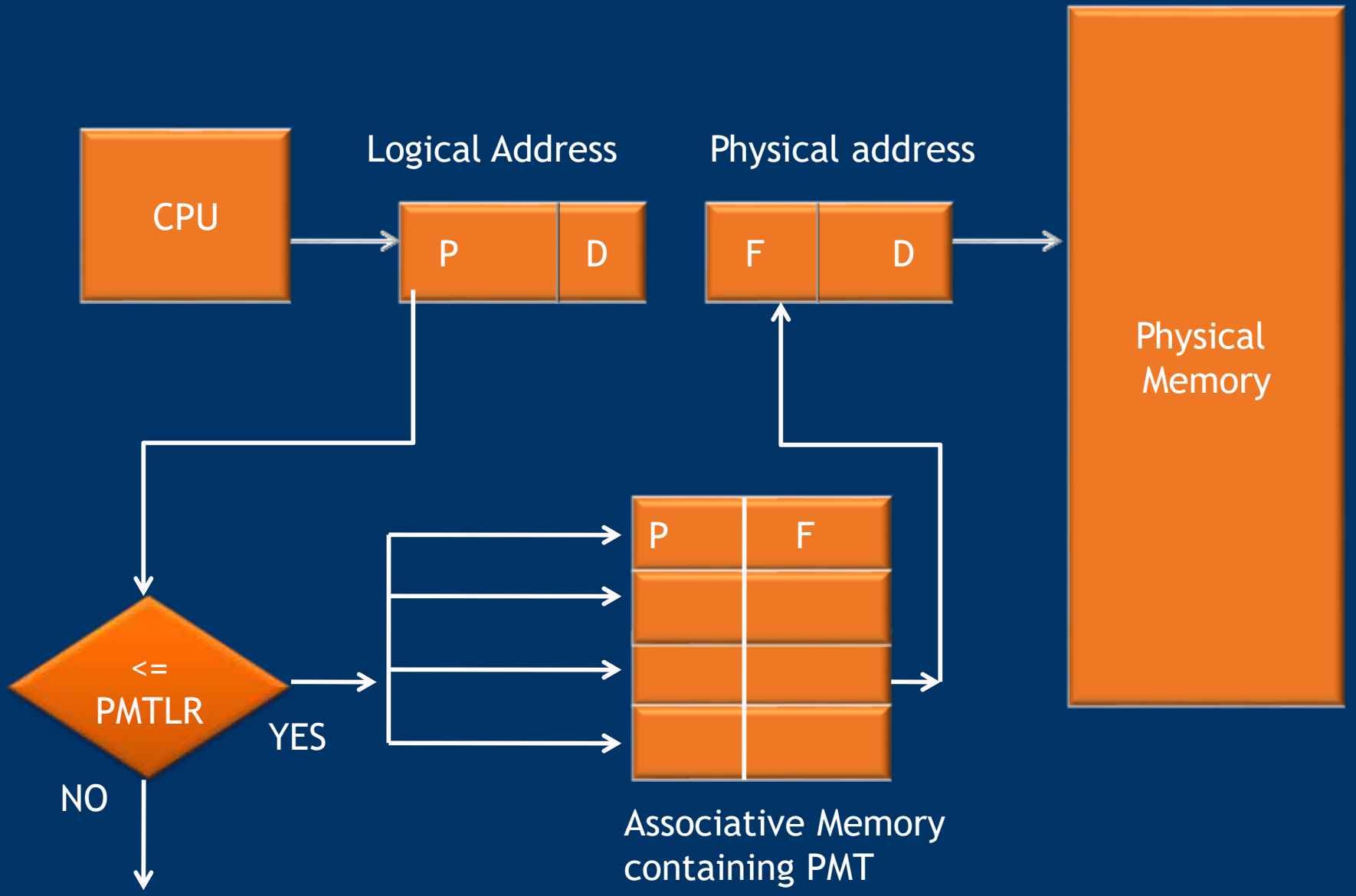
PMT - Software Method



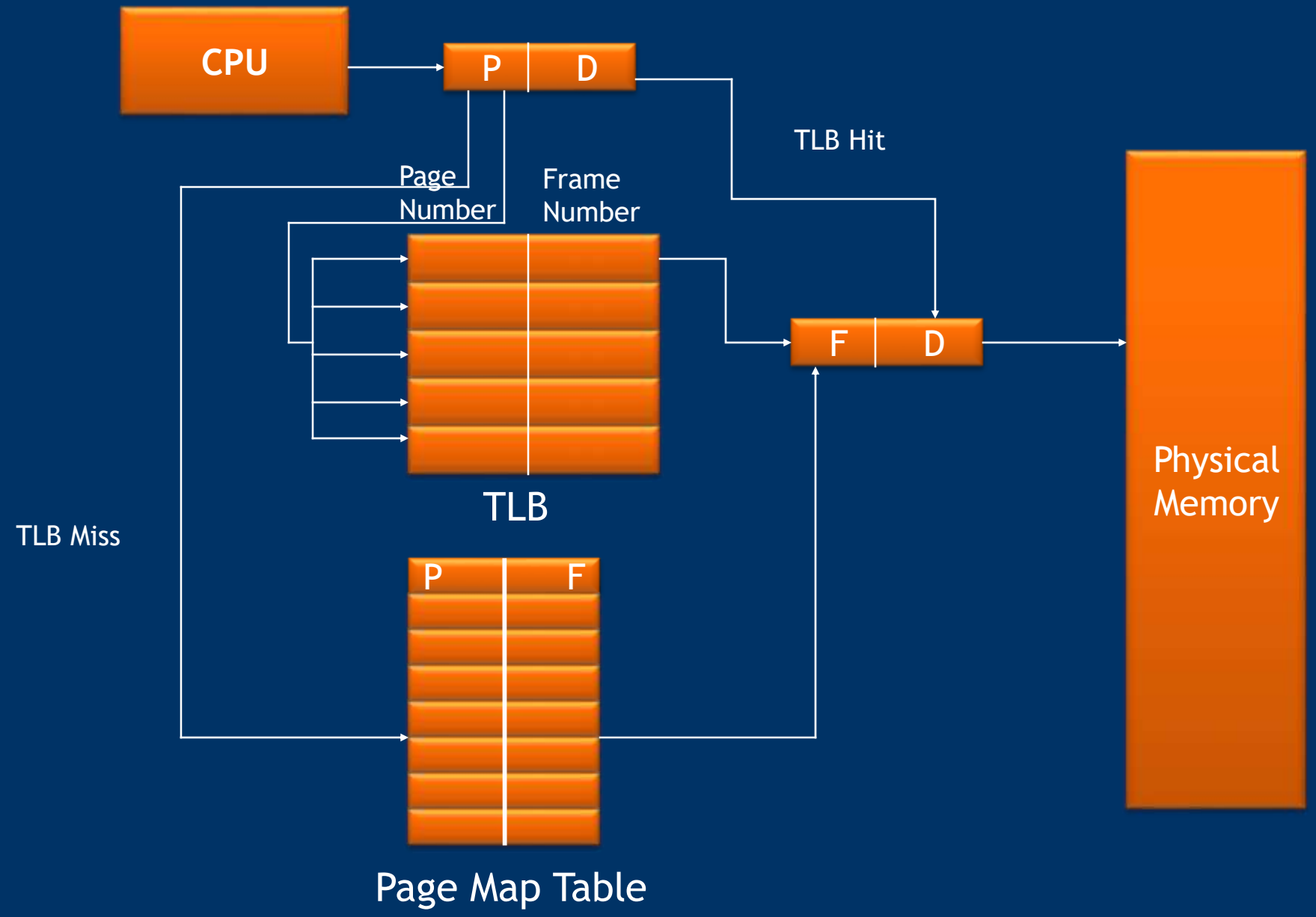
Hardware Method

- Use Associative Registers / Associative Memory for PMT.
- Table search is done in hardware itself.
- Overhead is Very Low.
- Associative Memory is very Expensive.

PMT - Hardware Method



Hybrid Method With Translation Look Aside Buffer (TLB)



Paging - Drawbacks

- **Fixed sized Pages/Frames**
  - Internal Fragmentation.
- **Selection of page size**
  - Small - Reduce Internal Fragmentation but increase the PMT entries
    - Increased Search time.
  - Large – Chance of internal fragmentation.

Segmentation

- Segmentation is a memory management scheme that supports user's view of memory.
- A logical address space is a collection of segments.
- Segments are Variable sized.

Segmentation

- Each segment has name and length.
- The address specifies both the segment name and the offset within the segment.
- Segments are numbered and are referred to by a segment number.

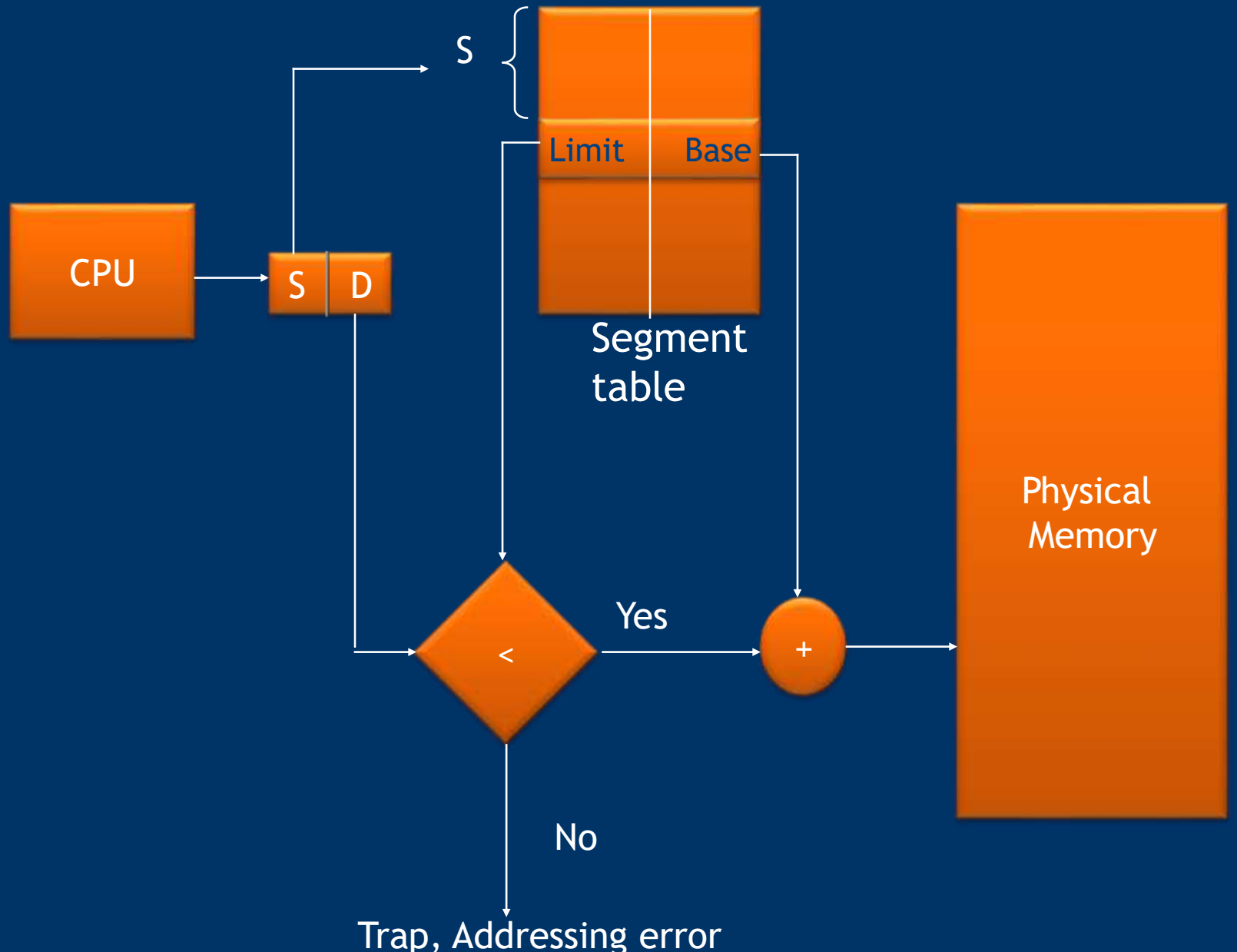
Segmentation

- Thus the logical address consists of

  <Segment- Number, Offset>

- In segmentation system a program or data are allowed to occupy in more than one partitions. The blocks need not be of same size and adjacent blocks. But with in a block data or programs are stored continuously.

Segmentation - Hardware

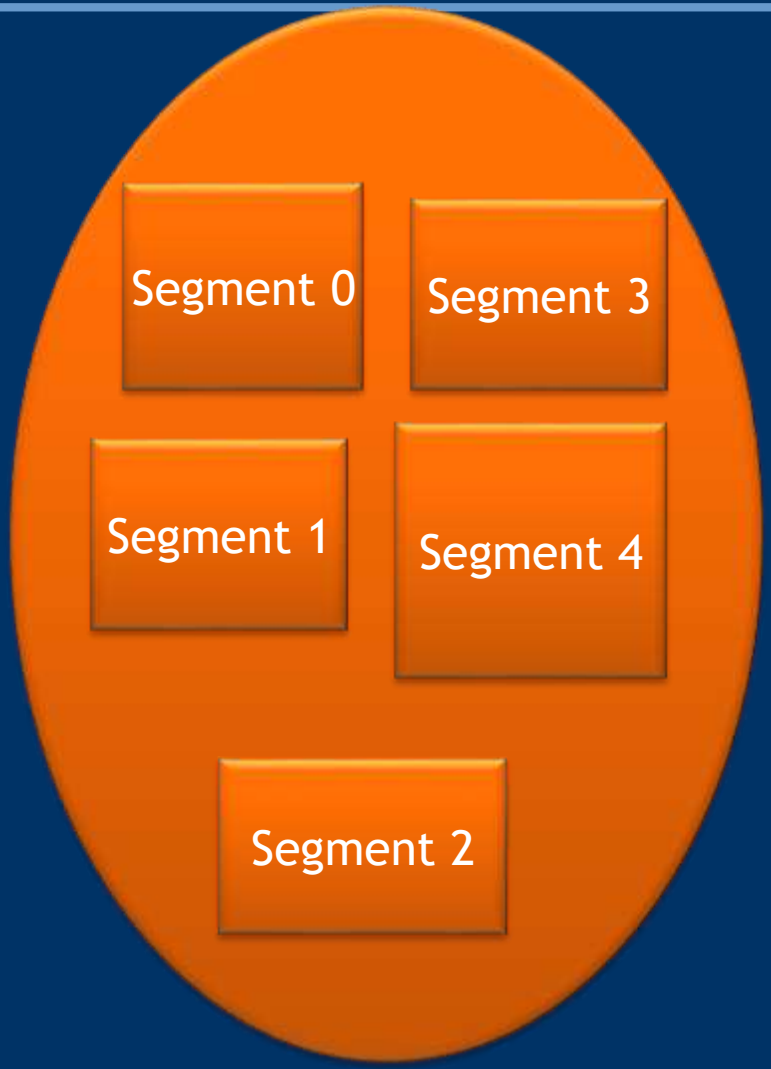


Segment Table

- **Segment Table**
  - Each entry of segment table has a segment base and segment limit.
  - The segment base contains the starting physical address where the segments resides in the main memory.
  - Segment limit specifies the length of the segment.

Segmentation

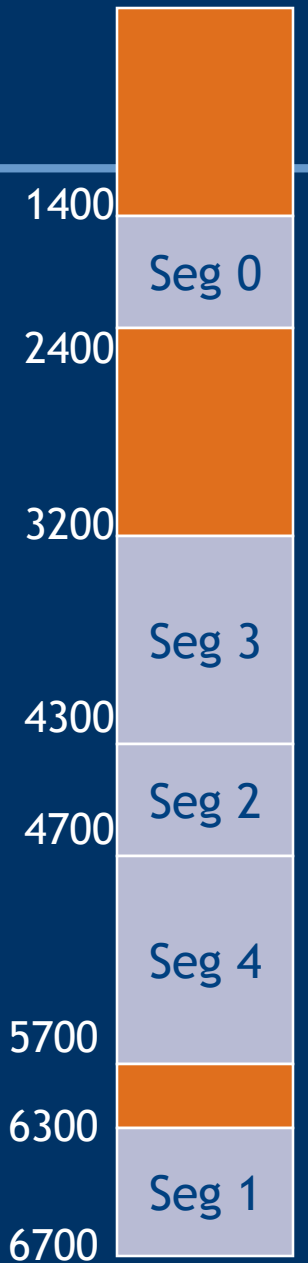
- The logical address has two parts – Segment number (s)and offset (d) .
- The segment number is the index to the segment table.
- The offset must be between 0 and segment limit. If it is not the OS will give an error message. If the offset is legal, it is added to the base to produce the actual physical address



User program

	Size	Base
0	1000	1400
1	400	1400
2	400	1400
3	1100	1400
4	1000	1400

Segment Table



Physical Memory