Project #1 – Creating and analyzing cache Denial of Service (DoS) attacks in a multicore system

GROUP #7

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Problem Statement

The objective of this project is to create a DoS attack on the shared Last Level Cache (LLC) of a multi-core system targeting write-back buffers and MSHRs through the following studies.

Study 1: Effect of read and write attacks on the victim applications' performance in presence of a malicious attacker cores.

Study 2: Vary LLC size, MSHR size and Write-back buffer size one at a time and analyse the effect on performance.

Study 3: Check the effect of cache-partitioning on the performance under such kind of DoS attacks.

Study 4: Perform the studies with at least 3 sets of different benchmarks.Each set should contain a combination of benchmark applications with both write-dominated and read-dominated memory access patterns to perform better analysis.

Goals and Expectations

Goals:

- To simulate the BwRead (Read attack), BwWrite (Write attack) DoS attacks on various multi-core platforms and record the impact on performance.
- To vary LLC size, writeback buffer size, MSHRs size, use cache partitioning, hardware prefetchers and check their impact on performance against DoS attacks.
- To test the above simulations on different benchmarks and draw conclusions.

Expectations:

- To reproduce the different results discussed in the research paper on embedded multicore platforms across benchmarks.

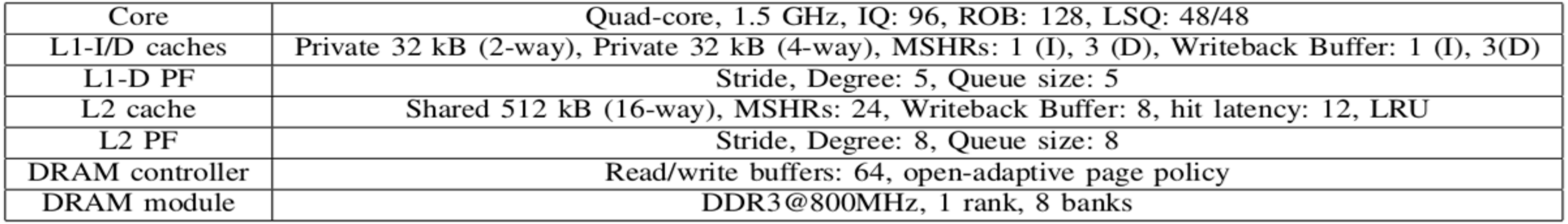
Completed Tasks

- Studied the effect of read and write attacks on the performance of victim script on a core in presence of a malicious attacker cores.
- Varied LLC size, MSHRs and Write-back buffer size one at a time and analyse the effect on performance.
- Analyzed the impact of hardware prefetchers on performance.
- Performed the above simulations on various multicore platforms [minor, hpi and DerivO3]
- Analyzed the results on susan, SD-VBS [K Means, PCA (text) and Disparity (vision)] benchmarks

Baseline configuration

CPU Type	4x Cortex-A53 (HPI)	4x Cortex-A7 (Minor)	4x Cortex-A15 (DerivO3)
Private Cache Shared Cache	32/32KB 512KB (16-way)	32/32KB 512KB (16-way)	32/32KB 2MB (16-way)
Memory	1GB LPDDR2	2GB LPDDR3	2GB LPDDR3

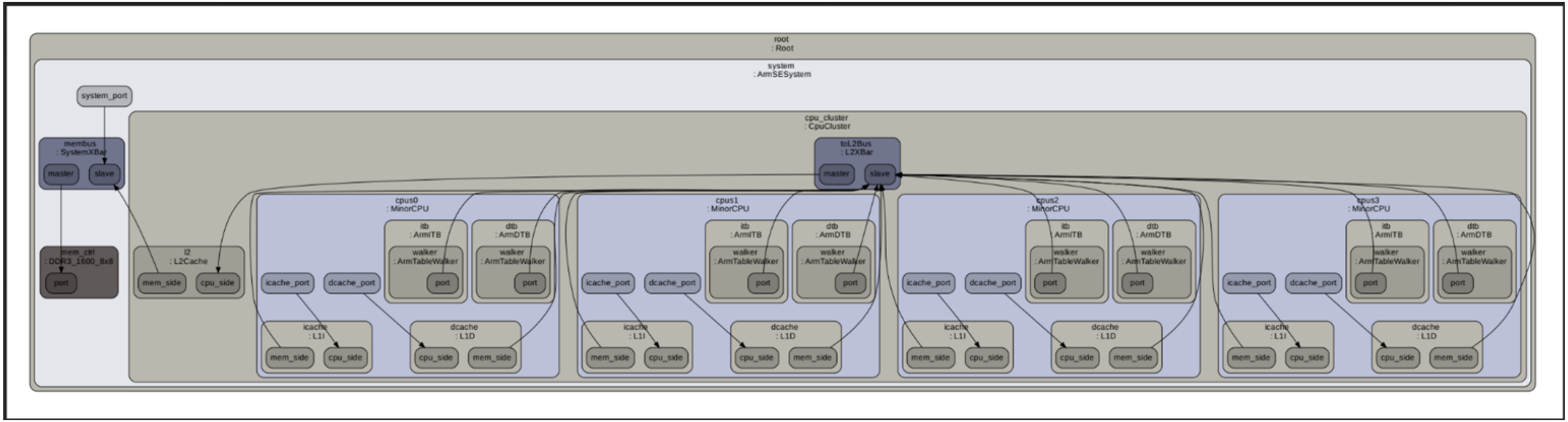
Configuration for impact of hardware prefetchers and writeback buffer



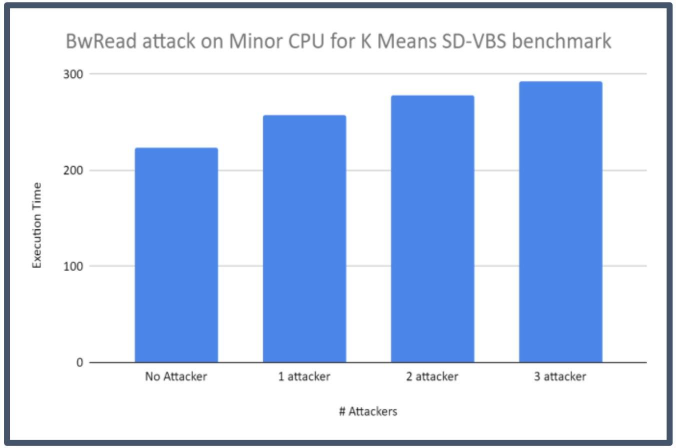
Core	Quad-core, 1.5 GHz, IQ: 96, ROB: 128, LSQ: 48/48
L1-I/D caches	Private 32 kB (2-way), Private 32 kB (4-way), MSHRs: 1 (I), 3 (D), Writeback Buffer: 1 (I), 3(D)
L1-D PF	Stride, Degree: 5, Queue size: 5
L2 cache	Shared 512 kB (16-way), MSHRs: 24, Writeback Buffer: 8, hit latency: 12, LRU
L2 PF	Stride, Degree: 8, Queue size: 8
DRAM controller	Read/write buffers: 64, open-adaptive page policy
DRAM module	DDR3@800MHz, 1 rank, 8 banks

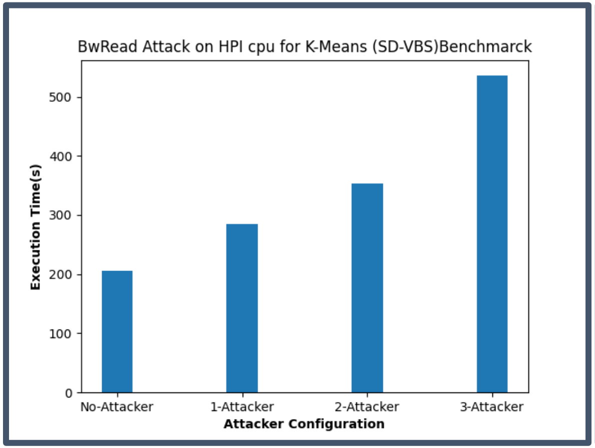
TABLE II: Baseline simulation parameters for Gem5 and Ramulator.

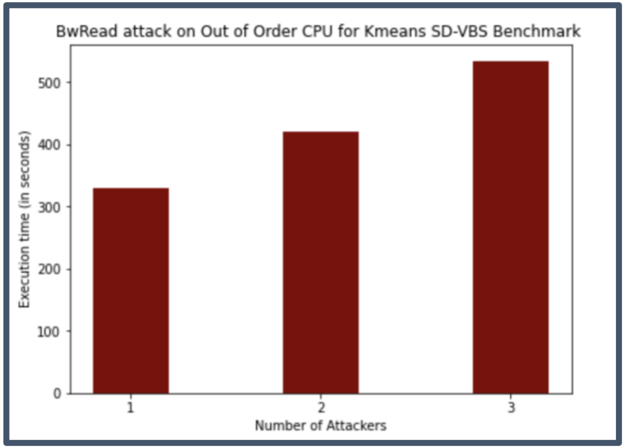
System Architecture (4-core)



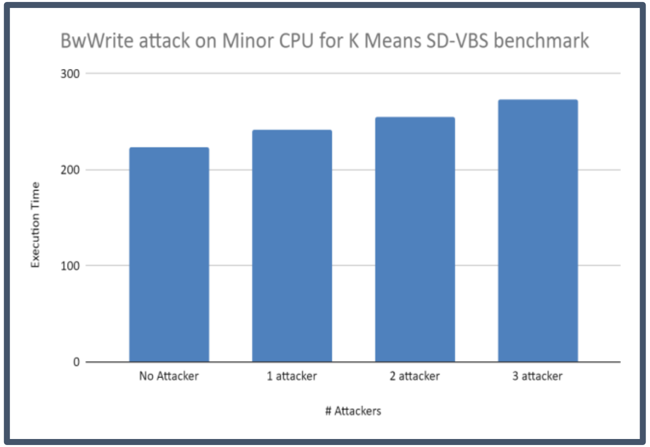
Impact of BwRead attacks

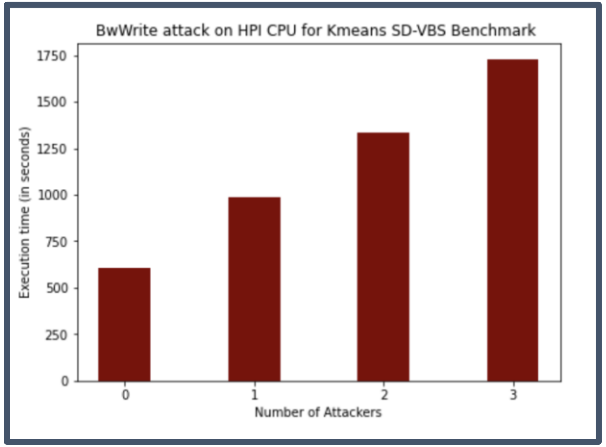


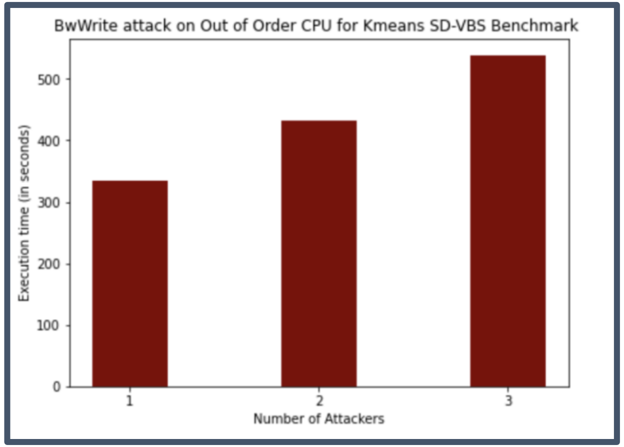




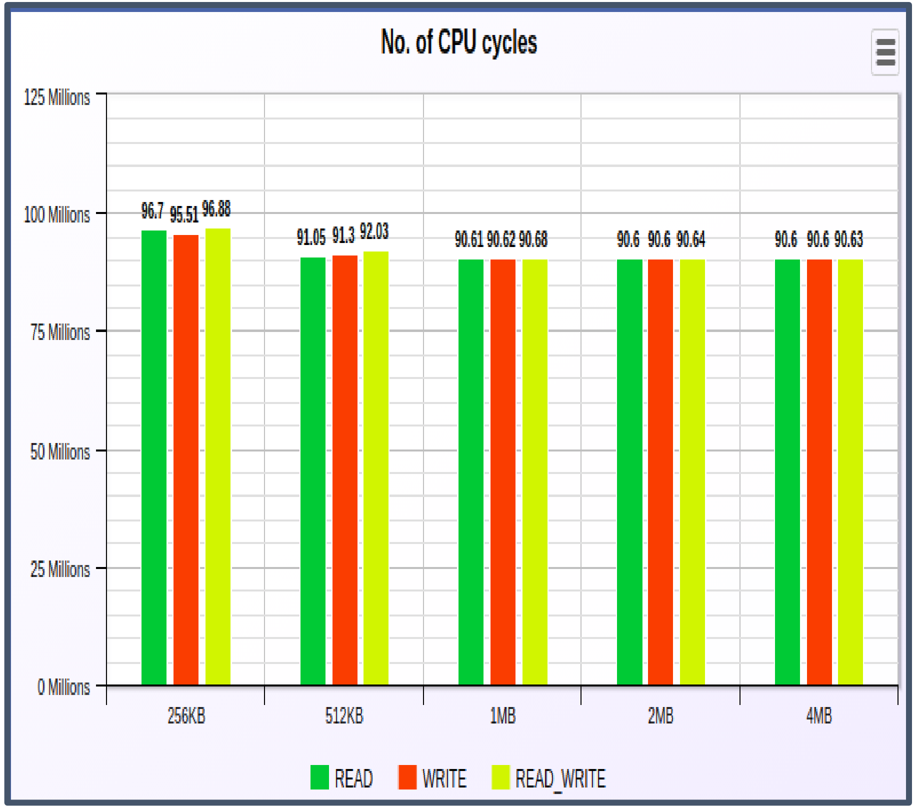
Impact of BwWrite attacks

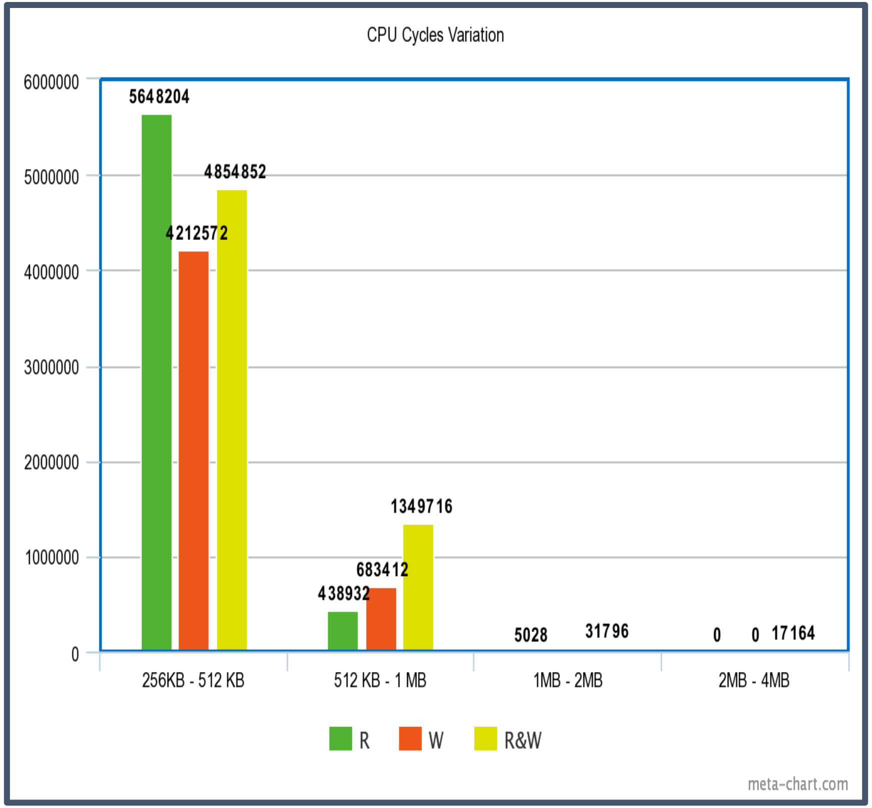

BwWrite attack on Minor CPU for K Means SD-VBS benchmark


BwWrite attack on HPI CPU for Kmeans SD-VBS Benchmark

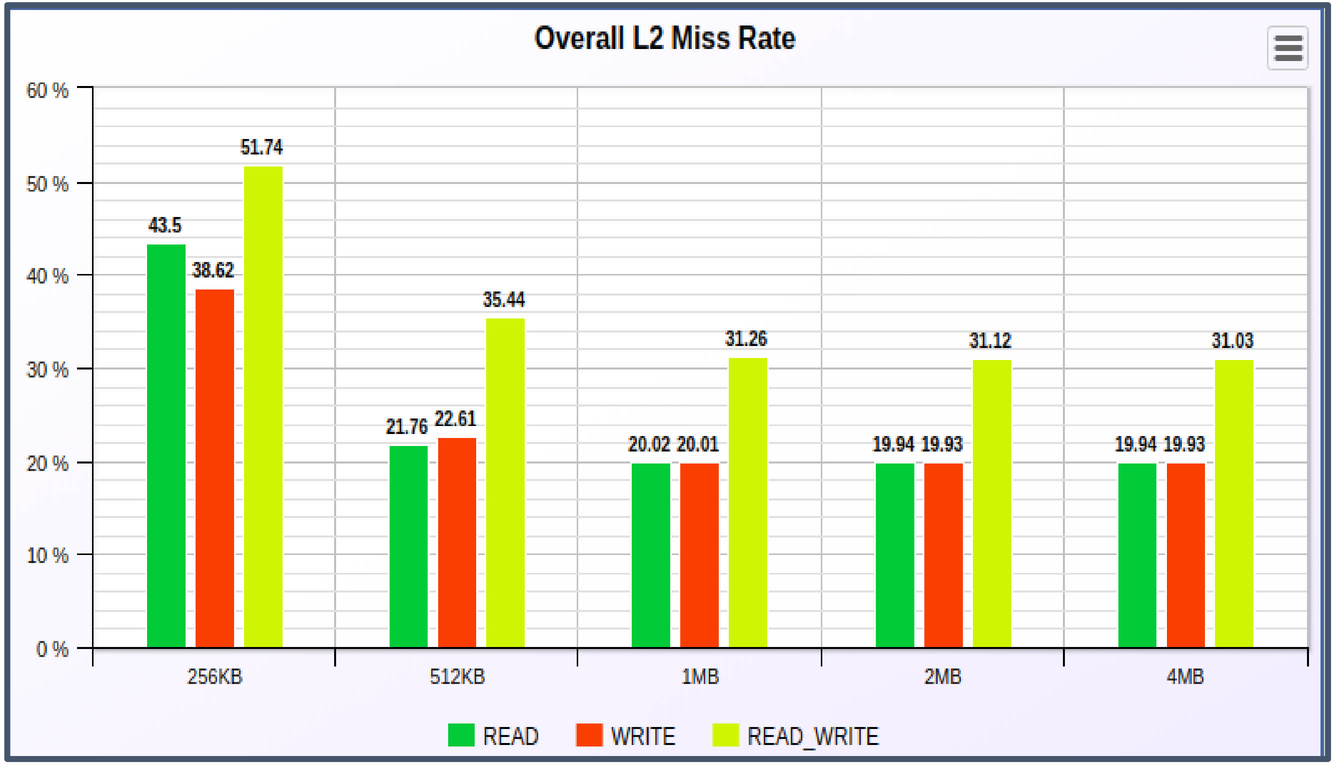

BwWrite attack on Out of Order CPU for Kmeans SD-VBS Benchmark

Impact of L2 Cache Size on CPU cycles (Minor)

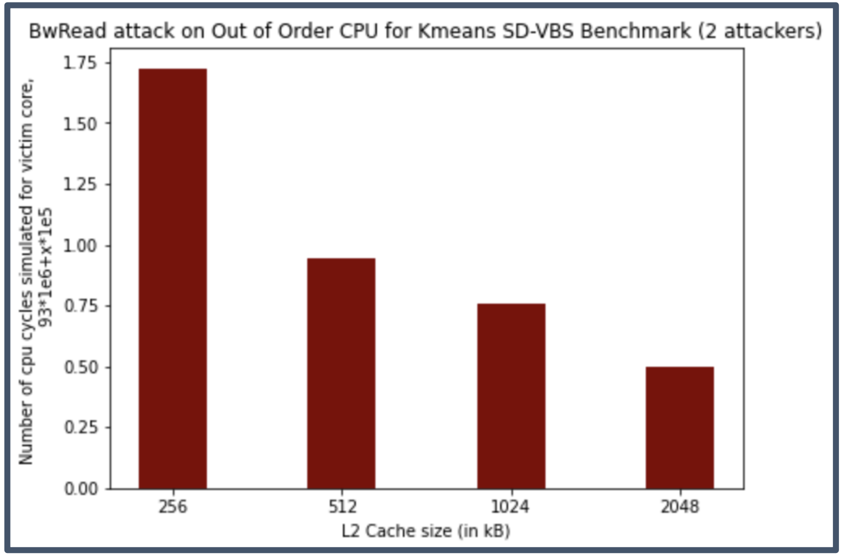


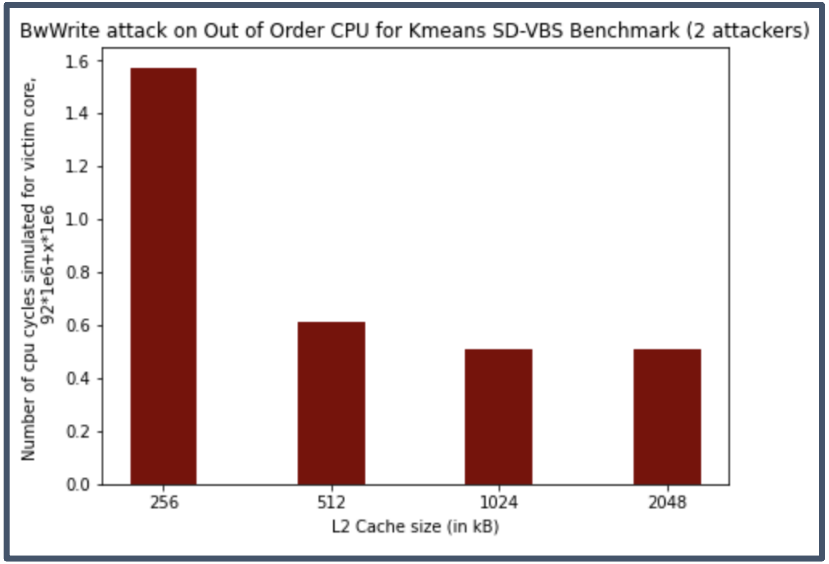


Impact of L2 Cache Size on Miss Rate(Minor)

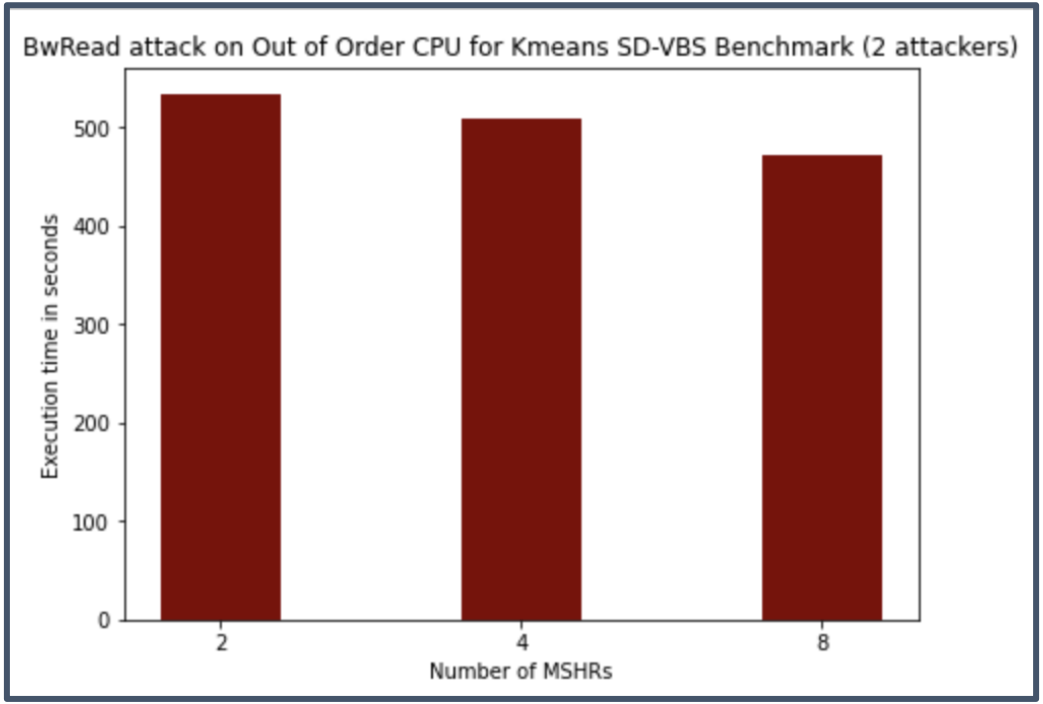


Impact of L2 Cache Size on CPU Cycles (DerivO3)

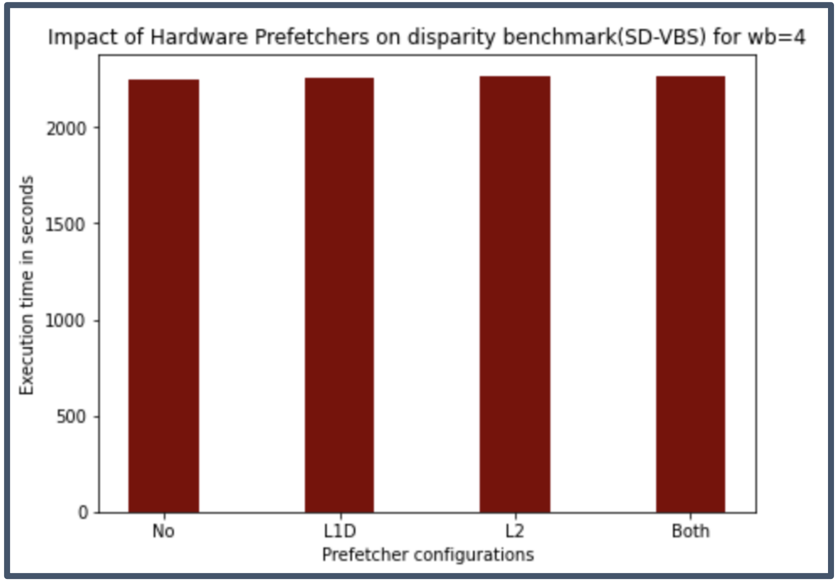


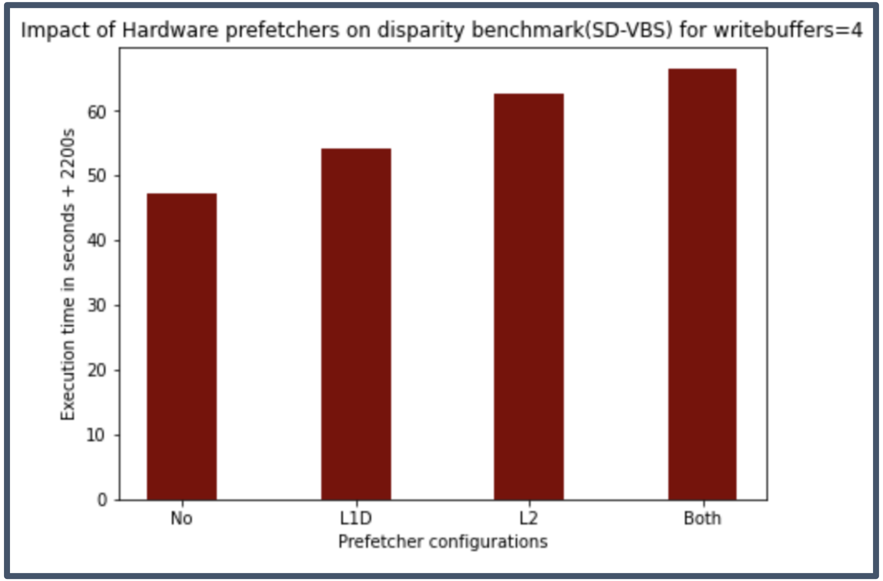


Impact of MSHRs

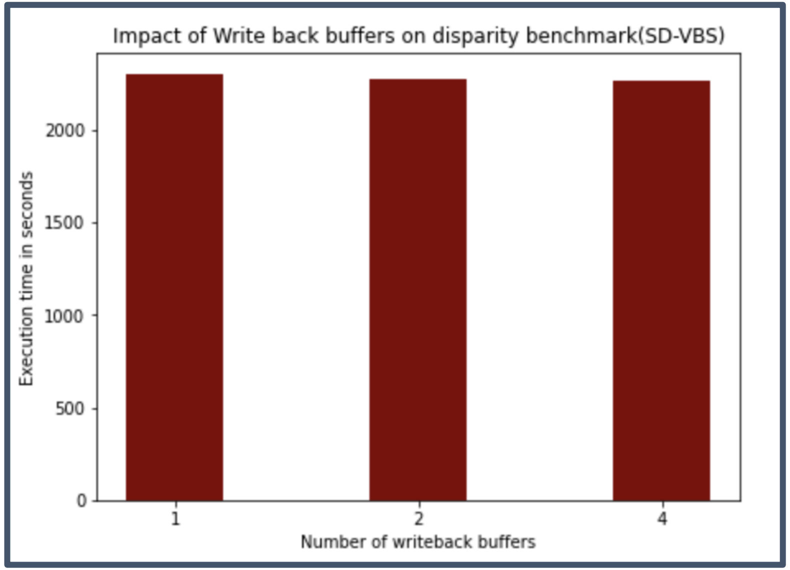


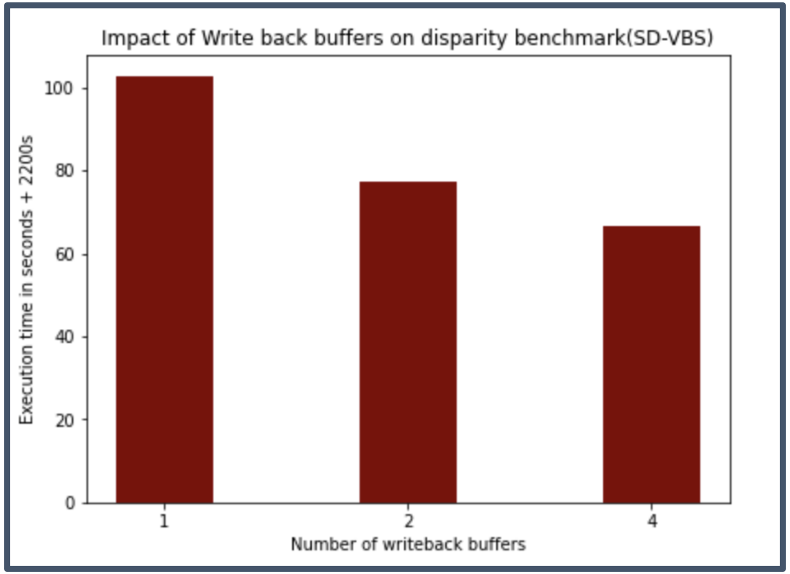
Impact of Hardware Prefetchers





Impact of Writeback Buffers





Roadblocks

- Configuring private caches for each core and the shared cache for all the cores.
- Fixing the binary generation for attack as well as Susan, SD-VBS benchmark scripts. (Binaries were to be linked statically)
- SD-VBS benchmark had all binaries and makefile compatible with x86.
- Choosing the right cross compiler to compile scripts on ARM ISA.
- Vision benchmarks had no makefile.
- Combining multiple scripts to generate ARM binary was a challenge
- Choosing the right set of parameters for impact analysis of hardware prefetchers, writeback buffer was a huge challenge since results weren’t good for the attacks described in the paper.
- Integrating O3 CPU was a challenge.

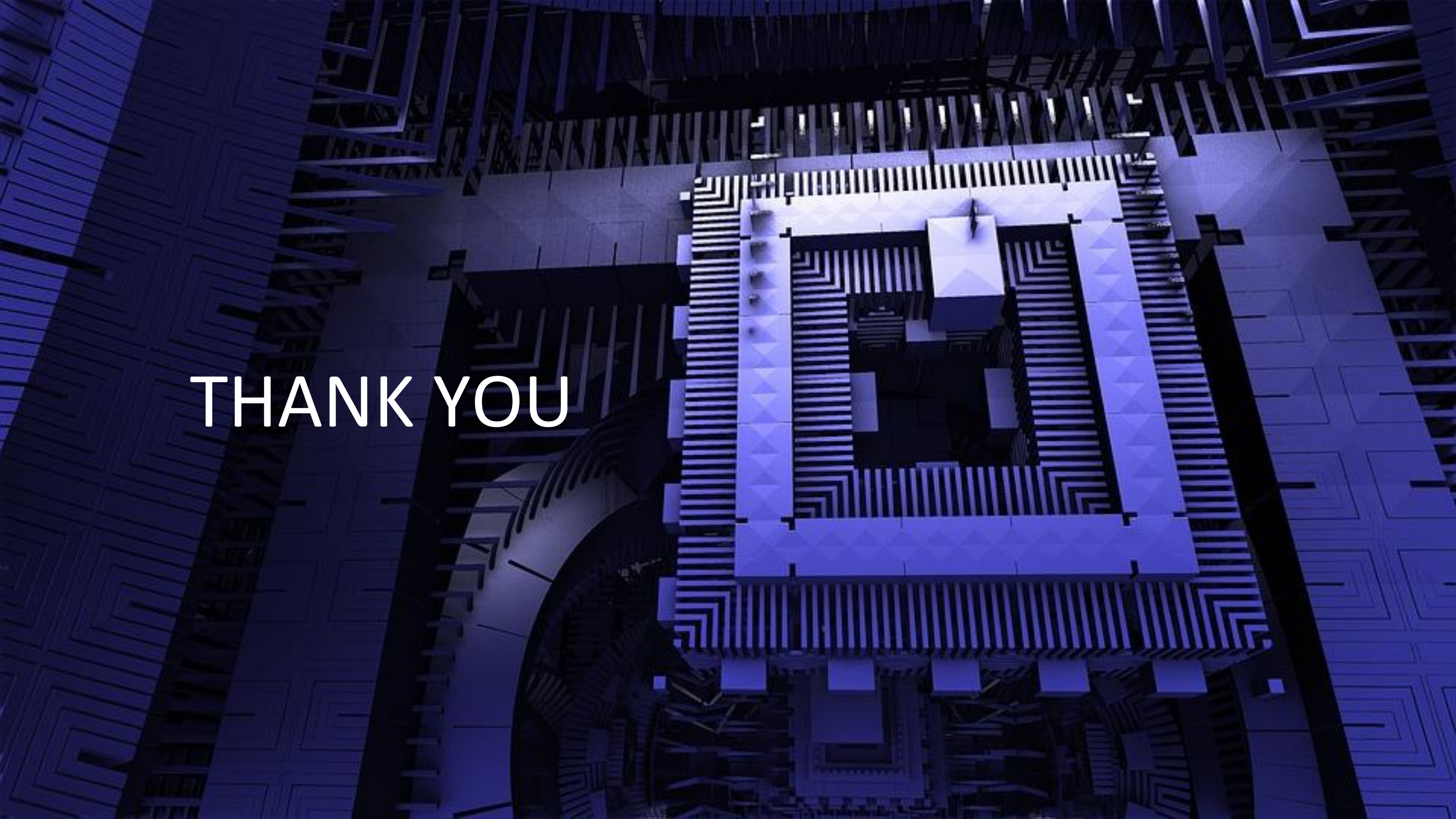
Weekly tasks performed

Week #	Dates	Tasks done
Week 1	Sep 29 - Oct 4	Research paper study
Week 2	Oct 5 - Oct 11	Research paper study and discussion
Week 3	Oct 12 - Oct 18	Mid Sem Exam week
Week 4	Oct 19 - Oct 25	Project PPT and video preparation
Week 5	Oct 26 - Nov 1	Getting accustomed with ARM based architectures.
Week 6	Nov 2 - Nov 8	Debugging through system architecture and parallel execution on ARM CPUs.
Week 7	Nov 9 - Nov 15	BwRead and BwWrite based DoS attacks on minor, hpi CPU, record statistics and analyze the output on Susan benchmark
Week 8	Nov 16 - Nov 22	Conducting experiments to assess the impact of writeback buffer size, LLC size on benchmarks and recording the results on minor, hpi cpu on Susan benchmark
Week 9	Nov 23 - Nov 29	BwRead and BwWrite based DoS attacks on minor, hpi CPU, record statistics and analyze the output , conducting experiments to assess the impact of cache partitioning, hardware prefetchers, MSHRs, writeback buffer size, LLC size on benchmarks and recording the results on SD-VBS benchmark (K Means, Disparity, PCA)
Final	Nov 30 - Dec 19	DerivO3 CPU experiments + hardware prefetchers + writeback buffer impact experiments on minor CPU and documentation.

Work Distribution

Benchmarks used - Susan, SD-VBS [K-Means, PCA (both text) and Disparity(Image)]

Student Name	Contribution
P. Akshay Kumar	Binary generation for attacking scripts, Susan and SD-VBS for ARM architecture, Read, write attacks simulation on Minor CPU for all benchmarks, all simulations related to DerivO3 processor and final report.
Abhishek Singh Chauhan	BwRead and BwWrite attacks on HPI CPU and impact of writeback buffer size on HPI CPU on all benchmarks and appendix
Abhishek Pundir	Impact of hardware prefetchers and impact of writeback buffer size on all benchmarks on minor and HPI CPU. Creation of new attacking scripts and appendix.
Vishal Sharma	Impact of L2 cache size, MSHRs on Minor CPU on all benchmarks, video preparation and appendix.
Anannya	Impact of L2 cache size, MSHRs on HPI CPU on all benchmarks, final report and final presentation.



THANK YOU