Akshaya Naapa Ramesh

Littleton, MA 01460 | akshayan@umich.edu | (978) 501-4570 | akshayanr.com

EDUCATION

University of Michigan **Ann Arbor, MI**
Bachelor of Science in Engineering in Computer Engineering *December 2025*

GPA: 3.78/4.00
Activities: Michigan Mars Rover, ECE Student Ambassador, Women In ECE
Honors: Dean's List, Michigan EV Scholar (2024), NCWIT Aspirations In Computing: National Honorable Mention (2022)

Coursework: Advanced Embedded Systems, Embedded Control Systems, Computer Organization/Architecture, Digital Integrated Circuits, Data Structures & Algorithms, Logic Design, Electronic Circuits, Signals & Systems, Computer Science Pragmatics (UNIX Tools & Scripting)

SKILLS

Software/OS: C/C++, System Verilog/Verilog, Python, Matlab, Java, JavaScript, Linux, UNIX, Windows, MacOS, SQL
Embedded Systems/Digital Design: Communication Protocols (I2C, SPI, UART, CAN), FPGA, ARMv7 ISA
Equipment: STM32 Nucleo Dev Board, Arduino, Logic Analyzer, Oscilloscope, SMD Soldering
Applications: Altium, Git, STM32Cube, LTSpice, ModelSim, Quartus Prime, Docker, Jupyter Notebook, Android Studio, Angular, SpringBoot, Jira
Certifications: Fundamentals of Verification & System Verilog (Udemy), Learning FPGA Development (LinkedIn Learning), Android Basics (Udacity)

PROJECT EXPERIENCE

Michigan Mars Rover Team, University of Michigan **Ann Arbor, MI**
Embedded Hardware & Software Team Member *Aug. 2022 - Present*

- Designed 24v-converter and brushed dc motor controller printed circuit boards on Altium to assist power distribution and motor control of various components of rover
- Worked in schematic design and layout of a CAN transceiver to aid in team's transition to CAN communication protocol
- SMD soldered and assembled various printed circuit boards integral to rover operations
- Debugged several brushed dc motor controller boards to ensure their functionality in rover arm.

WORK EXPERIENCE

General Motors, Inc. **Warren, MI**
Software Engineering Intern - Profitability: Mechatronics & Sensing Hardware *June 2024 - Aug. 2024*

- Organized and built wire-harness materials catalog in SQL to assist engineers' design decisions
- Rewrote existing SQL queries to fix various errors on PowerBI dashboards on EV vehicle power distribution systems

University of Michigan **Ann Arbor, MI**
ECE Department Grader - EECS 215 : Introduction to Electronic Circuits *Aug. 2024 - Present*

- Graded student assignments in the course to assist course instructors in 350+ student course

Supplemental Instruction Leader - EECS 280: Programming & Introductory Data Structures (C++) *Aug. 2023 - Present*

- Conducted weekly lectures reviewing course topics on Object Oriented Programming and Data Structures in C++
- Taught basics of Git and debugging to help new students learn standard practices while working on projects

SquareTrade, Inc. **Brisbane, CA**
Fullstack Software Engineering Intern - Consumer Applications (Remote) *June 2023 - Aug. 2023*

- Built consumer electronic warranty replacement portal in Angular & Spring Boot to extend current TV replacement application
- Designed algorithm that matches original product to replacement options with potential business partners' APIs improving current portal's manual feature matching approach

PROJECTS | Github: https://github.com/akshayanr

Automated Pill Dispenser - Embedded Systems Project | *STM32L4 MCU, SPI, UART* *Feb 2024 - May 2024*

- Built a interactive, automated pill dispensing system with biometric security system, touch display, and pill detection features
- Designed Custom User Interface & Graphics on ILI9488 TFT display with SPI Communication
- Configured Pixy2 Camera with SPI Communication to build pill scanning mechanism
- Developed fingerprint management system with Arduino Uno using UART communication with fingerprint sensor

4-Function Calculator - Logic Design Project | *Verilog, ModelSim, Quartus Prime, Altera DE2-115* *May 2023*

- Built an RTL sequential calculator in Verilog that performs addition, subtraction, multiplication, and division
- Implemented ripple carry adder and Booth's multiplication algorithm with error checking
- Tested design through testbench simulations on ModelSim and manual operations on Altera DE2-115

Dorm Security Lock System | *Verilog, ModelSim, Quartus Prime* *Aug. 2023 - Present*

- Designed a RTL security lock system in Verilog to improve Finite State Machine logic in UM dorm door locks
- Developed edge case test benches and simulated design in ModelSim