Write up

The simulator results did not match for all trace files. Only Mcf trace file is perfectly matching.

The experiments were carried out as follows

1) Upper limit on c1 and c2 was decided

2) Then keeping everything else 0 (i.e. s1, s2 and k) b1 and b2 were varied till a minimum AAT was achieved for each file.

3) Then in a similar fashion keeping everything else constant and k=0, s1 and s2 were varied till a minimum AAT was achieved for each file.

4) Lastly only k was varied.

Some of the results along with the final result have been shown below for each trace file.

A) Mcf output

1) Trace file output

```
$ ./cachesim < traces/mcf.trace
Cache Settings
C1: 12
B1: 5
S1: 3
C2: 15
B2: 6
S2: 5
K: 2

generating set associative cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 507700
Reads Issued by CPU: 280182
L1 Read misses: 2041
L2 Read misses: 5502
Writes Issued by CPU: 227518
L1 Write misses: 8513
L2 Write misses: 0
Write backs to Main Memory: 4854
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 8.143281
```

2) Experiments

```
$ ./cachesim < traces/mcf.trace
Cache Settings
C1: 15
B1: 6
S1: 0
C2: 17
B2: 11
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 507700
Reads Issued by CPU: 280182
L1 Read misses: 3829
L2 Read misses: 3500
Writes Issued by CPU: 227518
L1 Write misses: 6004
L2 Write misses: 1334
Write backs to Main Memory: 3519
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 5.524388
```

```
$ ./cachesim < traces/mcf.trace
Cache Settings
C1: 15
B1: 7
S1: 0
C2: 17
B2: 11
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 507700
Reads Issued by CPU: 280182
L1 Read misses: 5148
L2 Read misses: 3114
Writes Issued by CPU: 227518
L1 Write misses: 4145
L2 Write misses: 777
Write backs to Main Memory: 2976
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 5.139988
```

```
Cache Settings
C1: 15
B1: 6
S1: 0
C2: 17
B2: 11
S2: 4
K: 0

generating direct mapped cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 507700
Reads Issued by CPU: 280182
L1 Read misses: 3829
L2 Read misses: 223
Writes Issued by CPU: 227518
L1 Write misses: 6004
L2 Write misses: 25
Write backs to Main Memory: 145
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 2.328077
```

```
$ ./cachesim < traces/mcf.trace
Cache Settings
C1: 15
B1: 6
S1: 0
C2: 17
B2: 11
S2: 4
K: 4

generating direct mapped cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 507700
Reads Issued by CPU: 280182
L1 Read misses: 3829
L2 Read misses: 223
Writes Issued by CPU: 227518
L1 Write misses: 6004
L2 Write misses: 25
Write backs to Main Memory: 145
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 2.328077
```

Final result cache specifications are 15,6,0,17,11,4,4 for MCF

B) Astar output

1) Trace file output

```
$ ./cachesim < traces/astar.trace
Cache Settings
C1: 12
B1: 5
S1: 3
C2: 15
B2: 6
S2: 5
K: 2

generating set associative cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 501468
Reads Issued by CPU: 289766
L1 Read misses: 14177
L2 Read misses: 19733
Writes Issued by CPU: 211702
L1 Write misses: 39111
L2 Write misses: 33
Write backs to Main Memory: 19711
Prefetched blocks: 7243
Successful prefetches: 7172
Average access time (AAT): 22.912818
```

2)experiments

```
$ ./cachesim < traces/astar.trace
Cache Settings
C1: 15
B1: 7
S1: 0
C2: 17
B2: 11
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 501468
Reads Issued by CPU: 289766
L1 Read misses: 9787
L2 Read misses: 4445
Writes Issued by CPU: 211702
L1 Write misses: 10889
L2 Write misses: 707
Write backs to Main Memory: 2167
Prefetched blocks: 240
Successful prefetches: 233
Average access time (AAT): 6.596911
```

```
$ ./cachesim < traces/astar.trace
Cache Settings
C1: 15
B1: 7
S1: 0
C2: 17
B2: 11
S2: 4
K: 0

generating direct mapped cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 501468
Reads Issued by CPU: 289766
L1 Read misses: 9787
L2 Read misses: 1720
Writes Issued by CPU: 211702
L1 Write misses: 10889
L2 Write misses: 95
Write backs to Main Memory: 814
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 3.945858
```

```
$ ./cachesim < traces/astar.trace
Cache Settings
C1: 15
B1: 7
S1: 0
C2: 17
B2: 11
S2: 5
K: 2

generating direct mapped cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 501468
Reads Issued by CPU: 289766
L1 Read misses: 9787
L2 Read misses: 1456
Writes Issued by CPU: 211702
L1 Write misses: 10889
L2 Write misses: 87
Write backs to Main Memory: 804
Prefetched blocks: 262
Successful prefetches: 251
Average access time (AAT): 3.699123
```

Final result Cache settings are 15,7,0,17,11,5,2 for Astar

C) Perlbench

1) Trace file output

```
$ ./cachesim < traces/perlbench.trace
Cache Settings
C1: 12
B1: 5
S1: 3
C2: 15
B2: 6
S2: 5
K: 2

generating set associative cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 507441
Reads Issued by CPU: 302052
L1 Read misses: 35427
L2 Read misses: 13748
Writes Issued by CPU: 205389
L1 Write misses: 14441
L2 Write misses: 2
Write backs to Main Memory: 6148
Prefetched blocks: 1134
Successful prefetches: 1027
Average access time (AAT): 16.736043
```

2) Experiments

```
Cache Settings
C1: 15
B1: 6
S1: 0
C2: 17
B2: 11
S2: 0
K: 2

generating direct mapped cache for l
generating direct mapped cache for l
Cache Statistics
L1 Accesses: 507441
Reads Issued by CPU: 302052
L1 Read misses: 21796
L2 Read misses: 6833
Writes Issued by CPU: 205389
L1 Write misses: 9280
L2 Write misses: 2575
Write backs to Main Memory: 3806
Prefetched blocks: 28
Successful prefetches: 17
Average access time (AAT): 8.977765
```

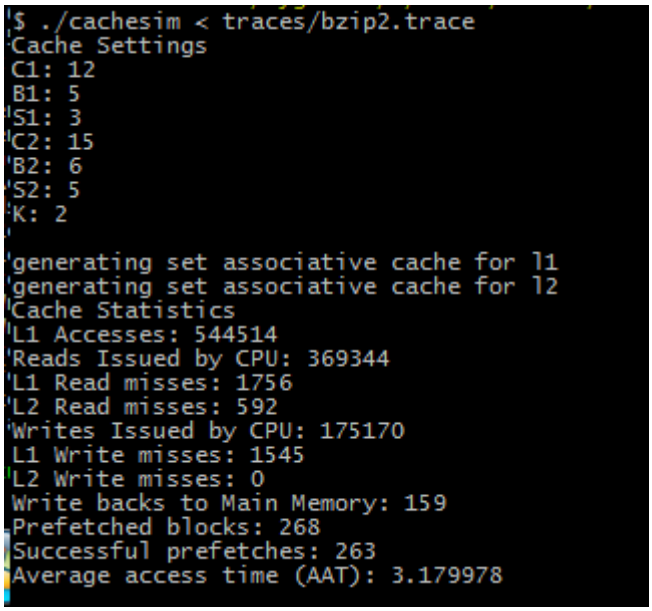
```
$ ./cachesim < traces/perlbench.trace
Cache Settings
C1: 15
B1: 5
S1: 0
C2: 17
B2: 10
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 507441
Reads Issued by CPU: 302052
L1 Read misses: 22578
L2 Read misses: 6629
Writes Issued by CPU: 205389
L1 Write misses: 12389
L2 Write misses: 2781
Write backs to Main Memory: 3868
Prefetched blocks: 10
Successful prefetches: 6
Average access time (AAT): 8.807428
```

```
Cache Settings
C1: 15
B1: 5
S1: 0
C2: 17
B2: 10
S2: 6
K: 0

generating direct mapped cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 507441
Reads Issued by CPU: 302052
L1 Read misses: 22578
L2 Read misses: 2226
Writes Issued by CPU: 205389
L1 Write misses: 12389
L2 Write misses: 329
Write backs to Main Memory: 790
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 4.634373
```

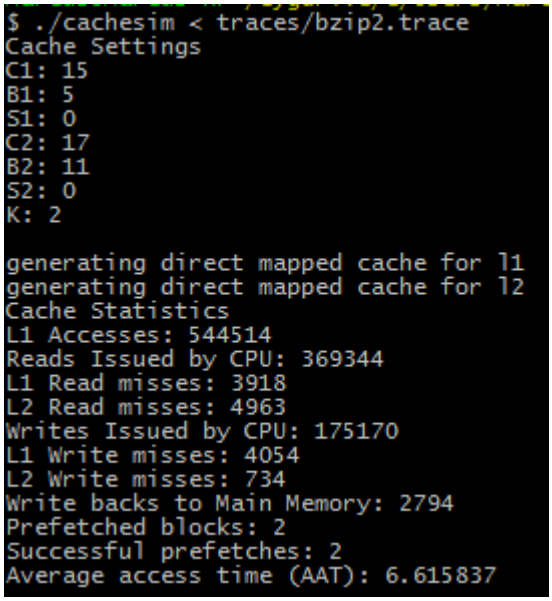
3) Final result Cache settings for perlbench are 15,5,0,17,10,6,0

D) Bzip2

1) Trace file output



2) experiments



```
$ ./cachesim < traces/bzip2.trace
Cache Settings
C1: 15
B1: 3
S1: 0
C2: 17
B2: 11
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 544514
Reads Issued by CPU: 369344
L1 Read misses: 6076
L2 Read misses: 3880
Writes Issued by CPU: 175170
L1 Write misses: 6263
L2 Write misses: 973
Write backs to Main Memory: 2310
Prefetched blocks: 2
Successful prefetches: 2
Average access time (AAT): 5.653452
```

```
$ ./cachesim < traces/bzip2.trace
Cache Settings
C1: 15
B1: 3
S1: 0
C2: 17
B2: 12
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 544514
Reads Issued by CPU: 369344
L1 Read misses: 6076
L2 Read misses: 3867
Writes Issued by CPU: 175170
L1 Write misses: 6263
L2 Write misses: 973
Write backs to Main Memory: 2310
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 5.641515
```

```
$ ./cachesim < traces/bzip2.trace
Cache Settings
C1: 15
B1: 2
S1: 0
C2: 17
B2: 12
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 544514
Reads Issued by CPU: 369344
L1 Read misses: 6824
L2 Read misses: 3800
Writes Issued by CPU: 175170
L1 Write misses: 8891
L2 Write misses: 1006
Write backs to Main Memory: 2244
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 5.604793
```

```
$ ./cachesim < traces/bzip2.trace
Cache Settings
C1: 15
B1: 1
S1: 0
C2: 17
B2: 12
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 544514
Reads Issued by CPU: 369344
L1 Read misses: 7682
L2 Read misses: 3245
Writes Issued by CPU: 175170
L1 Write misses: 13955
L2 Write misses: 843
Write backs to Main Memory: 1861
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 5.138667
```

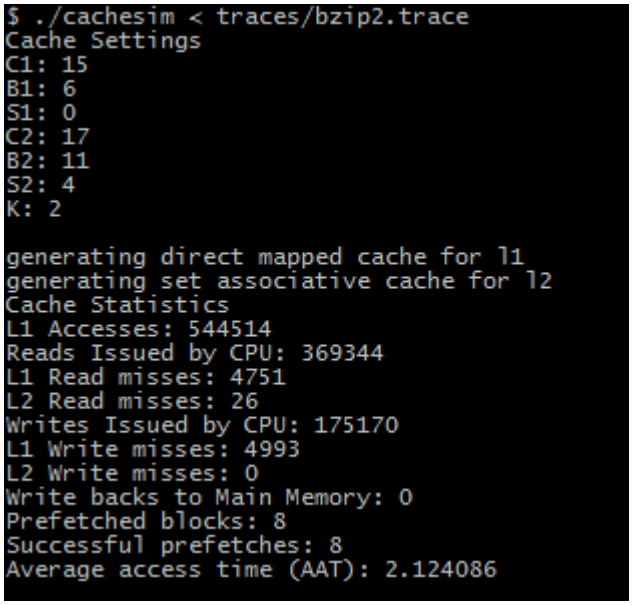
```
C1: 15
B1: 0
S1: 0
C2: 17
B2: 12
S2: 0
K: 2

generating direct mapped cache for l1
generating direct mapped cache for l2
Cache Statistics
L1 Accesses: 544514
Reads Issued by CPU: 369344
L1 Read misses: 9721
L2 Read misses: 2628
Writes Issued by CPU: 175170
L1 Write misses: 24435
L2 Write misses: 633
Write backs to Main Memory: 1399
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 4.664071
```

```
$ ./cachesim < traces/bzip2.trace
Cache Settings
C1: 15
B1: 0
S1: 1
C2: 17
B2: 12
S2: 2
K: 0

generating set associative cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 544514
Reads Issued by CPU: 369344
L1 Read misses: 8896
L2 Read misses: 19
Writes Issued by CPU: 175170
L1 Write misses: 22706
L2 Write misses: 0
Write backs to Main Memory: 0
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 2.496025
```

```
$ ./cachesim < traces/bzip2.trace
Cache Settings
C1: 15
B1: 0
S1: 1
C2: 17
B2: 12
S2: 2
K: 4

generating set associative cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 544514
Reads Issued by CPU: 369344
L1 Read misses: 8896
L2 Read misses: 19
Writes Issued by CPU: 175170
L1 Write misses: 22706
L2 Write misses: 0
Write backs to Main Memory: 0
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 2.496025
```

```
$ ./cachesim < traces/mcf.trace
Cache Settings
C1: 15
B1: 6
S1: 0
C2: 17
B2: 11
S2: 3
K: 0

generating direct mapped cache for l1
generating set associative cache for l2
Cache Statistics
L1 Accesses: 507700
Reads Issued by CPU: 280182
L1 Read misses: 3829
L2 Read misses: 236
Writes Issued by CPU: 227518
L1 Write misses: 6004
L2 Write misses: 16
Write backs to Main Memory: 139
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 2.333133
```

```
$ ./cachesim < traces/bzip2.trace
Cache Settings
C1: 15
B1: 6
S1: 0
C2: 17
B2: 11
S2: 4
K: 0

generating direct mapped cache for l1
generating set associative cache for
Cache Statistics
L1 Accesses: 544514
Reads Issued by CPU: 369344
L1 Read misses: 4751
L2 Read misses: 34
Writes Issued by CPU: 175170
L1 Write misses: 4993
L2 Write misses: 0
Write backs to Main Memory: 0
Prefetched blocks: 0
Successful prefetches: 0
Average access time (AAT): 2.131432
```



Final result cache settings for bzip2 are (15,6,0,17,11,4,2)