INTERNSHIP REPORT

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PROJECT 2:

DESIGNING OF BIAS GENERATION AND SINGLE STAGE OPERATIONAL AMPLIFIER CIRCUIT

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1. OBJECTIVE

This report provides an in-depth analysis of the design principles and operational functionalities of both the Bias-generator and Single-stage operational amplifier circuit, adhering to predetermined parameters. Through comprehensive examination, the study aims to assess the performance and efficacy of these circuits by elucidating their design methodologies, circuit realization techniques, and operational behaviors. By offering a detailed exploration of their design concepts and practical implementations, this work seeks to provide a holistic understanding of the functioning of these circuits.

2. BIAS GENERATOR

A bias generation circuit is a fundamental component in electronic circuits, particularly in analog circuits such as amplifiers and oscillators. Its primary function is to establish a stable operating point for active devices like transistors or operational amplifiers. The operating point, also known as bias point or quiescent point, ensures that the active device operates in its linear region, where it can accurately amplify or process signals without distortion.

It ensures optimal performance by setting the operating parameters within desired ranges. By maintaining stable bias conditions, it minimizes distortion and improves linearity in signal processing. This circuit plays a vital role in maintaining circuit stability despite variations in temperature, power supply, and component characteristics. Overall, the bias generation circuit is essential for ensuring reliable and consistent operation of electronic systems.

i. SPECIFICATION OF THE DESIGN:

Design a cascode Bias Generator circuit using NMOS to produce 3 different branch currents of 1.5mA, 4mA and 6mA respectively. The bias current is 30uA.

ii. SCHEMATIC :

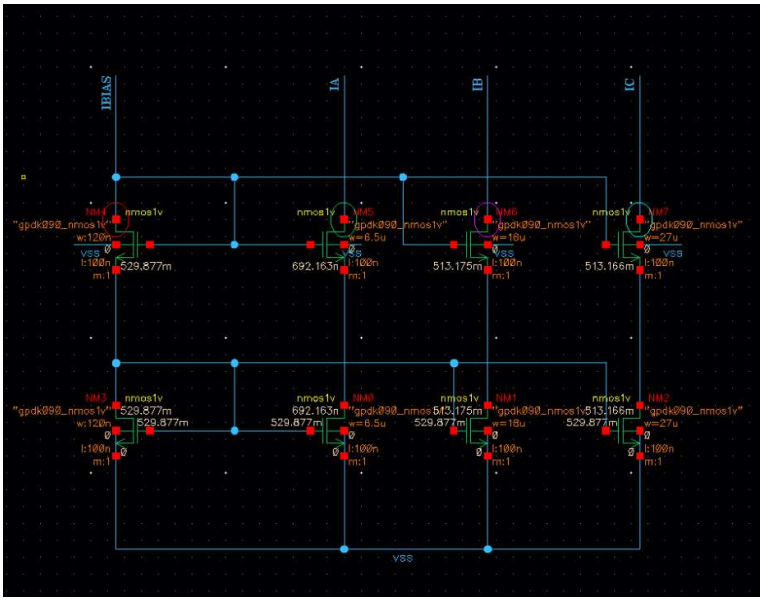
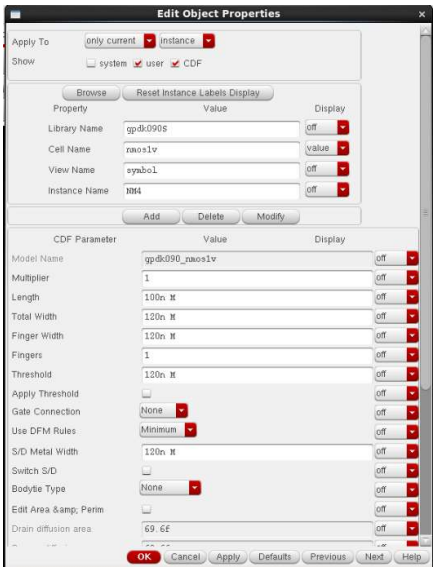


Fig no 2.1 Schematic Diagram of Bias-generator without specifications

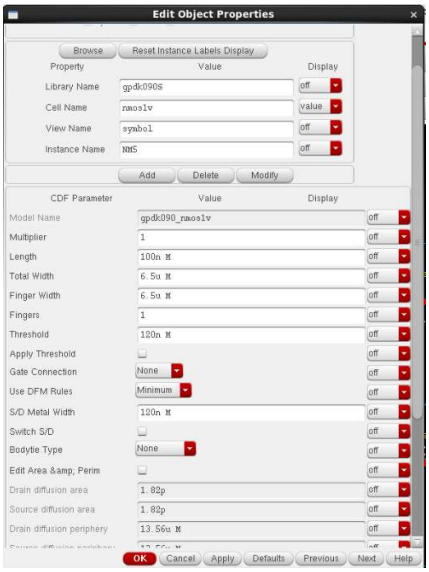
STRENGTH DETERMINATION:

In order to achieve the specification of the design, the first step is to fix the strength or transistor width of the reference devices. The left most NMOSs are the reference devices in this circuit.

- We fixed the reference NMOS strength as 1X i.e, the width of the reference devices is given as 120n.
- With accordance to the reference devices current flow through IA, IB and IC terminals were identified by dc analysis.
- Strength of the devices are varied to achieve the specification.
- After all analysis the strength of the transistors were fixed as follows:
  - **First column transistor width:** 6.5um
  - **Second column transistor width:** 18um
  - **Third column transistor width:** 27um



A



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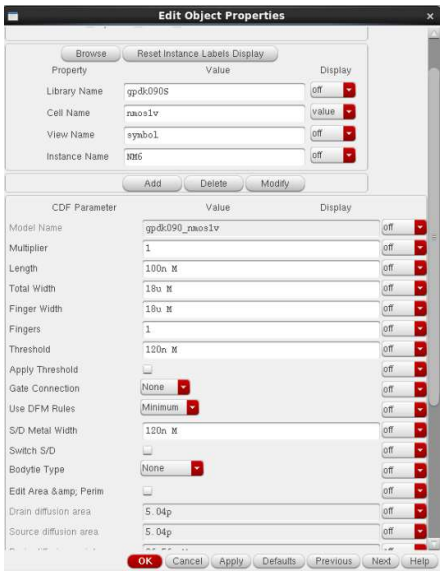

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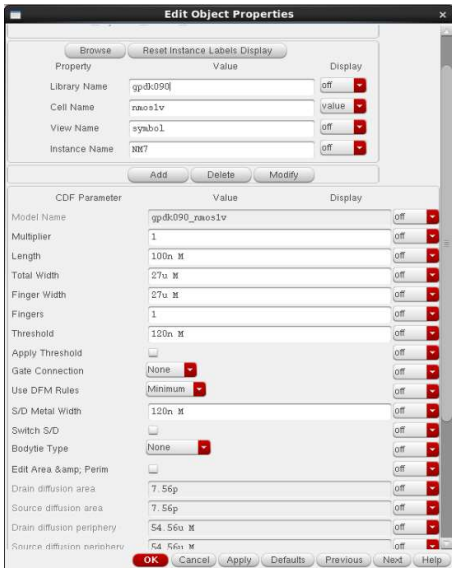
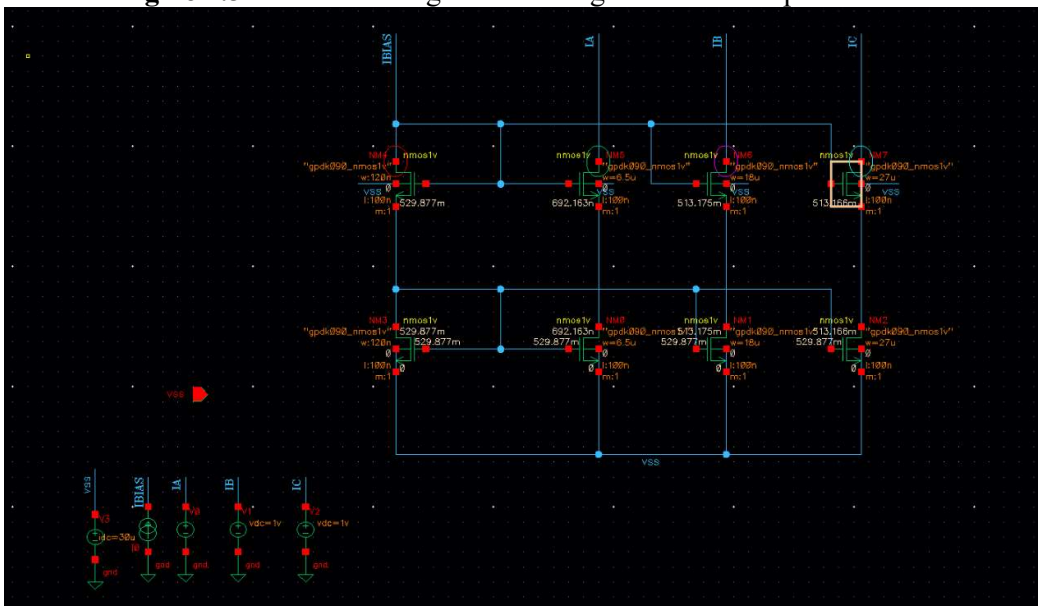


D

Fig no 2.2 Parameters of (A)FIRST COLUMN (B)SECOND COLUMN (C)THIRD COLUMN (D)FORTH COLUMN

FINAL SCHEMATIC :

Fig no 2.3 Schematic Diagram of Bias-generator with specifications



iii. DC ANALYSIS:

DC analysis, or Direct Current analysis, is a method used in electronics to study the behavior of electronic circuits under steady-state conditions when all voltages and currents are constant with respect to time. In DC analysis, capacitors are treated as open circuits, and inductors are treated as short circuits, effectively removing their transient effects.

- DC analysis gives us the node current values for the given bias voltage.
- By varying the strength of the transistors we can observe the change in drain node current of each device by running dc analysis
- We increase the strength and run DC analysis again and again until we meet our specifications.

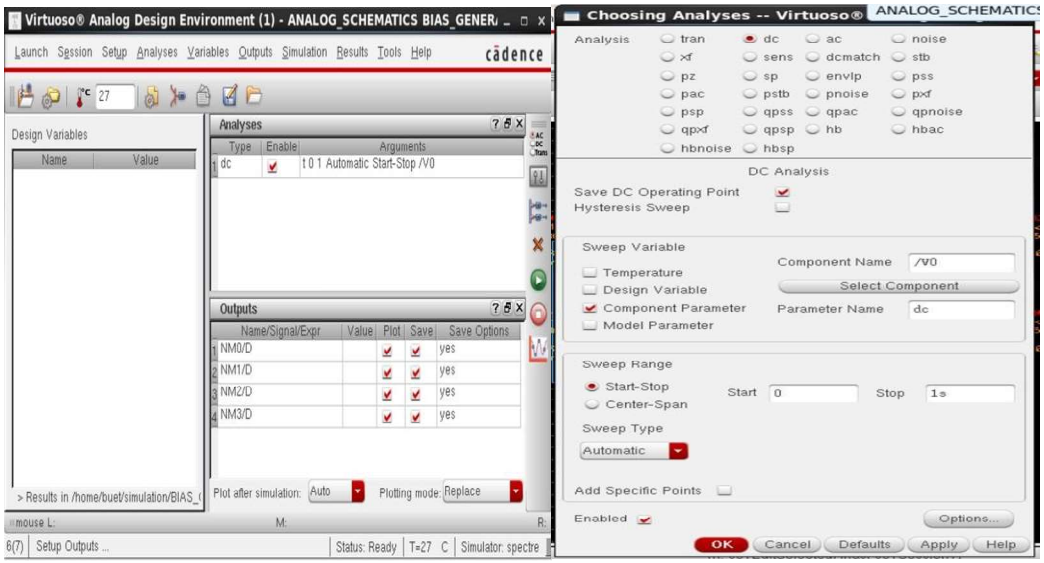


Fig no 2.4 ADL setup for Bias-generator dc analysis

DC ANALYSIS OUTPUT WAVEFORM:

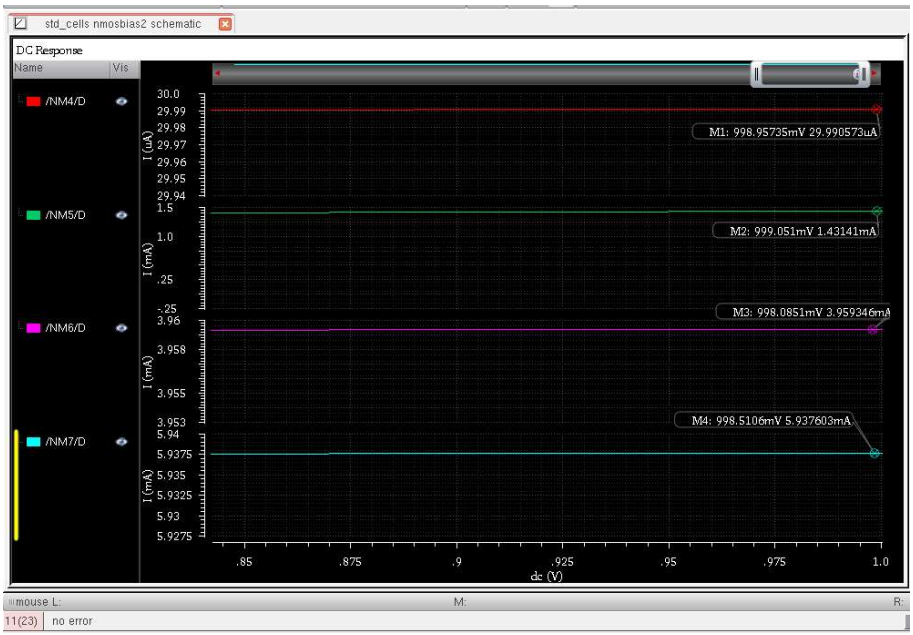


Fig no 2.5 ac analysis output waveform

INPUT CURRENT : 30u

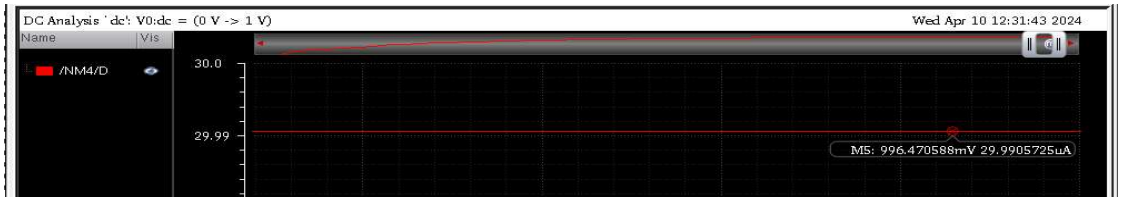


Fig no 2.6 Input current graph

OUTPUT CURRENTS: IA: 1.5mA , IB: 4mA, IC: 6mA

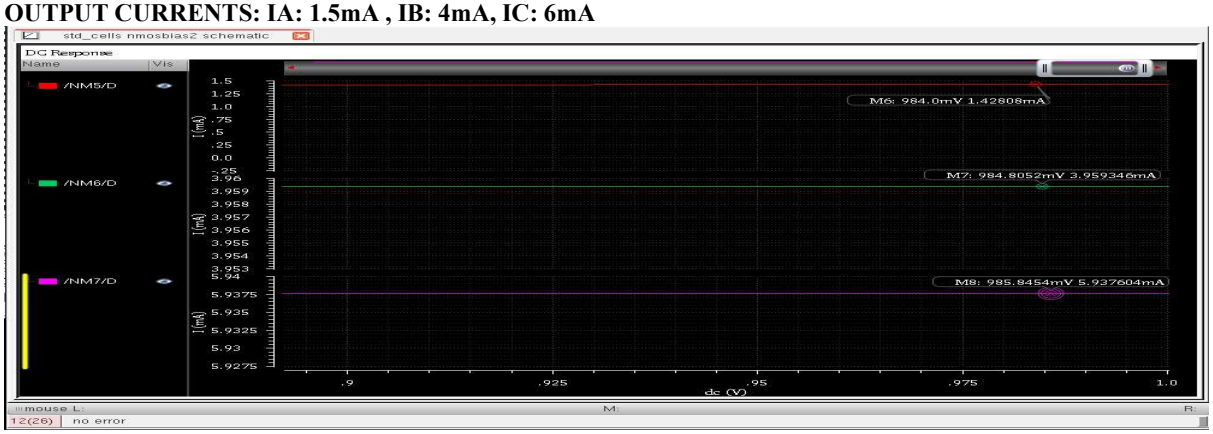


Fig no 2.7 Output current graph

v. CONCLUSION

In conclusion, the bias generator circuit is designed for the given specifications. Through careful design and implementation, the bias generator ensures optimal performance by minimizing distortion, improving linearity, and enhancing circuit stability. Its significance lies in enabling reliable and efficient signal processing across a wide range of applications. Moving forward, continued research and development efforts will further refine bias generator designs, contributing to advancements in electronic technology and facilitating the creation of more sophisticated and high-performance electronic systems.

SIMULATION FINDINGS OF BIAS GENERATOR:

- **First column transistor width:** 6.5 um, IA= 1.5mA
- **Second column transistor width:** 18um, IB= 4mA
- **Third column transistor width:** 27um, IC= 6mA

1. SINGLE STAGE DIFFERENTIAL AMPLIFIER

A single-stage operational amplifier, often referred to simply as an op-amp, is a fundamental building block in electronics used for amplification, signal conditioning, filtering, and many other applications. It typically consists of a high-gain differential amplifier stage followed by additional circuitry for stabilization and signal processing.
A single-stage operational amplifier (op-amp) can indeed be constructed using a current mirror configuration.
By using a current mirror configuration, a single-stage operational amplifier can achieve high gain, precise current matching, and improved linearity. It's a common approach in integrated circuit design, particularly for low-power and high-frequency applications where compactness and efficiency are crucial.

i. SPECIFICATION OF THE DESIGN:

Design a differential amplifier with VDD = 1.8V, IN_P = 1.4, IN_N = 0.7, Load Capacitance = 12pF, Slew rate = 5 V/u sec for a GBP of 5 MHz (Base L = 1u, Base W = 10u).

ii. SCHEMATIC:

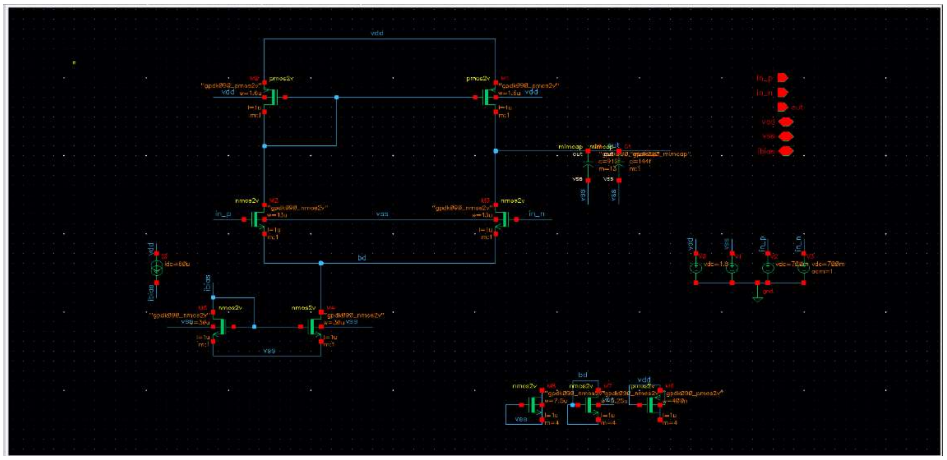


Fig no 3.1 Schematic diagram of single stage differential amplifier

In order to design the circuit we must follow the below steps

- Firstly we need to calculate the bias current for the circuit. As we know the slew rate of the design we can find the bias current using the formula

$$\mathbf{I_o = C\ SR}$$

- The bias current we obtained is 60um
- Next step is to assume the values of W, L, V_{th}.
- Let us assume W=10um, L=1um, V_{th} = 0.44 V.
- For the circuit to be linear and stable all the transistors should be in saturation region. So Vds > Vgs - Vth , Vgs = 1.4V , we get Vds = 0.835V and Vd = 0.965V.
- For the calculation of W/L ratio we need to know the beta_eff value. So we run dc analysis for the below circuit.

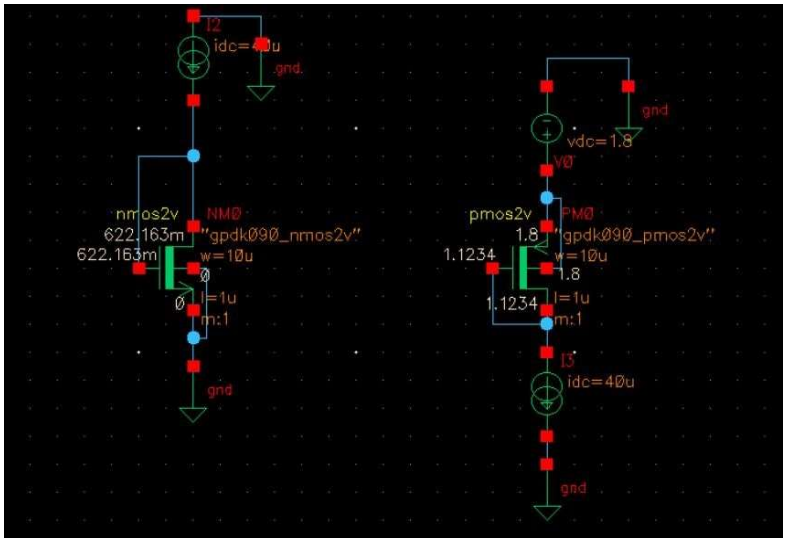


Fig no 3.2 Threshold voltages and beta_eff are to be found for nMOS and pMOS

Beta_eff found : PMOS : 1679.11u , NMOS: 2852.2u

Threshold voltage found : PMOS : -0.417 V, NMOS: 0.435 V

- Further calculation is given below:

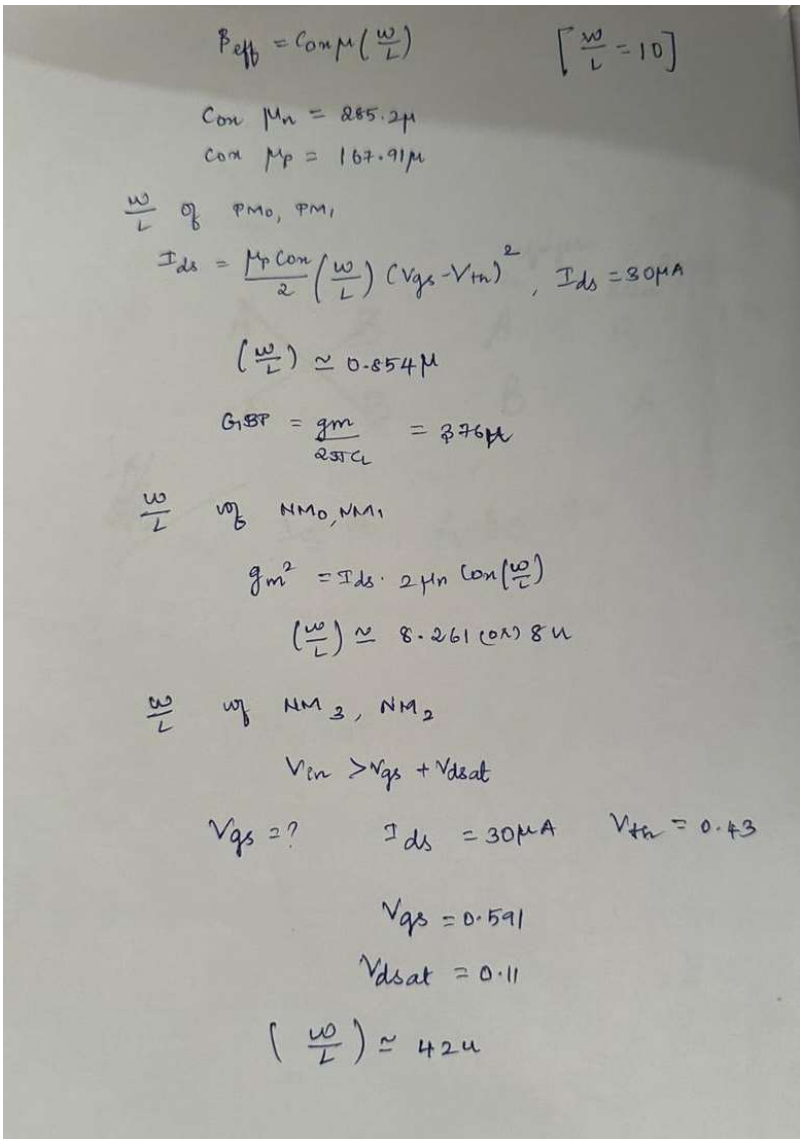


Fig no 3.3 Calculation to find W/L ratio

iii. DC ANALYSIS:

DC analysis id used to check whether all the transistors are in saturation region. If the device is not in saturation region width of the transistor is increased and DC analysis is done again.

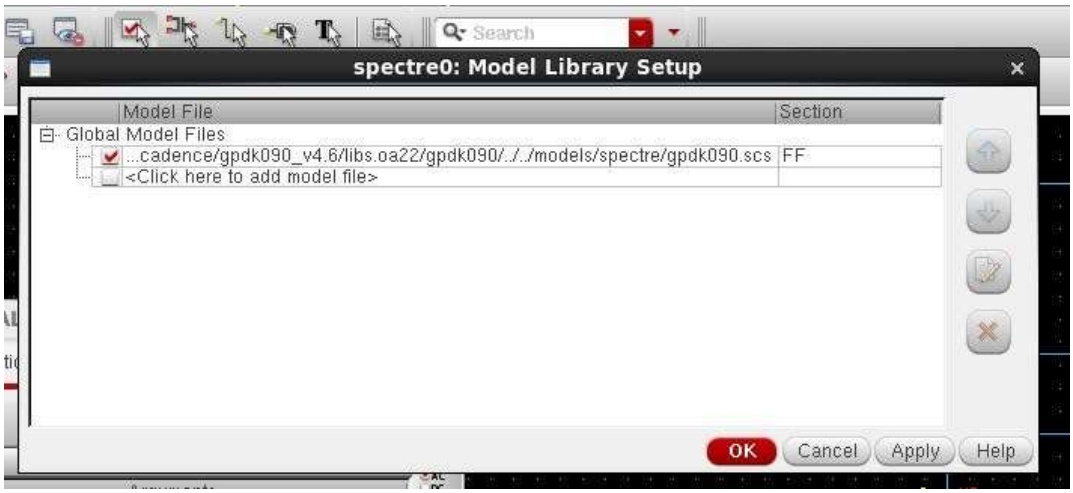


Fig no 3.4 Model Library setup (pMOS and nMOS set to work in fast mode)

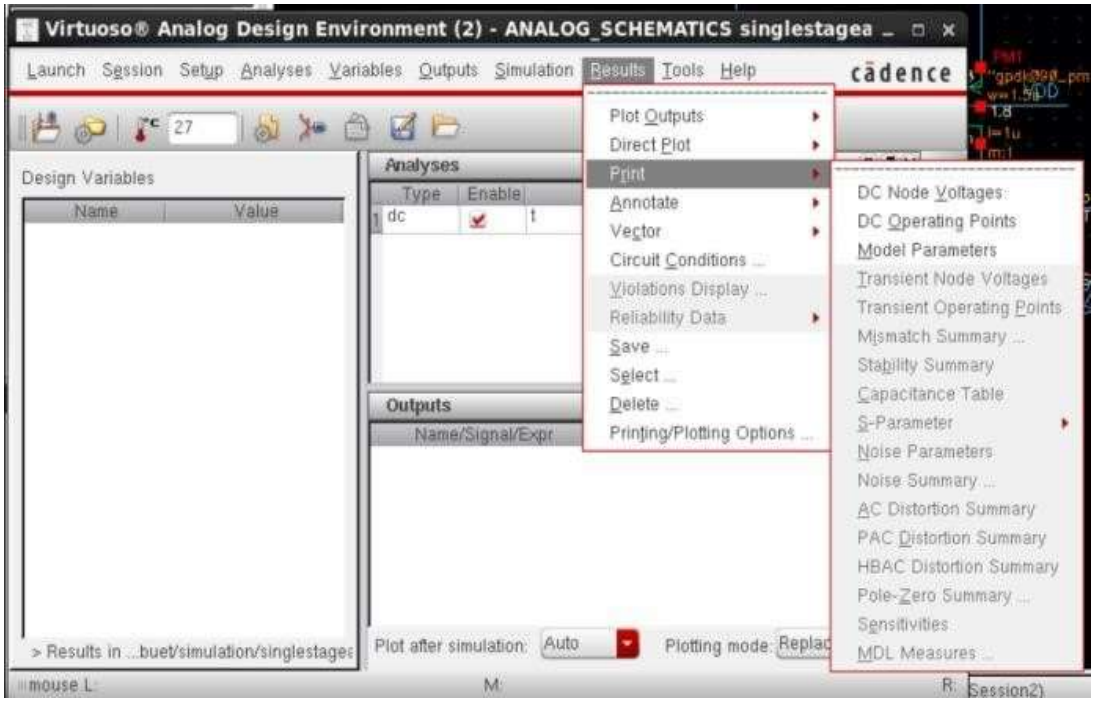


Fig no 3.5 ADE L Setup for dc analysis of single stage differential amplifier

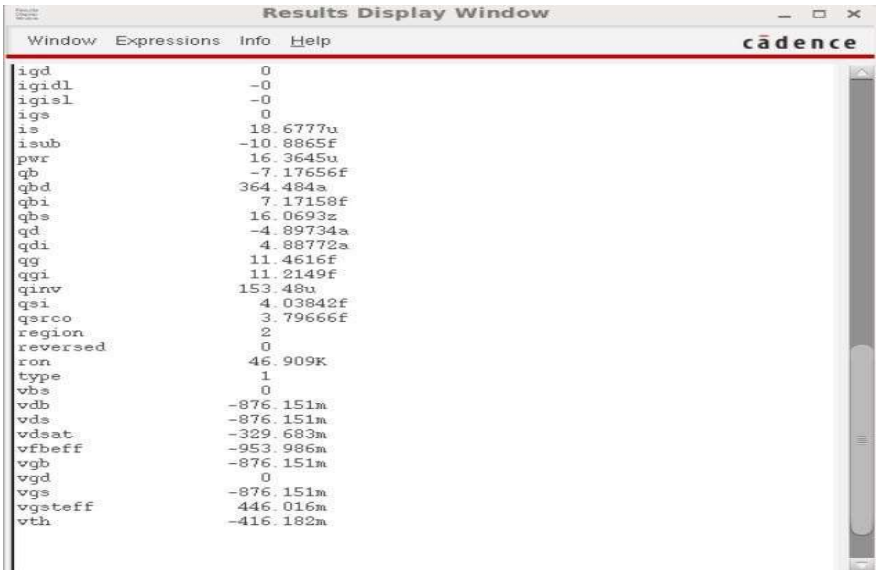


Fig no 3.6 All the transistors have to be in saturation region

iv. AC ANALYSIS:

AC analysis is done to check whether our design meets expected the gain bandwidth product. If the value of GBP is less than expected we increase the width of the NM0 and NM1 transistors and run the AC analysis plot again.

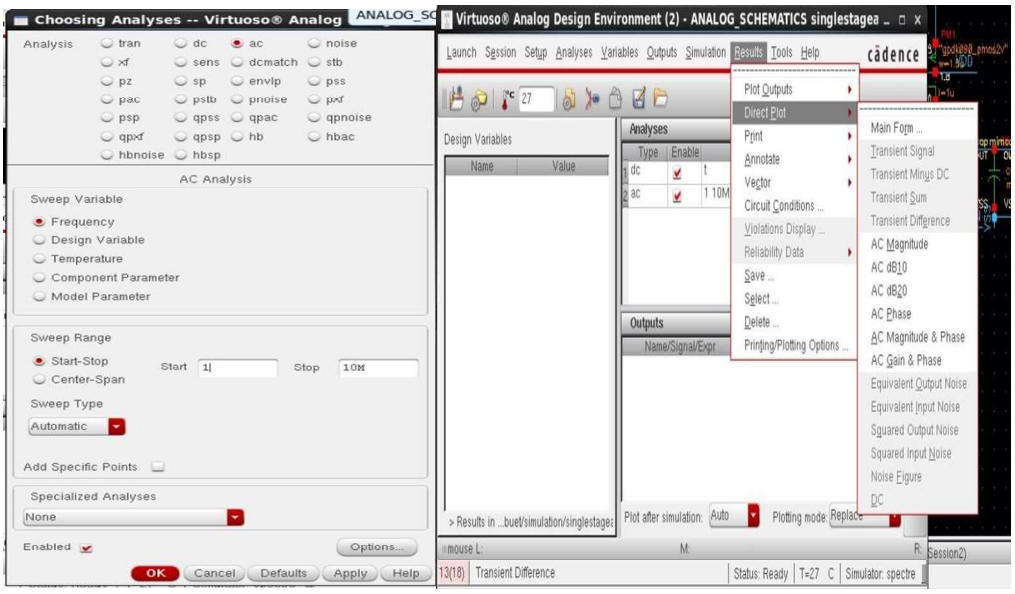


Fig no 3.7 ADE L setup for ac analysis of single stage differential amplifier

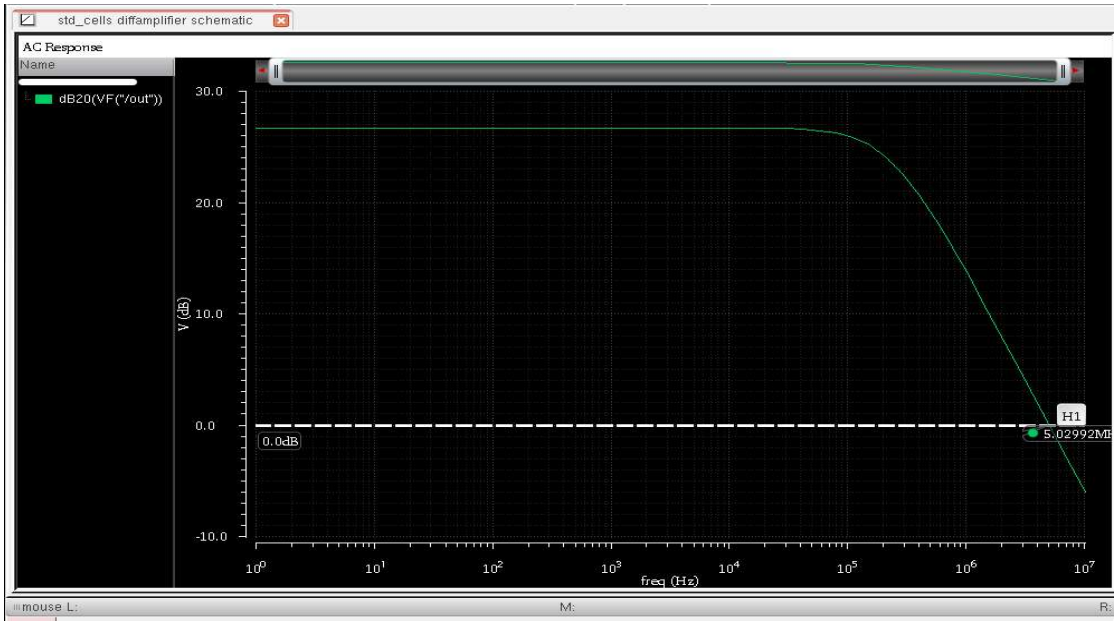


Fig no 3.8 AC analysis output waveform (the required gain bandwidth product hasbeen obtained)

- After all analysis the strength of the transistors were fixed as follows:
  - **M1,M2 transistor width & length :** 1.6um
  - **M3,M4 transistor width & length :** 13um
  - **M5,M6 transistor width & length :** 30um

v. LAYOUT:

MATCHING PROCESS:

Matching process is crucial in analog circuits where precise matching between components is necessary to achieve desired performance metrics such as gain, bandwidth, linearity, and noise performance.

TYPES:

1. INTERDIGITIZATION
2. COMMON CENTROID

Here we used common centroid matching method to design the layout.

Pattern of matching:

A B
B A
D C
C D
E F
F E

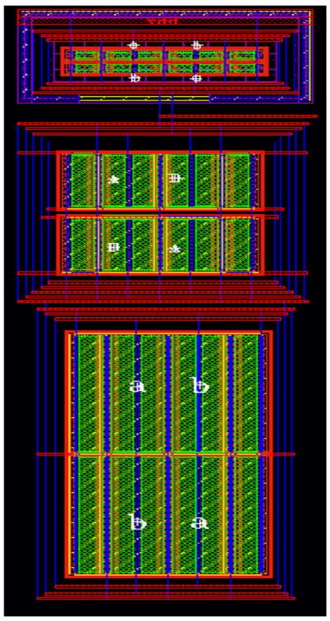


Fig no 3.9 Layout of single stage differential amplifier

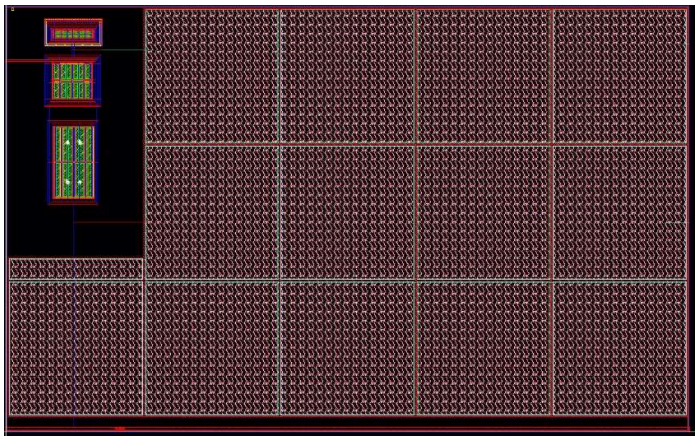


Fig no 3.10 Layout of single stage differential amplifier with mimcap

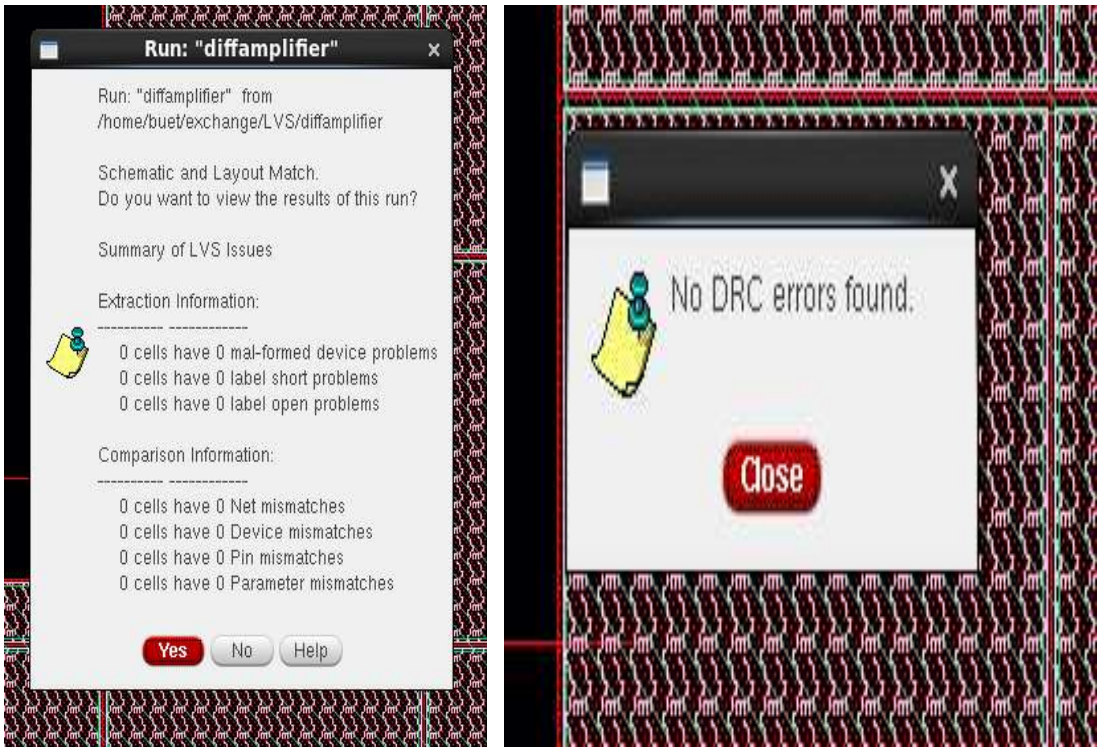


Fig no 3.11 LVS and DRC clear screenshots

vi. CONCLUSION

In conclusion, the design of the single-stage amplifier circuit is designed for given specification. This circuits represents a critical aspect of electronic circuitry. Through meticulous design methodologies and thorough analysis of operational characteristics, the circuits exhibit improved linearity, reduced distortion, and enhanced stability.

SIMULATION FINDINGS OF SINGLE STAGE OPERATIONAL AMPLIFIER :

- **M1,M2 transistor width & length :** 1.6um
- **M3,M4 transistor width & length :** 13um
- **M5,M6 transistor width & length :** 20um
- **Gain bandwidth ratio achieved:** 5.02MHz

LAYOUT DISCRIPTION:

- **Area of the layout:** 14771.702 (153.92 X 95.97)
- **No of dummy & void cells used:** 12 & 0
- **No of metal layers used:** 3