System level design of CMOS image sensor with high dynamic range and fill factor

K. Akshay,Parvathy R Pillai and B. Bhuvan

This letter presents the system level design of a novel complementary metal-oxide semiconductor (CMOS) image sensor. The proposed image sensor consists of one transistor and photodiode per pixel and hence has a very high fill factor. Therefore, the imagers using the proposed pixel can have increased pixel density compared to the imagers employing conventional 3-T/4-T pixels. The logarithmic behaviour of the proposed pixel ensures a high dynamic range to the image sensor. Further, the operation of a conventional image sensor involves charge integration, charge transfer, voltage measurement, analog to digital conversion and finally storage in the memory after some signal processing. But the proposed image sensor, even though operates in a different way, parallelizes some of these steps and hence is suited for video applications demanding large frame rates.

Introduction: Complementary metal-oxide semiconductor (CMOS) image sensor has replaced charge coupled devices (CCD) in most of the applications owing to its low cost, low power consumption and ease of integration with the other circuitries in an image sensor chip [1, 2]. Despite these promising features, the performance of a conventional linear mode active pixel sensor (APS) is limited by low dynamic range, making it unsuitable for low light photographic applications [3]. CMOS sensors with logarithmic response were introduced later that could achieve much higher dynamic range. Despite its limitations such as low output voltage swing (0.2 - 0.3 V) and around two orders of magnitude higher fixed pattern noise (FPN) than a linear mode APS [4], these logarithmic sensors were widely studied and used for applications demanding wide dynamic range. In this letter, we propose a CMOS image sensor that can outperform the conventional architectures in terms of fill factor (ratio of photosensitive area to total area of a pixel) while achieving high dynamic range and speed of operation simultaneously.

Theory: CMOS image sensors with logarithmic response generally has a photodiode in reverse bias configuration with its n side connected to the source of a diode connected metal-oxide semiconductor field effect transistor (MOSFET). As the subthreshold current-voltage (I-V) characteristics of a MOSFET is exponential, the photocurrent flowing through the photodiode and the MOSFET, creates a gate to source voltage proportional to the logarithmic value of the photocurrent [5]. But, the proposed image sensor provides logarithmic response by utilizing a fundamental property of the photodiode alone. That is, the open circuit voltage across a photodiode is logarithmically related to the photocurrent produced by the light falling on it. When a light of intensity, ϕ_1, falls on the photodiode, it generates a photocurrent, $I_{\phi 1}$, proportional to the light intensity as shown in Fig. 1.

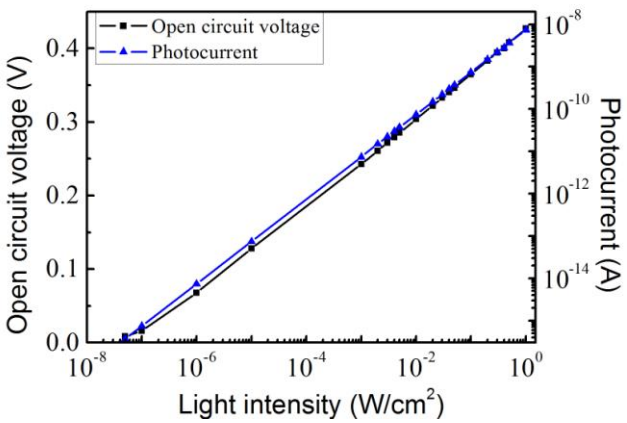

Fig. 1 *TCAD simulation plot showing photocurrent and open circuit voltage across a photodiode vs light intensity (Note that light intensity and photocurrent are in logarithmic axes while voltage axis is linear)*

A forward biasing voltage, V_{oc1} proportional to the logarithm of the light intensity appears across the photodiode if it is in open circuit configuration as shown in Fig. 1.

Now, consider Fig. 2. Here, the photodiode is illuminated with light of intensity, ϕ_1. The device is also forward biased with a voltage source, V_s. The photocurrent, $I_{\phi 1}$ flows from n to p side. The forward bias voltage creates a current, I_f in the opposite direction from p to n side. The forward biasing voltage, V_s could be tuned so that the forward current is of the same magnitude as photocurrent (i.e. $I_f = I_{SC1}$). This results in a net zero current in the external circuit (i.e. I = 0). At this condition, the voltage across the resistor, R, connected in series with the photodiode is zero. The forward biasing voltage required to meet this zero external current condition is a measure of the intensity of light. Further, note that this forward biasing voltage is equal to the open circuit voltage developed across the photodiode when kept in open circuit configuration.

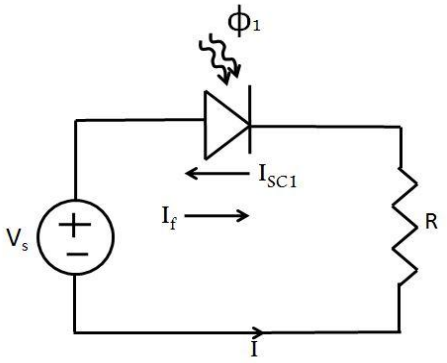

Fig. 2 *Schematic representation of the photodiode under both optical and electrical excitation*

Proposed image sensor: Utilising the fundamental theory explained above, we propose a novel high fill factor and high dynamic range CMOS image sensor whose system level block diagram is shown in Fig. 3. The photodiode has its p side connected to a MOSFET in linear region (V_G to be designed accordingly) that acts as a resistor. A digital ramp is applied at the source side of the MOSFET. The amplitude of the ramp (V_{r0}) at which the drain current of the MOSFET becomes zero is sensed and converted simultaneously into its digital equivalent with the help of a comparator (high gain amplifier) and a counter as shown in Fig 3. The input to the high gain amplifier moves from negative to positive as the ramp amplitude becomes smaller than V_{r0}. When I = 0, $V_{r0} = V_{OC}$ and indicates the light intensity as explained earlier. The conversion ends as the output of the high gain amplifier changes its polarity. V_C is a master control signal. It has to be high for the ramp to start. But, another provision also has to be there to stop the ramp when $Av_i = 0$. All of this has to be taken care while designing the block named X, which can activate or deactivate the ramp generator with its control signal, V_s. Once the ramp is disabled, the value stored in the counter is read out. As the digital ramp and the counter are controlled by the same clock, they follow a linear relation. V_{r0} is logarithmically related to light intensity and so is the digital count corresponding to it. This digital count is similar to the count obtained after the analog-to-digital conversion operation in a conventional image sensor. As here, the digital count is obtained instantly after the detection of the zero current ramp bias voltage, this image sensor offers advantage of higher speed of operation and hence is suited for video applications demanding large frame rates.

Image sensor array: The column parallel architecture of an imager with the proposed pixel is presented in Fig. 4. Hence, we use the idea explained above to propose an image sensor array illustrated in Fig. 4. As each pixel has only a photodiode and a MOSFET, the proposed pixel has high fill factor. The above mentioned statement is true when compared with the conventional logarithmic pixel also. The conventional logarithmic pixel employs one more MOSFET which is

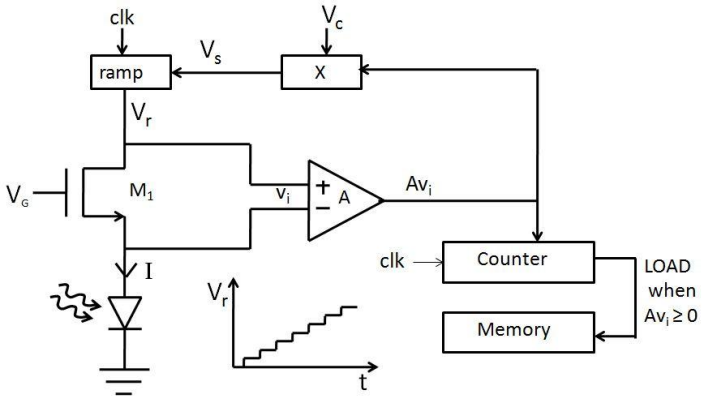

Fig. 3 *Block level diagram of the proposed image sensor*

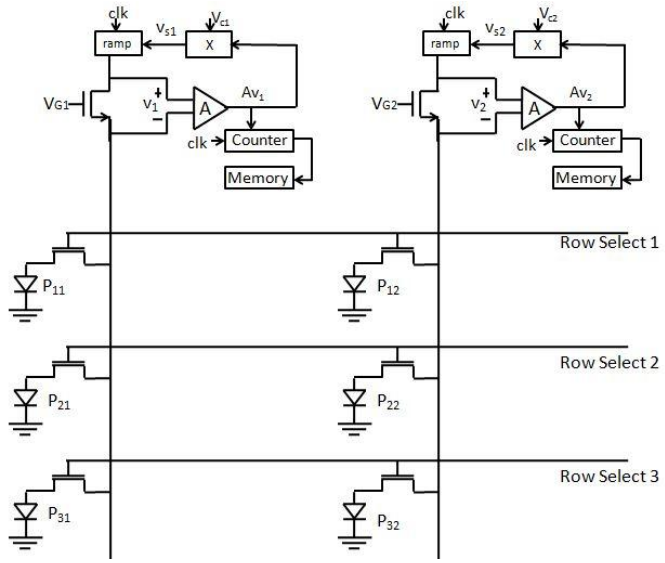

Fig. 4 *Proposed image sensor array. Note that, only a 3×2 array is illustrated, for clarity. This can be extended two dimensionally to obtain large array of pixels. P_{ij} is the pixel in i^{th} row and j^{th} column*

the input device of the source follower in the readout path. Hence, an image sensor chip fabricated with this sensor array can have a large density of pixels. When light falls on this array, all pixels in a single row can be measured simultaneously by activating a row select signal. The row select and all V_{Gj} (where j is the column number) signal amplitudes should be such that all MOSFETS in the pixels of the selected row should be biased in linear region, where they act as simple resistors. From TCAD simulations, it was confirmed that the open circuit voltage for all realistic light intensities is less than 0.4 V for the photodiode used in the design (see Fig. 1). Also, the typical threshold voltage of an n-MOSFET in 0.18 µm technology with 1.8 V supply is below 0.45 V. Hence, it is safe to set the row select and all V_{Gj} signals to 1.8 V. Further, the maximum ramp voltage required would be the open circuit voltage for the maximum expected light intensity. From this, we set the maximum ramp voltage to be 0.4 V. The ramp height is decided depending on the resolution of light intensity desired for the application. For illustration of further operation, we choose an arbitrary small step height of 10 mV. This means that a maximum of 40 steps can be taken by the ramp before it saturates to 0.4 V. If we have a linear counter, the maximum count would be 40. This can be further enhanced by using mode counters that switch between different modes based on the light intensity for getting larger counts. A typical timing scheme used to measure the light incident on pixel P_{11} is illustrated in Fig.5. As the proposed image sensor is not based on charge collection, transfer and measurement, no integration period is to be given before applying V_{C1}, V_{G1}, and 'Row Select 1' signal.

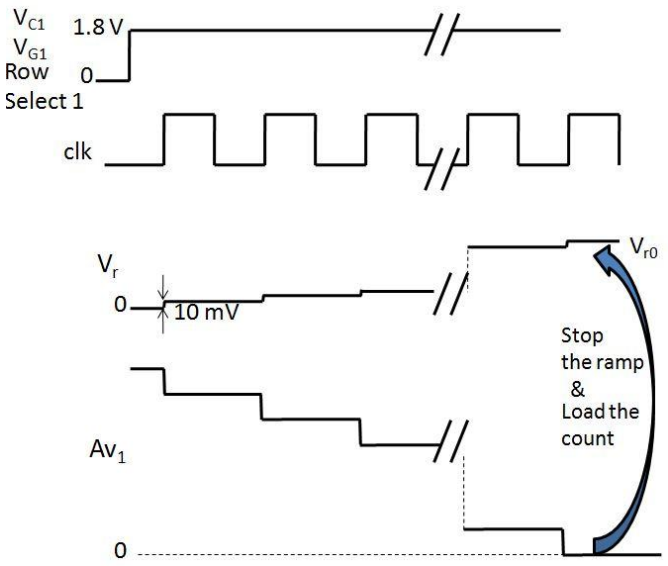

Fig. 5 *Timing diagram showing the sequence in which signals are to be applied and controlled while measuring the intensity of light falling on the pixel, P_{11} in Fig. 3.*

Conclusion: It has been shown that by utilising the logarithmic relation between open circuit voltage and photocurrent, a high dynamic range CMOS image sensor can be realized. The proposed sensor has a high fill factor owing to the presence of a single photodiode and MOSFET per pixel and hence image sensor chips with large pixel density can be realized. Further, it is best suited for high quality video applications demanding large frame rates. This is due to the fact that, no separate integration and charge transfer times are required. Besides, an accelerated analog to digital conversion with logarithmic pixel reduces the conversion period significantly. For example, a 40 clock cycle conversion period is proposed here for a dynamic range of 70 dB whereas the conventional slope analog to digital converters with linear pixel demands ZZZZ clock cycles for the same dynamic range.

K. Akshay, Parvathy R Pillai and B. Bhuvan (National Institute of Technology Calicut, India)
E-mail:

References

1 Fossum, E. R., and Hondongwa, D. B.: 'A review of the pinned photodiode for CCD and CMOS image sensors', *IEEE J. Electron Devices Soc.*, 2014 , **2**, (3), pp. 33-43, doi: 10.1109/JEDS.2014.2306412

2 Fossum, E. R.: 'CMOS image sensors: Electronic camera-on-a-chip', *IEEE transactions on electron devices*, 1997, **44**, (10), pp. 1689-1698, doi: 10.1109/16.628824

3 Ho. J. S. *et al.*: 'A new design for a 1280 x 1024 digital CMOS image sensor with enhanced sensitivity, dynamic range and FPN', *VLSI Technology, Systems, and Applications Int. Symp.*, 1999, pp. 235–238, doi: 10.1109/VTSA.1999.786043

4 Lai, L. W., Lai, C. H., and King, Y. C.: 'A novel logarithmic response CMOS image sensor with high output voltage swing and in-pixel fixed-pattern noise reduction', *IEEE Sensors Journal*, 2004, **4**, (1), pp. 122-126, doi: 10.1109/JSEN.2003.820339

5 Loose, M., Meier, K., and Schemmel, J.: 'A self-calibrating single-chip CMOS camera with logarithmic response', *IEEE Journal of Solid-state circuits*, 2001, **36**, (4), pp. 586-596, doi: 10.1109/4.913736