DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

End Semester Examination – Winter 2018

Course: B. Tech. in Electronics and Telecommunication Engineering **Sem: III**

Subject Name: Digital Logic design **Subject Code: BTEXC305**

Max Marks: 60 **Date:10/12/2018** **Duration: 3 Hr.**

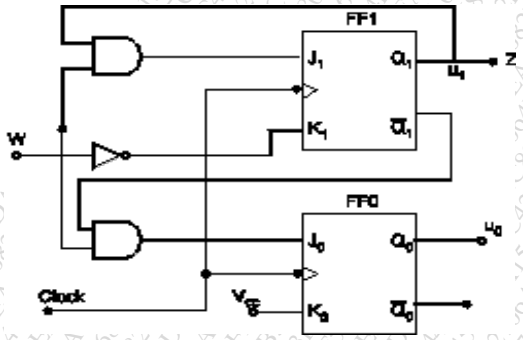
Instructions to the Students:

1. The level question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.

2. Use of non-programmable scientific calculators is allowed.

3. Assume suitable data wherever necessary and mention it clearly.

			(COs)	Marks
Q. 1	A)	Simplify following expression using K-Map $f(A,B,C,D) = \sum m(1,4,7,12,13,14,15) + d(0,5,8)$	(1,2)	06
	B)	Implement following using multiplexer (a) Half-adder (b) Half-subtractor	(1,2)	06
Q. 2	A)	Design 3-bit synchronous up counter using JK flip flop.	(2,3)	06
	B)	Draw and explain Universal shift Register.	(2,3)	06
Q. 3		Draw state diagram for given sequential circuit shown in figure 1.	(2,3)	12



Q.4	A)	Define and explain: i)Fan in and Fan out ii) Noise immunity iii) Propagation Delay	(2)	06
	B)	Explain in brief the operation of CMOS NAND Gate with schematic diagram.	(2)	06
Q5.	A)	Implement given Boolean functions using PLA, PAL and PROM F1 (A,B,C)= $\sum m(0,2,6,7)$ F2(A,B,C)= $\sum m(1,3,4,5,7)$	(2,3)	06
	B)	Write VHDL code for Mux 4:1 using dataflow and behavioural architecture style.	(4)	06
Q6.	A)	Draw combinational circuit for Binary Parallel Adder and Subtractor.	(3)	06
	B)	Draw Asynchronous 4 bit up counter with clock waveform.	(2,3)	06

******************************The End*****************************