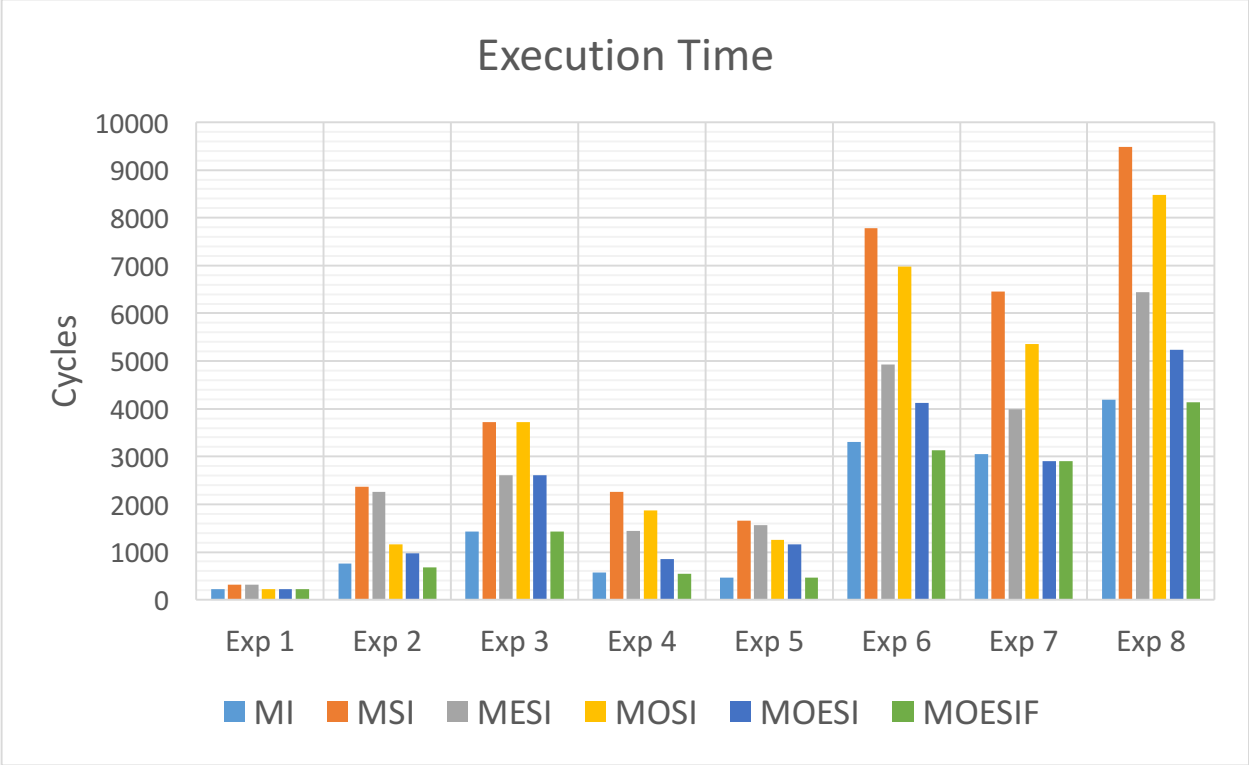
Project 3: Report

Experiment Results

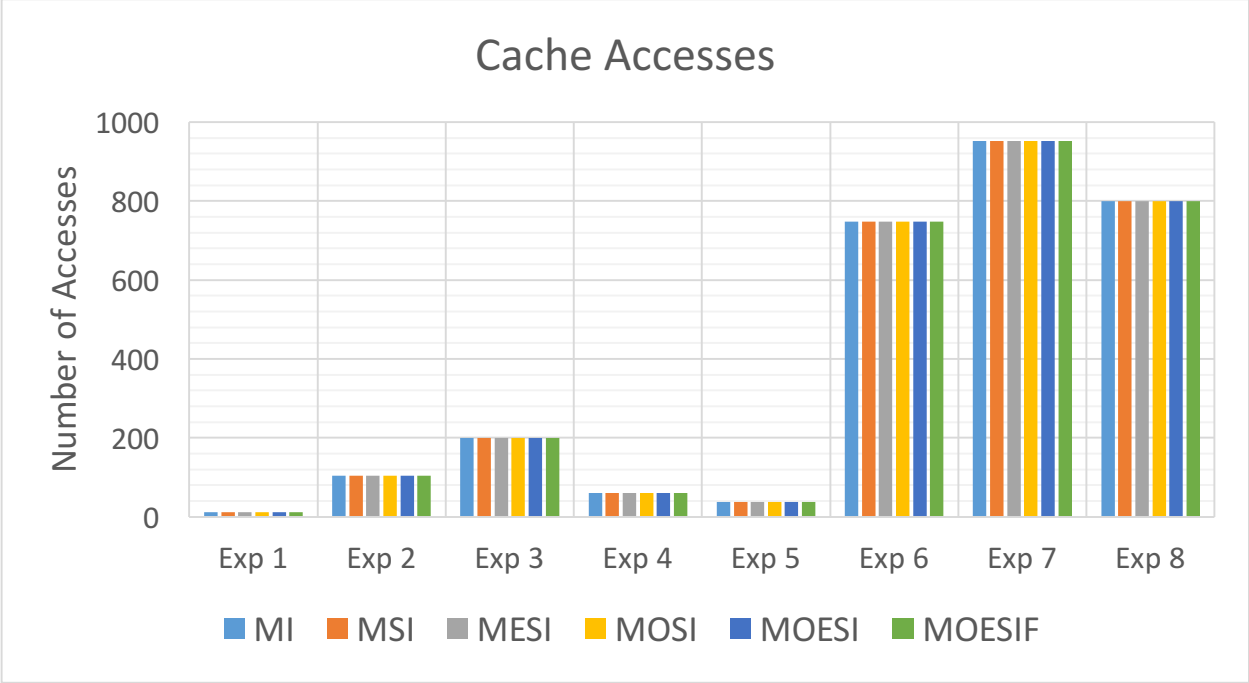
Below are charts that show the results of running all 8 provided experiments using each of the implemented cache coherence protocols.

Parameter Charts

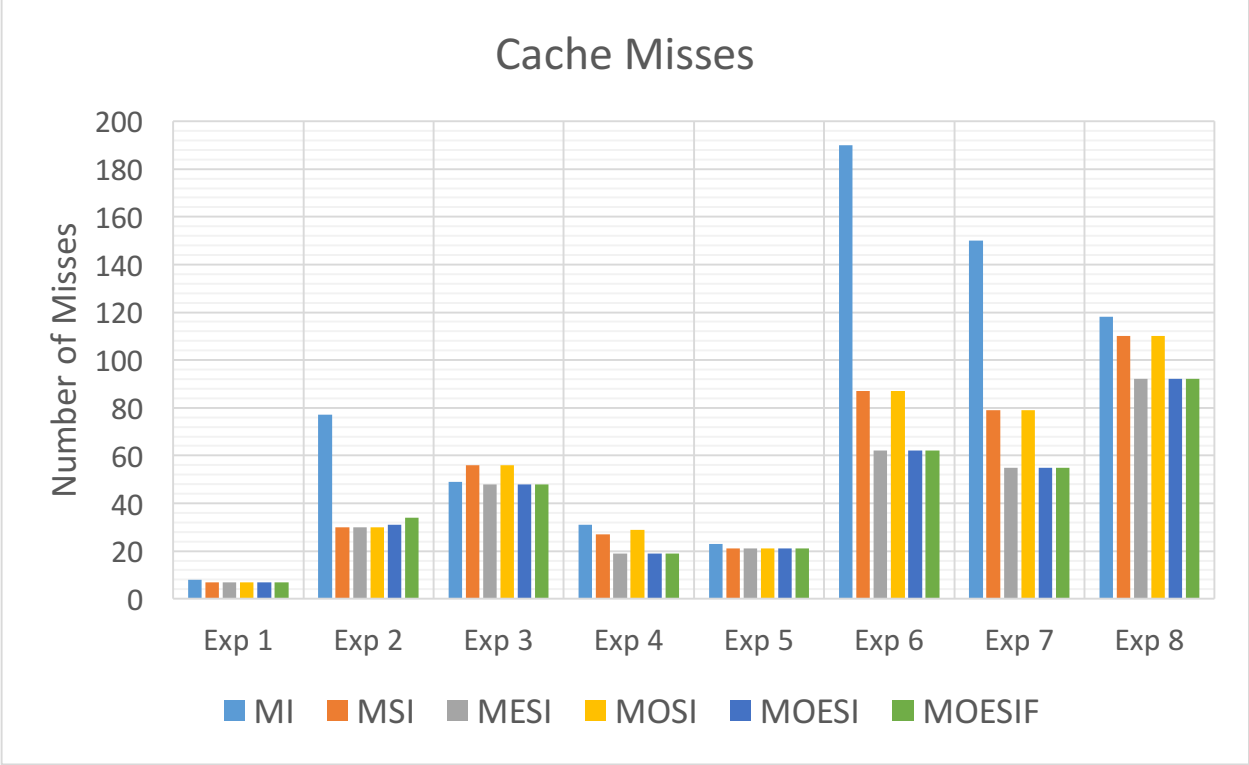
For execution time, we see that MI, MOESI, and MOESIF perform consistently better than the remaining protocols for all of the experiments.



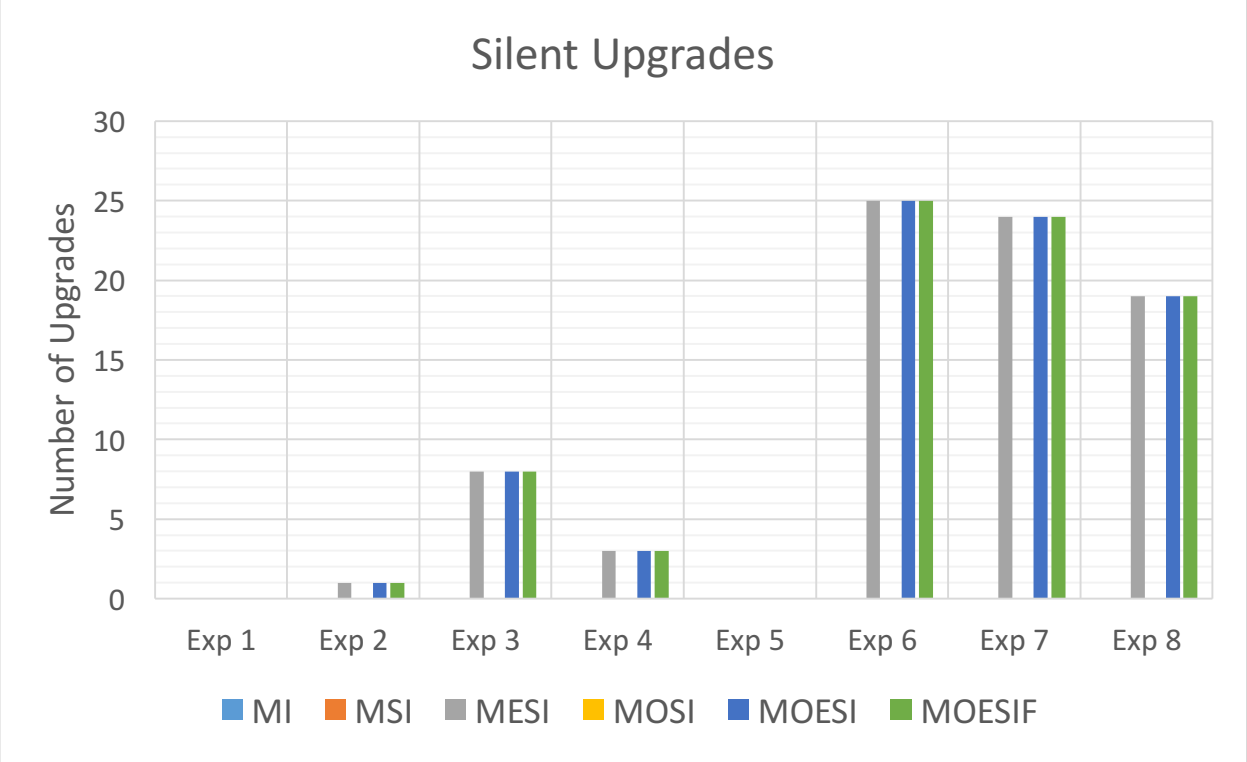
Cache accesses are uniform within each experiment given that the traces are the same.



As for cache misses, MI performs much worse than the rest for experiments 2, 6, and 7. The remaining protocols perform about the same.

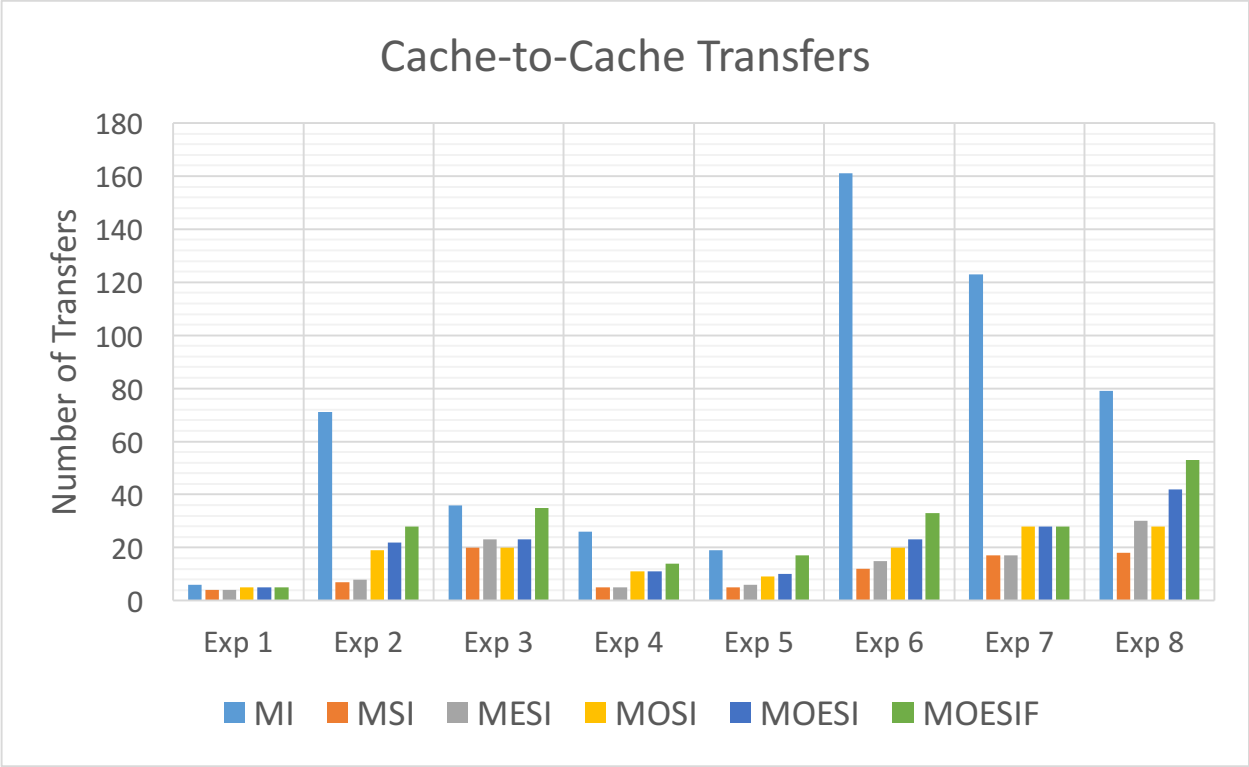


Silent upgrades are only present in protocols with an E state (i.e., MESI, MOESI, and MOESIF), and are not present in experiments 1 and 5.



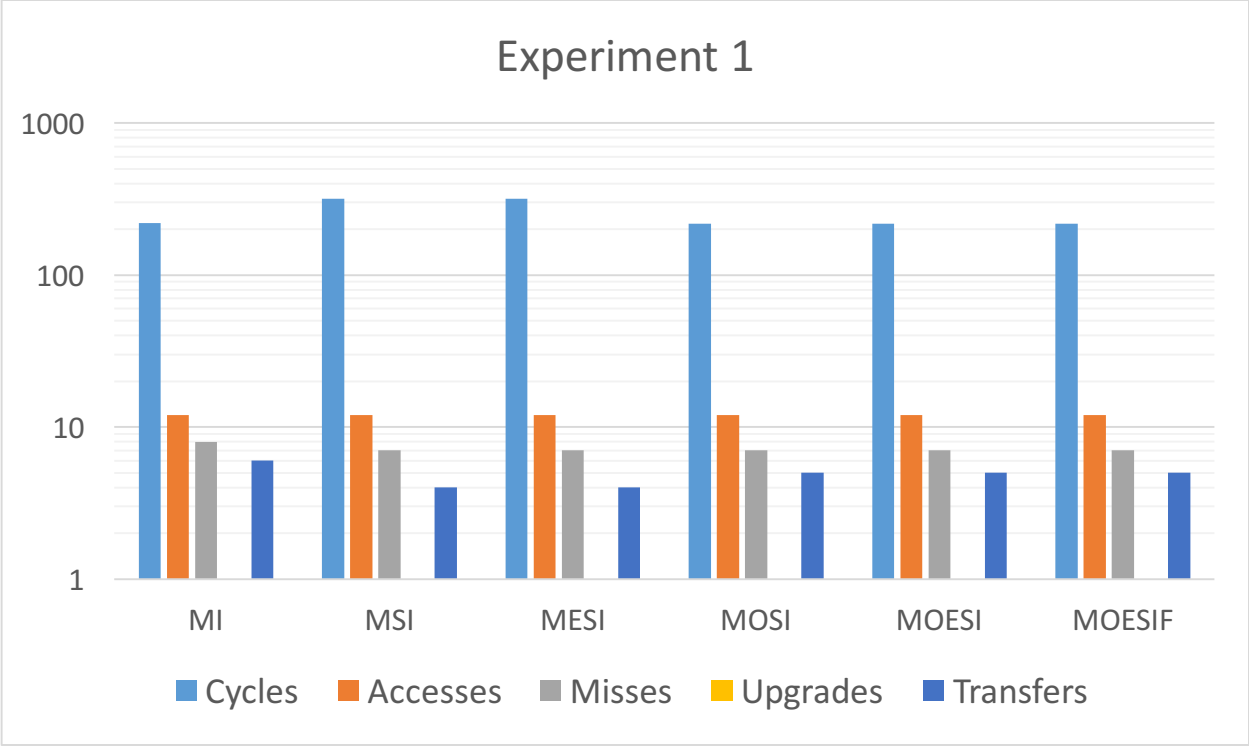
For cache-to-cache transfers, MI performs significantly more such transfers in most of the experiments. The reason is the absence of a S state – in other words, a block is either "dirty" or invalid. Furthermore, each cache will stored a copy of the block locally, so cache-to-cache transfers become the main method to get a block not currently in the local cache.

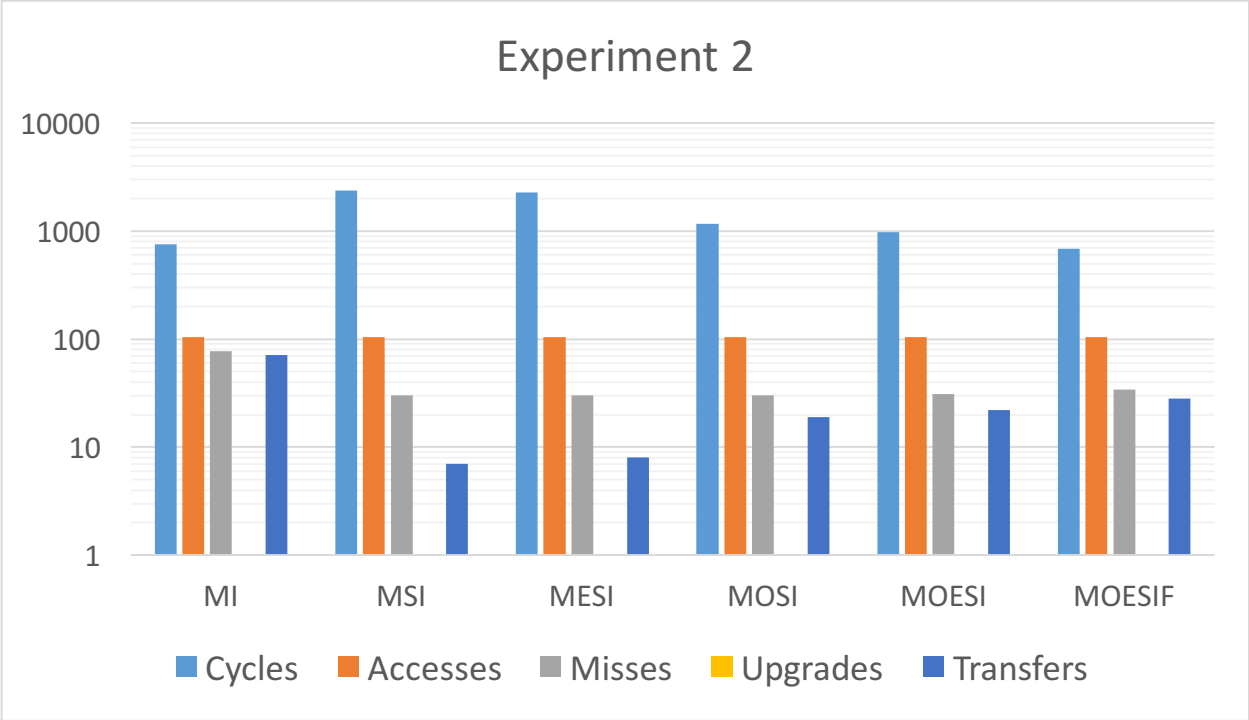
Furthermore, MOESIF seems to perform more transfers than the remaining protocols. One explanation for this is the presence of the F state.

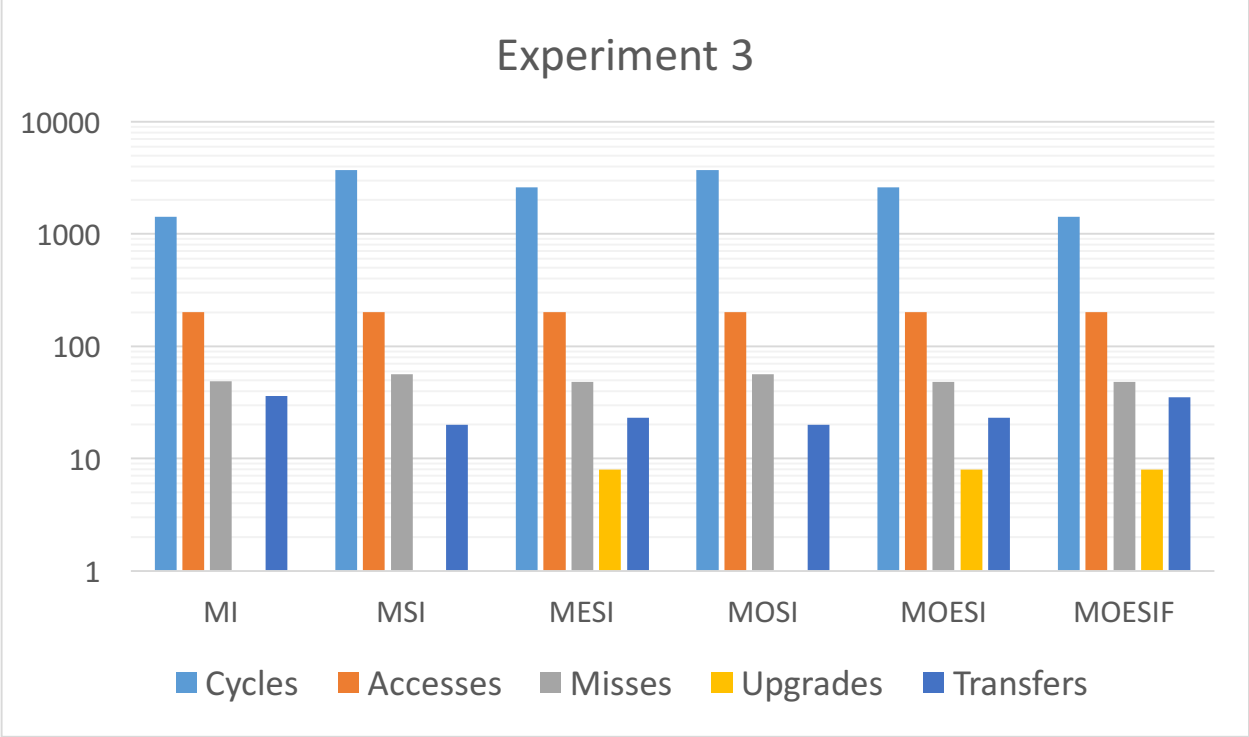


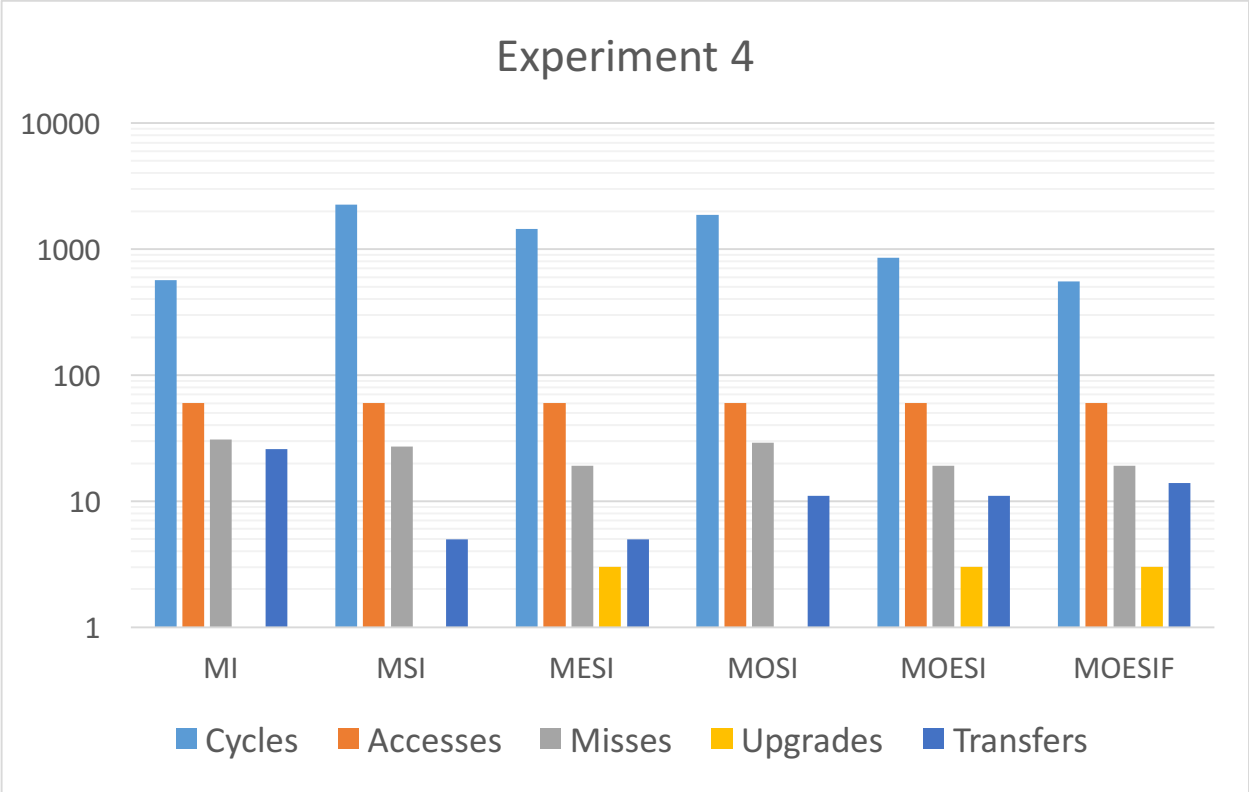
Experiment Charts

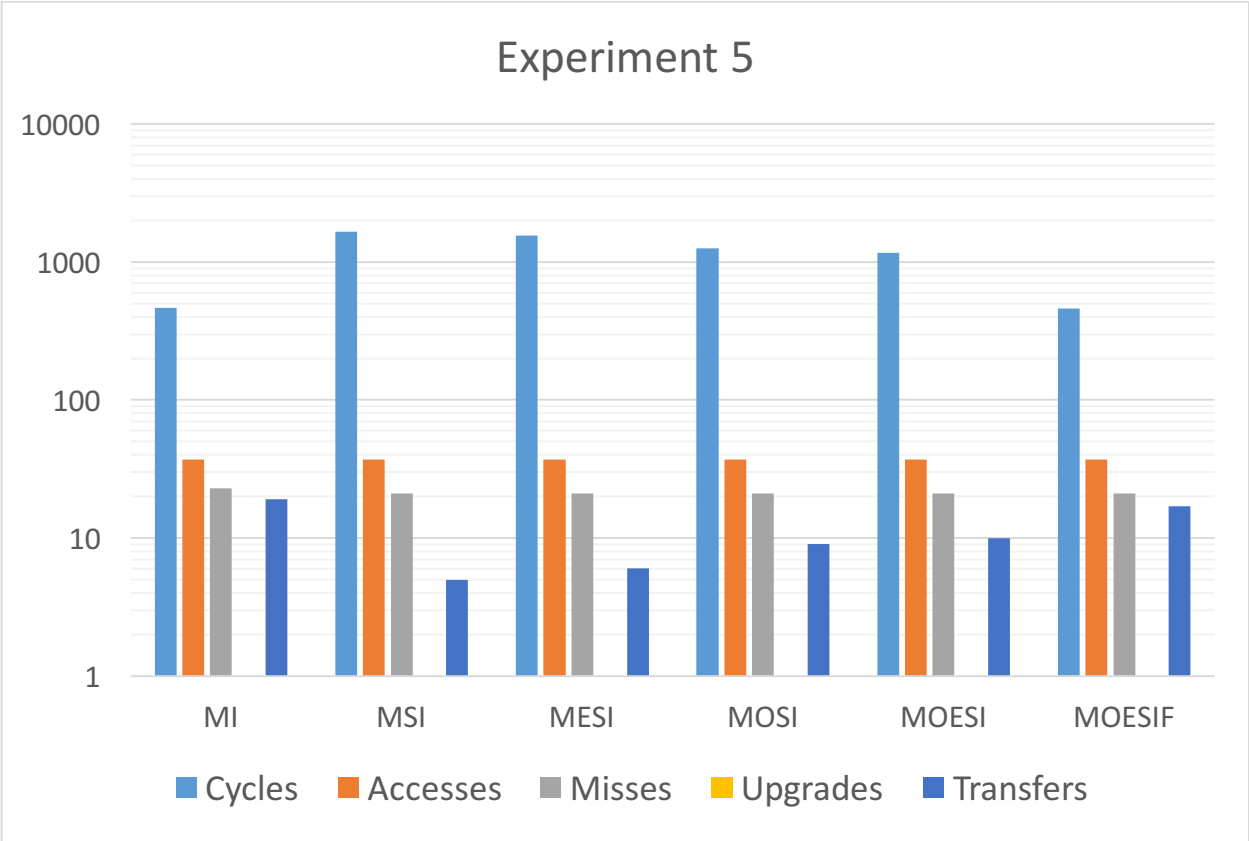
The following charts show protocol performance across each single experiment. Note that the charts are plotted in *logarithmic* scale.

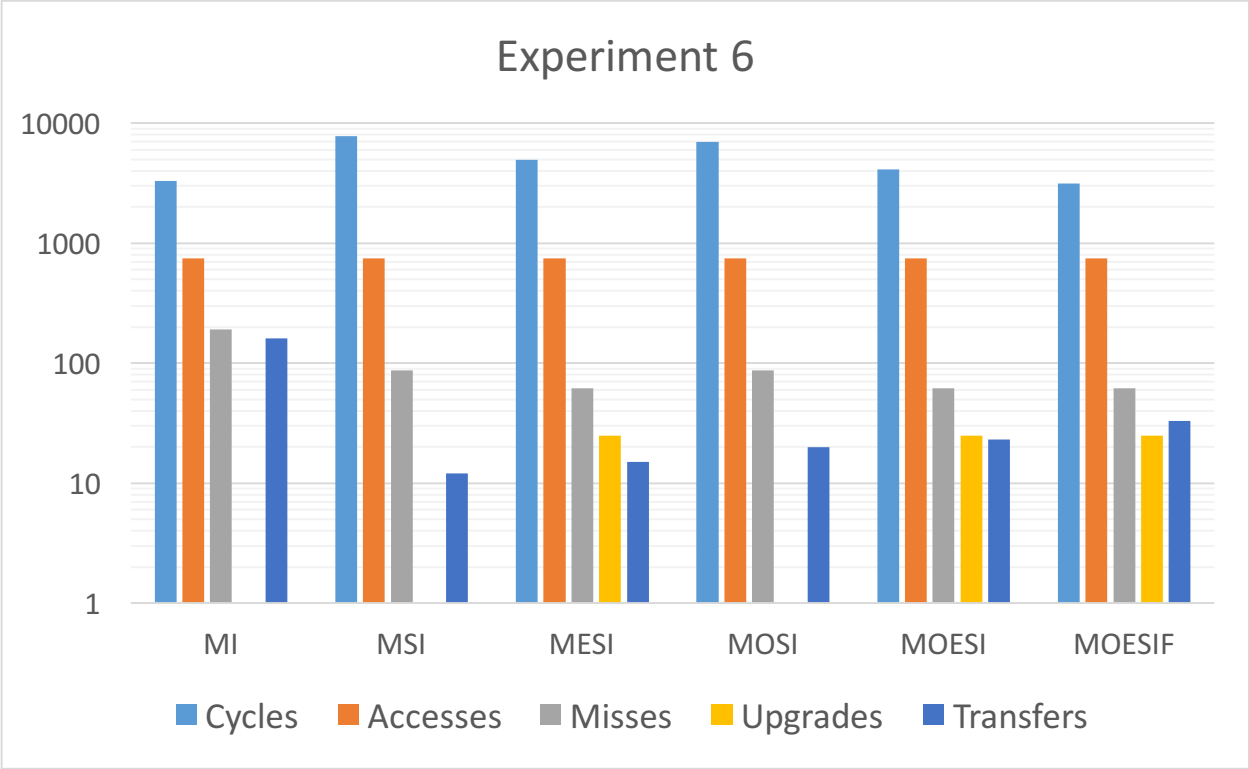


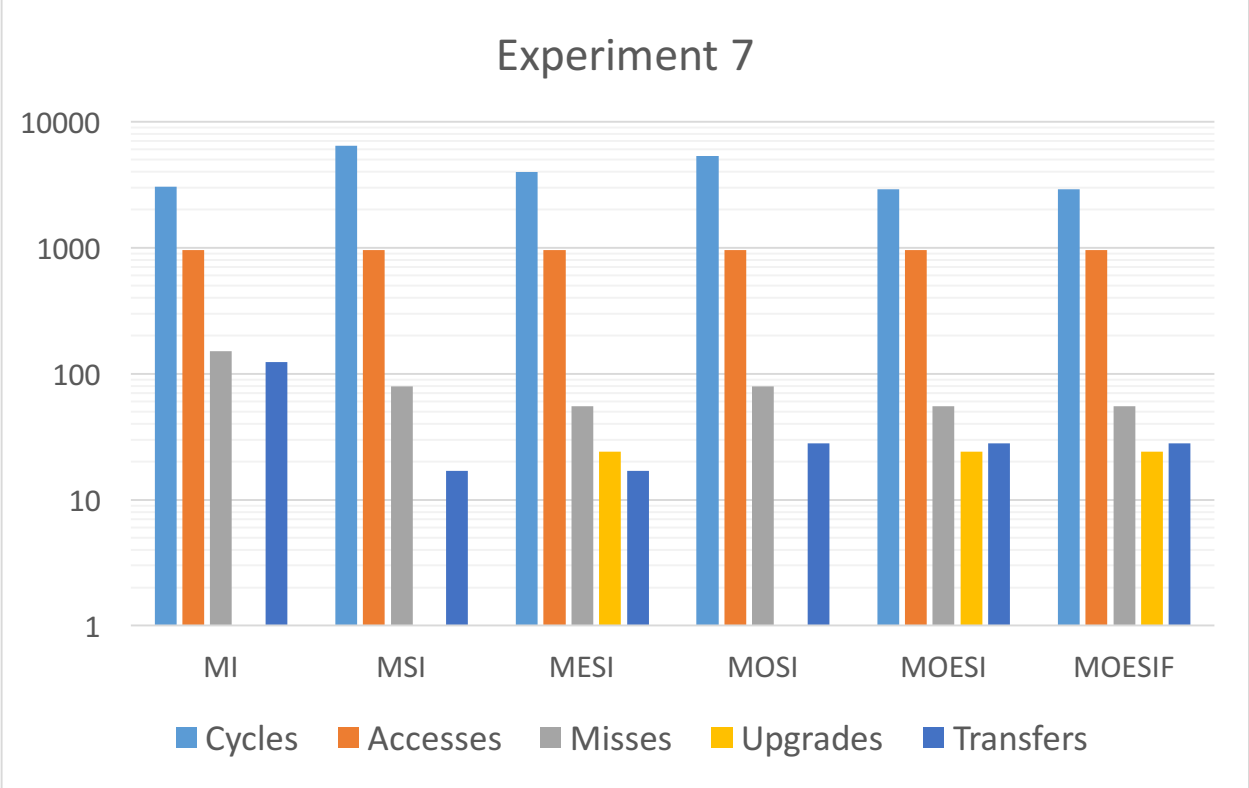

Experiment 2
10000
1000
100
10
1
MI
MSI
MESI
MOSI
MOESI
MOESIF
Cycles
Accesses
Misses
Upgrades
Transfers

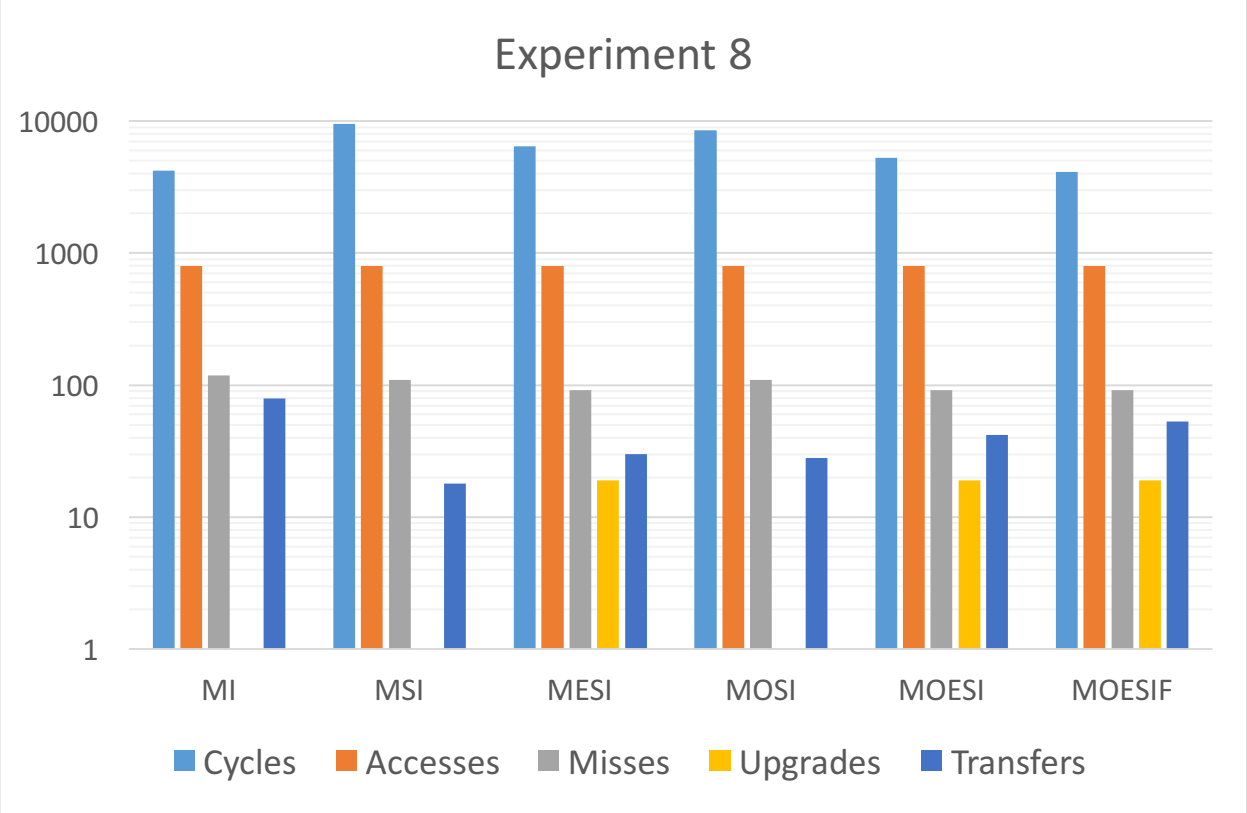

Experiment 3
10000
1000
100
10
1
MI
MSI
MESI
MOSI
MOESI
MOESIF
Cycles
Accesses
Misses
Upgrades
Transfers


Experiment 4
10000
1000
100
10
1
MI
MSI
MESI
MOSI
MOESI
MOESIF
Cycles
Accesses
Misses
Upgrades
Transfers


Experiment 5
10000
1000
100
10
1
MI
MSI
MESI
MOSI
MOESI
MOESIF
Cycles
Accesses
Misses
Upgrades
Transfers


Experiment 6
10000
1000
100
10
1
MI
MSI
MESI
MOSI
MOESI
MOESIF
Cycles
Accesses
Misses
Upgrades
Transfers


Experiment 7
10000
1000
100
10
1
MI
MSI
MESI
MOSI
MOESI
MOESIF
Cycles
Accesses
Misses
Upgrades
Transfers



Discussion

First, MI clearly performs the best among the protocols, while also having the highest number of misses and cache-to-cache transfers across almost all experiments. There are a number of reasons why this is the case. Firstly, the relative access time of bus-to-bus transfers and L2/memory access seems to favor the excessive bus-to-bus transfers. Secondly, the unlimited cache size means evictions will never take place, so MI works well. In general, in a real implementation, MI would cause excessive bus traffic and will face issues with capacity misses. Therefore, in a realistic scenario, MI would perform poorly relative to the other protocols.

We can see that, in the case of MI, the number of cache-to-cache transfers correlates directly with the number of cache misses for experiments 2, 6, and 7. For the remaining protocols, we notice that MESI, MOESI, and MOESIF have approximately the same number of cache misses across all experiments; the same can be said about MSI and MOSI. As for cache misses, the absolute number of misses directly correlates with the absolute number of cache accesses; all of these are compulsory misses due to the infinite size.

Silent upgrades are only present in protocols with an E state. However, experiments 1 and 5 both lack silent upgrades. In the case of trace 5, only one processor has cache blocks in the E state and

no other processor accesses them, so no upgrade takes place. As for trace 1, no block moves into the E state because all processors access the same blocks (i.e., they all go to S)!