1. Description

1.1. Project

Project Name	QSPITest
Board Name	custom
Generated with:	STM32CubeMX 5.5.0
Date	01/24/2020

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F412
MCU name	STM32F412ZGTx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

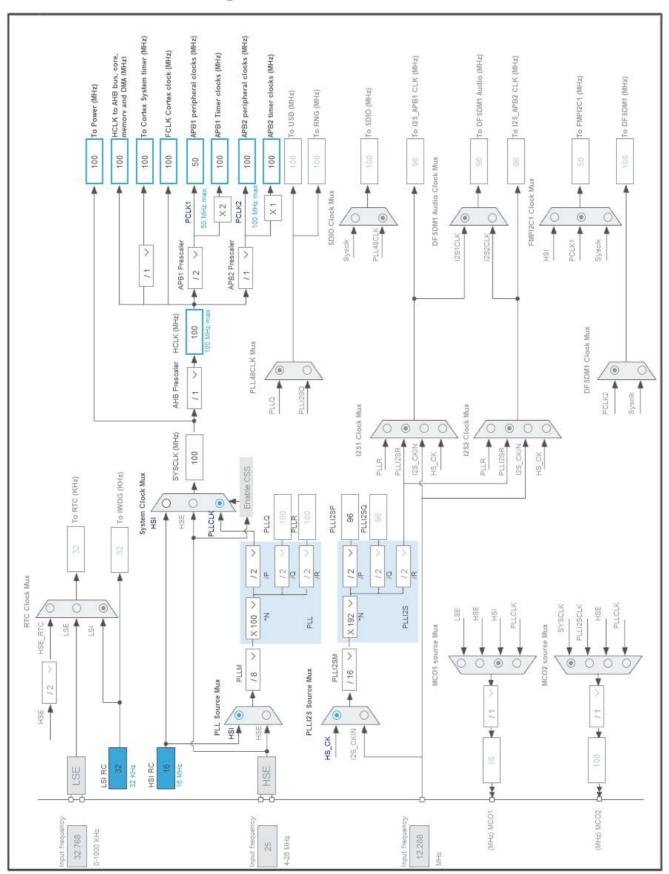


3. Pins Configuration

Pin Number LQFP144	Pin Name (function after	Pin Type	Alternate Function(s)	Label
	reset)			
1	PE2	I/O	QUADSPI_BK1_IO2	
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
48	PB2	I/O	QUADSPI_CLK	
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
77	PD8	I/O	USART3_TX	
78	PD9	I/O	USART3_RX	
80	PD11	I/O	QUADSPI_BK1_IO0	
81	PD12	I/O	QUADSPI_BK1_IO1	
82	PD13	I/O	QUADSPI_BK1_IO3	
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD_USB	Power		
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power	310_01M0 0WDIO	
107	VSS VSS	Power		
108	VDD	Power	eve ITOX OWOLK	
109	PA14	I/O	SYS_JTCK-SWCLK	
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
136	PB6	I/O	QUADSPI_BK1_NCS	
138	BOOT0	Boot		
143	PDR_ON	Power		
144	VDD	Power		

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value	
Project Name	QSPITest	
Project Folder	D:\ST\TouchGFXDemo\QSPITest	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F4 V1.24.2	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F412
мси	STM32F412ZGTx
Datasheet	028087_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	null

7. IPs and Middleware Configuration 7.1. GPIO

7.2. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.2.1. Parameter Settings:

General Parameters:

Clock Prescaler 0 *
Fifo Threshold 4 *

Sample Shifting Half Cycle *

Flash Size 23 *

Chip Select High Time 6 Cycles *

 Clock Mode
 Low

 Flash ID
 Flash ID 1

 Dual Flash
 Disabled

7.3. RCC

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. USART3

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
QUADSPI	PE2	QUADSPI_BK1_I O2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD11	QUADSPI_BK1_I O0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD12	QUADSPI_BK1_I O1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD13	QUADSPI_BK1_I O3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB6	QUADSPI_BK1_ NCS	Alternate Function Push Pull	Pull-up *	Very High	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
QUADSPI global interrupt	true	0		
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
USART3 global interrupt	unused			
FPU global interrupt	unused			

^{*} User modified value

9. Software Pack Report	9.	Software	Pack	Report
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