

指令	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OpCode: AND/EOR/SUB/RSB/ ADD/ADC/SBC/RSC/ TST/TEQ/CMP/CMN/ ORR/MOV/BIC/MVN	Condition field				0	0	1	OpCode				S	Rn				Rd				Operand 2															
MUL/MLA					0	0	0	0	0	0	0	A	S	Rd				Rn				Rs				1	0	1	1	Rm						
UMULL/UMLAL/ SMULL/SMLAL					0	0	0	0	1	U	A	S	RdHi				RdLo				Rs				1	0	0	1	Rm							
MRS					0	0	0	1	0	Ps	0	0	1	1	1	1	Rd				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSR					0	0	0	1	0	Pd	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Rm					
MSR(only flag)					0	0	1	1	0	Pd	1	0	1	0	0	0	1	1	1	1	Source operand															
B/BL					1	0	1	L	Offset																											
BX					0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	Rn				
SWI					1	1	1	1	Comment field (ignored by Processor)																											
LDRB/STRB/ LDRW/STRW					0	1	I	P	U	B	W	L	Rn				Rd				Offset															
LDRH/STRH/ LDRSB/STRSH					0	0	0	P	U	0	W	L	Rn				Rd				0	0	0	0	1	S	H	1	Rm							
					0	0	0	P	U	1	W	L	Rn				Rd				Offset				1	S	H	1	Offset							
LDM/STM					1	0	0	P	U	S	W	L	Rn				Register list																			
SWP					0	0	0	1	0	B	0	0	Rn				Rd				0	0	0	0	1	0	0	1	Rm							
CDP	1	1	1	0	CP Opc				CRn				CRd				CP#				CP				0	CRm										
MRC/MCR	1	1	1	0	CP Opc				L	CRn				Rd				CP#				CP				1	CRm									
LDC/STC	1	1	0	P	U	N	W	L	Rn				CRd				CP#				Offset															
Undefined	0	1	1	xxxxxxxxxxxxxxxxxxxxxxx																											1	xxx				
指令	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				

ARMV4T	数据处理指令	算术运算指令	ADD、ADC、SUB、SBC、RSB、RSC、MUL、MLA、UMULL、UMLAL、SMULL、SMLAL
		逻辑运算指令	AND、ORR、EOR、BIC
		比较指令	CMP、CMN、TEQ、TST
		数据传送指令	LDR、LDM
	数据存取指令	数据加载指令	LDR、LDM
		数据存储指令	STR、STM
		数据交换指令	SWP
	控制流指令	分支跳转指令	B、BL、BX
		异常产生指令 (软件中断指令)	SWI
	协处理器指令	CDP、MCR、MRC、LDC、STC	