指令	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OpCode: AND/EOR/SUB/RSB/ ADD/ADC/SBC/RSC/ TST/TEQ/CMP/CMN/ ORR/MOV/BIC/MVN	Condition field				0	0	1	OpCode				S	Rn				Rd				Operand 2											
MUL/MLA					0	0	0	0	0	0	A	S	Rd				Rn				Rs				1	0	1	1	Rm			
UMULL/UMLAL/ SMULL/SMLAL					0	0	0	0	1	U	A	S	RdHi				RdLo				Rs				1	0	0	1	Rm			
MRS					0	0	0	1	0	Ps	0	0	1	1	1	1	Rd				0	0	0	0	0	0	0	0	0	0	0	0
MSR					0	0	0	1	0	Pd	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	Rm			
MSR(only flag)					0	0	I	1	0	Pd	1	0	1	0	0	0	1	1	1	1	Source operand											
B/BL					1	0	1	L	Offset																							
BX					0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	Rn			
SWI					1	1	1	1	Comment field (ignored by Processor)																							
LDRB/STRB/ LDRW/STRW					0	1	I	P	U	B	W	L	Rn				Rd				Offset											
LDRH/STRH/					0	0	0	P	U	0	W	L	Rn				Rd				0	0	0	0	1	S	H	1	Rm			
LDRSB/STRSH					0	0	0	P	U	1	W	L	Rn				Rd				Offset				1	S	H	1	Offset			
LDM/STM					1	0	0	P	U	S	W	L	Rn				Register list															
SWP					0	0	0	1	0	B	0	0	Rn				Rd				0	0	0	0	1	0	0	1	Rm			
CDP					1	1	1	0	CP Opc				CRn				CRd				CP#				CP			0	CRm			
MRC/MCR					1	1	1	0	CP Opc			L	CRn				Rd				CP#				CP			1	CRm			
LDC/STC					1	1	0	P	U	N	W	L	Rn				CRd				CP#				Offset							
Undefined					0	1	1	xxxxxxxxxxxxxxxxxxxx																					1	xxx			
指令	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0