CS223 : Assignment 1, Date of Demonstration 12th Jan 2018, Lab Timing (2PM-5PM), 10% (5%+ 5%) weight

Part I (Breadboard and IC part)

Implement and Demonstrate 3 inputs and 2 output **Binary Full Adder** using Breadboard, ICs and Hookup Wires.

Part II (VHDL and FPGA)

Implement 3 inputs and 2 output **Binary Full Adder** using HDL (either VHDL or Verilog, preferred VHDL), synthesize and simulate your design entry. After that Download bit file of your design to FPGA board and demonstrate the working of your design on FPGA.

Evaluation Procedure

All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please show your ID card at the time of demonstration (as it is difficult to remember faces of all the 90 students of your batch**).**

Grading will be based on (a) Correctness, (b) Quality of design, (c) Wire optimization, (d) Optimum number of chip used,(e) Cleanliness in design (Wire and Chips should be organized to look good), (f) Use of proper Comment/Naming/Labeling of the wires and (g) Questionnaire and explanation.

For HDL codes the quality will be based on FPGA minimum resource utilization (Synthesis Report: optimized number of LUTs, register, Minimum Clock), coding style (Use of proper Comment/Naming/Labeling of the wires), performance, comments, and questionnaire and explanation.

Helps

***List of IC available in our LAB**: http://jatinga.iitg.ernet.in/~asahu/cs223/ICs-HWLAB-CS223.pdf*
***Installation Procedure for Xilinx ISE/Vivado**: http://jatinga.iitg.ernet.in/~asahu/cs223/ISELicence.txt*
***Many links are given to VHDL resource at** http://jatinga.iitg.ernet.in/~asahu/cs223/*

You can take help from TAs. All the TAs and Instructor of CS223 will be available in Lab timing. You can ask TAs or Raktajit Pathak (Room CSE H101) or Bhriguraj Borah (Room CSE Server Room) about licensing and installation of Xillinx ISE/Vivado software.

Breadboard and required ICs may be issued from Hemanta Nath (Hardware Lab). You are not allowed to take Breadboard out of the Hardware Lab. Also required FPGA Board can be issued from Hemanta Nath (Hardware Lab). We will issue up to three FPGA Boards (one BASYS, one ZYBO and one ATLYS) for each group for the whole semester. You need to keep the board with you for the whole semester and you are allowed to take issued FPGA board to your Hostel. Based on your requirement, please issue the board from Lab in charge.

We have tested working of Xilinx ISE/Vivado on Window 7, Window 10 and Ubuntu 14.04 PC.