

# **CS223: Hardware Lab**

## **Digital Circuit Design using (a) Breadboard and ICs and (b) FPGA**

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# Outline

- Course Administrative
  - Assignments, Grading, Timing, Rules
- ASIC / FPGA Design process
- What is VHDL : Requirement of VHDL
- VHDL
  - basic language concepts
  - basic design methodology
  - examples

## **CS223: Administration**

- Course timing : 2PM-5PM, FRIDAY
- Venue : Hardware Lab
- Class Attendance is NOT mandatory
- There will be LAB assignments
  - Using breadboard and ICs
  - Using HDL and FPGA board
    - Need coding, simulation, synthesis, demonstration on FPGA board

# CS223: Administration

Sl	W	Deadline	Part I	Part II
1	(5+5)%	12 Jan	BB+ICs	HDL+FPGA
2	(5+5)%	25 Jan	BB+ICs	HDL+FPGA
3	(6+6)%	09 Feb	BB+ICs	HDL+FPGA
4	(7+7)%	23 Feb	BB+ICs	HDL+FPGA
5	10%	16 Mar	HDL+FPGA	
6	12%	06 Apr	HDL+FPGA	
7	12%	20 Apr	HDL+FPGA	
8	20%	Before ES	Written test/Viva	

# Digital Design Using Breadboard and IC

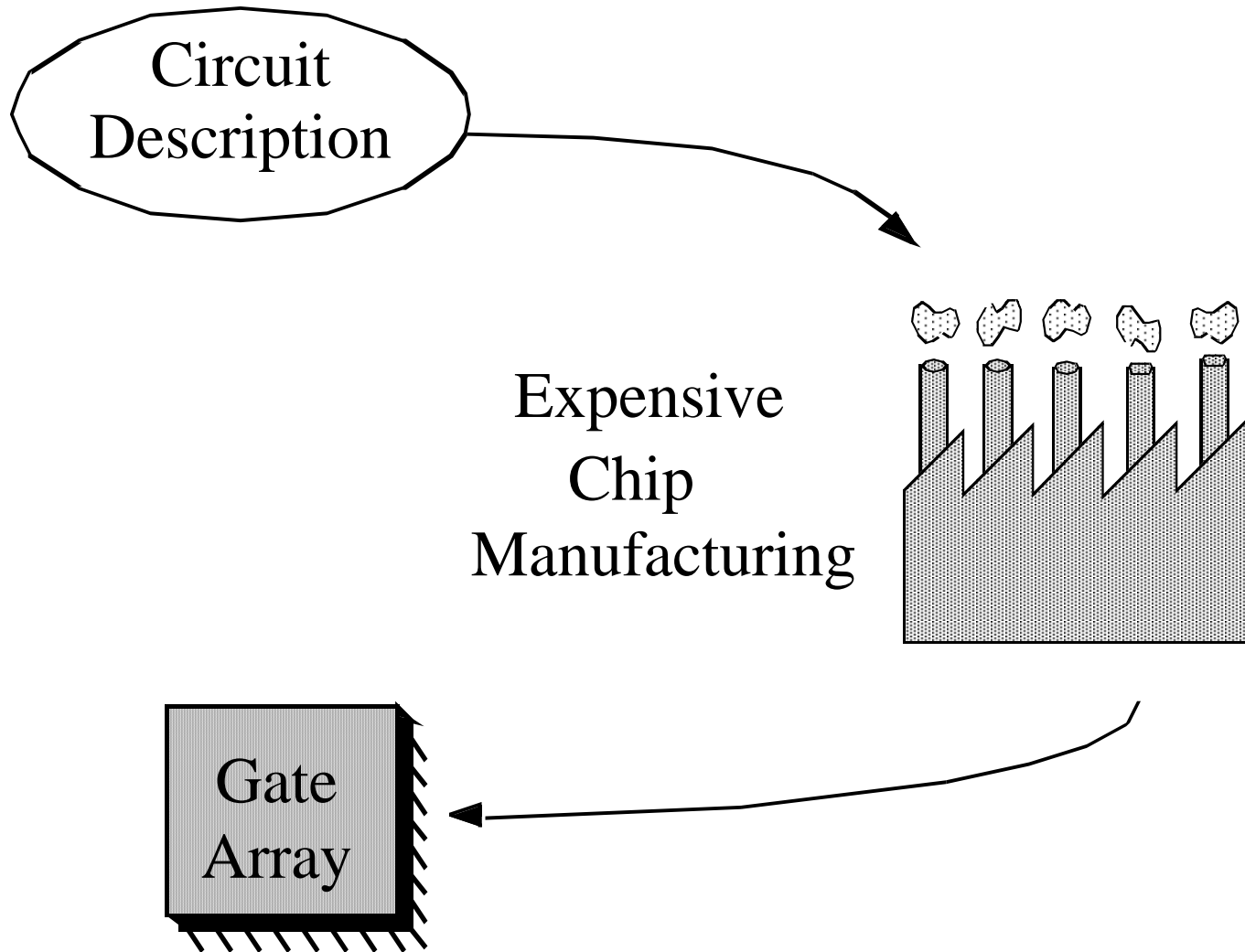
- Breadboard
  - You can put IC components to design circuit
  - Inbuilt power supply, LEDs, Input switches
- ICs
  - Gates, FF, Counter, Mux, Register, ALU, Adder
  - Memory, Buffers, ShiftReg, 7-Seg Display
- Hookup Wires
- Design will be limited to available components and size of the breadboard == > Not suitable for bigger design == > FPGA == > Soft Design

# Digital Design Using Breadboard and IC

- Main work
  - Need to read SPEC of the required Ics for your design
  - SPEC from internet
  - Use the ICs based on the SPEC
- Careful
  - **Using ICs wrongly may BLOW UP == > Permanent loss**
  - **Using 7-SEG LED without resistor: blow up == > Permanent loss**
- Design will be limited to available components and size of the breadboard == > Not suitable for bigger design == > FPGA == > Soft Design

# FPGAs

- FPGA: Field-Programmable Gate Array

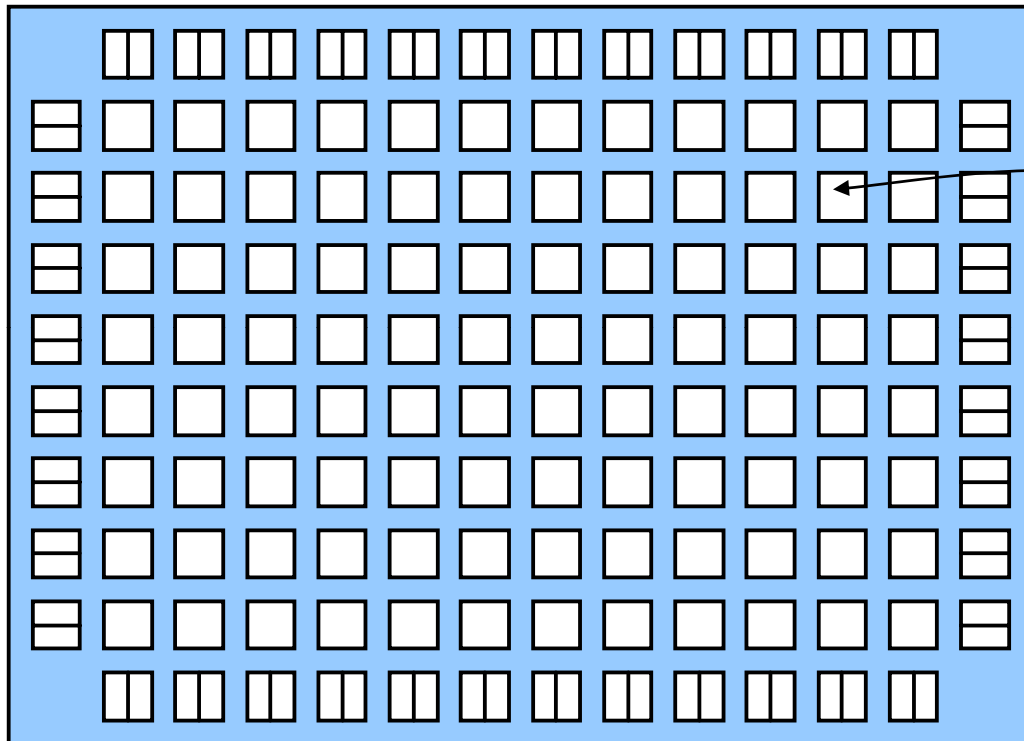


# **FPGA - Field Programmable Gate Array**

- **Programmable logic blocks**
  - Implement combinatorial and sequential logic.
  - Based on LUT and DFF.
- **Programmable I/O blocks**
  - Configurable I/Os for external connections
  - Supports various voltages and tri-states.
- **Programmable interconnect**
  - Wires to connect inputs , outputs and logic blocks.
  - Clocks
  - short distance local connections
  - long distance connections across chip



# What's Inside an FPGA?



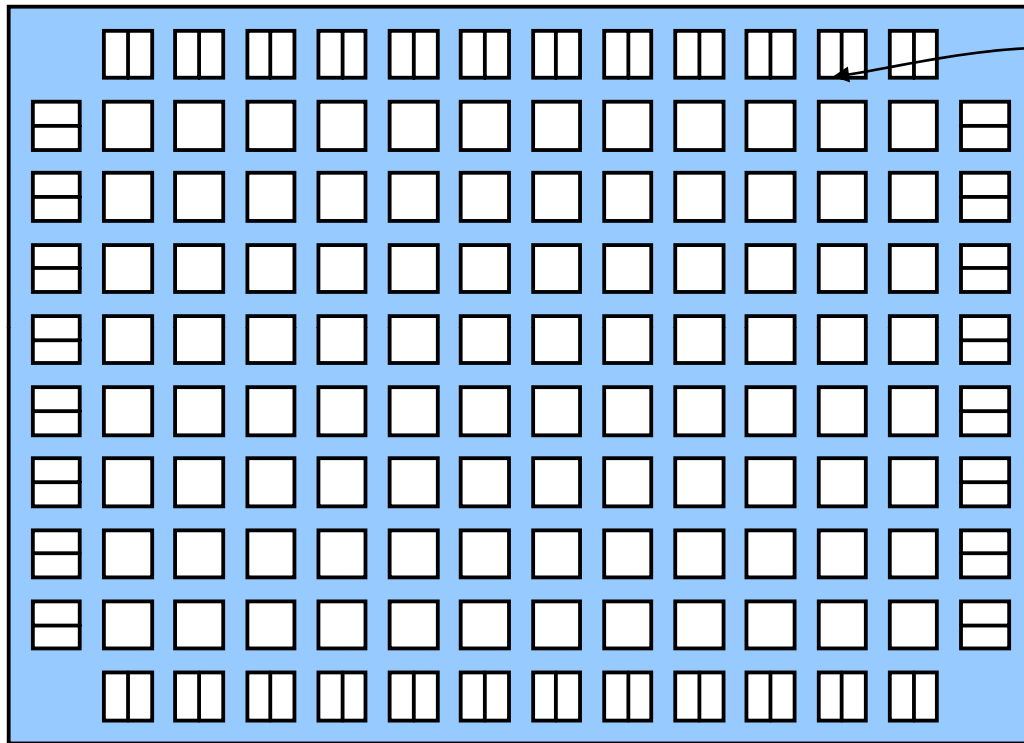
Logic Blocks

- used to implement logic
- lookup tables and flip-flops

Altera: LABs

Xilinx: CLBs

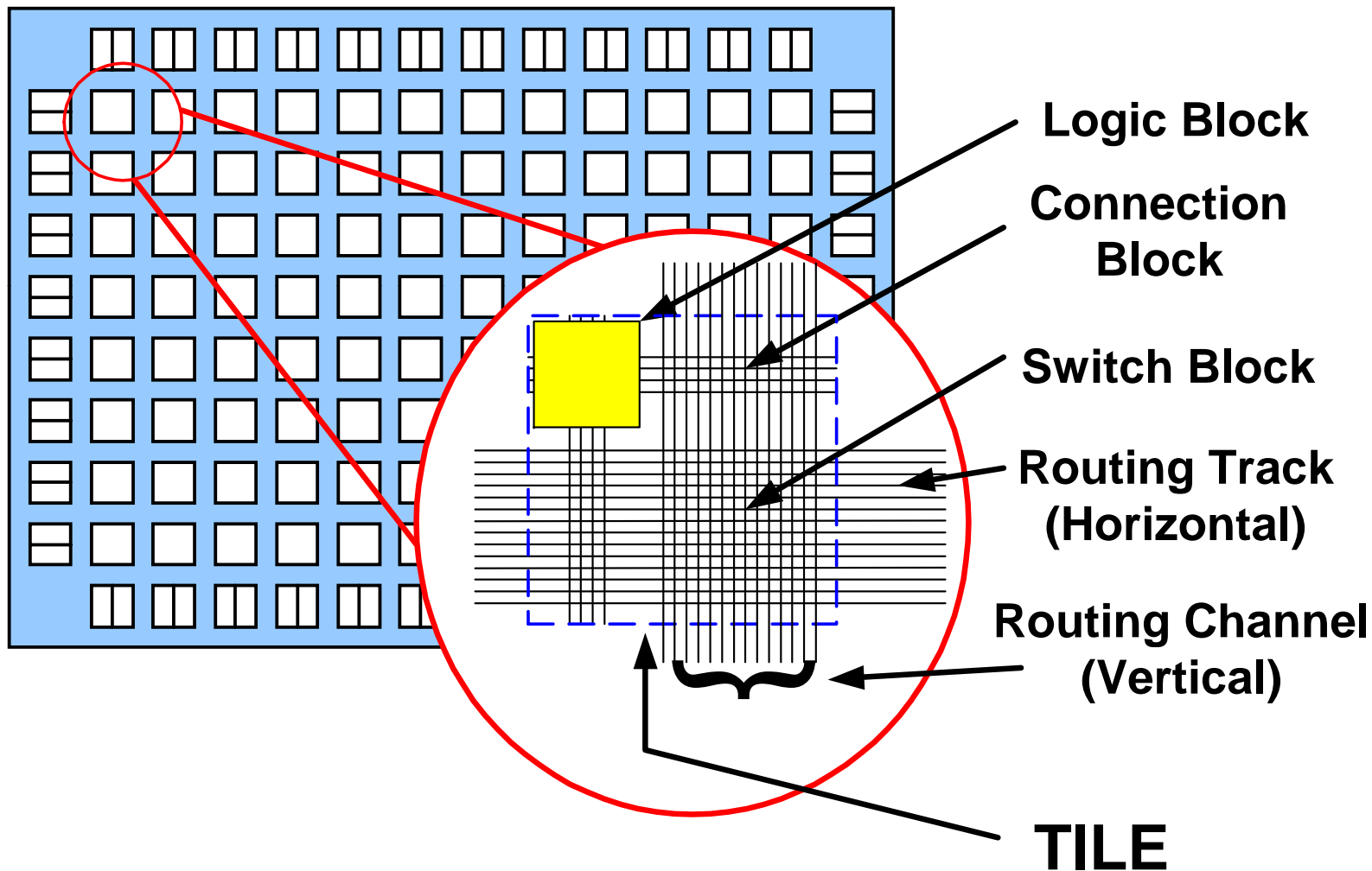
# What's Inside an FPGA?



I/O Blocks

- interface off-chip
- can usually support many I/O Standards

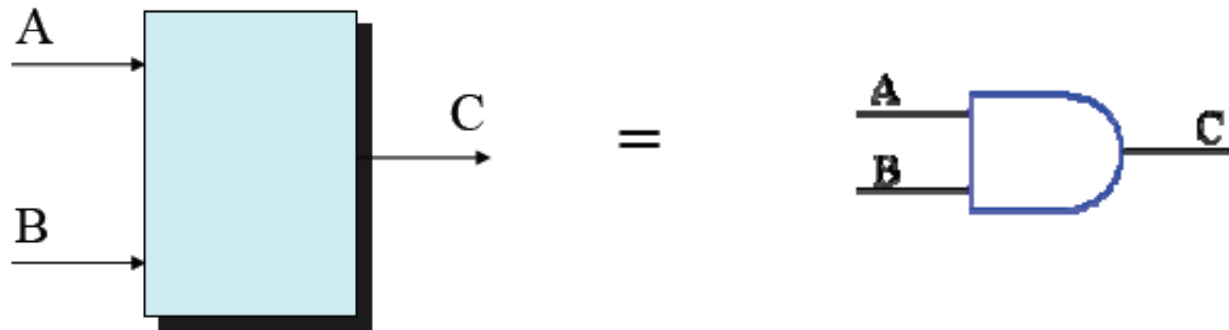
# What's Inside an FPGA?



# FPGA Structures

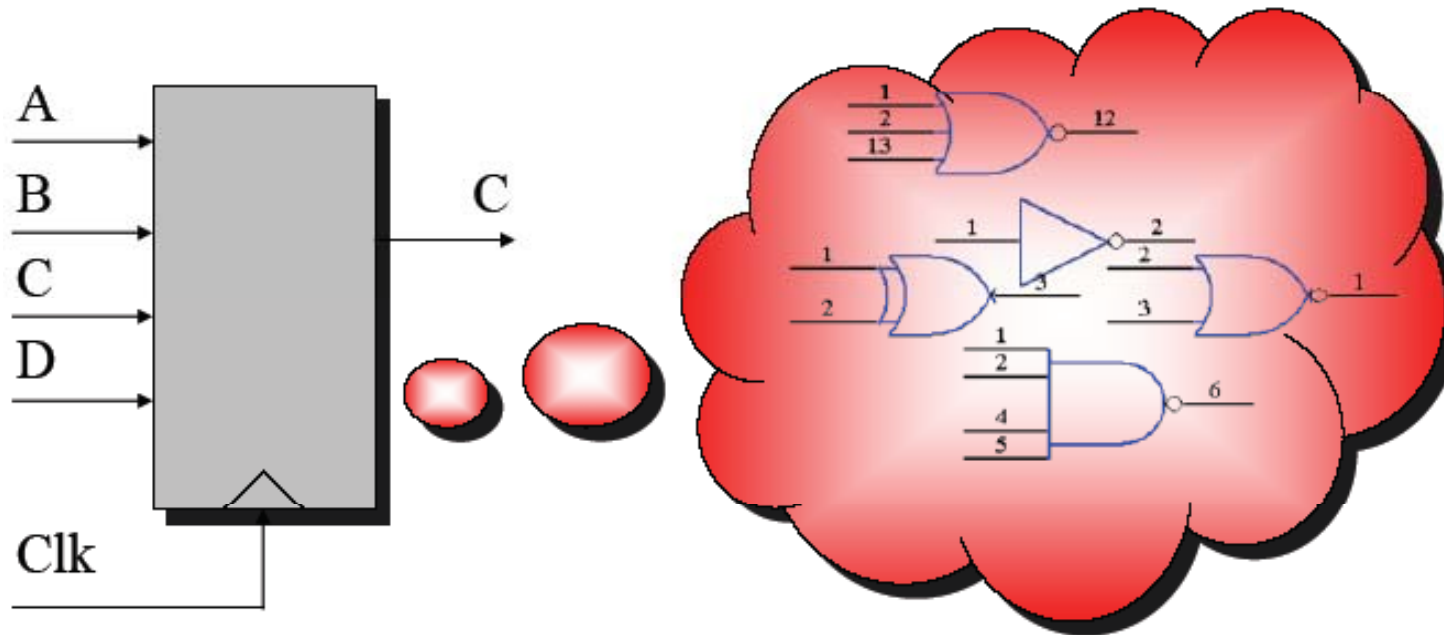
- Basic Lookup Table (LUT)

<b>A</b>	<b>B</b>	<b>C</b>
0	0	0
0	1	0
1	0	0
1	1	1



# FPGA Structures

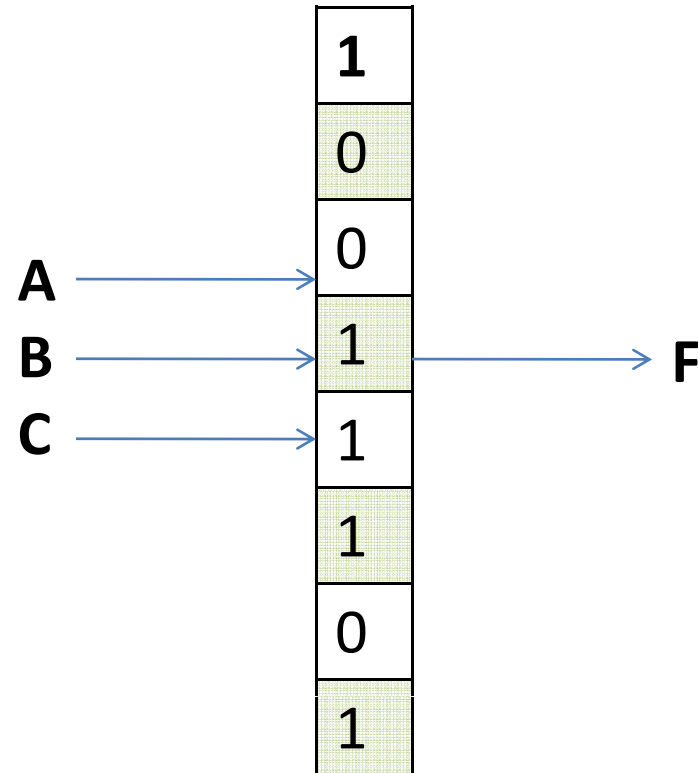
- Synchronous Look-UP



# CLB : Conf Logic Block

- Implement any Boolean Function using LUTs
  - Suppose any 3 input one output function can be implemented using a 8 Loc x1 bit RAM (memory)

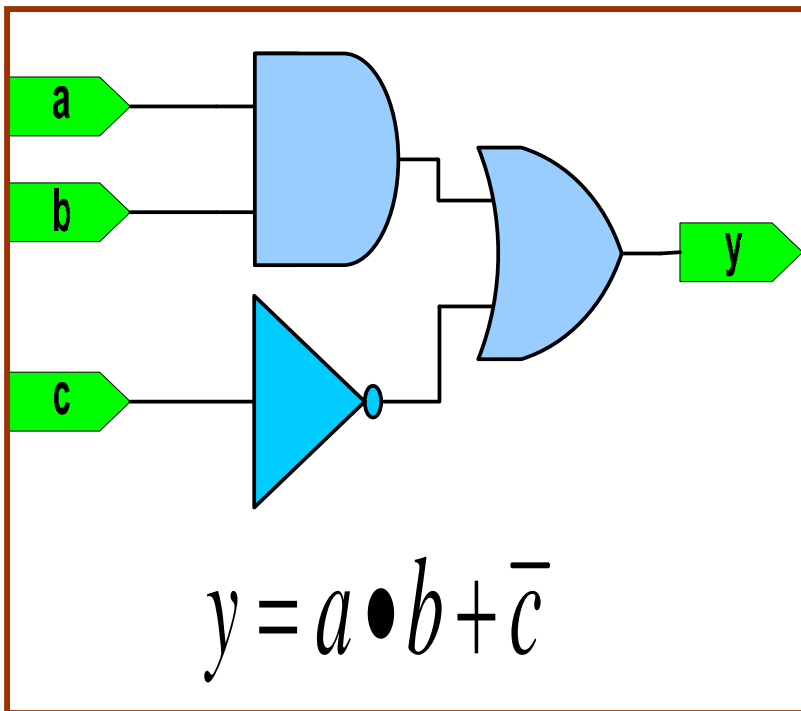
A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



# Configuring LUT

- LUT is a RAM with data width of 1bit.
- The contents are programmed at power up

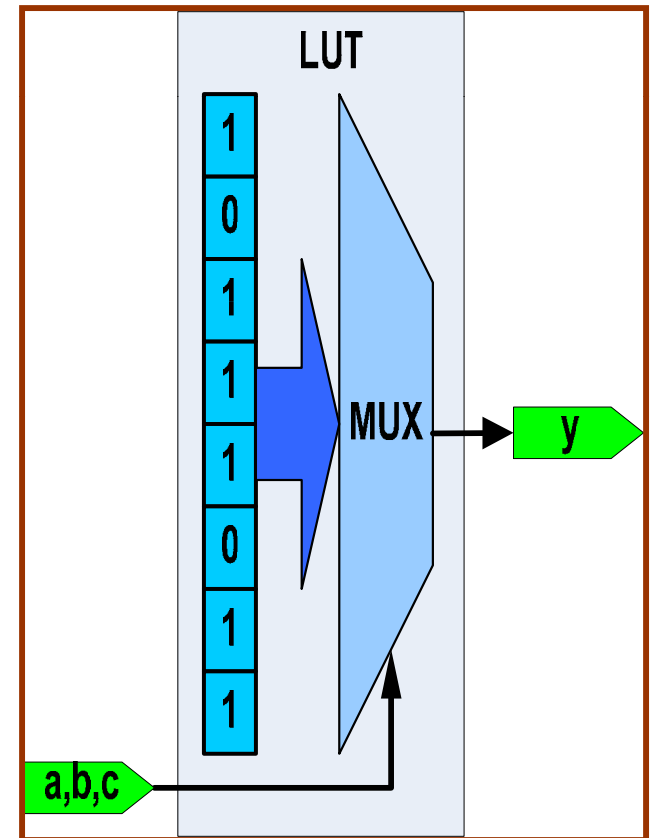
Required Function



Truth Table

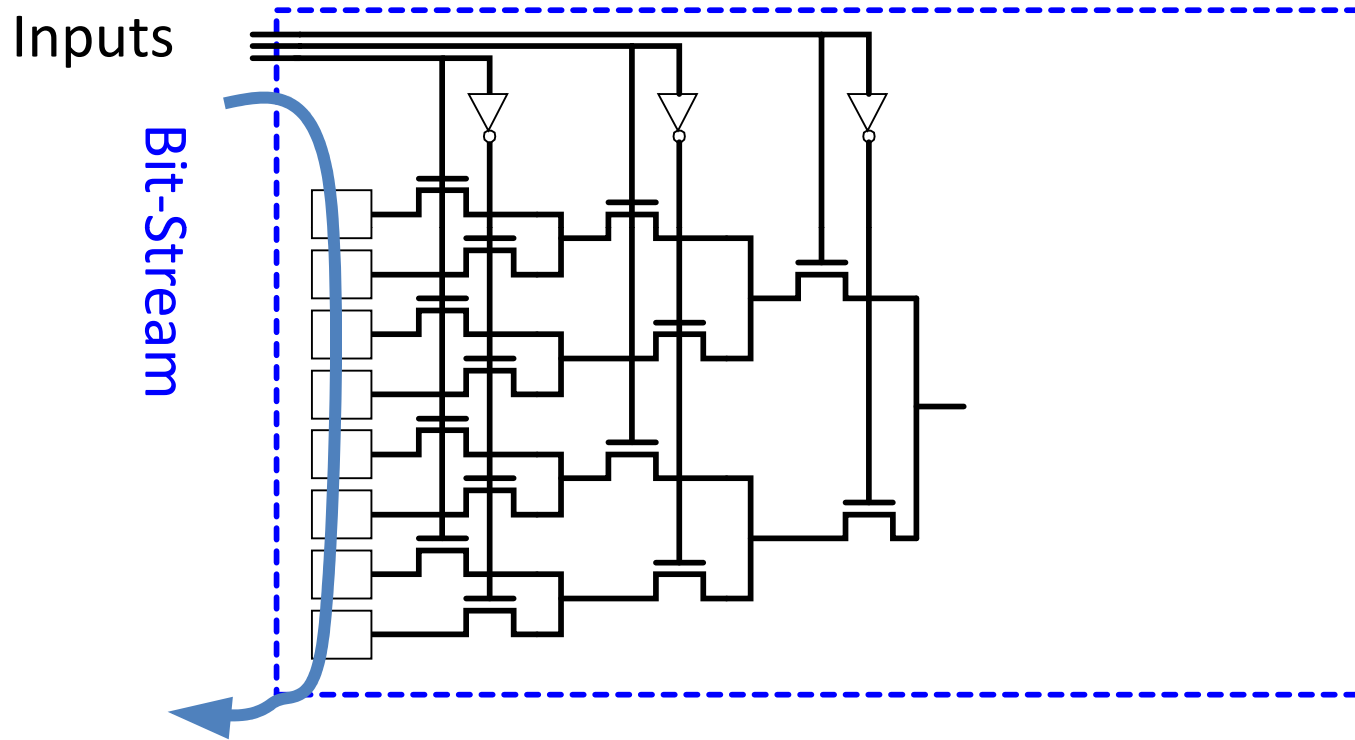
a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Programmed LUT



# Logic Block:

## Basic Logic Gate: Lookup-Table



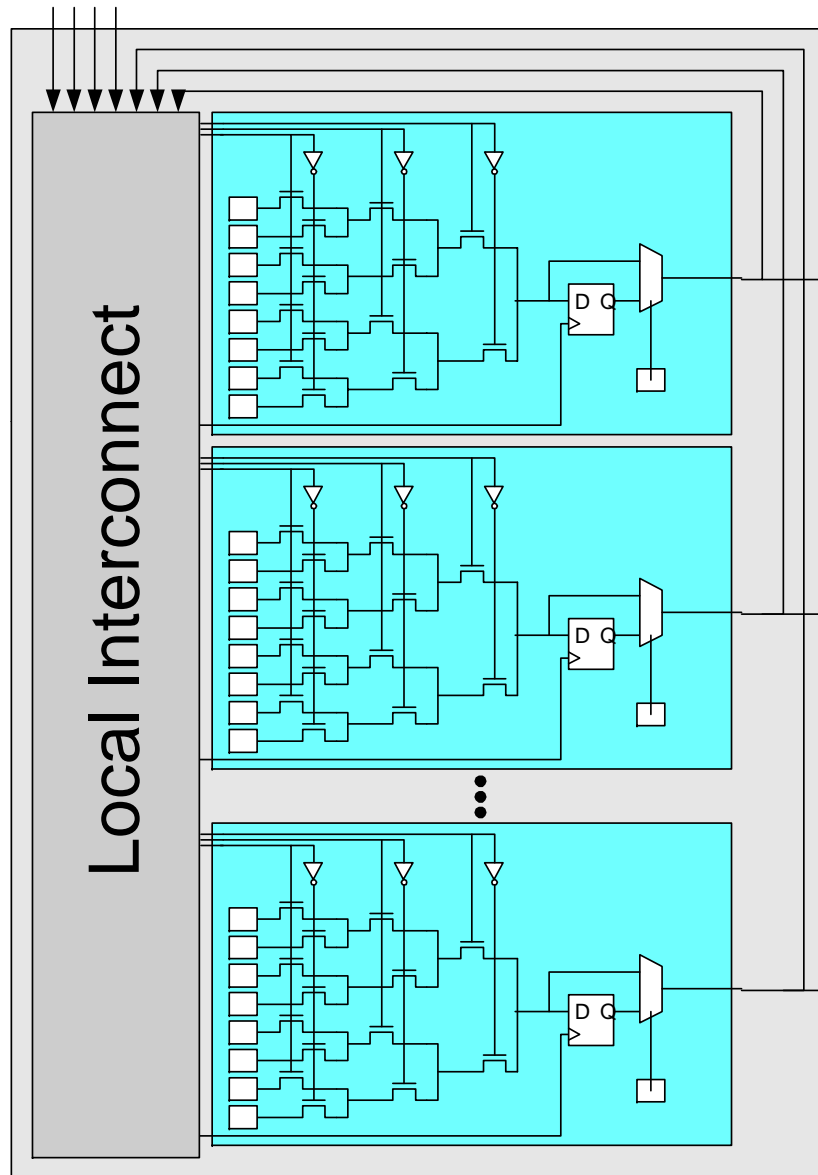
Function of each lookup table can be configured by shifting in bit-stream.



## CLB : Conf Logic Block

- Use Shannon's law to implement any Boolean function of N inputs using
  - Two Block of CLB of N-1 input
- Example
  - $F(A,B,C) = A' \cdot F(0,B,C) + A \cdot F(1,B,C)$ 
    - $F(0,B,C) = 1 \cdot F(0, B, C) + 0 \cdot F(1,B,C) = F(0, B, C)$
    - $F(1,B,C) = 0 \cdot F(0, B, C) + 1 \cdot F(1,B,C) = F(1, B, C)$
- Can be extended to higher inputs

# Logic Clusters



Several lookup tables are grouped into “clusters”

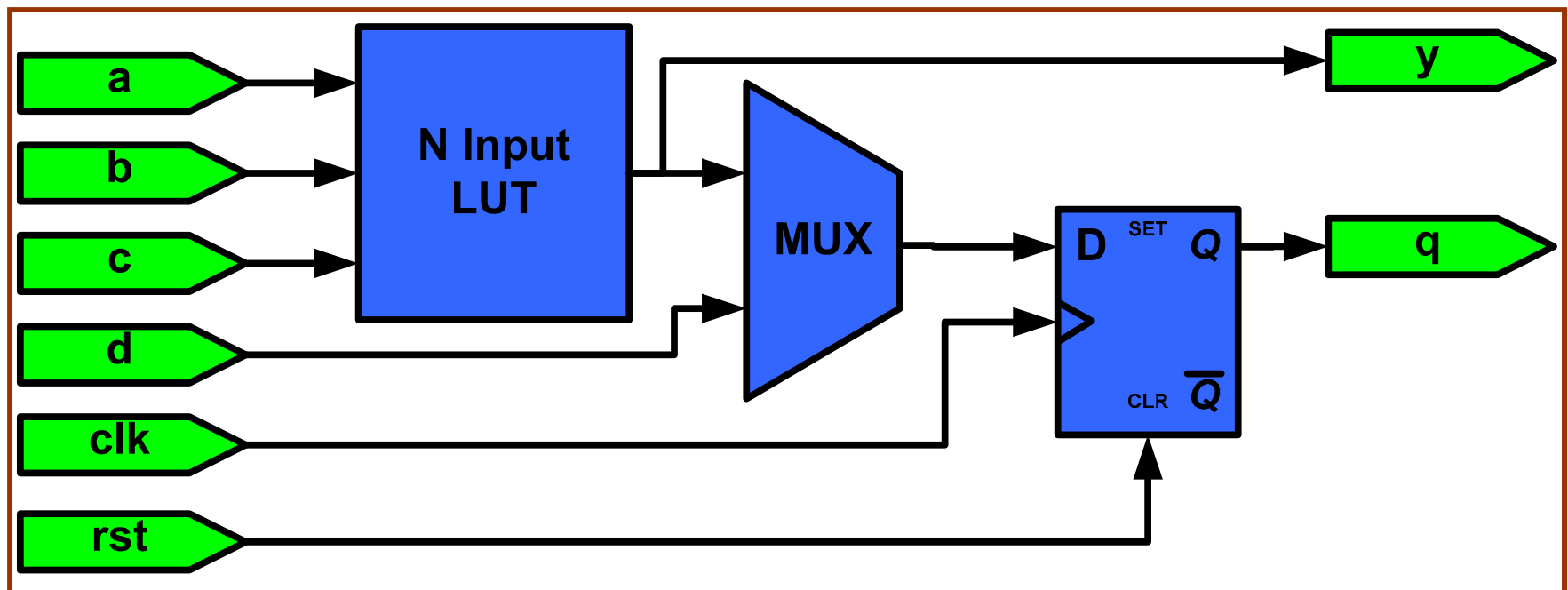
- Typically 8 to 10 lookup tables per cluster

Connections between lookup tables in the same cluster are fast

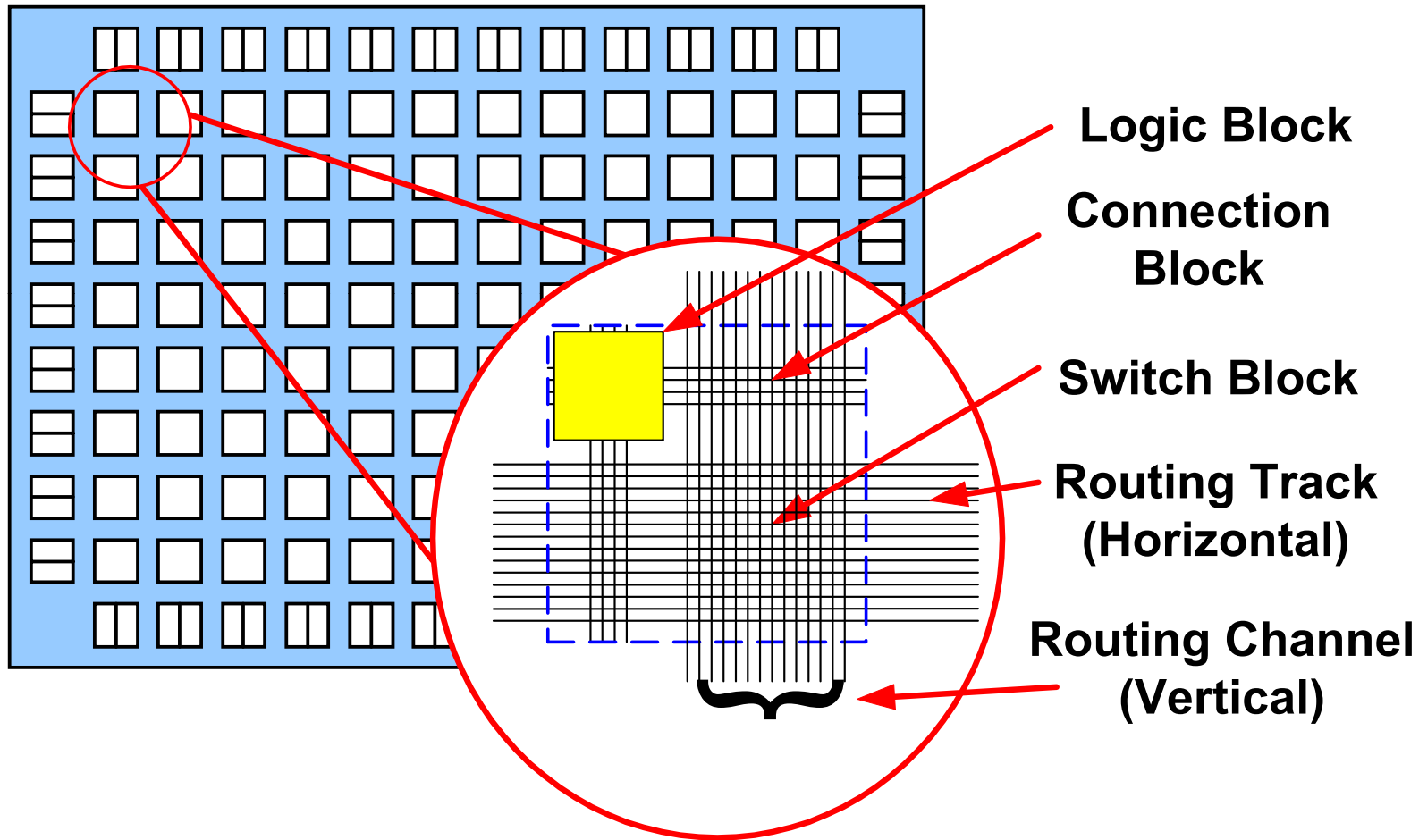
Connections between lookup tables in different clusters are slow

# CLB : Conf Logic Block

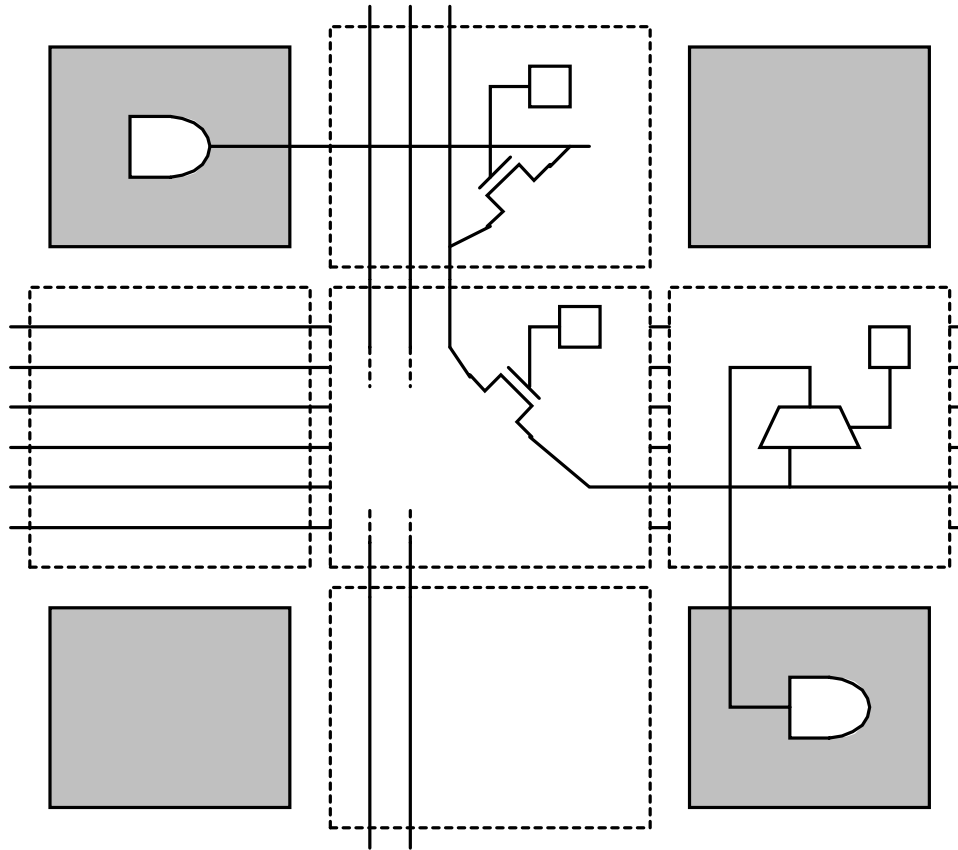
- If Clocked D-Flip available in CLB along with LUTs, we can implement any Sequential circuit
- Clocked Circuit can be implemented



# What's Inside an FPGA?

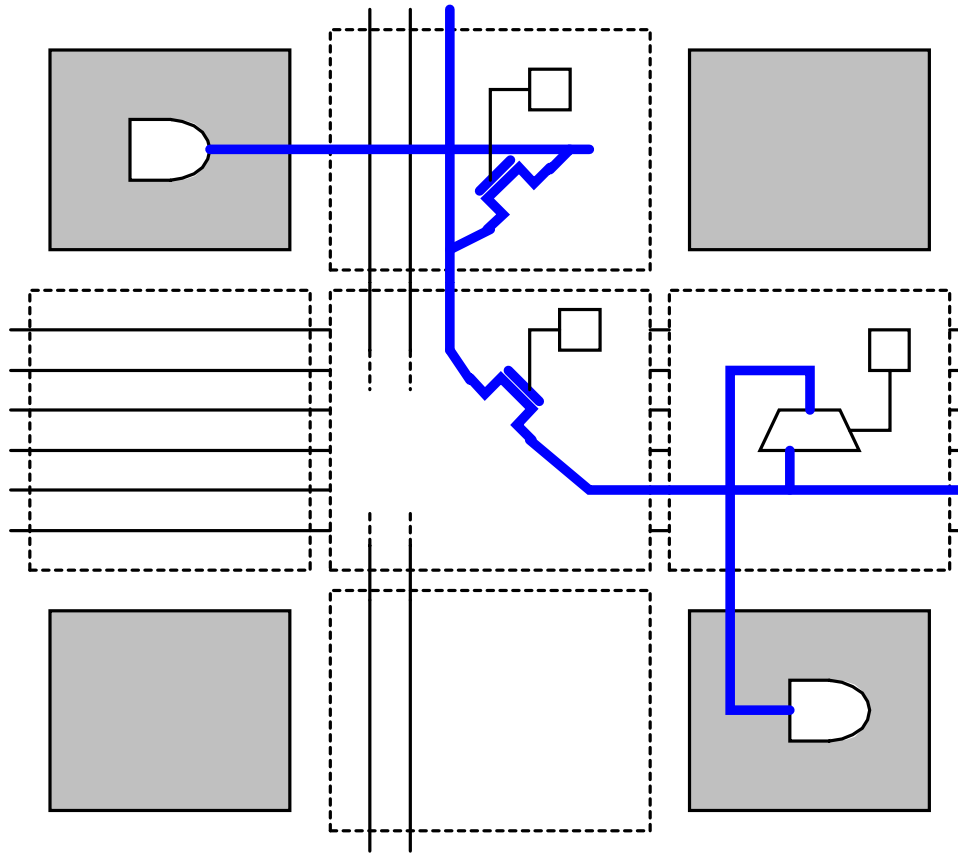


# Reconfigurable Logic:



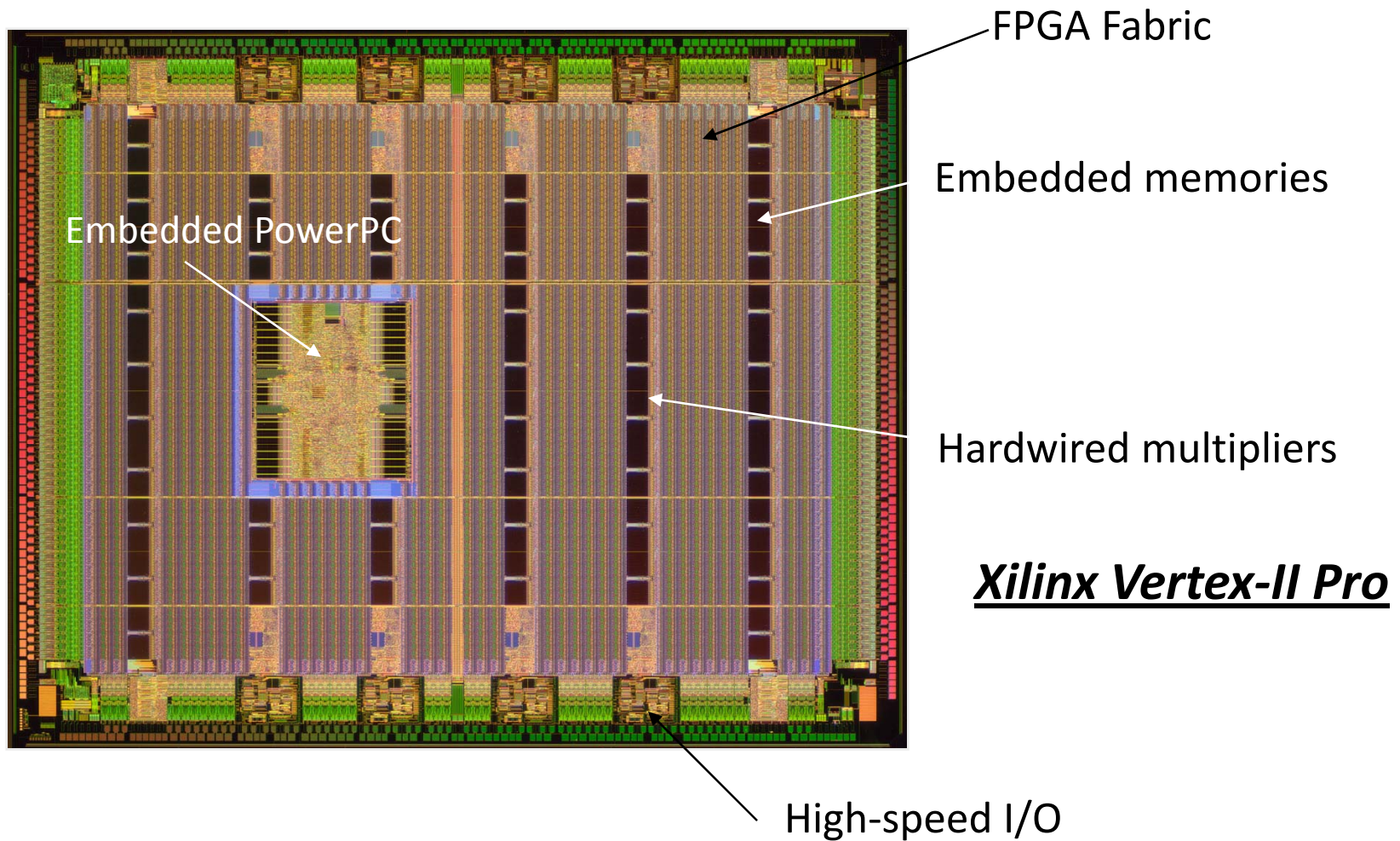
Connect Logic  
Blocks using  
Fixed Metal  
Tracks and  
Programmable  
Switches

# Reconfigurable Logic:



Connect Logic  
Blocks using  
Fixed Metal  
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Programmable  
Switches

# Implementing Systems in an FPGA



# FPGA Advantages

- **Designing with FPGA: Faster, Cheaper**
- **Ideal for customized designs**
  - Product differentiation in a fast-changing market
- **Offer the advantages of high integration**
  - High complexity, density, reliability
  - Low cost, power consumption, small phy. size
- **Avoid the problems of ASICs**
  - high NRE cost, long delay in design and testing
  - increasingly demanding electrical issues



# FPGA Advantages

- **Very fast custom logic**
  - massively parallel operation
- **Faster than micro-controllers/and processors**
  - much faster than DSP engines
- **More flexible than dedicated chipsets**
  - allows unlimited product differentiation
- **More affordable and less risky than ASICs**
  - no NRE, min order size, or inventory risk
- **Reprogrammable at any time**
  - in design, in manufacturing, after installation

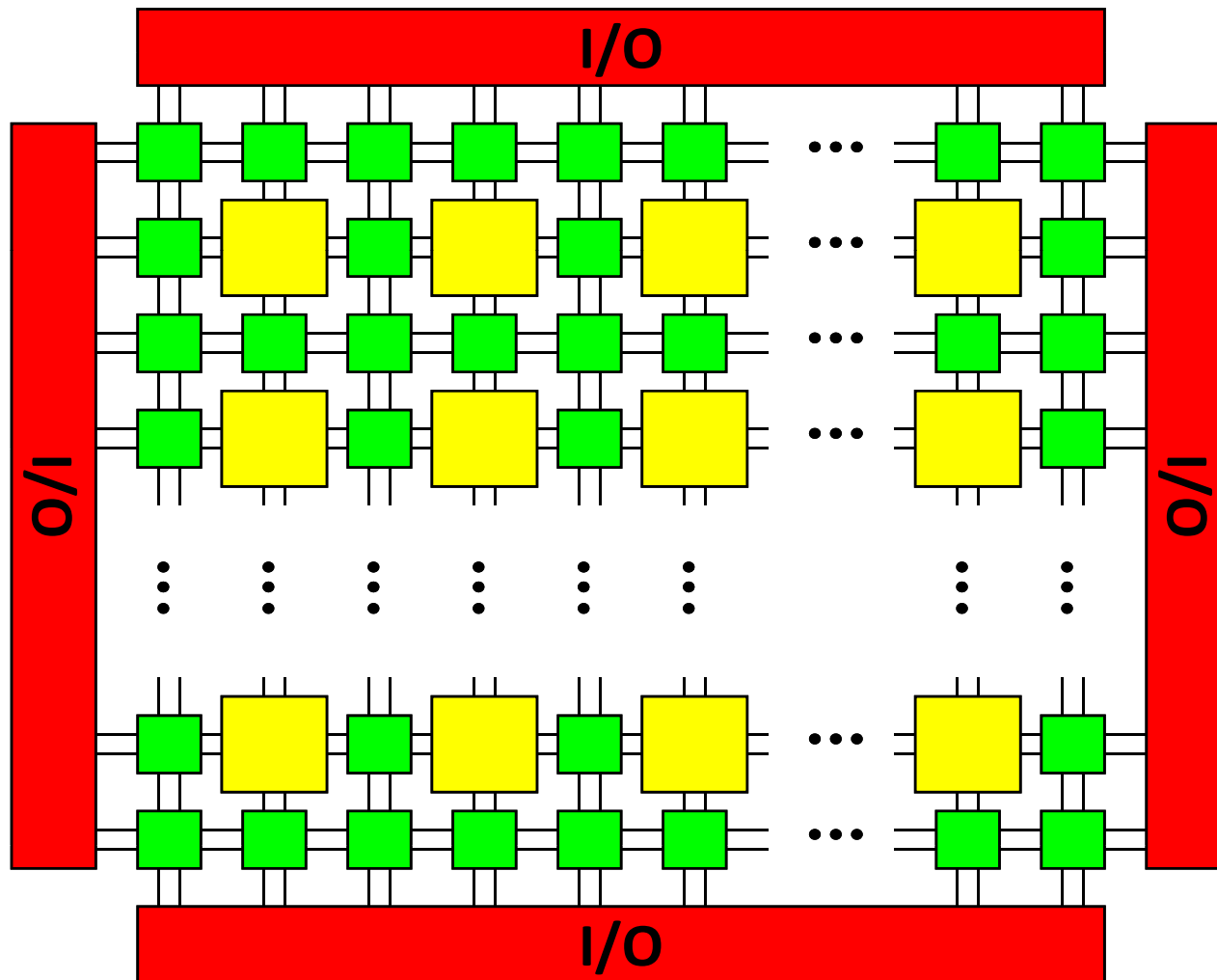
# User Expectations

- **Logic capacity at reasonable cost**
  - 100,000 to a several million gates
  - On-chip fast RAM
- **Clock speed**
  - 150 MHz and above, global clocks, clock management
- **Versatile I/O**
  - To accommodate a variety of standards
- **Design effort and time**
  - synthesis, fast compile times, tested and proven cores
- **Power consumption**
  - must stay within reasonable limits

# Field Programmable Device

- **Basic Section of FPD:**
  - Logical Block
  - Routing (Switch Matrix)
  - Input Output Block
- **More Advanced FPD Contains:**
  - On-chip Memory
  - Embedded Processor
  - Clock Management
  - High-Speed Transceiver

# FPGA - Field Programmable Gate Array



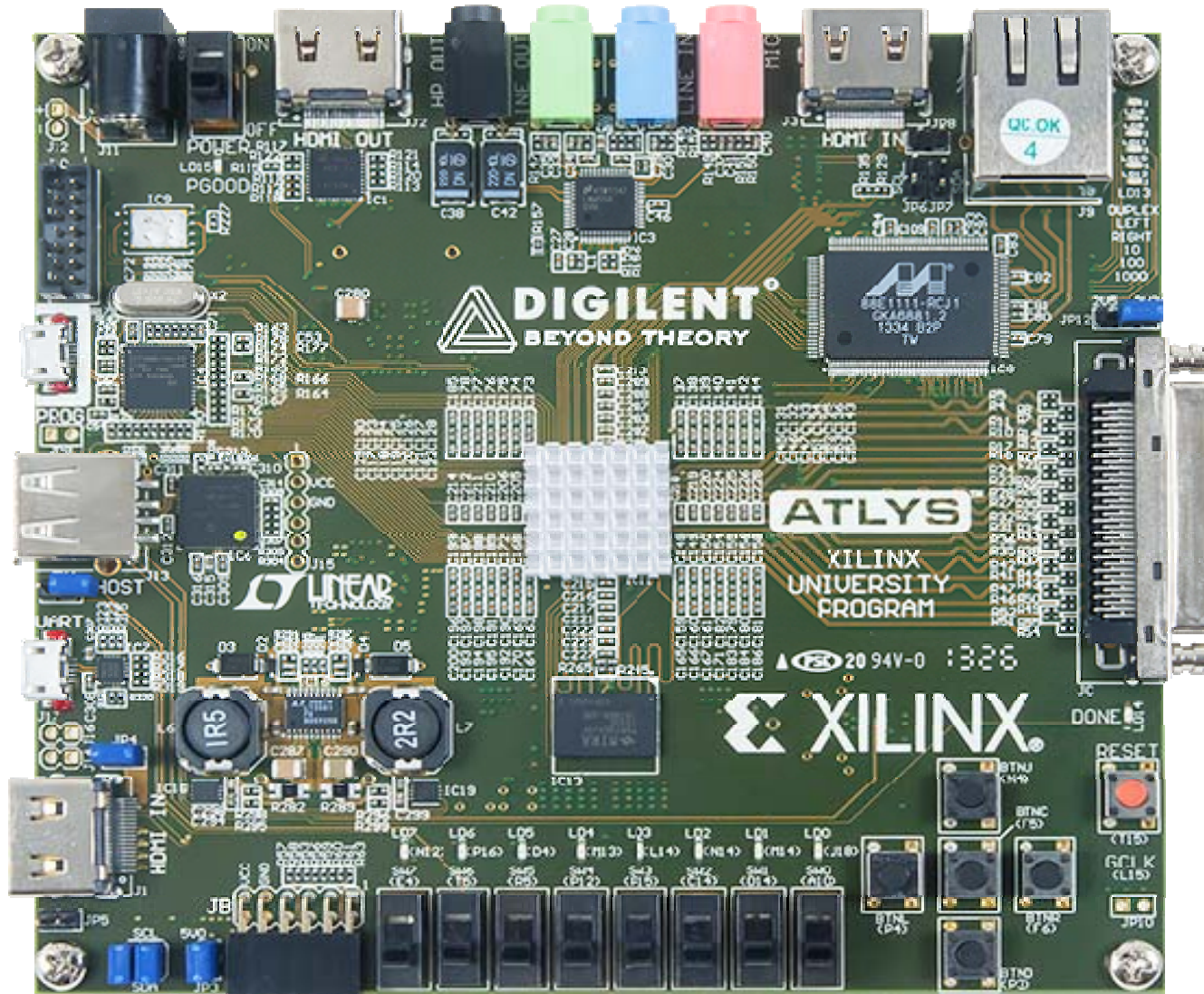
# Special FPGA functions

- Internal SRAM
- Embedded Multipliers and DSP blocks
- Embedded logic analyzer
- **Embedded CPUs**
- High speed I/O (~10GHz)
- DDR/DDRII/DDRIII SDRAM interfaces
- PLLs

# Digilent Xilinx Atlys FPGA Board

- [Xilinx Spartan-6](#) LX45 FPGA,
- 6,822 slices : four 6-input LUTs and eight flip-flops
- 2.1Mbits of block RAM, 128 MB DDR2
- 58 DSP slices
- JTAG programming , RJ-45 Ethernet port
- 4 HDMI video ports
- AC-97 Audio Codec mic, & headphone
- Two on-board USB2
- USB-UART and USB-HID port
- GPIO includes 8 LEDs, 6 buttons, and 8 slide switches

# Digilent Xilinx Atlys FPGA Board

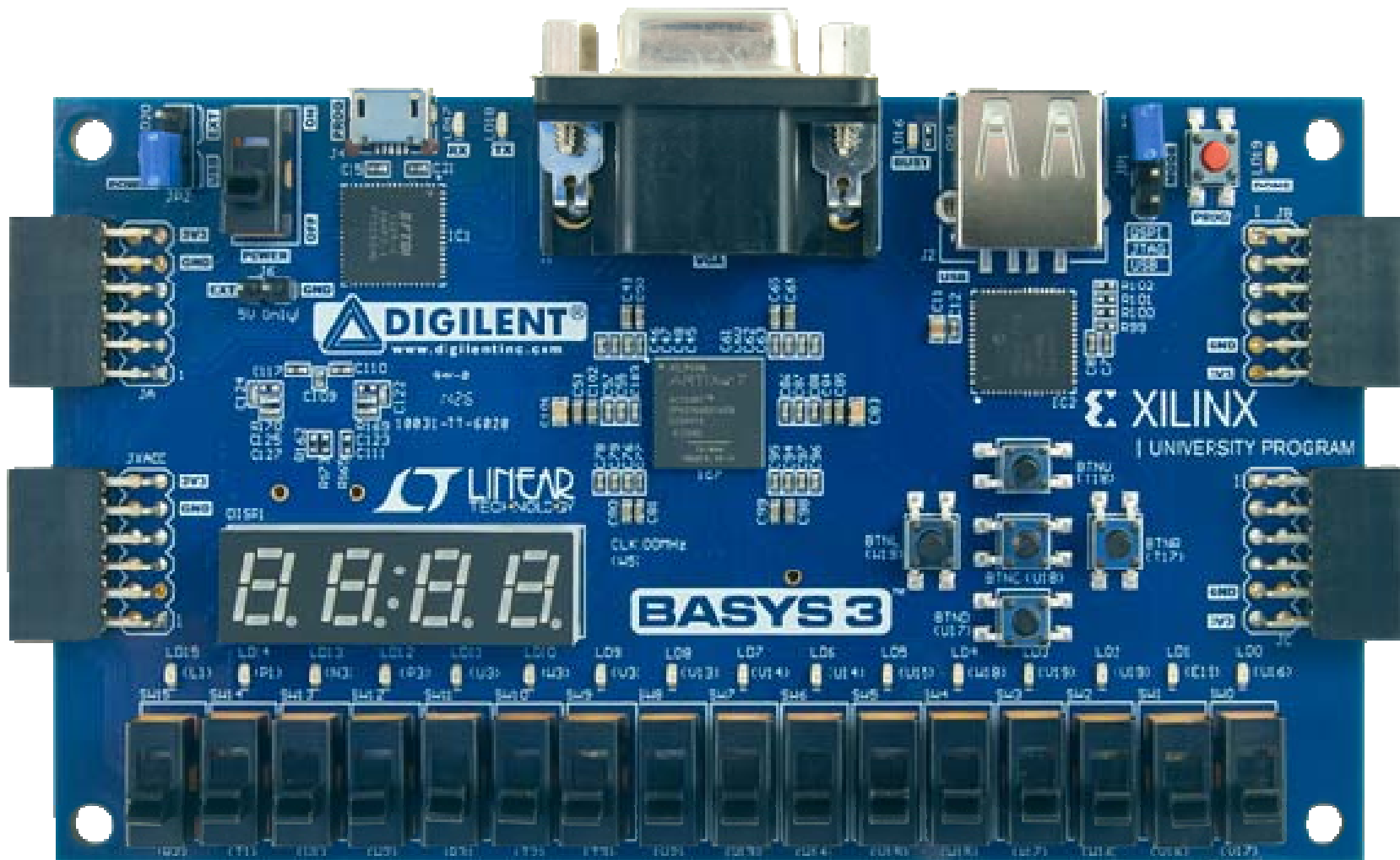


# Digilent Xilinx Basys 3 FPGA Board

- [Xilinx Artix-7 FPGA](#)
- 33,280 logic cells in 5200 slices (four 6-input LUTs and 8 flip-flops)  
1,800 Kbits of fast block RAM
- 90 DSP slices
- ADC, USB-JTAG port, USB-UART Bridge , 12-bit VGA output
- USB HID Host for mice, keyboards
- 16 user switches, 16 user LEDs, 5 user pushbuttons , 4-digit 7-segment display



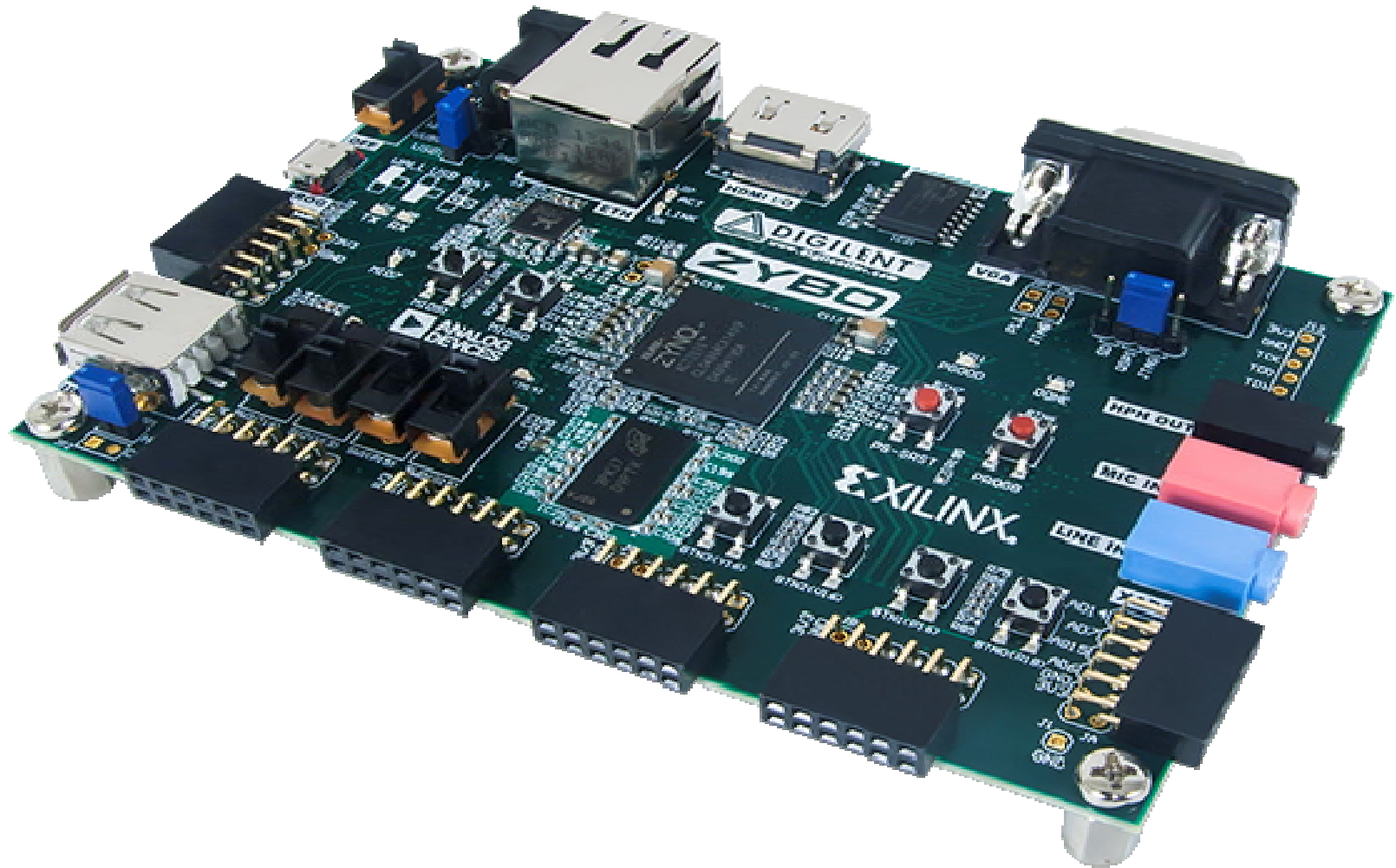
# Digilent Xilinx Basys 3 FPGA Board



# Digilent Xilinx Zybo FPGA Board

- [Xilinx Zynq-7000 \(XC7Z010-1CLG400C\)](#)
- 28,000 logic cells
- 240 KB Block RAM
- 80 DSP slices , Dual channel, 12-bit, ADC
- **650 MHz dual-core Cortex™-A9 processor**
- JTAG programming and UART to USB converter
- 1G Ethernet, USB 2.0, SDIO, SPI, UART, I2C
- Dual-role HDMI port , VGA port, Ethernet PHY
- OTG USB 2.0 PHY (supports host and device)
- GPIO: 6 pushbuttons, 4 slide switches, 5 LEDs

# Digilent Xilinx ZYBO FPGA Board



Thanks