Akul Malhotra

Education

2016 - 2020 **BITS Pilani, Pilani Campus, India.**
Bachelor of Engineering (Hons.) in Electrical and Electronics Engineering.
CGPA: 9.08/10.
Relevant courses: Analog and Digital VLSI Design, Microelectronic Circuits, Analog Electronics, Electronic Devices, Digital Signal Processing, Computer Architecture, Deep Learning Specialization (Coursera)

Research Experience

Aug '19 - Jan'20 **Research Intern at Pennsylvania State University, USA**
Undergraduate thesis: Hardware Acceleration of Bayesian Neural Networks using post CMOS devices.
Thesis Advisor: Dr. Abhronil Sengupta

- Designed an **all-spin bayesian neural network** using the stochastic switching property and the multilevel states of magnetic tunnel junctions (MTJs).
- Implemented an in-memory computing bayesian neural network exploiting the **cycle to cycle variability** of metal oxide resistive random access memories to generate Gaussian random numbers.
- Also worked on solving matrix equations in one step with cross-point resistive arrays.

May '19 - July '19 **MITACS Globalink Research intern at University of Calgary**
Recipient of *MITACS scholarship* for the project: Characterization and Localization of an urban noise nuisance-The Ranchland's Hum
Project Advisor: Dr. Mike Smith, Dept. of Electrical Engineering.

- Worked in **Small Microsystems for Improving Life Expectancy (SMILE) Lab**. The project's aim was to investigate what are the various elements that make **noise annoying to humans**.
- Used **A-Weighting** and **IEC 61400-11 edition 3.0**, a previously existing metric for measuring wind turbine noise annoyance, to determine the frequencies of the urban noise causing most annoyance to the residents of the area.

Aug '18 - Dec '18 **Undergraduate Research Assistant at the Oyster Lab (VLSI design lab), BITS Pilani**
Project topic: Design of low power circuits using post CMOS devices
Project Advisor: Dr. Nitin Chaturvedi

- Designed a **nonvolatile SRAM cell** which uses **STT-MTJ** as the nonvolatile component for backup and restore operation during power off.
- Designed a **write termination circuit** for the SRAM cell to sense completion of write operation and stop current flow in the circuit, reducing energy consumption by **17.88 percent**.
- Also worked on the design of a 4-phase, dual rail **nonvolatile pipeline** for logic circuits, based on **Ivan E. Sutherland's** concept of '*Micropipelines*'.

May '18 - Aug '18 **Research Intern at National Institute of Oceanography, India**
Project topic: Marine Soundscape Analysis of the Angria Bank Coral Reef Region
Project Advisor: Mr. Vasudev Mahale, Senior Scientist

- Worked on analysing the **marine soundscape** of the Angria Bank coral reef region in the Arabian Sea using passive acoustic monitoring.
- Studied the temporal variations in the biophony using **power spectral density**, **Short Time Fourier Transform and Recurrence Quantification Analysis** (RQA).
- Developed a technique to extract a ship's characteristic **sound signature** using the sound analysis software **Raven** and **MATLAB**.

Publications

1. K. Monga, **A. Malhotra**, N. Chaturvedi and S. Gurunayaranan, "A Novel Low Power Non-Volatile SRAM Cell with Self Write Termination," 2019 10th International Conference on Computing, Communication and Networking Technologies (ICCCNT), Kanpur, India, 2019, pp. 1-4.

2. **A Malhotra**, S. Lu, K. Yang, A. Sengupta, "Exploiting Oxide Based Resistive RAM Variability for Bayesian Neural Network Hardware Design," in IEEE Transactions on Nanotechnology, vol. 19, pp. 328-331, 2020.

3. K. Yang, **A. Malhotra**, S. Lu and A. Sengupta, "All-Spin Bayesian Neural Networks," in IEEE Transactions on Electron Devices, vol. 67, no. 3, pp. 1340-1347, 2020.

4. **A. Malhotra** and A. Chintanpalli, "A Real Time Wavelet Filtering for ECG Baseline Wandering Removal," 2020 International Conference on Artificial Intelligence and Signal Processing (AISP), Amravati, India, 2020, pp. 1-5.

Projects

Jan '20 - Present — **SINR optimization in Cell-Free Massive MIMO Systems**
Project supervisor - *Dr. S.M. Zafaruddin*
Working on improving the signal to interference noise ratio (SINR) and the bit rate of cell-free massive MIMO systems. Various techniques like **channel estimation**, optimization using **power control coefficients** and **access point selection** are being implemented on the system to improve the desired parameters.

Jan '19 - May '19 — **Removal of baseline wandering in ECG signals using TMS320C5535**
Project supervisor - *Dr. Ananthakrishna Chintanpalli*
Worked on removal of base line wandering in ECG signals (obtained from **PhysioBank ATM**) by passing them through a **wavelet based high pass filter** as well as traditional high pass filters. Compared the output of **Butterworth, Chebyshev, Elliptic** and **Equiripple filters**. Implemented the algorithms on **Code Composer Studio v4** along with **Texas Instruments' DSP kit TMS320C5535.** A paper based on this project has been accepted in AISP 2020, an international IEEE conference.

Aug '18 - Nov '18 — **Design of a RF adapter to make PS/2 keyboard wireless**
Project supervisor - *Mr. Devesh Samaiya*
Used **LPC 2148's** and an RF transmitter and receiver module to make a PS/2 keyboard function wirelessly. The PS/2 keyboard was interfaced to the transmitter LPC 2148 using **UART**. The receiver LPC 2148 was configured as an **HID keyboard**, which then sent the received value to the PC via USB. **A transmission and reception coding scheme** was designed to reduce error probability, which arises due to noise at the transmission and reception terminals. More details about this project can be found on **hackaday.io** .

Sept '18 - Nov '18 — **Design of a 4 bit binary to greycode converter**
Course project - *Analog and Digital VLSI Design*
Designed a 4 bit binary to greycode converter operating at **1GHz**, having a load capacitance of **500fF**. **Transmission gate** design style was used and the **critical path delay** was minimized by developing a resistance model for the XOR gates.The design was made on the **Schematics L tool** and the layout on **Layout Suite** of Cadence Virtuoso. The layout passed the **DRC** and **LVS** tests.

Mar '19 - Apr '19 — **Automatic Voltage Regulator using PID controller**
Course project - *Power Systems*
Designed a PID controller to regulate the output voltage at 230V. The **bacterial foraging algorithm** was used to optimize the parameters of the PID controller.

Teaching Experience

Jan '19 - May '19 — **Teaching Assistant for Microelectronic Circuits**
- Organized lectures and tutorials for over 250 students to help them learn the applications of **LT Spice** in analog design.
- Assisted them in writing scripts as well as carrying out circuit simulations.

Jan '19 - May '19 — **Teaching Assistant for Microprocessor Programming and Interfacing**
- Taught **assembly level programming** and the use of **MASM** and **Debugx** to a lab section of 100 students and evaluated their performance every week.
- Created a video lecture explaining certain functionalities of the software **Proteus**, which was used by the students for the course project.

Achievements

2019 — **MITACS Globalink Scholarship** - One of the 800 students selected out of 10,000+ applicants from 10 countries. Allotted a research internship at University of Calgary, Canada.

2018 — Presented the results of my work done at the National Institute of Oceanography, India as a talk titled **"Marine Soundscape Analysis of the Angria Bank Reef Region"** at the **Western Pacific Acoustics Conference (WESPAC)**, New Delhi, Nov. 2018.

Skills

Languages: MATLAB, C, C++, Java, Python (Pytorch and Keras), MASM, Verilog HDL
Simulation softwares: HSPICE, Cadence Virtuoso, Eagle CAD, Simulink
Publishing: LaTeX

Positions of Responsibility

TEDx BITS Pilani- *Sponsorship Head*
Led a team of 10+ students to raise cash and kind sponsorship for TEDx BITS Pilani 2019. Planned and made decisions regarding the event along with the other executive committee members.