Sequential Circuit

Flip Flops / Memory Components

Ver. 3

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Topics

- 1-Bit Memory Devices
  - Latches (event-driven devices)
    - SR Latch
    - JK Latch
    - D Latch
  - Flip-Flops (clock-driven devices)
    - JK Flip-Flop
    - D Flip-Flop

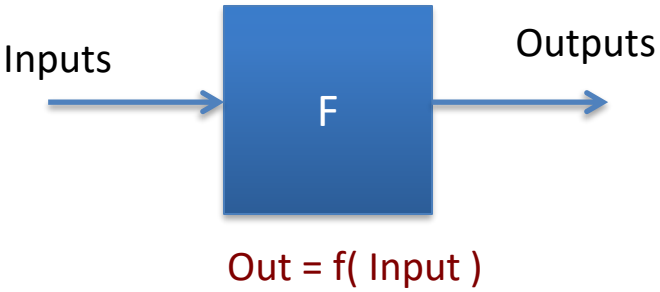
Burger Ch 4 and 5.

Null Ch 3.

Combinational vs. Sequential Circuit

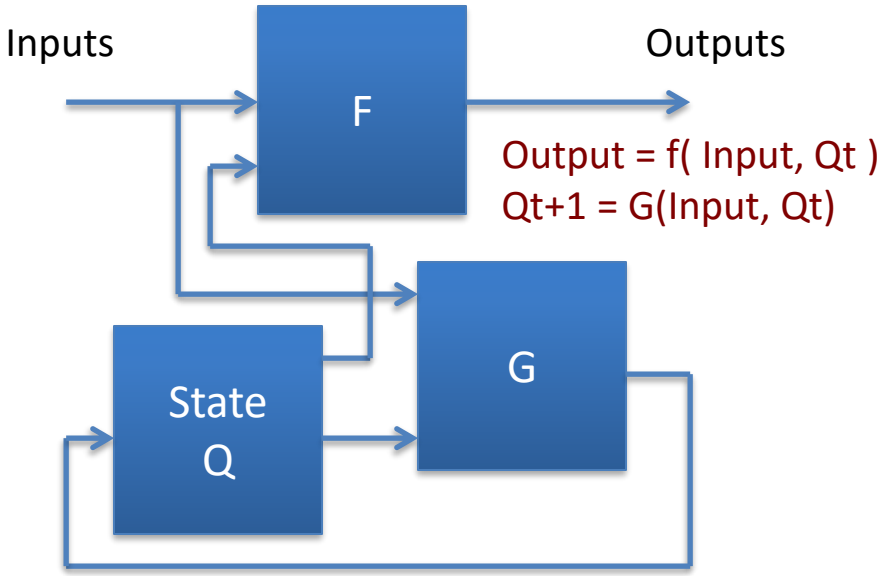
Combinational

- No state and time



Sequential

- Maintaining states
- States transiting along time with inputs and the current states



Asynchronous vs. Synchronous Logic

Event-driven (Asynchronous)

- States and outputs change with random events.
- 1-bit memory device: Latch
  - SR Latch
  - D Latch

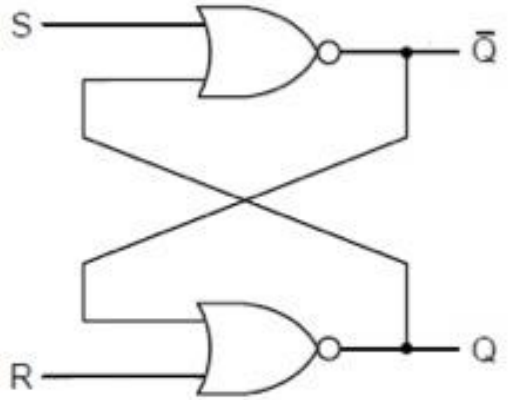
Clock-driven (Synchronous)

- States and outputs change with periodic clock signals.
- 1-bit memory device: Flip-Flop
  - D Flip-Flop
  - JK Flip-Flop

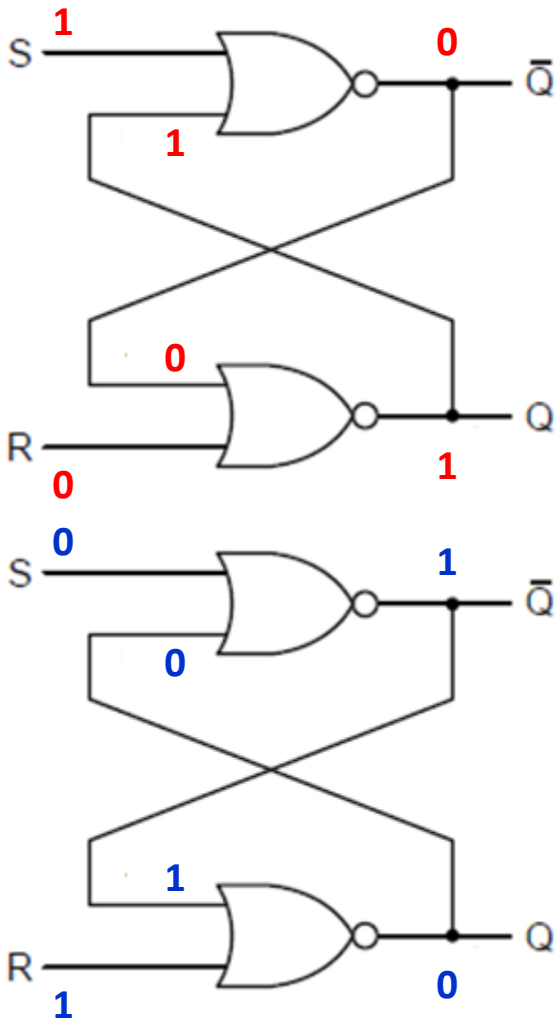
SR Latch

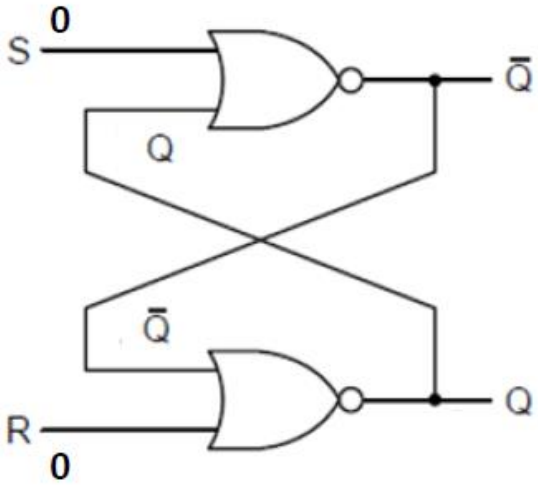
Characteristic Table

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	—



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

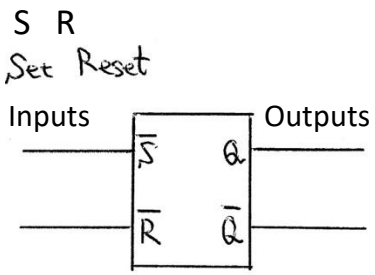




When S=1 and R=1, the output will be in “race condition” (forbidden state)

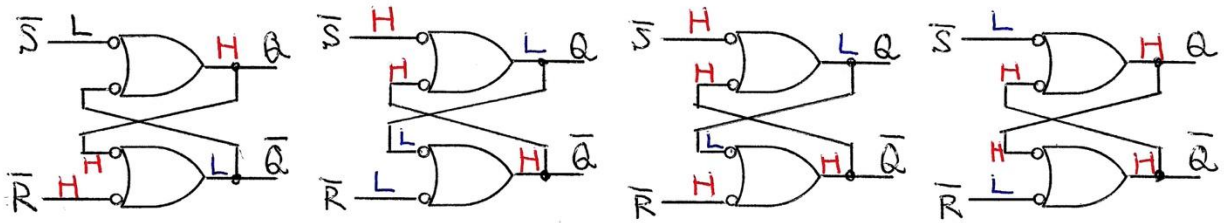
SR Latch

Active Low



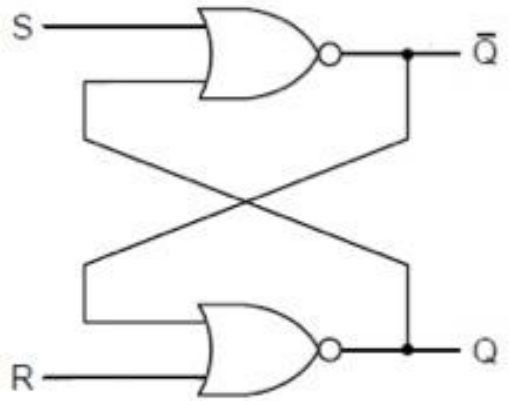
active low

$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
L	H	H	L	Set
H	L	L	H	Reset
H	H	Q_{n-1}	$\bar{Q}_{n-1}$	→ No change (latch)
L	L	H	H	→ Undefined

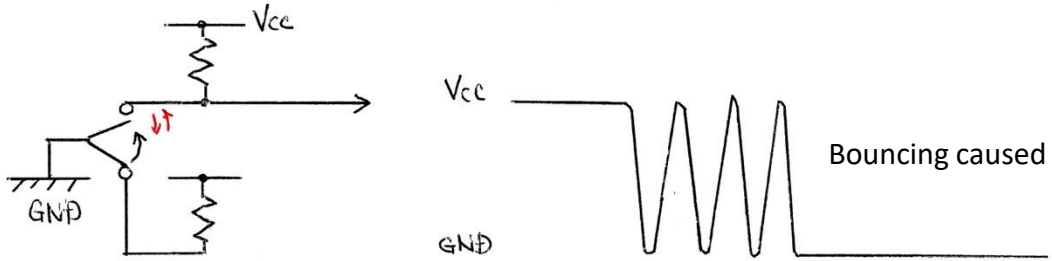


Active High (Textbook Spec.)

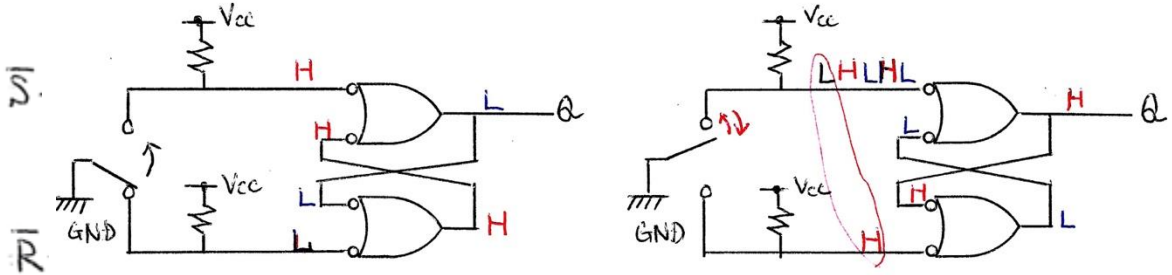
S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	—



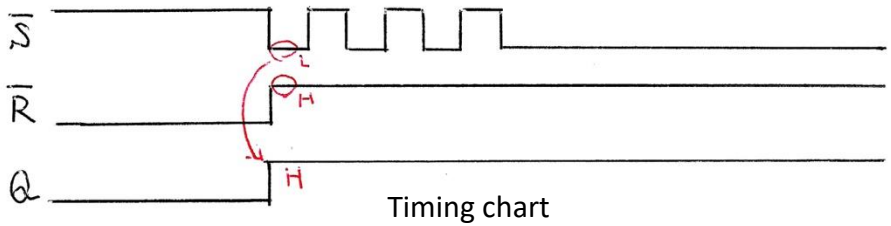
SR Latch Application: Switch Debouncer



Bouncing caused by a switch



Once a state is set, bouncing repeats no change and set in Q



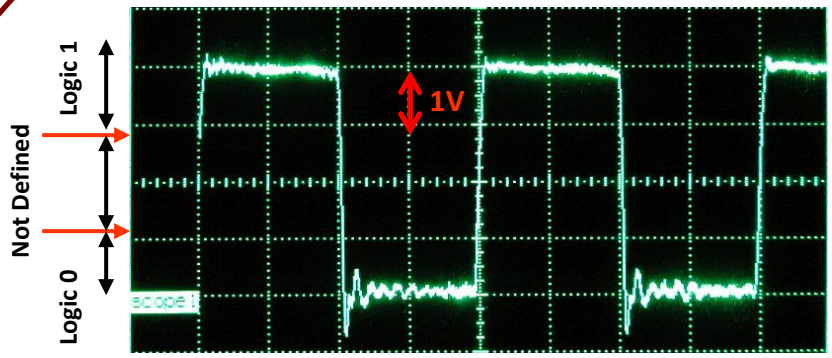
Timing chart

Clocks and Time

- The ***clock*** in a digital system is an electronic analog of the pendulum which synchronizes the circuits in a computer system
  - The master control signal
  - Changes occur on the rising or falling edges of a clock pulse
- Frequencies are the inverse of time (speed)

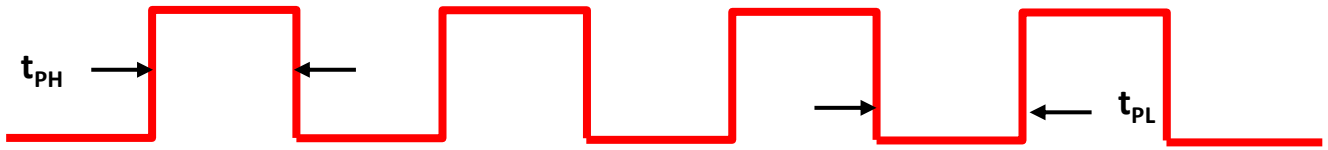
Frequency		Speed	Time
1 kilohertz	KHz	10^3 Hz	1msec
1 megahertz	MHz	10^6 Hz	1µsec
IBM PC (with Intel 486)	50 MHz		20nsec
1 gigahertz	GHz	10^9 Hz	1nsec
Dell Precision T550 (Intel Zeon X5698)	4.4 GHz		
1 terahertz	THz	10^{12} Hz	1psec

This is the TTL (74 series) level.

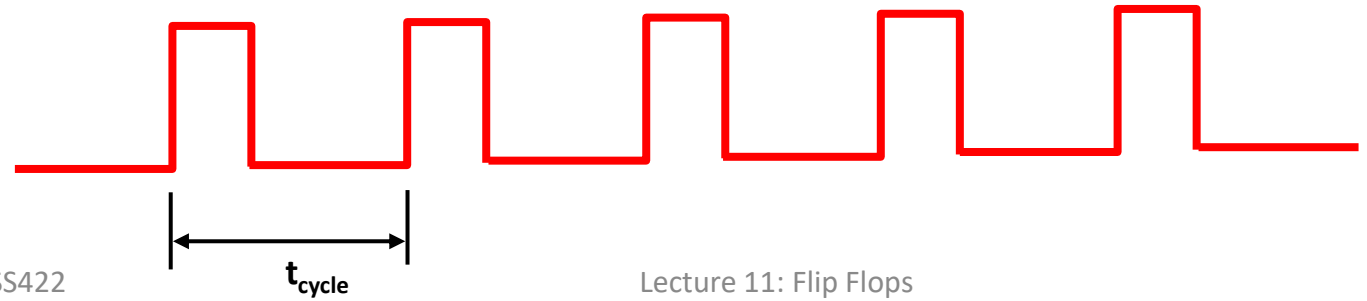


Clocks and Pulses

- Clocks are continuous streams of pulses



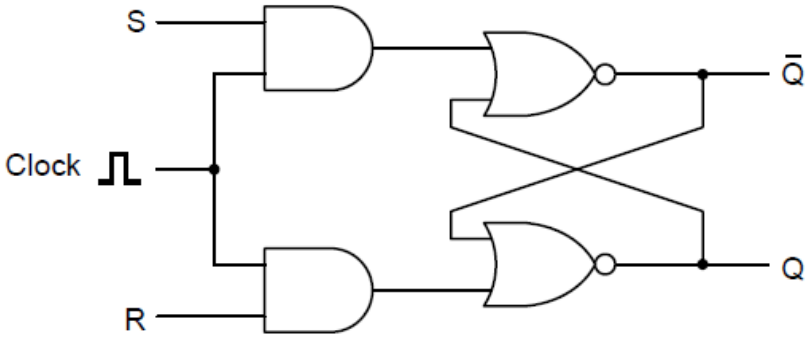
- Duty cycle = $t_{PH} / (t_{PH} + t_{PL})$ x 100%
  - The clock signal shown above has a 50% duty cycle
  - The clock signal shown below has a 25% duty cycle
  - ***Period:*** The time to complete one clock cycle
    - Period = $\mathbf{t_{cycle}}$
  - ***Frequency:*** The inverse of the period, f = 1/period



Clocked SR Latch and D Latch

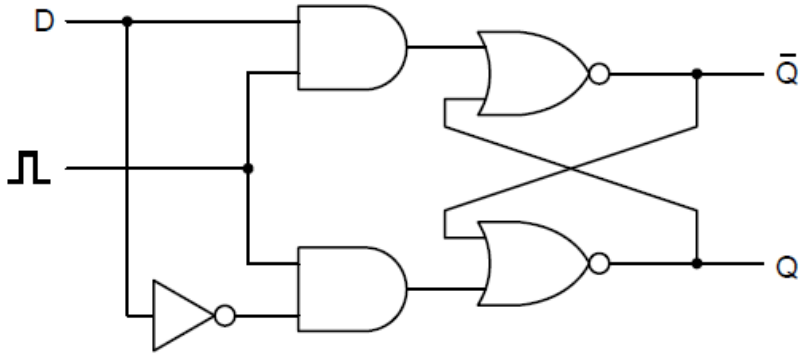
Clocked SR Latch

- Prevent the latch from changing state except at certain specific time.
- When clock is 1, the latch is sensitive to S or R.



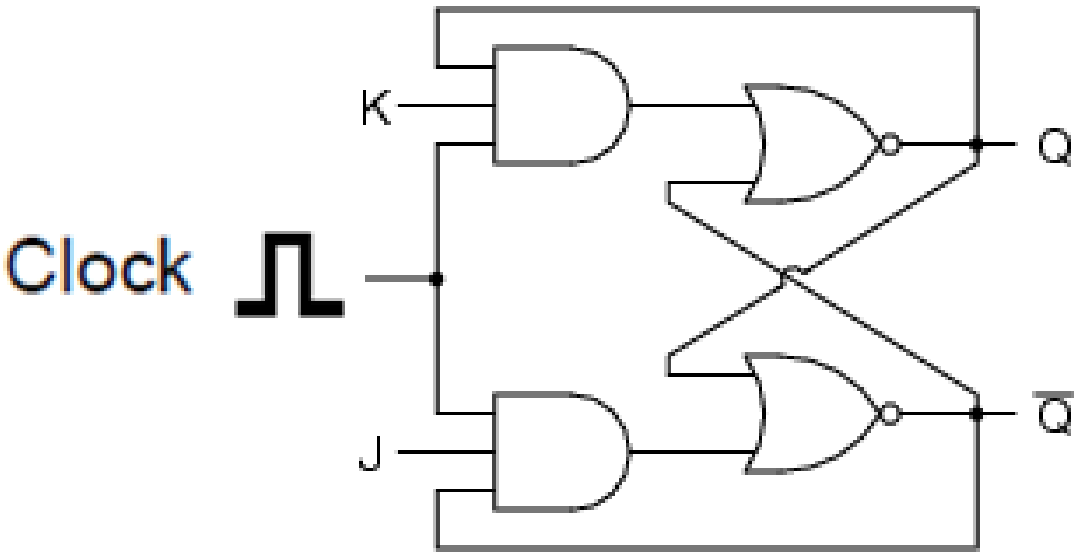
Clocked D Latch

- **Avoid the SR latch's instability by giving R as the inverse of S.**
- Stored value is available at Q
- To load the current value of D, give a positive pulse on the clock line.



Clocked JK Latch

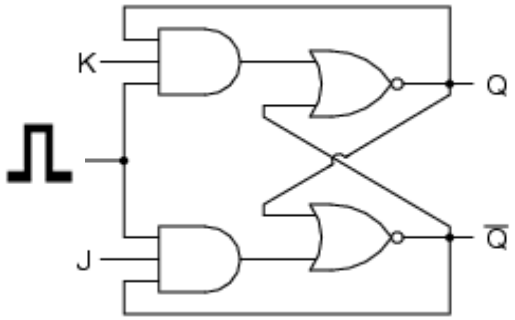
- Avoid the SR latch's instability by preventing the inputs being 1 at the same time.
- In this case all possible combinations of input values are valid!



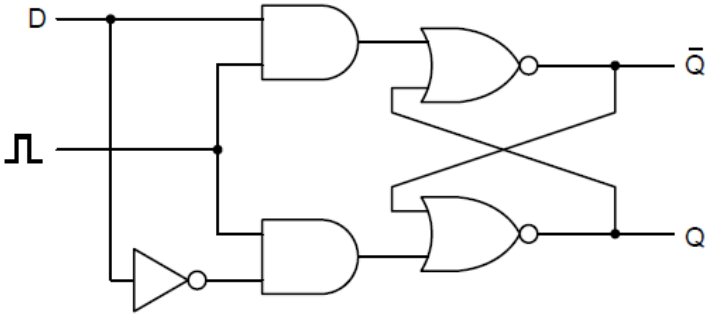
C	J	K	Q	$\overline{Q}$
⌐	0	0	latch	latch
⌐	0	1	0	1
⌐	1	0	1	0
⌐	1	1	toggle	toggle
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

Issue with Clock Signal

- What if the input signal (J and K in JK Latch or D in D latch) gets changed when the clock is HIGH?

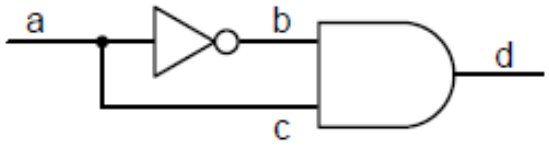


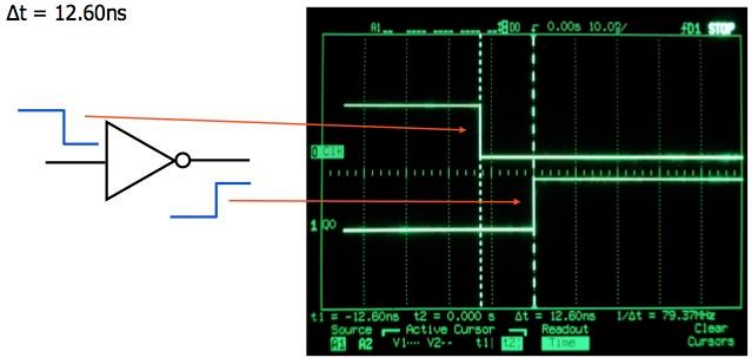
C	J	K	Q	$\overline{Q}$
⌐¬	0	0	latch	latch
⌐¬	0	1	0	1
⌐¬	1	0	1	0
⌐¬	1	1	toggle	toggle
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

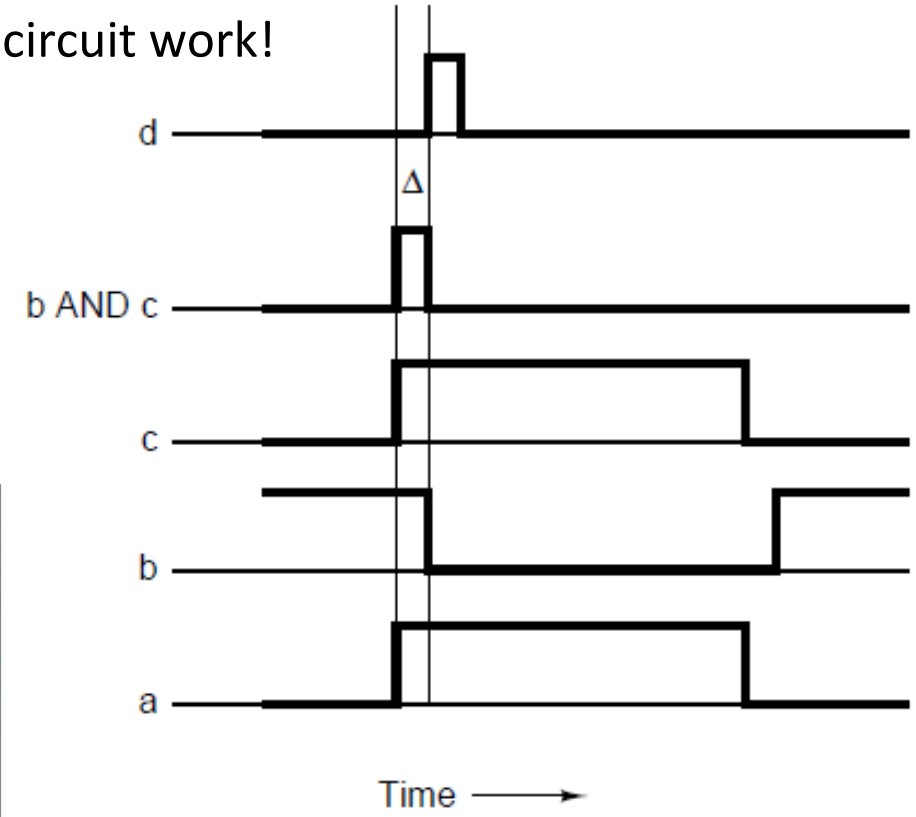


Creating an Edge

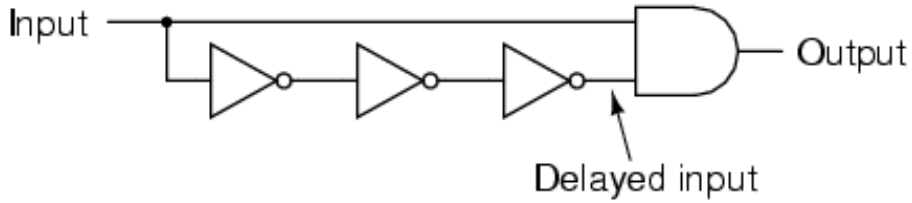
- Delay in the inverter makes the circuit work!

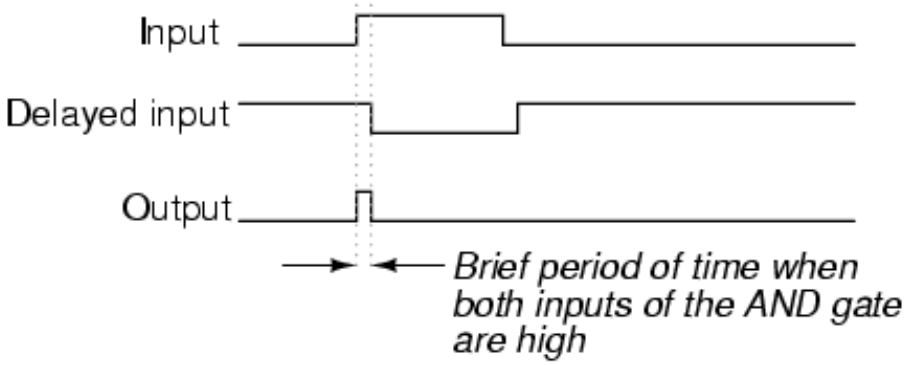


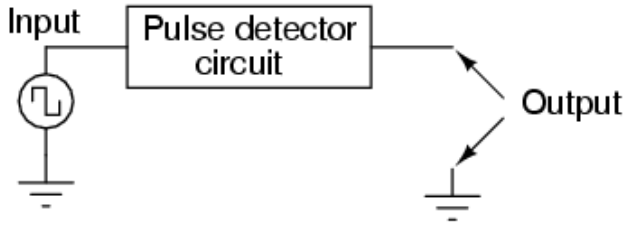


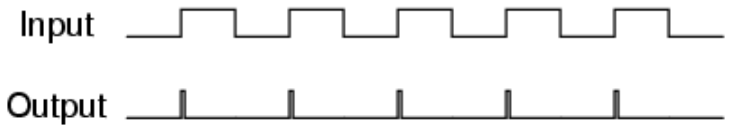


Rising-Edge Pulse Detector

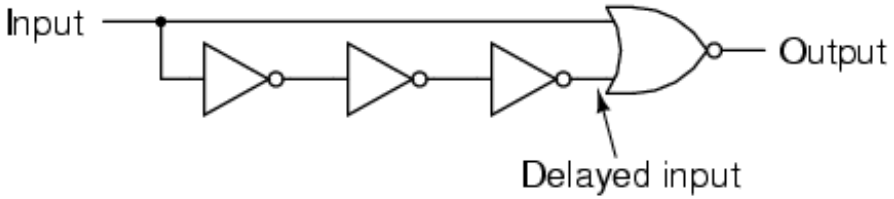


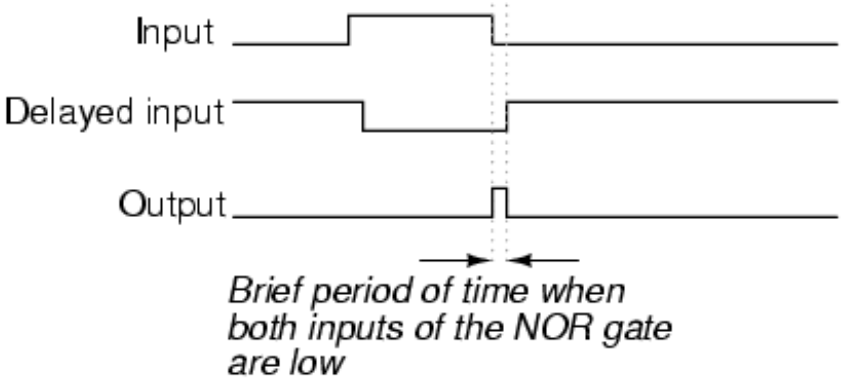


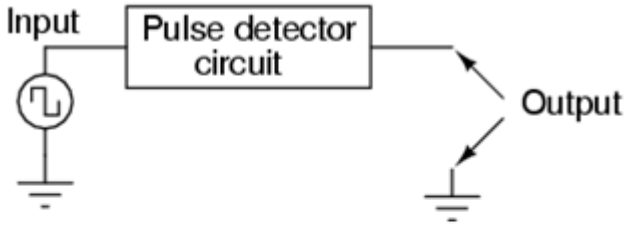


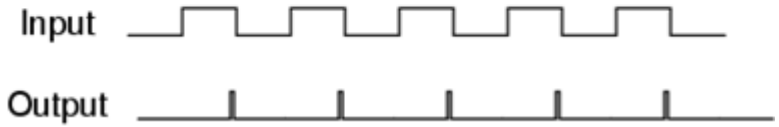


Falling-Edge Pulse Detector

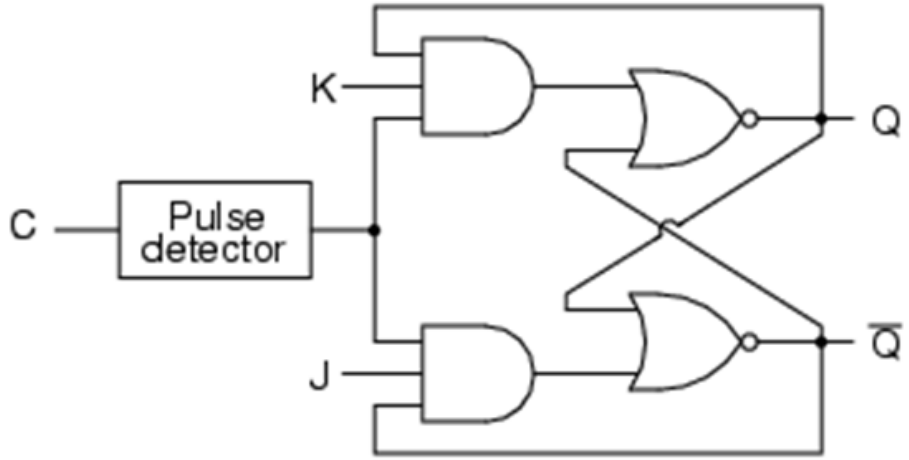




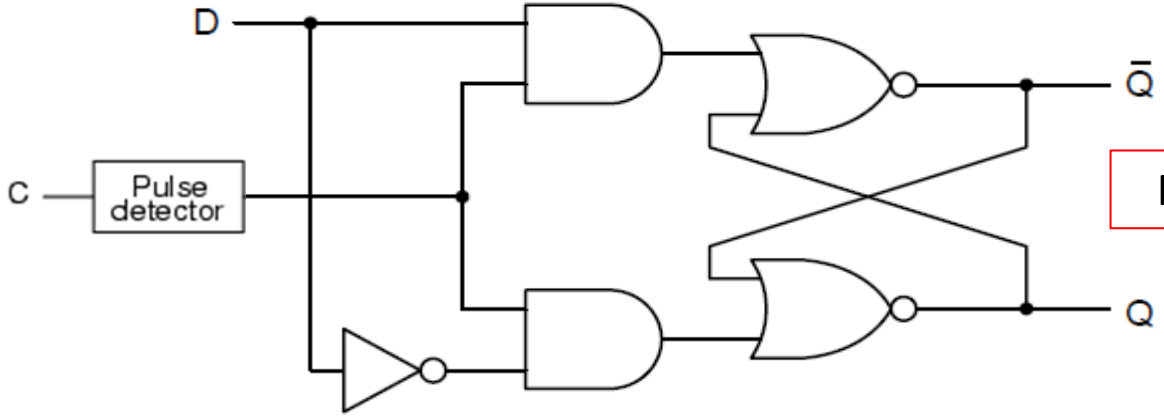




Using Pulse Detector in Circuit



Now called JK Flip-Flop

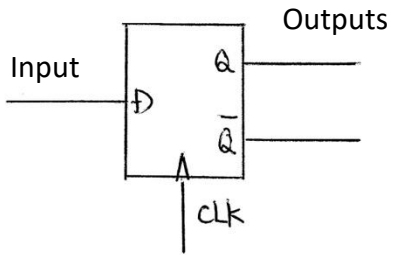


Now called D Flip-Flop

Latch vs. Flip-Flop

	Latch	Flip-Flop
Similarities	• Basic components for sequential circuit design • They are bi-state devices. It is in one of two states. • Without inputs, they remain in that state. • They have two outputs which are always the complements of each other.	
Differences	**Level triggered**: State changes when the clock is active.	**Edge triggered**: State transition occurs when the clock transition from 0 to 1 or from 1 to 0.

D Flip-Flop and JK Flip-Flop



D	CLK	Q	$\bar{Q}$
L	↑	L	H
H	↑	H	L
*	L	Q_0	$\bar{Q}_0$

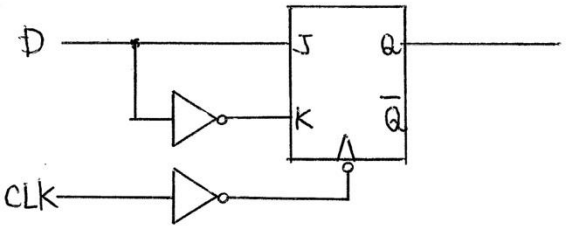
Set upon an up edge of the clock

D	CLK	Q State	J	K	Jk/FF CLK
0	↑	0 Reset	0	1	↓
1	↑	1 Set	1	0	↓
*	0	Q_0 No Change	*	*	1

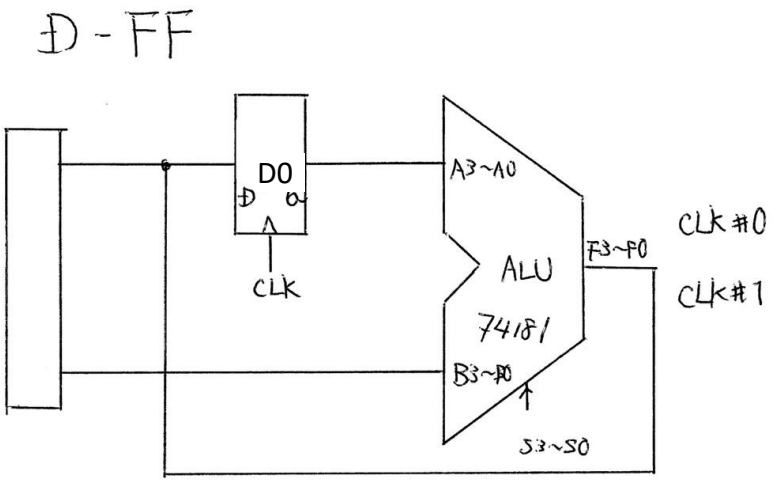
$J = D$

$Q = \bar{D}$

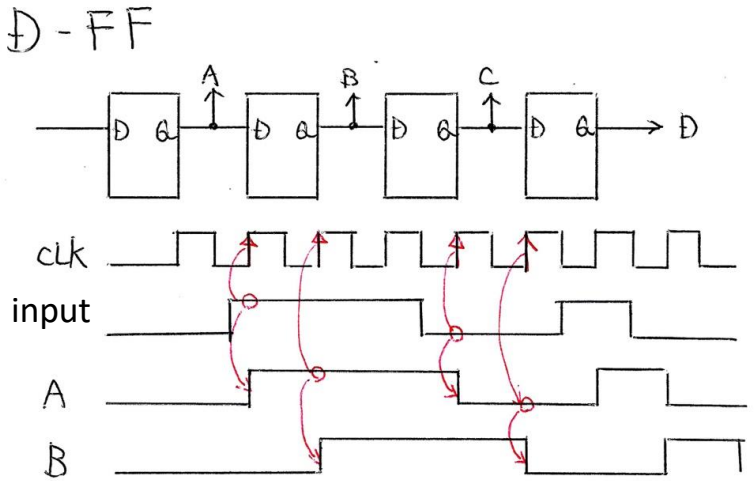
Jk/FF's CLK = $\overline{\text{D/FF's CLK}}$



D Flip-Flop Application

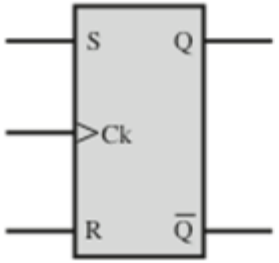
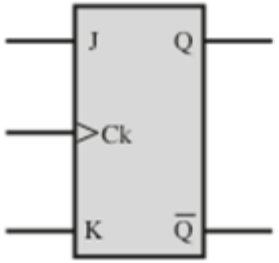
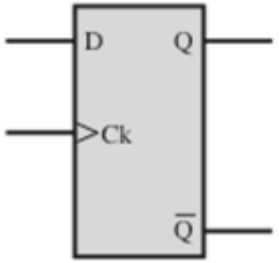


Application 1: Data Register



Application 2: Shift Register

Characteristic Table for FF

Name	Graphical Symbol	Characteristic Table
S-R		S R Q_{n+1} 0 0 Q_n 0 1 0 1 0 1 1 1 –
J-K		J K Q_{n+1} 0 0 Q_n 0 1 0 1 0 1 1 1 $\overline{Q_n}$
D		D Q_{n+1} 0 0 1 1

Summary

- Understand the difference between latches and flip-flops
- Understand the reason why
  - Transiting from SR to JK latches
  - Transiting from JK latch to master-slave JK flip-flop
- Understand what applications use SR latch and D flip-flop