Autumn 2022, Homework 7 (10 points in total)

Q1. (**5 pts**) **Memory devices** with 7 address lines, 8 data lines will be used in a memory system for a computer with the following specifications:

- 27-bit address bus, (where A1-A0 are used for a byte access in 8-data lines)
- 32-bit data bus, (which can access bytes, words, and long words)
- Memory at pages 0 to N

Answer the following questions, and show your work.

Q1-1. How many addressable memory locations are in each memory device?

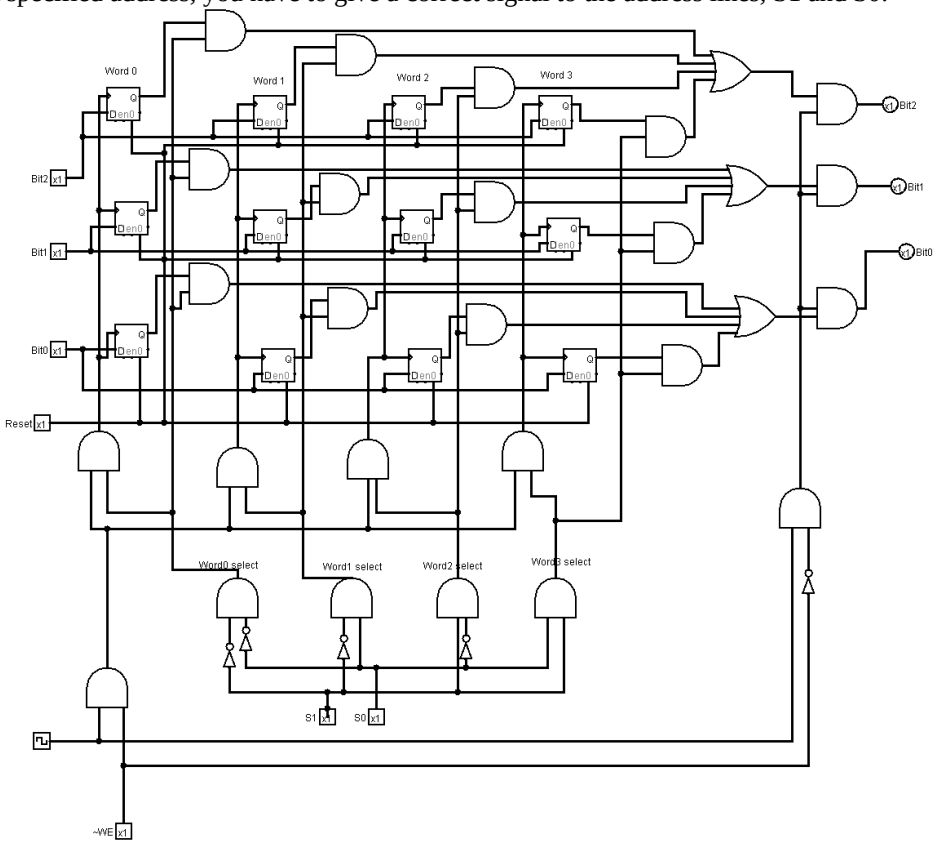
2^k = 2^7 = 128 memory locations

Q1-2. What is the total number of memory devices required in this memory design?

(2^25 * 32) / (2^7 * 8) = 1048576

Q2. (5 pts) Circuit and memory

The following circuit is a simple implementation for 4X3 memory chip. In this configuration, your memory chip has four addressable space and each data in the address is 3-bit long. In order to write/read a data into/from a specified address, you have to give a correct signal to the address lines, S1 and S0.



Q2-1. Suppose you want to write data 101 to word 3 (i.e., address 3). How will you set the values in each input signal listed in the following table?

NOTE: In general, "~WE" means that "low" signal asserts write enable, in other words "low" enables a write to memory. However, when you play with this Logisim example, you'll find that their logic is opposite!

RESET	S1	S0	Bit2	Bit1	Bit0	~WE
0	1	1	1	0	1	0

Q2-2. Suppose you want to read data from the address 1. Give the correct value to each input signal listed in the following table. If some bits do not affect, then mark as X (don't care).

RESET	S1	S0	Bit2	Bit1	Bit0	~WE
0	0	1	x	x	x	1

Note: Don't simulate this circuit with Logisim to fill out the above table. Their logic may behave in "high" enables rather than "low" enables.