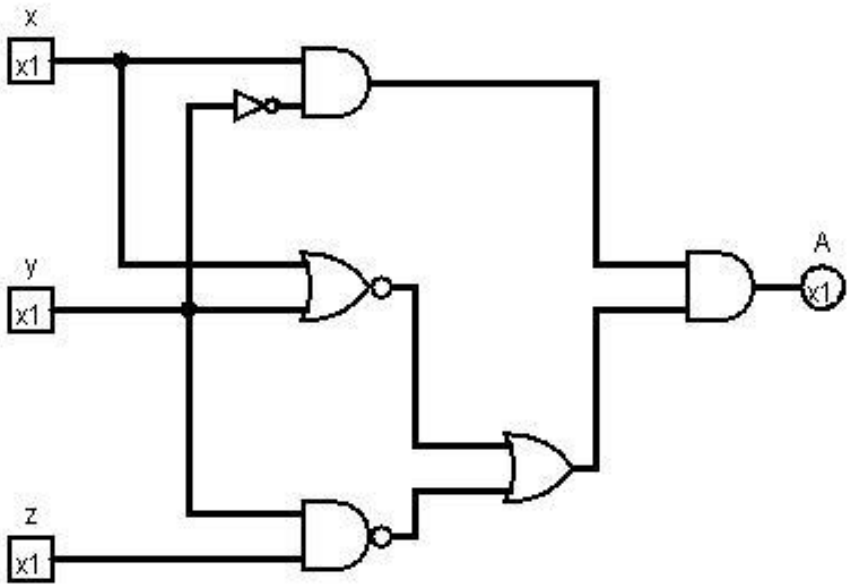
CSS 422, Spring 2022 (Peng), Final Exam Prep Questions

1. Consider the combinational circuit shown below



(1) Derive a Boolean equation for the output A. You don't need to simplify it.

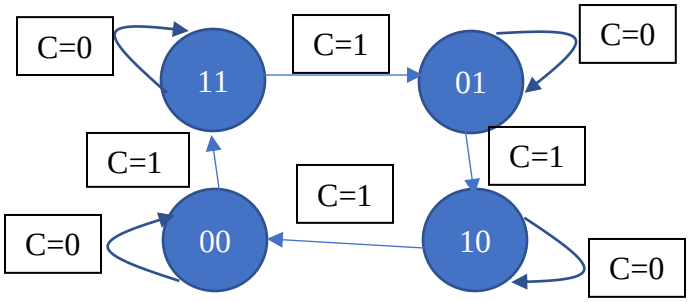
A = x~y (~(x+y) + ~(yz))

(2) Draw a truth table for the circuit.

X	Y	Z	A
0	**0**	**0**	**0**
0	**0**	**1**	**0**
0	**1**	**0**	**0**
0	**1**	**1**	**0**
1	**0**	**0**	**1**
1	**0**	**1**	**1**
1	**1**	**0**	**0**
1	**1**	**1**	**0**

2. This is a sequential circuit system with two flip-flops and one input signal C. The output of each flip-flop is named as A and B, respectively. The value of "AB" is considered a system state. The state changes as follows: if C is 0, the state does not change; if C is 1, the state changes in the order of 11, 01, 10, 00, and repeat. Please use JK flip-flops to design such a circuit with the required state changes.

(1) Draw a state diagram of the system.



(2) Construct a state transition table with JK FFs (you can ignore extra cells if unneeded).

	Input C = 0		Input C = 1		Input C = 0		Input C = 1		Input C = 0		Input C = 1	
Current state	Next state	Output	Next state	Output	Inputs to JK FF-A				Inputs to JK FF-B			
A_tB_t	$A_{t+1}B_{t+1}$	$A_{t+1}B_{t+1}$	$A_{t+1}B_{t+1}$	$A_{t+1}B_{t+1}$	JA	KA	JA	KA	JB	KB	JB	KB
00	**00**	**00**	**11**	**11**	**0**	**x**	**1**	**x**	**0**	**x**	**1**	**x**
01	**01**	**01**	**10**	**10**	**0**	**x**	**1**	**x**	**x**	**0**	**x**	**1**
10	**10**	**10**	**00**	**00**	**x**	**0**	**x**	**1**	**0**	**x**	**0**	**x**
11	**11**	**11**	**01**	**01**	**x**	**0**	**x**	**1**	**x**	**0**	**x**	**0**

(3) Based on the state transition table, for each output (the inputs for JK-FFs), draw K-maps and derive Boolean equations using K-maps. Make the equations as simple as possible.

K-map for JA: JA = C

	~A~B	~AB	AB	A~B
C	1	1	x	x
~C	0	0	x	x

K-map for KA: KA =C

	~A~B	~AB	AB	A~B
C	x	x	1	1
~C	x	x	0	0

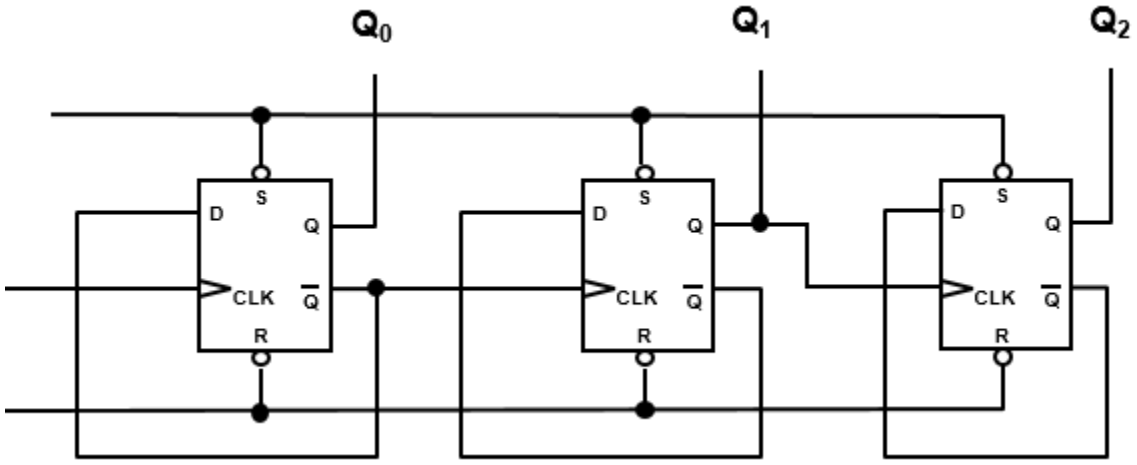
K-map for JB: JB = ~AC

	~A~B	~AB	AB	A~B
C	1	x	x	0
~C	0	x	x	0

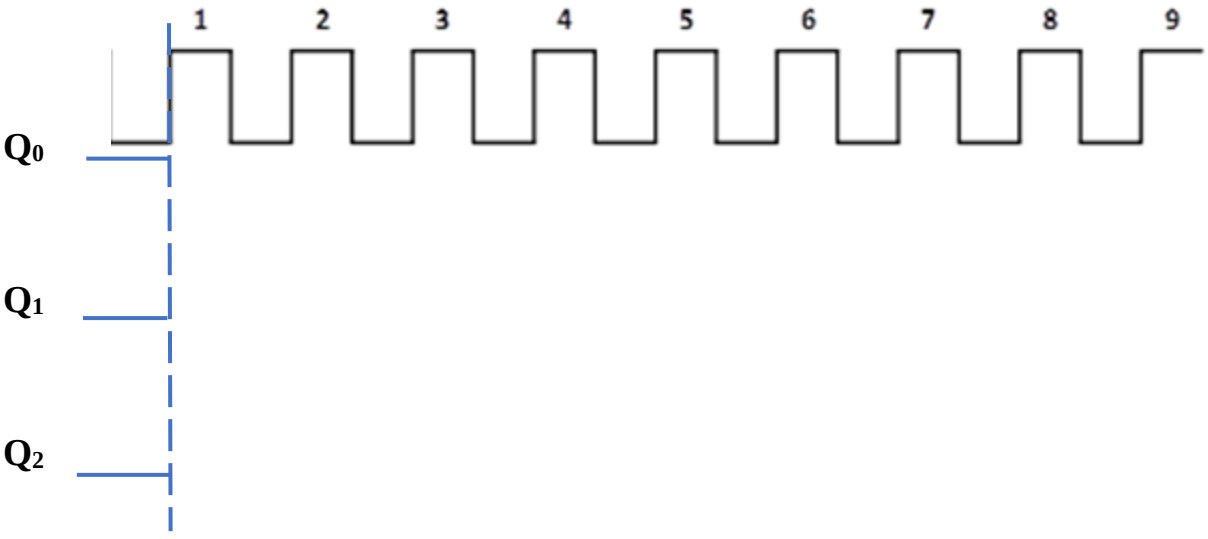
K-map for KB: KB = ~AC

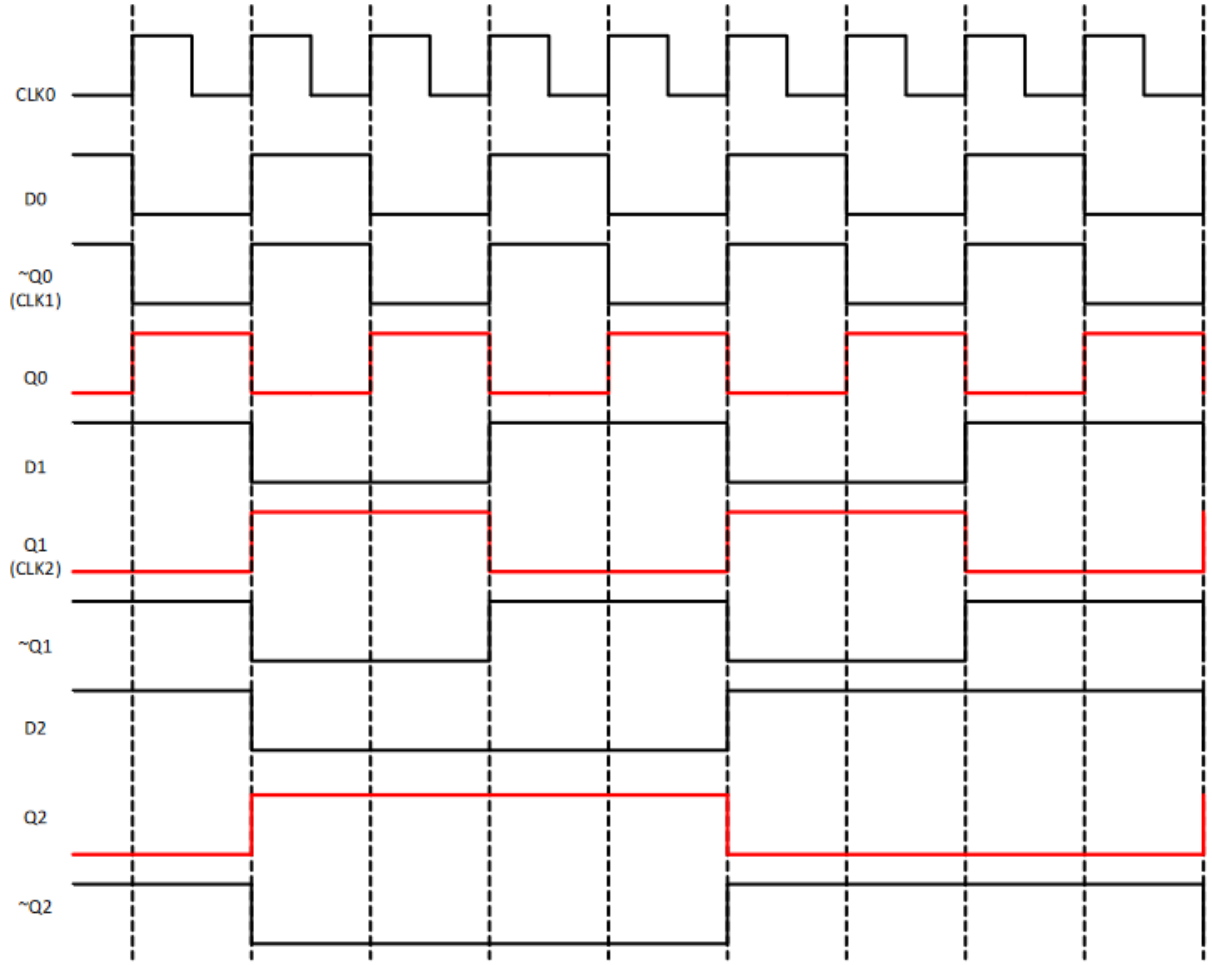
	~A~B	~AB	AB	A~B
C	x	1	0	x
~C	x	0	0	x

3. Given the following circuit, please analyze its behavior.
   You can assume Q2, Q1 and Q0 are all 0 before the first clock rising edge.
   NOTICE: Q2, Q1 and Q0 will start changing at the first clock rising edge as indicated by the dashed line!!! Pay attention to the last D-FF (Q2), which is connected differently!!!



(1) Express the signals as the clock wave forms.





(2) Please fill in the value of Q2, Q1 and Q0 in the following table.

Clock	Q2	Q1	Q0
1	**0**	**0**	**1**
2	**1**	**1**	**0**
3	**1**	**1**	**1**
4	**1**	**0**	**0**
5	**1**	**0**	**1**

6	**0**	**1**	**0**
7	**0**	**1**	**1**
8	**0**	**0**	**0**
9	**0**	**0**	**1**

4. A processor has an on-chip instruction cache with the following specifications:
    - The CPU clock frequency is 100 MHz.
    - The processor has 32-bit wide address and data busses.
    - The main memory uses all 32-bit address space, and each address can access one byte of data.
    - The instruction cache size is 256K bytes.
    - The instruction cache is organized as a direct-mapping cache.
    - The average cache hit rate is 99%.
    - Cache refill line = 128 bytes.
    - Instructions that are located in-cache execute in 1 clock cycle.
    - Instructions that are not found in the on-chip cache will cause the processor to stop all program execution and do a burst memory read access of one refill line from main memory to the cache.
    - Every burst access from main memory requires an address set-up time of 16 clock cycles, and then all subsequent burst fetches from main memory require 4 clock cycles per memory fetch.

    (1) What is the effective instruction execution time for this processor?

HR = 0.99, MR = 0.01
EET = 0.99*1C + 0.01 * (16 + 4*128/4) = 2.43CC
2.43CC * 10ns/CC = 24.3ns

(2) Divide the address bits of main memory into tag, block, and offset bits. After dividing the address bits, please tell what the tag, set, and offset are for the address $CDEF1234.

Offset bits: $\log_2 128 = 7$, block bits: $\log_2(256K/128) = 11$, tag bits: 32 – 7 – 11 = 14
0xCDEF1234 = 1100 1101 1110 1111 0001 0010 0011 0100
Tag value: 0x337B, block value: 0x624, offset value: 0x34.

(3) If the cache mapping function is change to fully associative mapping, and other specifications stay the same, please divide the address bits of main memory into tag and offset bits. After dividing the address bits, please tell what tag and offset are for the address $CDEF1234.

Offset bits: $\log_2 128 = 7$, tag bits: 32 – 7 = 25
0xCDEF1234 = 1100 1101 1110 1111 0001 0010 0011 0100
Tag value: 0x19BDE24, offset value: 0x34.

5. Suppose a microprocessor has 24-bit address bus and 32-bit wide data bus. Assume that this microprocessor will be connected to a memory system M that is built with a number of memory chips, each of which has a 256K address space and each address can access 8-bit data.
   (1) How many address lines and data lines does this microprocessor have?
   (2) How many bytes of memory the memory system M should have (The capacity of the memory system)?
   (3) How many memory chips are needed to satisfy the memory system's capacity needs?

24 address lines and 32 data lines

2^24 * 4B = 64MB

64MB/256KB = 256