Akuma Akuma-Ukpo
Hamza Lemsaddek
Lab 2

Lab 2 Report

Abstract: The goal was to develop VHDL models for a 4 to 1 multiplexor, 1-2^y demux, 4 and 8 bit shift registers and 4 bit adder/subtractor. By developing VHDL models for each circuit, we are able to understand dataflow within a bit calculator. By developing test benches for each architecture, we are able to offer almost real-time simulation of processes within the circuits.

Division of Labor:

- The components as listed above were 4 to 1 mux + test bench, 1-3^y demux + test bench, 4 bit shifter + test bench, 8 bit shifter + test bench , 4 bit adder / subtractor + test bench. Akuma was responsible for 4 to 1 mux, 4 and 8 bit shift registers along with their respective test benches while Hamza was responsible for Demux, adder/subtractor along with test benches.

Strategy:

- Since a VHDL test bench and behavioral templates were provided by the professor, we used the templates as a means to identify missing ports, signals and functions which we needed to implement in each calculator circuit. We identified logic for addition, shifting, subtraction and multiplication and compiled logic diagrams for each component. Moreover we identified ports, wires and signals in each of these diagrams and added them to our VHDL models. Demux and mux logic were derived from our truth tables
  e.g.

```
with sel select output <=
in1 when "00",
in2 when "01",
in3 when "10",
in4 when others;
```

  Our test benches were meant to test all possible cases and times for each simulation. We were able to observe real -time waveforms for each circuit and used this data to compare to our VHDL code.

  See attached waveforms and respective code snippets

Results:

- 4 bit mux performed as expected, it was difficult to observe output as first due to very small units in the waveform but we were able to adjust filters and observe 10ns clock cycles. Running our test-benches and processes allowed us to tweak inputs and observe corresponding changes in the waveform. Our 8 bit shifter had differences in clock speed possibly due to our implementation. Clock speed was slower by approximately 1 ns in comparison to the 4 bit shifter.

Conclusion:

Akuma Akuma-Ukpo
Hamza Lemsaddek
Lab 2

- The project took longer than expected. My team needed two additional days to complete the project due to work scheduling, unavailability during the holidays as well as exams and job interviews. We were able to simplify our VHDL logic enough to produce simple but efficient test cases. Our adder/subtractor was the biggest challenge because we were dealing with larger data and more complicated shifting /bit manipulation. We continuously ran into errors (syntax, dependencies) which we were unable to detect since we did not use a highly detailed IDE. Using the command line was fast but not as efficient when detecting errors in code.

Appendix 1:

- **Akuma – 12 hours**
- **Hamza – 11 hours**

Appendix II: All files have are in the attached zip

Appendix III: Test code and waveform files have been attached