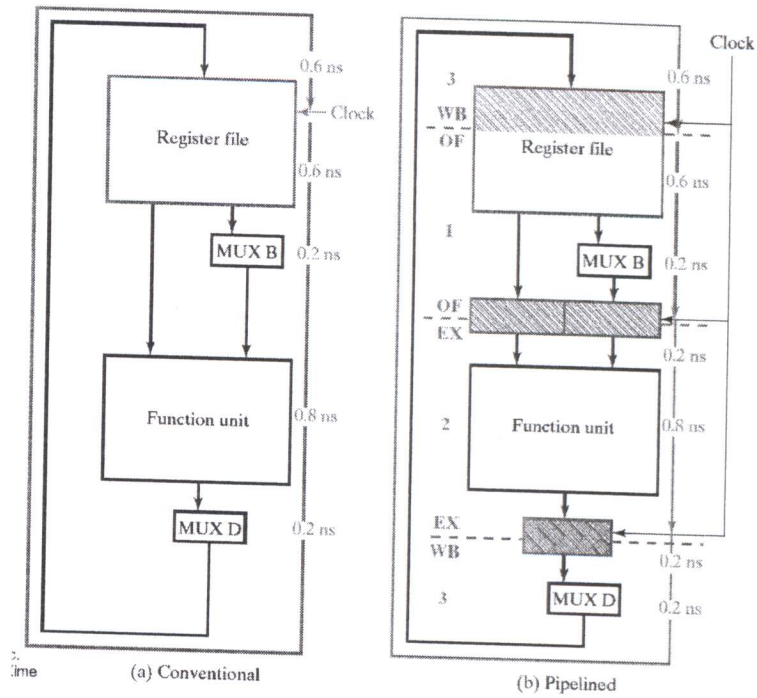
Student Name:

ROBT305 Embedded Systems Quiz #2

Collect 6 out of 7 points. Please provide precise answers.

1. The pipelined datapath is similar to the one in Fig (b) with the delays **from top to bottom** replaced by the following values: 0.5 ns, 0.5 ns, 0.1 ns, 0.1 ns, 0.7 ns, 0.1 ns and 0.1 ns.
   a) Define the maximum clock frequency **(1 point)**



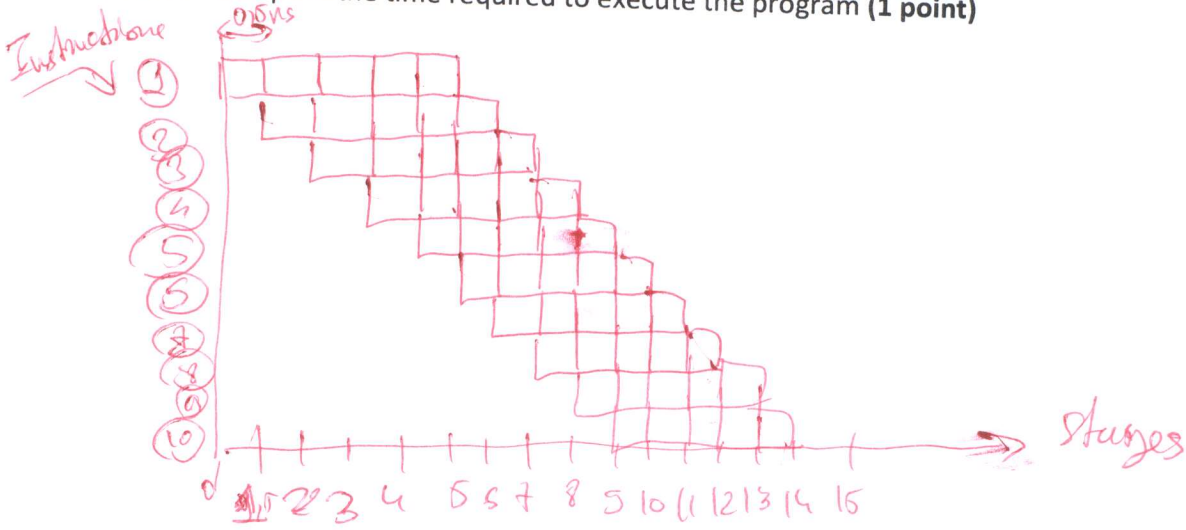
$t = 0{,}8$ ns – longest time for one of the stages

max frequency $= \frac{1}{0{,}8\text{ ns}} = 1{,}25$ GHz

b) Using the maximum clock frequency from a) define the latency time (time to process an instruction) in the pipelined datapath **(1 point)**

3 stages × 0,8 ns/stage = 2,4 ns – time to process an instruction in 3 stages

2. A program consisting of a sequence of ten sequential instructions (e.g. without branch or jump instructions) is to be executed in a 5 stage pipelined RISC computer with a clock period of 0.5 ns. Compute the time required to execute the program **(1 point)**

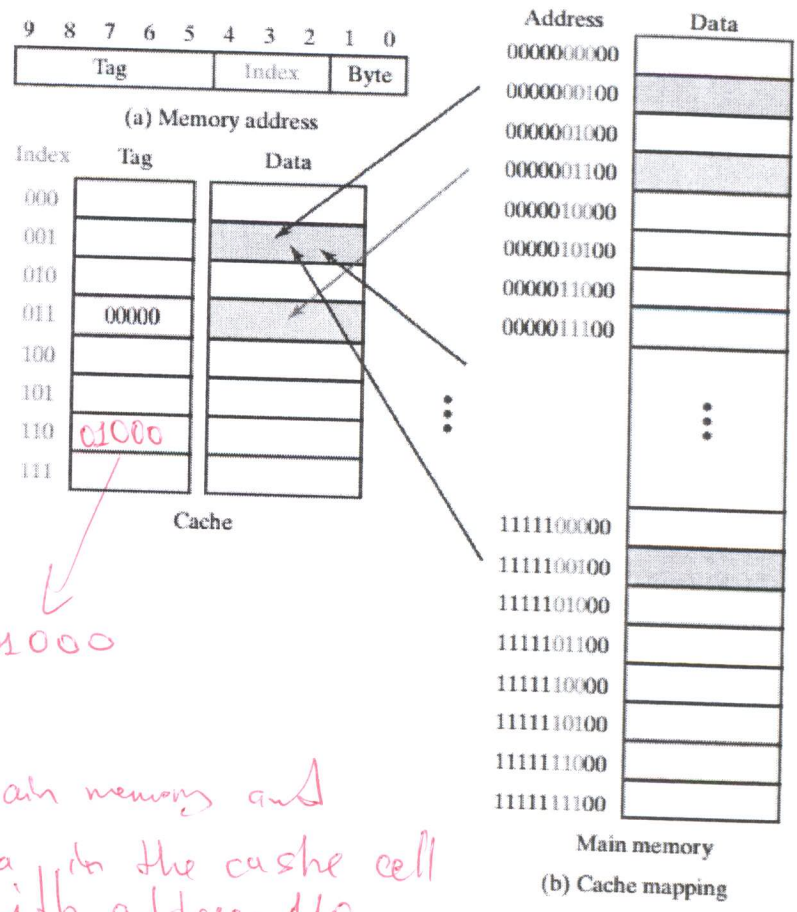


14 stages × 0,5 ns = 7 ns

3. Describe by your own worlds, how a processor handles an interrupt request? **(1 point)**

See slides, textbook

4. In the cashe memory example, assume that the cashe cell with index 110 contains tag 01000. Describe by your own worlds how CPU will fetch an instruction with memory address 0110011000 **(1 points)**



memory address

0110011000

tag | cache index

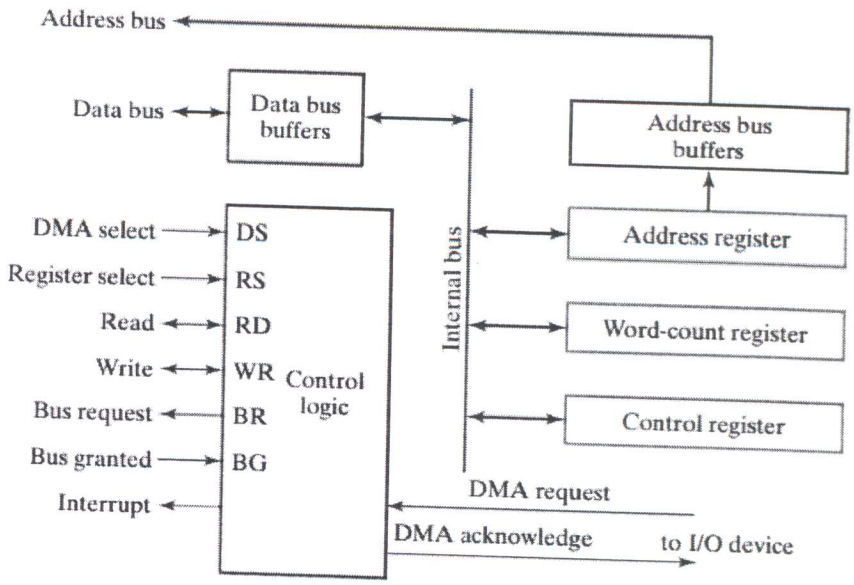
of desired instruction ∴ 01100 ≠ 01000

CPU retrieves data from main memory and rewrites tag and data in the cashe cell with address 110.

5. What is the watchdog timer? **(1 points)**

See slides, textbook

6. Explain the operation of the DMA controller below. **(1 point)**



See slides, textbook