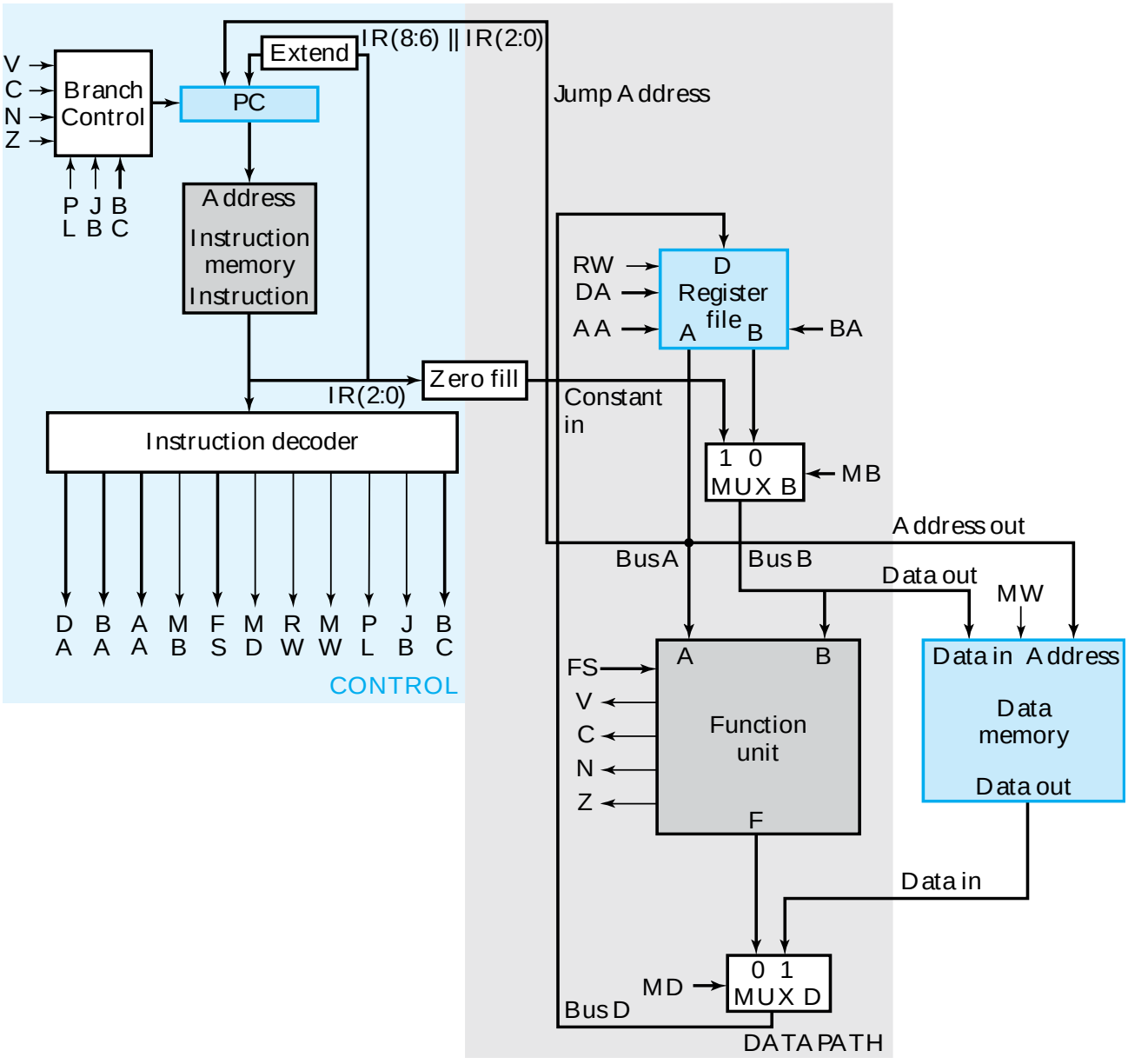
Student Name:

ROBT305 Embedded Systems Quiz #1

Please provide precise answers to the questions below. Collect 8 out 9 points

1. A block diagram of a single cycle computer with 8 registers, the instruction set and a PC control combination table are given below. Complete the table below for executing instructions



PC Operation	PL	JB	BC
Count Up	0	X	X
Jump	1	1	X
Branch on Negative (else Count Up)	1	0	1
Branch on Zero (else Count Up)	1	0	0

Instruction	Opcode	Mne-monic	Format	Description	Status Bits
Move A	0000000	MOVA	RD, RA	R[DR] ← R[SA]*	N, Z
Increment	0000001	INC	RD, RA	R[DR] ← R[SA] + 1*	N, Z
Add	0000010	ADD	RD, RA, RB	R[DR] ← R[SA] + R[SB]*	N, Z
Subtract	0000101	SUB	RD, RA, RB	R[DR] ← R[SA] – R[SB]*	N, Z
Decrement	0000110	DEC	RD, RA	R[DR] ← R[SA] – 1*	N, Z
AND	0001000	AND	RD, RA, RB	R[DR] ← R[SA] ∧ R[SB]*	N, Z
OR	0001001	OR	RD, RA, RB	R[DR] ← R[SA] ∨ R[SB]*	N, Z
Exclusive OR	0001010	XOR	RD, RA, RB	R[DR] ← R[SA] ⊕ R[SB]*	N, Z
NOT	0001011	NOT	RD, RA	R[DR] ← $\overline{R[SA]}$ *	N, Z
Move B	0001100	MOVB	RD, RB	R[DR] ← R[SB]*	
Shift Right	0001101	SHR	RD, RB	R[DR] ← sr R[SB]*	
Shift Left	0001110	SHL	RD, RB	R[DR] ← sl R[SB]*	
Load Immediate	1001100	LDI	RD, OP	R[DR] ← zf OP*	
Add Immediate	1000010	ADI	RD, RA, OP	R[DR] ← R[SA] + zf OP*	N, Z
Load	0010000	LD	RD, RA	R[DR] ← M[SA]*	
Store	0100000	ST	RA, RB	M[SA] ← R[SB]*	
Branch on Zero	1100000	BRZ	RA, AD	if (R[SA] = 0) PC ← PC + se AD, if (R[SA] ≠ 0) PC ← PC + 1	N, Z
Branch on Negative	1100001	BRN	RA, AD	if (R[SA] < 0) PC ← PC + se AD, if (R[SA] ≥ 0) PC ← PC + 1	N, Z
Jump	1110000	JMP	RA	PC ← R[SA]	

Instruction-Register transfer	DA	AA	BA	MB	Opcode	MD	RW	MW	PL	JB	BC
M[R3] ← R4 **(1 point)**	XXX	011	100	0	0100000	X	0	1	0	X	X
R1←R3 – R2 **(1 point)**	001	011	010	0	0000101	0	1	0	0	X	X
if (R4<0) PC←PC + sePC else PC←PC + 1 **(2 points)**	XXX	100	XXX	X	1100001	X	0	0	1	0	1

2. A simple datapath similar to the one in question 1 has 64 registers. How many bit address lines are needed for selecting registers in the datapath? **(1 point)**

$2^6 = 64 \Rightarrow$ 6 bit address lines

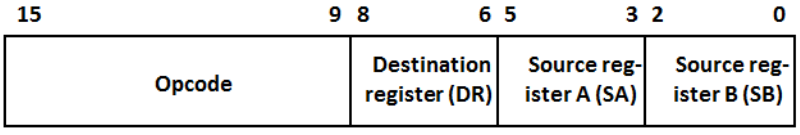
3. What is the purpose of the **Zero fill** block in the datapath. **(1 point)**

fill most significant bits with zeros because only 3 bits are in use, so total n-bit word is created for n-bit buses.

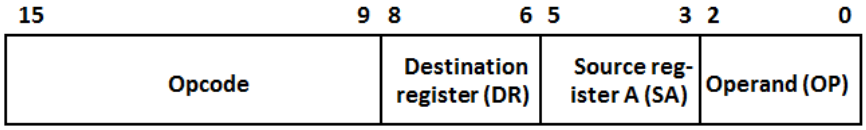
00...00 XXX

3 bit in registers

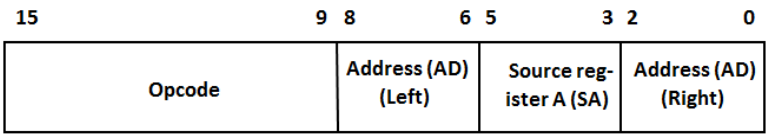
4. The format of different types of instructions for a simple computer with 8 registers each holding 16 bits is given below. The instruction set architecture is given in question 1



(a) Register



(b) Immediate



(c) Jump and Branch

At the beginning of the operation, PC has the decimal value 10. Initial values of the register file registers are given on the left. The operations executed at each cycle are given in the middle. Based on this information, fill the memory content as much as you can (assume the memory contains instructions and data). Explain your reasoning **(3 points).**

Register	Decimal Value
R0	21
R1	18
R2	20
R3	23
R4	4242
R5	2449
R6	15
R7	10

Operations:

1 LD R6, R1
2 LD R5, R2
3 DEC R5, R5
4 AND R4, R6, R5
5 ADI R4, R6, #4
6 ST R0, R4
7 JMP R7

1. R6 = 0000 1111 1111 0000
2. R5 = 0000 0000 0000 0010
3. R5 = 0000 0000 0000 0001
4. R4 = 0000 0000 0000 0000
5. R4 = 0000 1111 1111 0100

Decimal Memory Address	Memory Content
10	0010000 110 001 xxx
11	0010000 101 010 xxx
12	0000 110 101 101 xxx
13	000 1000 100 110 101
14	100 0010 100 110 100
15	0100000 xxx 000 100
16	111 0000 xxx 111 xxx
17	uknown
18	0000 1111 1111 0000
19	uknown
20	0000 0000 0000 0010
21	0000 1111 1111 0100

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