TECHNISCHE UNIVERSITÄT WIEN
Vienna | Austria

Runtime Modul Power Monitoring

SoC Lab - Final Presentation WS2020

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Motivation

Why dynamic Power Monitoring?

- Static power analysis may not sufficient for dynamic application

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Why Modul Power Monitoring?

- Decoupling the module power from the overall system
- Analysis of individual modules possible

Goals

Development of a design that:

- monitors the dynamic power consumption of a specified module

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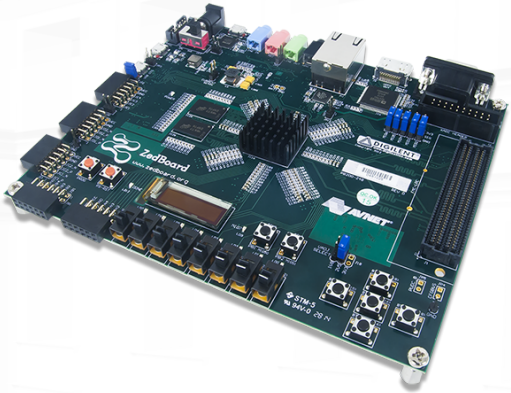
- transmits the current power value out of the Embedded System for further usage

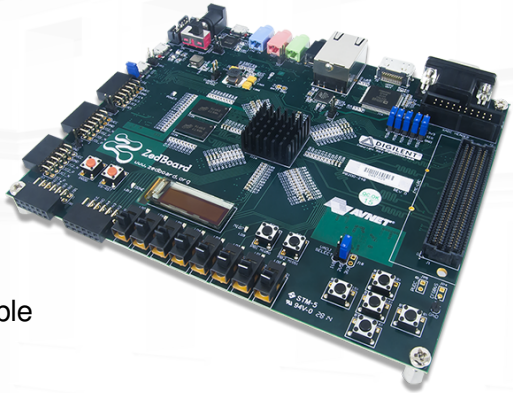


[Picture: https://www.mouser.at]

Goals

Development of a design that:

- monitors the dynamic power consumption of a specified module
- transmits the current power value out of the Embedded System for further usage
- should consume as less power as possible



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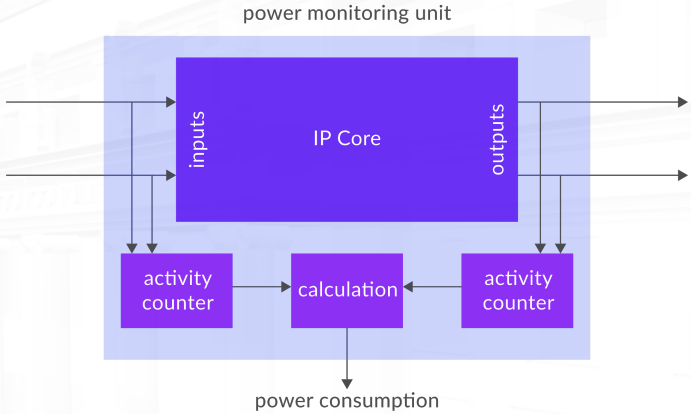
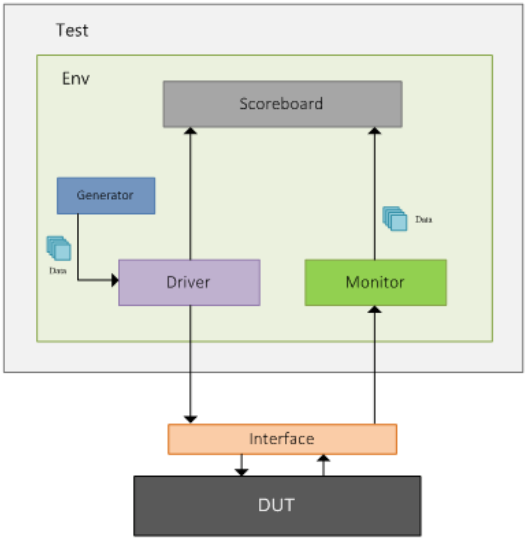
Project structure



Description

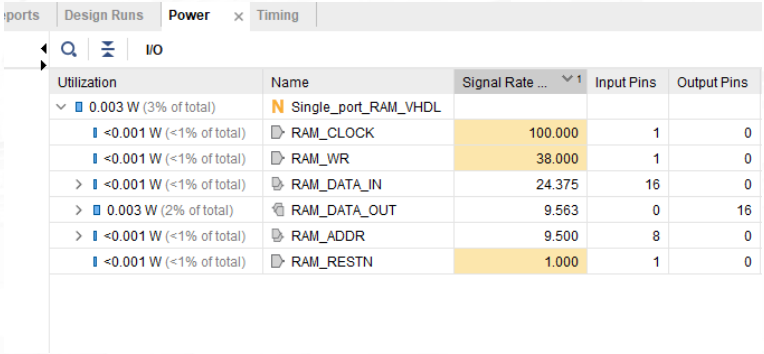
Important design aspects:

- Testbench



Description

Power Report



ports | Design Runs | Power | Timing

I/O

Utilization	Name	Signal Rate ...	Input Pins	Output Pins
0.003 W (3% of total)	Single_port_RAM_VHDL			
<0.001 W (<1% of total)	RAM_CLOCK	100.000	1	0
<0.001 W (<1% of total)	RAM_WR	38.000	1	0
<0.001 W (<1% of total)	RAM_DATA_IN	24.375	16	0
0.003 W (2% of total)	RAM_DATA_OUT	9.563	0	16
<0.001 W (<1% of total)	RAM_ADDR	9.500	8	0
<0.001 W (<1% of total)	RAM_RESTN	1.000	1	0

Description

Important design aspects:

- Testbench
- Activity Counter

$$P_{dyn} = \sum_{i \in N} \alpha_i C_i V_{dd}^2 f$$

Description

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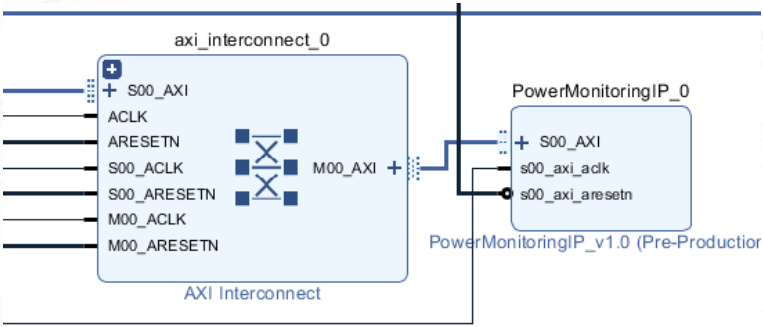

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- Testbench
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- Top design + AXI
- Embedded Application

Live Presentation

Challenges

- finding the significant signals for monitoring
  - difficult and highly design specific

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  - difficult and highly design specific
- finding the correct calculation parameters
  - precise knowledge about the implemented design needed (e.g. capacitance)
- keep the monitoring circuit as small as possible
  - the more accurate the calculation, the higher the needed resources will be


Questions ?