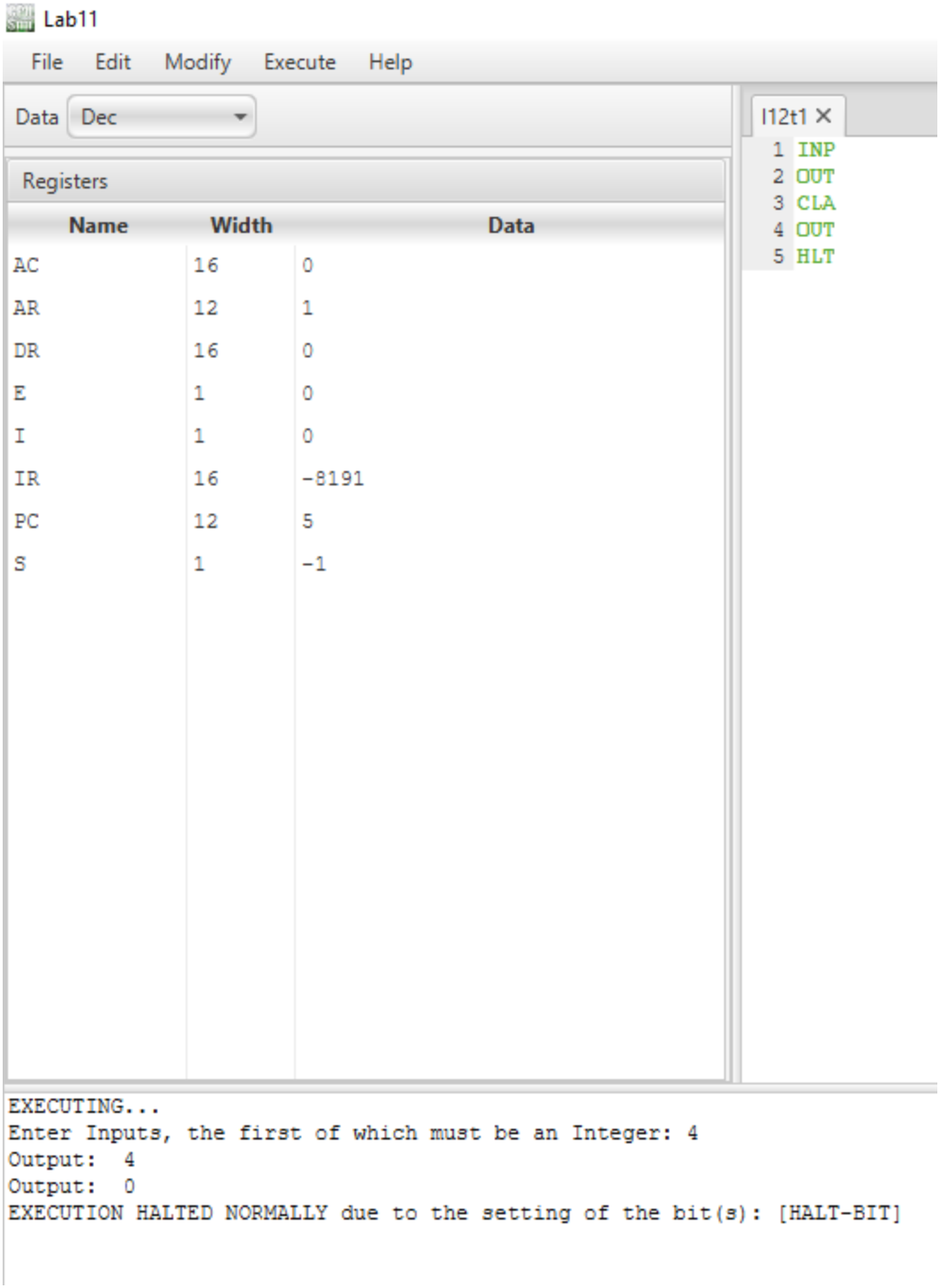
ALEENA SAEED

BSCS-4

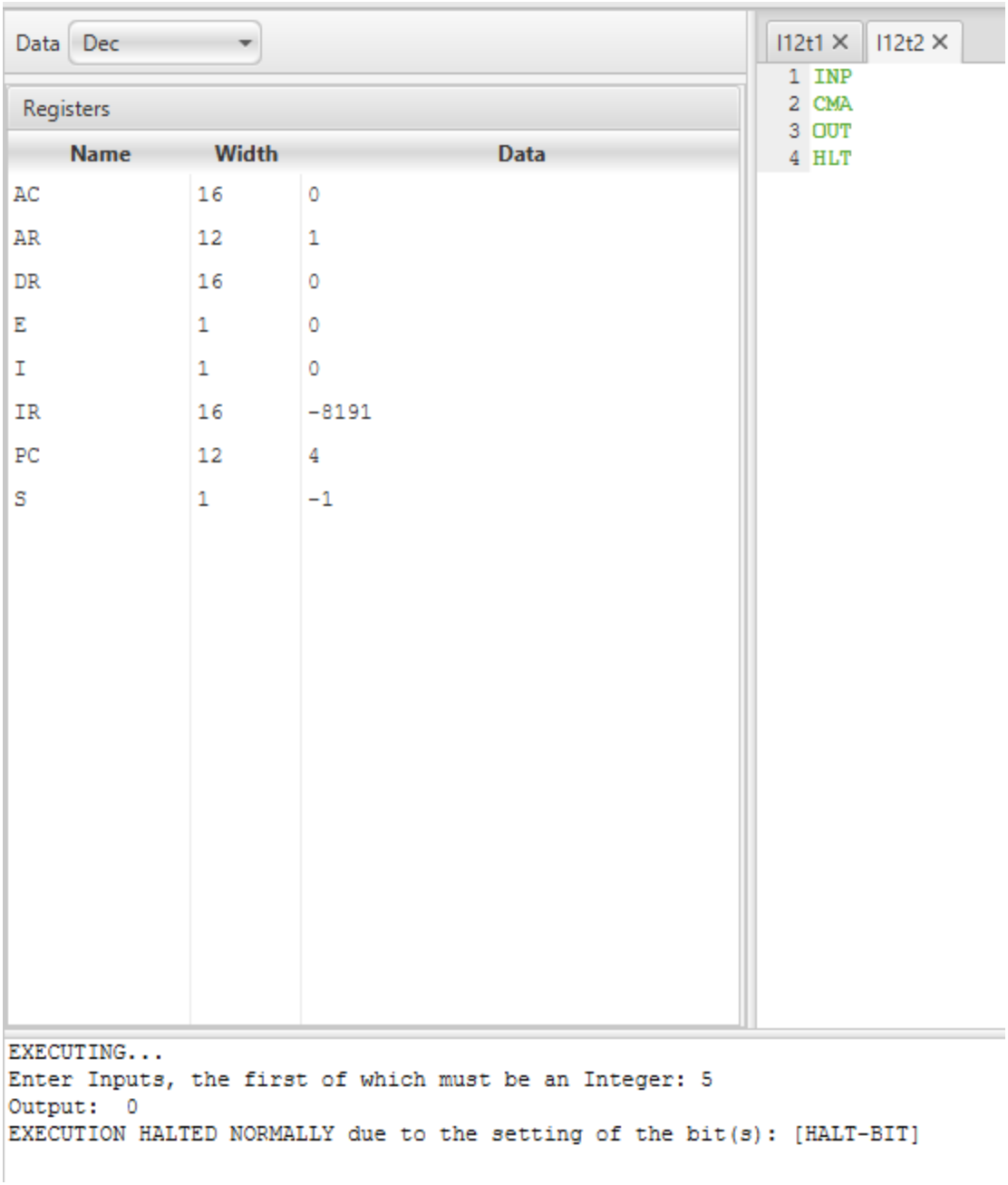
COMPUTER ARCHITECTURE _ LAB 12

56270

TASK 1:


Lab11
File Edit Modify Execute Help
Data Dec
Registers
Name Width Data
AC 16 0
AR 12 1
DR 16 0
E 1 0
I 1 0
IR 16 -8191
PC 12 5
S 1 -1
I12t1
1 INP
2 OUT
3 CLA
4 OUT
5 HLT
EXECUTING...
Enter Inputs, the first of which must be an Integer: 4
Output: 4
Output: 0
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]

TASK 2:


Data
Dec
Registers
Name
Width
Data
AC 16 0
AR 12 1
DR 16 0
E 1 0
I 1 0
IR 16 -8191
PC 12 4
S 1 -1
I12t1
I12t2
1 INP
2 CMA
3 OUT
4 HLT
EXECUTING...
Enter Inputs, the first of which must be an Integer: 5
Output: 0
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]

TASK 3:

Data Dec

Registers

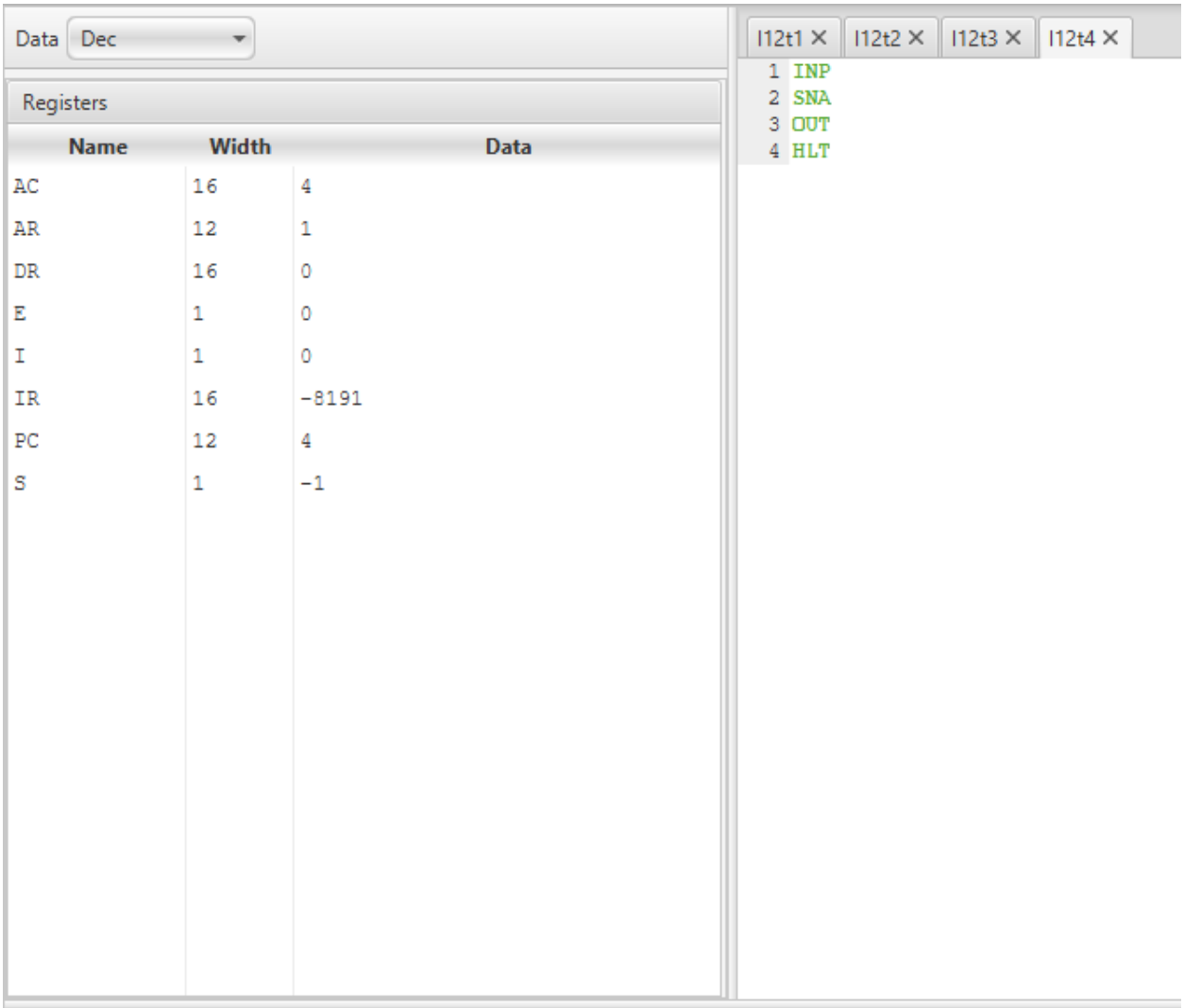
Name	Width	Data
AC	16	7
AR	12	1
DR	16	0
E	1	0
I	1	0
IR	16	-8191
PC	12	4
S	1	-1

I12t1 × I12t2 × I1

```
1 INP
2 INC
3 OUT
4 HLT
```

```
EXECUTING...
Enter Inputs, the first of which must be an Integer: 4
Output:  7
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

TASK 4:


Data
Dec
Registers
Name
Width
Data
AC 16 4
AR 12 1
DR 16 0
E 1 0
I 1 0
IR 16 -8191
PC 12 4
S 1 -1
I12t1
I12t2
I12t3
I12t4
1 INP
2 SNA
3 OUT
4 HLT
EXECUTING...
Enter Inputs, the first of which must be an Integer: 4
Output: 4
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]

TASK 5:

Data Dec

Registers

Name	Width	Data
AC	16	0
AR	12	1
DR	16	0
E	1	0
I	1	0
IR	16	-8191
PC	12	4
S	1	-1

I12t1 × I12t2 × I12t3 × I12t4 × I12t5 ×

```
1 INP
2 SPA
3 OUT
4 HLT
```

```
EXECUTING...
Enter Inputs, the first of which must be an Integer: 5
Output:  0
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```