Henry Ott Consultants

Electromagnetic Compatibility Consulting and Training

PCB Stack-Up

Part 1. Introduction

PCB stack-up is an important factor in determining the EMC performance of a product. A good stack-up can be very effective in reducing radiation from the loops on the PCB (differential-mode emission), as well as the cables attached to the board (common-mode emission). On the other hand a poor stack-up can increase the radiation from both of these mechanisms considerably.

Four factors are important with respect to board stack-up considerations:

1. The number of layers,
2. The number and types of planes (power and/or ground) used,
3. The ordering or sequence of the layers, and
4. The spacing between the layers.

Usually not much consideration is given except as to the number of layers. In many cases the other three factors are of equal importance. Item number four is sometimes not even known by the PCB designer. In deciding on the number of layers, the following should be considered:

1. The number of signals to be routed and cost,
2. Frequency,
3. Will the product have to meet Class A or Class B emission requirements,
4. Will the PCB be in a shielded or unshielded enclosure, and
5. The EMC engineering expertise of the design team.

Often only the first item is considered. In reality all the items are of critical importance and should be considered equally. If an optimum design is to be achieved in the minimum amount of time and at the lowest cost, the last item can be especially important and should not be ignored.

Multi-layer boards using ground and/or power planes provide significant reduction in radiated emission over two layer PCBs. A rule of thumb, that is often used, is that a four-layer board will produce 15 dB less radiation than a two-layer board, all other factors being equal. Boards containing planes are much better than those without planes for the following reasons:

1. They allow signals to be routed in a microstrip (or stripline) configuration. These configurations are controlled impedance transmission lines with much less radiation than the random traces used on a two-layer board.
2. The ground plane decreases the ground impedance (and therefore the ground noise) significantly.

Although two-layer boards have been used successfully in unshielded enclosures at 20 to 25 MHz, these cases are the exception rather than the rule. Above about ten or fifteen MHz, multi-layer boards should normally be considered.

When using multi-layer boards there are **five objectives** that you should try to achieve. They are:

1. A signal layer should always be adjacent to a plane.
2. Signal layers should be tightly coupled (close) to their adjacent planes.
3. Power and Ground planes should be closely coupled together.
4. High-speed signals should be routed on buried layers located between planes. In this way the planes can act as shields and contain the radiation from the high-speed traces.
5. Multiple ground planes are very advantageous, since they will lower the ground (reference plane) impedance of the board and reduce the common-mode radiation..

Often we are faced with the choice between close signal/plane coupling (objective #2) and close power plane/ground plane coupling (objective #3). With normal PCB construction techniques, there is not sufficient inter-plane capacitance between the adjacent power and ground planes to provide adequate decoupling below about 500 MHz. The decoupling, therefore, will have to be taken care of by other means and we should usually opt for tight coupling between the signal and the current return plane. The advantages of tight coupling between the signal (trace) layers and the current return planes will more than outweigh the disadvantage caused by the slight loss in interplane capacitance.

An eight-layer board is the fewest number of layers that can be used to achieve all five of the above objectives. On four and six layer board some of the above objectives will have to be compromised. Under those conditions you will have to determine which objectives

are the most important to the design at hand.

The above paragraph should not be construed to mean that you can't do a good EMC design on a four- or six-layer board, because you can. It only indicates that all the objectives cannot be met simultaneously and some compromise will be necessary. Since all the desired EMC objectives can be met with an eight-layer board, there is no reason for using more than eight layers other than to accommodate additional signal routing layers.

Another desirable objective, from a mechanical point of view, is to have the cross section of the board symmetrical (or balanced) in order to prevent warping. For example, on an eight-layer board if layer two is a plane, then layer seven should also be a plane. Therefore, all the configurations presented here use symmetrical, or balanced, construction. If a non-symmetrical, or unbalanced, construction is allowed additional stack-up configurations are possible.

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Return to top of page.

Return to HOC home page.

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Part 2. Four-Layer Boards

The most common four-layer board configuration is shown in Fig. 1 (power and ground planes may be reversed). It consists of four uniformly spaced layers with internal power and ground planes. The two external trace layers usually have orthogonal trace routing directions.

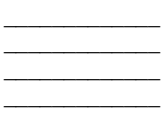


Figure 1

Although this configuration is significantly better than a two-layer board, it has a few, less that ideal characteristics. With respect to the list of objectives in Part 1, this stack-up only satisfies objective (1). If the layers are equally spaced, there is a large separation between the signal layer and the current return plane. There is also a large separation between the power and ground planes. With a four-layer board we cannot correct both of these deficiencies at the same time; therefore, we must decide which is most important to us. As mentioned previously, with normal PCB construction techniques there is not sufficient inter-plane capacitance between the adjacent power and ground planes to provide adequate decoupling. The decoupling, therefore, will have to be taken care of by other means and we should opt for tight coupling between the signal and the current return plane. The advantages of tight coupling between the signal (trace) layers and the current return planes will more than outweigh the disadvantage caused by the slight loss in interplane capacitance.

Therefore, the simplest way to improve the EMC performance of a four-layer board is to space the signal layers as close to the planes as possible (<0.010"), and use a large core (>0.040") between the power and ground planes as shown in Fig. 2. This has three advantages and few disadvantages. The signal loop areas are smaller and therefore produce less differential mode radiation. For the case of 0.005" spacing (trace layer to plane layer), this can amount to 10 dB or more reduction in the trace loop radiation compared a stack-up with equally spaced layers. Secondly, the tight coupling between the signal trace and the ground plane reduces the plane impedance (inductance) hence reducing the common-mode radiation from the cables connected to the board. Thirdly, the close trace to plane coupling will decrease the crosstalk between traces. For a fixed trace to trace spacing the crosstalk is proportional to the square of the trace height. This is one of the simplest, least costly, and most overlooked method of reducing radiation on a four-layer PCB. With this configuration we have satisfied both objectives (1) and (2).

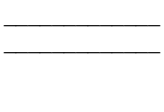


Figure 2

What other possibilities are there for a four-layer board stack-up? Well, we could become a little **non-conventional** and reverse the signal layers and the plane layers in Fig. 2, producing the stack-up shown in Fig 3a.

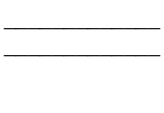


Figure 3a

The major advantage of this stack-up is that the planes on the outer layers provide shielding to the signal traces on the inner layers. The disadvantages are that the ground plane may be cut-up considerably with component mounting pads on a high density PCB. This can be alleviated somewhat, by reversing the planes and placing the power plane on the component side, and the ground plane on the other side of the board. Secondly, some people don't like to have an exposed power plane and thirdly, the buried signal layers make board rework difficult if not impossible. This stack-up satisfies objectives (1), (2), and partially satisfies objective (4).

Two of these three problems can be alleviated with the stack-up shown in Fig. 3b, where the two outer planes are ground planes and power is routed as a trace on the signal planes. The power should be routed as a grid, using wide traces, on the signal layers. Two added advantages of this configuration are that; (1) the two ground planes produce a much lower ground impedance and hence less common-mode cable radiation, and (2) the two ground planes can be stitched together around the periphery of the board to enclose all the signal traces in a faraday cage. From an EMC point of view this configuration, if properly done, is the best stack-up possible with a four-layer PCB. Now we have satisfied objectives, (1), (2), (4), and (5) while using only a four-layer board.

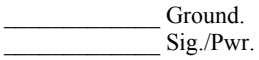
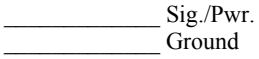


Figure 3b



A fourth possibility, not commonly used, but one that can be made to perform very well, is shown in Fig. 4. This is similar to Fig 2, but with the power plane replaced with a ground plane, and power routed as a trace on the signal layers.

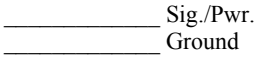
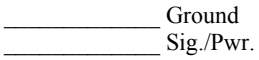


Figure 4



This stack-up overcomes the rework problem mentioned before, and still provides for the low ground impedance as a result of two ground planes. The planes however do not provide any shielding. This configuration satisfies objectives (1), (2), and (5) but not objectives (3) or (4).

So, as you can see there are more options available, than you might have originally thought, for four layer board stack-up. It is possible to satisfy four of our five objectives with a four layer PCB. The configurations of Figures 2, 3b, and 4 all can be made to perform well from an EMC point of view.

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Return to top of page.

Return to HOC home page.

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Part 3. Six-Layer Boards

Most six-layer boards consist of four signal routing layers and two planes. From an EMC perspective a six-layer board is usually preferred over a four-layer board.

One stack-up **NOT** to use on a six-layer board is the one shown in Figure 5. The planes provide no shielding for the signal layers, and two of the signal layers (1 and 6) are not adjacent to a plane. The only time this arrangement works even moderately well is if all the high frequency signals are routed on layers 2 and 5 and only very low frequency signals, or better yet no signals at all (just mounting pads), are routed on layers 1 and 6. If used, any unused area on layers 1 and 6 should be provided with "ground fill" and tied into the primary ground plane, with vias, at as many locations as possible.

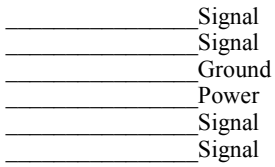

Figure 5

This configuration satisfies only one (number 3) of our original objectives.

With six layers available the principle of providing two buried layers for high-speed signals (as was done in Fig. 3) is easily implemented as shown in Fig. 6. This configuration also provides two surface layers for routing low speed signals.

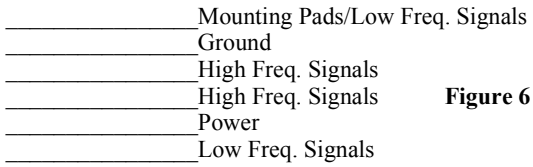

Figure 6

This is a probably the most common six-layer stack-up and can be very effective in controlling emissions, if done correctly. This configuration satisfies objectives 1, 2, & 4 but not objectives 3 & 5. Its main drawback is the separation of the power and ground planes. Due to this separation there is no significant interplane capacitance between power and ground Therefore, the decoupling must be designed very carefully to account for this fact. For more information on decoupling, see our Tech Tip on Decoupling.

Not nearly as common, but a good performing stack-up for a six-layer board is shown in Fig. 7.

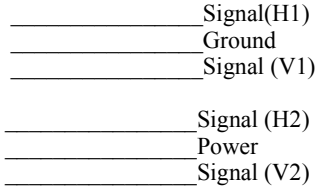

Figure 7

H1 indicates the horizontal routing layer for signal 1, and V1 indicates the vertical routing layer for signal 1. H2 and V2 represent the same for signal 2. This configuration has the advantage that orthogonal routed signals always reference the same plane. To understand why this is important see section on Changing Reference Planes in Part 6. The disadvantage is that the signals on layer one and six are not shielded. Therefore the signal layers should be placed very close to their adjacent planes, and the desired board thickness made up by the use of a thicker center core. Typical spacing for a 0.060" thick board might be

0.005"/0.005"/0.040"/0.005"/0.005". This configuration satisfies objectives 1 and 2, but not 3, 4, or 5.

Another excellent performing six-layer board is shown in Fig. 8. It provides two buried signal layers and adjacent power and ground planes and satisfies all five objectives. The big disadvantage, however, is that it only has two routing layers -- so it is not often used.

_____Ground/ Mounting Pads
_____Signal
_____Ground
_____Power
_____Signal
_____Ground

Figure 8

It is easier to achieve good EMC performance with a six-layer board than with a four-layer board. We also have the advantage of four signal routing layers instead of being limited to just two. As was the case for four-layer boards, it is possible to satisfy four of our five objectives with a six-layer PCB. All five objectives can be satisfied if we limit ourselves to only two signal routing layers. The configurations of Figures 6, 7, and 8 all can all be made to perform very well from an EMC point of view.

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Return to top of page.

Return to HOC home page.

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Part 4. Eight-Layer Boards

An eight-layer board can be used to add two more routing layers or to improve EMC performance by adding two more planes. Although we see examples of both cases, I would say that the majority of eight layer board stack-ups are used to improve EMC performance rather than add additional routing layers. The percentage increase in cost of an eight-layer board over a six-layer board is less than the percentage increase in going from four to six layers, hence making it easier to justify the cost increase for improved EMC performance. Therefore, most eight-layer boards (and all the ones that we will concentrate on here) consist of four wiring layers and four planes.

An eight-layer board provides us, for the first time, the opportunity to easily satisfy all of the five originally stated objectives. Although there are many stack-ups possible, we will only discuss a few of them that have proven themselves by providing excellent EMC performance. As stated above, eight layers is usually used to improve the EMC performance of the board, not to increase the number of routing layers.

An eight-layer board with six routing layers is definitely **not** recommended, no matter how you decide to stack-up the layers. If you need six routing layers you should be using a ten-layer board. Therefore, an eight-layer board can be thought of as a six-layer board with optimum EMC performance.

The basic stack-up of an eight-layer board with excellent EMC performance is shown in Fig 9.

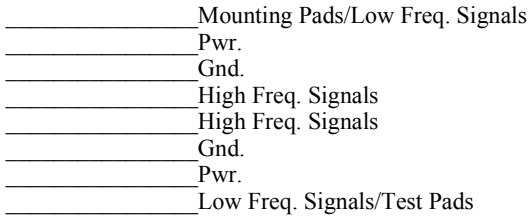

Figure 9

This configuration satisfies all the objectives listed in Part 1. All signal layers are adjacent to planes, and all the layers are closely coupled together. The high-speed signals are buried between planes, therefore the planes provide shielding to reduce the emissions from these signals. In addition the board uses multiple ground planes, thus decreasing the ground impedance.

For best EMC performance and Signal Integrity, when high frequency signals change layers (e.g., from layer 4 to 5) you should add a ground-to-ground via between the two ground planes, near the signal via, in order to provide an adjacent return path for the current. See "Changing Reference Planes" in Part 6, (**Return Path Discontinuties**) for a discussion of why this is important.

The stack-up in Fig. 9 can be further improved by using some form of embedded PCB capacitance technology (e.g. Zycon Buried Capacitanceú) for layers 2-3 and 6-7. For more information on embedded PCB capacitance technology, see our **Tech Tip on Decoupling**. This approach provides a significant improvement in the high frequency decoupling and may allow the use of significantly fewer discrete decoupling capacitors.

Another excellent configuration, and one of my favorite, is shown in Figure 10. This configuration is similar to that of Fig. 7 but includes two outer layer ground planes. With this arrangement all routing layers are buried between planes and are therefore shielded.

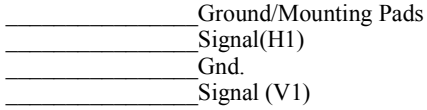

Figure 10

_____Signal (H2)
_____Pwr.
_____Signal (V2)
_____Ground/Mounting pads if double sided surface mount

H1 indicates the horizontal routing layer for signal 1, and V1 indicates the vertical routing layer for signal 1. H2 and V2 represent the same for signal 2. Although not commonly used this configuration also satisfies all the five objectives presented previously, and has the added advantage of routing orthogonal signals adjacent to the same plane. To understand why this is important see the section on **Return Path Discontinuites**. Typical layer spacing for this configuration might be 0.010"/0.005"/0.005"/0.20"/0.005"/0.005"/0.010"

Another possibility for an eight-layer board is to modify Fig. 10 by moving the planes to the center as shown in Fig. 11. This has the advantage of having a tightly coupled power-ground plane pair at the expense of not being able to shield the traces.

_____Signal(H1)
_____Gnd.
_____Signal (V1)

_____Gnd.
_____Pwr.

Figure 11

_____Signal (H2)
_____Gnd.
_____Signal (V2)

This is basically an eight-layer version of Fig. 7. It has all the advantages listed for Fig. 7, plus a tightly coupled power-ground plane pair in the center. Typical layer spacing for this configuration might be 0.006"/0.006"/0.015"/0.006"/0.015"/0.006"/0.006." This configuration satisfies objectives 1 and 2, 3, and 5, but not 4. This is an excellent performing configuration with good signal intergity and is often preferred over the stack-up of Figure 10 because of the tightly coupled power/ground planes. One of my favorites.

The stack-up in Fig. 11 can be further improved by using some form of **embedded PCB capacitance** technology (e.g. Zycon Buried Capacitanceú) for layers 4-5.

There is very little EMC advantage to use a board with more than eight layers. More that eight layers is usually used only when additional layers are required for signal trace routing. If six routing layers are needed, a ten-layer board should be used.

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Return to top of page.

Return to HOC home page.

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September 13, 2004

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Part 5. Ten-Layer Boards

A ten-layer board should be used when six routing layers are required. Ten-layer boards, therefore, usually have six signal layers and four planes. Having more than six signal layers on a ten-layer board is **not** recommended. Ten-layers is also the largest number of layers that can usually be conveniently fabricated in a 0.062" thick board. Occasionally you will see a twelve-layer board fabricated as a 0.062" thick board, but the number of fabricators capable of producing it are limited..

High layer count boards (ten +) require thin dielectrics (typically 0.006" or less on a 0.062" thick board) and therefore they automatically have tight coupling between layers. When properly stacked and routed they can meet all of our objectives and will have excellent EMC performance and signal integrity.

A very common and nearly ideal stack-up for a ten-layer board is shown in Figure 12. The reason that this stack-up has such good performance is the tight coupling of the signal and return planes, the shielding of the high-speed signal layers, the existence of multiple ground planes, as well as a tightly coupled power/ground plane pair in the center of the board. High-speed signals normally would be routed on the signal layers buried between planes (layers 3-4 and 7-8 in this case).

_____Signal (low-speed signals)
_____Gnd.
_____Signal (high-speed signals & clocks)
_____Signal (high-speed signals & clocks)
_____Pwr.
_____Gnd.
_____Signal (high-speed signals & clocks)
_____Signal (high-speed signals & clocks)
_____Gnd. or Pwr.
_____Signal (low-speed signals)

Figure 12

The common way to pair orthogonally routed signals in this configuration would be to pair layers 1 & 10 (carrying only low-frequency signals), as well as pairing layers 3 & 4, and layers 7 & 8 (both carrying high-speed signals). By paring signals in this manner, the planes on layers 2 and 9 provide shielding to the high-frequency signal traces on the inner layers. In addition the signals on layers 3 & 4 are isolated from the signals on layers 7 & 8 by the center power/ground plane pair. For example, high-speed clocks might be routed on one of these pairs, and high-speed address and data buses routed on the other pair. In this way the bus lines are protected, against being contaminated with clock noise, by the intervening planes.

This configuration satisfies all of the five original objectives.

Another possibility for routing orthogonal signals on the ten-layer board shown in Fig. 12 is to pair layers 1 & 3, layers 4 & 7, and layers 8 & 10. In the case of layer pairs 1 & 3 as well as 8 & 10, this has the advantage of routing orthogonal signals with reference to the same plane. The disadvantage, of course, is that if layers 1 and/or 10 have high frequency signals on them there is no inherent shielding provided by the PCB planes. Therefore, these signal layers should be placed very close to their adjacent plane (which occurs naturally in the case of a ten-layer board).

Each of the routing configurations discussed above has some advantages and some disadvantages, either can be made to provide good EMC and signal integrity performance if laid out carefully.

The stack-up in Fig. 12 can be further improved on by the use of some form of **embedded PCB capacitance** technology (e.g. Zycon Buried Capacitanceú) for layers 5 and 6, thereby improving the high-frequency power/ground plane decoupling,

Fig. 13 shows another possible stack-up for a ten-layer board.

_____Ground/Mounting Pads
_____Signal (H1)
_____Signal (V1)
_____Ground
_____Signal (H2)
_____Signal (V2)
_____Power
_____Signal (H3)
_____Signal (V3)
_____Ground/Mounting pads if double sided surface mount

Figure 13

This configuration gives up the closely spaced power/ground plane pair. In return it provides three signal- routing-layer pairs shielded by the ground planes on the outer layers of the board, and isolated from each other by the internal power and ground plane. All signal layers are shielded and isolated from each other in this configuration. The stack-up of Fig. 13 is very desirable if you have very few low-speed signals to put on the outer signal layers (as in Fig. 12) and most of your signals are high-speed, since it provides three pairs of shielded signal routing layers.

One concern with this stack-up relates to how badly the outside ground planes will be cut-up by the component mounting pads and vias on a high density PCB. This issue has to be addressed and the outside layers carefully laid out.

This configuration satisfies objectives 1, 2, 4, and 5, but not 3.

A third possibility is shown in Fig. 14. This stack-up allows the routing of orthogonal signals adjacent to the same plane, but in the process also has to give up the closely spaced power/ground planes. This configuration is similar to the eight-layer board shown in Fig. 10, with the addition of the two outer low-frequency routing layers.

_____Signal (low-speed signals)
_____Pwr.
_____Signal (H1)
_____Gnd.
_____ Signal (V1)
_____ Signal (H2)
_____Gnd.
_____Signal (V2)
_____Gnd. or Pwr.
_____Signal (low-speed signals)

Figure 14

The configuration in Fig. 14 satisfies objectives 1, 2, 4, and 5, but not 3. It, however, has the additional advantage that orthogonal routed signals always reference the same plane.

The stack-up in Fig. 14 can be further improved by the use of some form of **embedded PCB capacitance** technology (e.g. Zycon Buried Capacitanceú) for layers 2 and 9 (thereby satisfying objective 3). This, however, effectively converts it to a twelve-layer board.

Summary

The previous sections have discussed various ways to stack-up high-speed, digital logic, PCBs having from four to ten layers. A good PCB stack-up reduces radiation, improves signal quality, and helps aid in the decoupling of the power bus. No one stack-up is best, there is a number of viable options in each case and some compromise of objectives is usually necessary.

In addition to the number of layers, the type of layer (plane or signal), and the ordering of the layers, the following factors are also very important in determining the EMC performance of the board:

- The layer spacing.
- The assigning of signal layer pairs for orthogonal routing of signals.
- The assignment of signals (clock, bus, high-speed, low-frequency, etc.) to which signal-routing-layer pairs.

This discussion on board stack-up has assumed a standard 0.062" thick board, with symmetrical cross-section, and conventional via technology. If blind, buried, or micro vias are considered, other factors come into play and additional board stack-ups not only become possible but in many cases desirable.

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Return to top of page.

Return to HOC home page.

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Part 6. Return Path Discontinuities

One of the keys in determining the optimum printed circuit board layout is to understand how and where the signal return currents actually flow. Most designers only think about where the signal current flows (obviously on the signal trace), and ignore the path taken by the return current. Of course, the fact that many designers think this way helps to keep EMC engineers employed

To address the above concern we must understand how high-frequency currents flow in conductors. First, **the lowest impedance return path is in a plane directly underneath the signal trace** (irrespective of whether this is a power or ground plane) since this provides the lowest inductance path. This also produces the smallest current loop area possible. Secondly, due to the "skin effect," high frequency currents cannot penetrate a conductor, and therefore, **at high-frequency all currents in conductors are surface currents**. This affect will occur at all frequencies above 30 MHz for 1 oz. copper layers in a PCB. Therefore, a plane in a PCB is really two conductors not one conductor. There will be a current on the top surface of the plane, and there can be a different current or no current at all on the bottom surface of the plane.

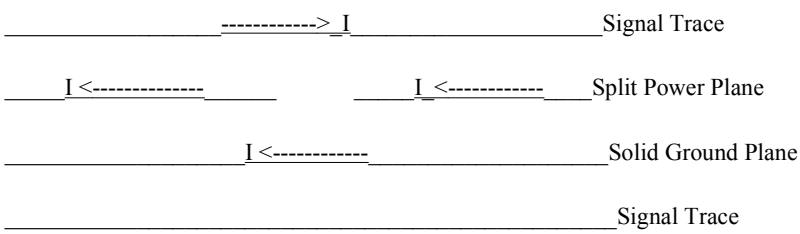
A major EMC problem occurs when there are discontinuities in the current return path. These discontinuities cause the return current to flow in larger loops, which increases the radiation from the board as well as increases the crosstalk between adjacent traces and causes waveform distortion. In addition in constant impedance PCBs the return path discontinuity will change the characteristic impedance of the trace. The most common return path discontinuities are discussed below.

Slots in Ground/Power Planes. When a trace crosses a slot in the adjacent power or ground plane, the return current is diverted from underneath the trace in order to go around the slot. This causes it to flow through a much bigger loop area. The longer the slot the bigger the loop area becomes. The most important thing that I can say about slots in ground planes, is don't have them! If you do have slots, make sure that no traces cross over them on adjacent layers.

If you absolutely must route a signal across a power or ground plane slot, place a few small stitching capacitors across the slot, one on either side of the trace (0.001 or 0.01 uF should be adequate). This will provide high-frequency continuity across the slot for the return current. To be effective the capacitors should be located within 0.1" of the trace.

For more information on slots in power/ground planes see our Tech Tip, **Slots in Ground Planes**.

Split Ground/Power Planes. When a trace crosses a split in the adjacent plane, as in the 4-layer board example shown below, the return current path is interrupted. The current must find another way to get across the split, which forces it to flow in a much bigger loop.



In the case shown above the current will divert to the nearest decoupling capacitor in order to cross over to the solid ground plane, then on the other side of the split the current must find another decoupling capacitor in order to return to the power plane that is adjacent to the trace. The interplane capacitance between the power and ground plane is too small to be effective except in the case of frequencies considerably above 500 MHz.

The best solution to this problem is to avoid crossing split planes with critical signal traces. In the case of the above example the signal should have been routed on the bottom signal layer since that was adjacent to the solid ground plane.

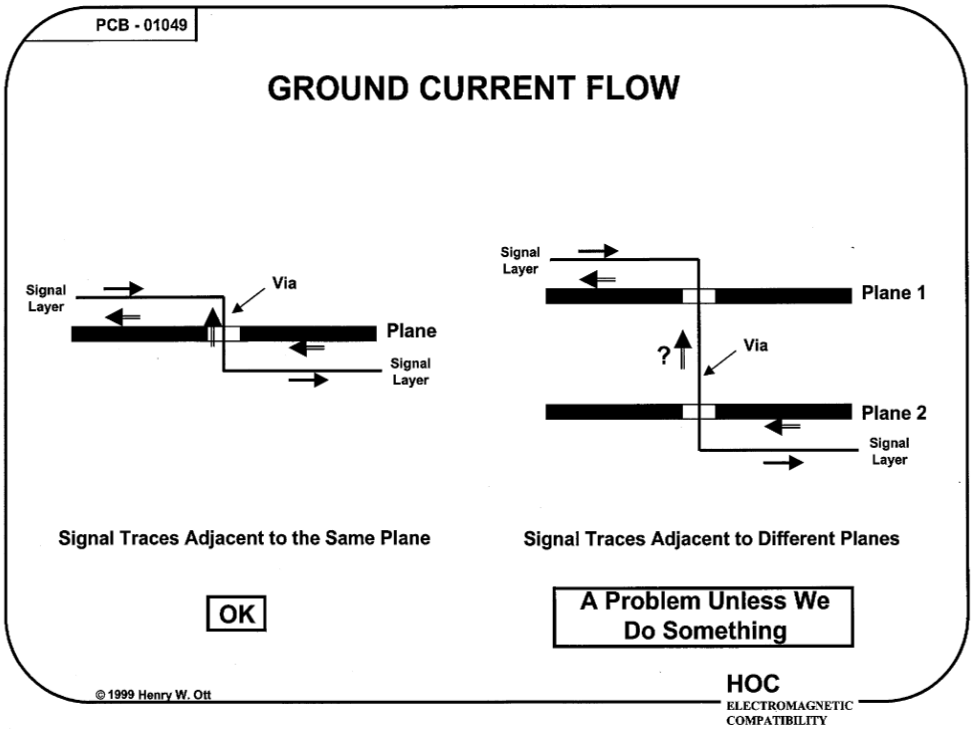
If you absolutely must route the signal across the split plane, place a few small stitching capacitors across the split, one on either side

of the trace. This will provide high-frequency continuity across the split while maintaining dc isolation between the isolated sections of the split plane. The capacitors should be located within 0.1" of the trace and have a value of 0.001 to 0.01 uF according to the frequency of the signal. This is far from an ideal solution, however, since the return current must now flow through a via, a trace, a mounting pad, a capacitor, a mounting pad, a trace, and finally a via to the other section of the split plane. This adds considerable additional inductance in the return path (5 to 10 nH minimum).

If in the above example both the power and ground planes are split, you are really in trouble. I leave it to you to figure out how the current gets across the split plane boundary. In some instances it may have to go all the way back to the power supply. If you have a split power and split ground plane the only acceptable solution may be to make sure that no signal traces cross the split plane boundary.

For additional information on split planes see our Tech Tip on **Grounding of Mixed Signal PCBs**.

Changing Reference Planes. When a signal trace changes from one layer to another on a PCB, the return current path is interrupted since the return current must also change reference planes (see right hand figure below). The question then becomes how does the return current get from one plane to another? As was the case for the split planes mentioned above the interplane capacitance is not usually large enough to be effective, so the return current will have to flow through the nearest decoupling capacitor in order to change planes. This obviously increases the loop area and is undesirable for all the reasons previously stated. One solution to this problem is to avoid switching reference planes for critical signals (such as clocks), if at all possible. If you must switch the return path from a power plane to a ground plane you should place an additional decoupling capacitor adjacent to the signal via in order to provide a high-frequency current path between the two planes for the signal return current. This is not an ideal solution, however, since the return current must now flow through a via, a trace, a mounting pad, a capacitor, a mounting pad, a trace, and finally a via to the other plane. This adds considerable additional inductance in the return path (typically 5 to 10 nH).



Note, that if the two reference planes are of the same type (either both power, or both ground) you can put a via (ground to ground or power to power) instead of a capacitor immediately adjacent to the signal via. This is a much better solution than using a capacitor to connect the planes together, since the added inductance in the return path will be considerably less.

Referencing the Top and Bottom of the Same Plane. Whenever a signal switches layers and references first the top and then the bottom of the same plane we must still ask the question, how does the return current get from the top to the bottom of the plane. Do to the "skin effect" the current cannot flow through the plane, it can only flow on the surface of the plane.

In order to drop a signal via through a plane a clearance hole must be provided in the plane, otherwise the signal would be shorted to the reference plane. The clearance hole provides a surface connecting the top and bottom of the plane and provides a path for the return current to flow from the top to the bottom of the plane (see left hand figure). Therefore, when a signal passes through a via and continues on the opposite side of the same plane a return current discontinuity does not exist. This is, therefore, the preferred way to route a critical signal if two routing layers must be used.

Summary. High-Speed clocks and other critical traces should be routed (in order of preference):

1. On only one layer adjacent to a plane.
2. On two layers that are adjacent to the same plane.
3. On two layers adjacent to two separate planes of the same type (ground or power) and connect the planes together with vias wherever the signal changes planes.

4. On two layers adjacent to two separate planes of different types (ground and power) and connect the planes together with capacitors wherever the signal changes reference planes.

Avoid routing clocks or other critical traces across slots or splits in the adjacent plane. The above guidelines are important for all PCBs carrying high-frequency signals, but are critically important in the case of boards with constant impedance transmission lines.

If you follow the guidelines presented in this series of articles, with respect to layer stack-up and the avoiding of return current discontinuities, you will produce better PCBs and avoid many of the most common EMC problems associated with boards. It will not guarantee you a perfect PCB layout but it will go a long way towards reducing the emission, increasing the immunity, and improving the signal quality of your boards.

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Return to top of page.

Return to HOC home page.

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