

My Learnings

[Microsoft Word - RIGHT THE FIRST TIME 09-15-08.doc](#)

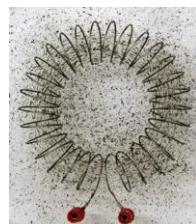
- Human body model, $1.5 \text{ k}\Omega$ in series with 100 pF .
- Electrical engineering rewards efficient design.
- Low frequency: generally, a few kHz to 1 MHz
- A lot of electronics, especially transistors, is about seeing a change and going down the chain of effects and if a subsequent value is fixed, the next effect has an inverse relationship applied to it, indicating the response to the change.
- copper at the highest practicable current density (typically between 2 and 8 A/mm^2)

Testing:

- Generally, outputs and controls should be off defaultly. Most things are off defaultly. Some things can be on defaultly. Must check what is On (generally more obvious than checking what is Off) and what is Off when testing.
- Test the interaction. Don't just follow the instructions. Also test the full interaction. This requires knowledge of the holistic idea of the test. A test tests a purpose, an idea, further testing of the idea should take place preferably.
- Be very careful when designing something. Soon it will be something you overlook. Make sure you are okay with overlooking your current design. NO Oversights!
- Question everything
- When a problem arises don't be afraid to actually dig and invest time. Don't do random stuff
- take ownership of testing and take ownership of a task and really try to explore different interactions
- to fully understand and pick something apart when testing
- be very careful. oscilloscope probes aren't so high impedance enough to not short something
- if you connect 12v to the gnd of the oscilloscope probe, you will short it.
- When power cycling, after powering off, wait some time before powering back on.

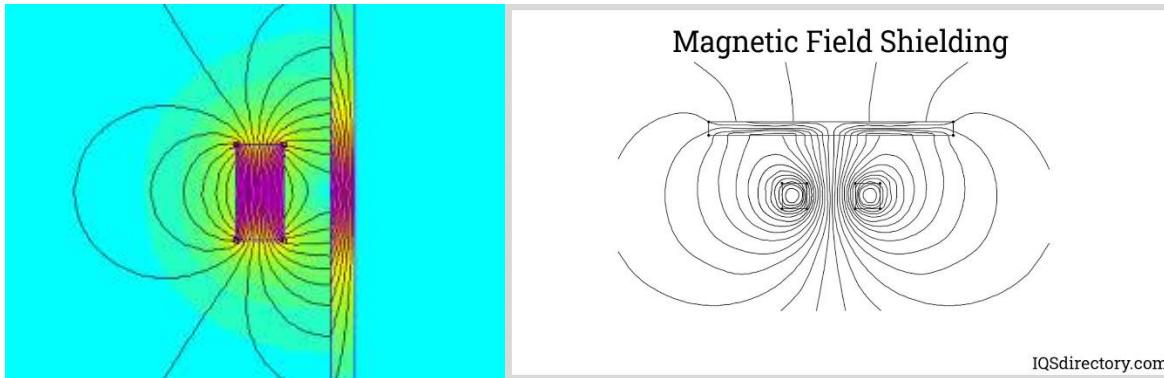
Electromagnetism:

- Iron fillings within a toroid



- A fundamental law: an electric current creates a magnetic field in that the lines of current and lines of magnetic field/force are *linked*, like Venn diagram.
 - o The *general* direction of the current is opposite the direction of the magnetic field.
- An electric current and magnetic field are inseparable; they increase and decrease together.

- Magnetic fields are more permeable and can pass through many materials and insulators. Magnetic fields are absorbed/redirected instead, by materials with high magnetic permeability, e.g. ferromagnetics. Electric fields and currents are shielded by insulators.



- Magnetomotive Force: The number of ampere-turns of the “exciting” winding. A measure of the magnetic field excitation and action.
 - o The ampere-turns are the cause of the magnetic field/force.
 - o 1 ampere-turn = 1 magnetomotive force.
 - o Equivalent ampere-turns only applies when turn area and turn depth is kept constant.
- Flux (=> flow): thought of as a displacement or FLOW of some incompressible ether along the lines of force; flux though of as the rate of flow (through a cross section).
 - o The sum of total field disturbance (magnitude) through a closed cross section perpendicular to direction of force.
 - o Total flux is same through all solenoidal (channel shaped), closed cross sections.

Permeability:

Inductance:

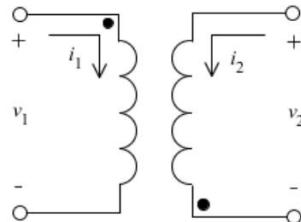
- Every current-carrying conductor will possess some sort of self-inductance due to the magnetic field associated with all current.
- Any magnetic field coupled with current from an electric field will cause the self-inductance of a current-carrying interconnect. The higher the magnetic field density about a current implies a higher (self) inductance.
 - o Hence, a higher back e.m.f. will be generated across that line due to changing currents.
- The ability of an electrical conductor to oppose a change in the electric current flowing through it.
 - o 1 H is defined as the inductance present that produces an e.m.f. of 1 V when the current changes by 1 A / s.
 - o A physical property defined by # turns, coil cross-sectional area, material, length.
 - Length effectively decreases the density of the self-inductance.

$$L = \frac{N^2 \mu_0 \mu_r A}{l}$$

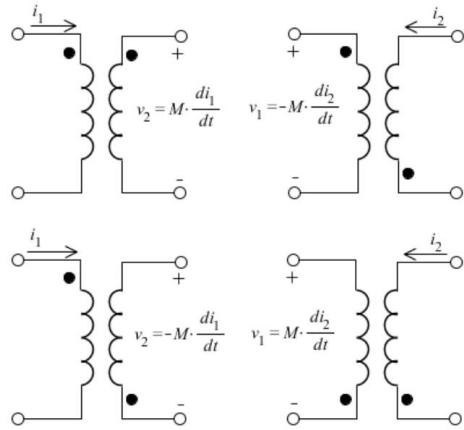
- Self-inductance: Current produces a magnetic flux; a change in current produces a change in magnetic flux; a change in magnetic flux produces an e.m.f. opposing the change in current => self-inductance.
- Mutual inductance (magnetic coupling): Current produces a magnetic flux in the 1st coil; a change in current produces a change in magnetic flux; an emf is generated in the 2nd coil such that the current generated has a changing magnetic flux opposite that of the first changing flux.
 - o Possesses an oscillatory nature.

$$M = \frac{N_2 \Phi_{21}}{I_1} = \frac{N_1 \Phi_{12}}{I_2}.$$

- The self-inductance (L) or mutual inductance (M) can be represented by $N\phi = AI$, where A is the [type]-inductance.
- The EMF, opposing the change in current, generated by inductance is proportional to the rate of change of the flux and thus current, and scales by the inductance.
- The windings for an inductor can be either CW or CCW and the direction of magnetic North, and the direction of the current is determined by your thumb w/ RHR, for a coil (not straight conductor).
- Dot convention tells us the polarity of the e.m.f. generated by mutual inductance and the direction of winding (CW/CCW) for coupled inductors.
 - o If both dots exist on the same side, the dotted sides represent the positive sides of the mutually induced e.m.f.s and the windings are oppositely wound
 - o If the dots are on opposite sides, the original voltage & current direction still represents the positive e.m.f. polarity but the secondly generated e.m.f. is negative at the other dot. This is by passive convention.



- The coupling coefficient [0,1] is the value that represents the percentage of the magnetic flux generated by one inductor that interacts with the another inductor; level of coupling.
 - o 1 implies perfectly linked; 0 implies uncoupled.
 - o Closer distance implies more magnetic coupling.
 - o Coupling coefficient scales with mutual inductance which scales with e.m.f. generated.



- Galvanometer: An electromechanical measuring instrument for electric current.
- Best Guide on inductors and transformers: [Coupled Inductors.pdf](#)
- [What is Inductance? - Definition, Self Inductance, Mutual Inductance, Difference](#)
- [Mutual Inductance: 14.3: Self-Inductance and Inductors - Physics LibreTexts](#) [14.2: Mutual Inductance - Physics LibreTexts](#)

Wire diameter and Inductance:

- For a constant current, a wire of smaller diameter will have a larger inductance. A Proximity problem.
- Total current (C/s) is the sum of smaller currents, all in the same direction, until the level of singular electron flow. Essentially for a given current we have $[6.241\ 509 \times 10^{18} e] * / \text{singular electron currents}$.
- These sub-currents will have self-inductance and mutual inductance, with the generated e.m.f. residing on the current sourcing side, since current is unidirectional at one instance, and the imperfect winding of the sub current can be assumed to be opposite.
- Hence the closer the singular currents are, or how thin the wire is, the more mutual inductance there will be, by the coupling coefficient.
- The polarity of induced voltage can vary depending on the direction of turning of the non-straight current flow. But change in current will always be opposed, and the closer currents, implies a higher mutual inductance and hence inductance value of the thinner wire.
 - o A change in current can cause other currents to increase OR decrease to oppose this change.
 - o An increasing current will, by mutual inductance, be opposed. The e.m.f. on other lines may inc. or dec. current, but generally, change in current is more opposed by proximity.
- The way I see it, is based on superposition. Let's say wires can be coiled CW or CCW such that the e.m.f. generated on mutually coupled lines can increase or decrease their current. Nonetheless, current change is opposed a singular one. Therefore, for a wire, with a myriad of changes in current in one direction, and random coiling, the change WILL still be opposed!
 - o Hence thinner wires w/ >> mutual inductance > inductance than thicker wires.
- [coil - Why is wire's inductance inversely proportional to its thickness? - Electrical Engineering Stack Exchange](#) and Above learnings on inductance.

Confinement:

- An electromagnetic field is confined when in a structure where the signal is in between two equal electromagnetic fields (Ground).
 - o Stitching vias can confine the electromagnetic field comprising a signal within the via structure.

Skin Effect and Proximity Effect:

- HF current higher at the outer levels of a conductor due to magnetic field causing back emfs (eddy currents) in the centre of the conductor.
- These effects of eddy currents caused by back-emf are only apparent in high frequencies (MHz level).

Inductance/Conductance:

- The breakdown voltage of an insulator is the minimum voltage that causes a portion of an insulator to experience electrical breakdown and become electrically conductive.
 - o For diodes, the breakdown voltage is the minimum reverse voltage that makes the diode conduct appreciably in reverse. Some devices (such as TRIACs) also have a forward breakdown voltage.

Signal Integrity:

- Increasing impedance decreases crosstalk, emi, but increases rail collapse. And vice versa. Impedance matching is independent, really.
- Noise: An undesired signal. Can be the superimposition of additional noise or the decrease of desired signal producing an undesired signal (rail-collapse noise).
- Generally important at clock frequencies above 100 MHz or rise times shorter than about 1 nsec.
- All about the interconnects; each interconnect is a transmission line with a signal and return path.
- Ringing is generally caused by impedance mismatches.
- The higher the frequency and the shorter the rise time, the more important it is to keep the impedance the signal sees constant.
- A signal sees an instantaneous impedance at each location on an interconnect.
 - o If instantaneous impedance is constant, SI is improved a lot.
- Constant instantaneous impedance across an interconnect (or net) implies:
 - o A characteristic impedance
 - o Uniform cross section.
 - o Uniform geometry & shape
- A change in instantaneous impedance, a discontinuity, implies reflections, attenuation, and distortion, which in high amount can lead to **false triggering**.
- Discontinuities:
 - o Changes in trace width/geometry
 - o Via; layer change
 - o Connector
 - o Stub, branching of a trace into parallel, tee
 - Branching discontinuity is caused by the impedance change at the junction

- End of net
 - High impedance OPEN at a receiver OR low impedance SHORT at driver output.
- The effect of a discontinuity, i.e. distortion, on a signal increases with shorter rise times and higher frequencies.
- One can see that due to the capacitive coupling and lower impedance of higher frequencies with capacitance, that signal rise time decrease with HF coupling out. HF attenuation, Hi-pass filter
 - When rise time approaches the period of a bit, distortion of info occurs.
 - **Inter-symbol interference (ISI)**; significant problem in > 1 Gbps serial links.
- The series resistance of a transmission line increases with the square root of frequency, and the shunt AC leakage current in the dielectric increases linearly with frequency.
-

Rail-Collapse:

- Ensuring rail collapse is minimized means decreasing the impedance of the circuit/PDN. Decreasing inductance and increasing capacitance, but also not increasing capacitance at certain points so that EMI coupling doesn't occur from radiated common mode currents/noise.
- Limit current (if possible). Can increase voltage, though power loss probably occurs.
- High interplanar capacitance, decoupling capacitors, minimize current loop size.

Crosstalk:

- Limit cross talk by decreasing parasitic capacitance and inductance. Capacitance allows coupling through an electric field, inductors allow coupling through a magnetic field through mutual inductance.
- This also means to limit high switching between voltage and current to minimize crosstalk, which is a problem in our high speed – necessary designs.
- These equations provide a good metric on crosstalk / (cap./ind. Coupling). M: mutual ind..

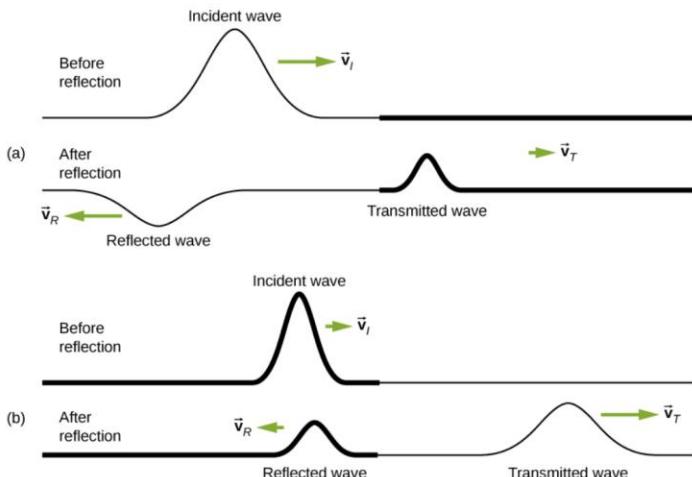
$$V_{\text{coupled}} = \frac{C_{\text{mutual}} \cdot \frac{dV}{dt} \cdot Z_{\text{load}}}{1 + j\omega C_{\text{mutual}} Z_{\text{load}}} \quad V_{\text{induced}} = M \cdot \frac{dI}{dt}$$

EMI:

- The radiated far-field strength from common currents will increase linearly with frequency and from differential currents will increase with the square of the frequency.
- Radiated emissions increase as frequency of signal increases.
- Often, the same physical designs that contribute to low rail-collapse noise will also contribute to lower emissions.
- Locate highspeed sections of a board away from where it can exit or couple.
- Common mode noise (from common mode current) is more noisy than differential noise/current since it gets out and couples.
- Sources of EMI:
 - Conversion of differential signal to common signal coupling out
 - Ground bounce creating common currents which couple out.

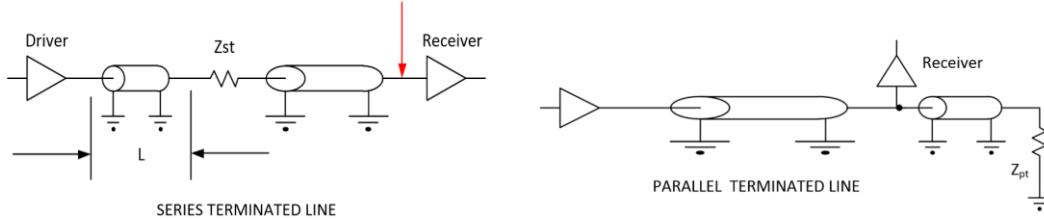
Termination:

- Termination resistors match the resistances of the line to the transmission line impedance, preventing reflections.
- Ideally, transmitters have 0 output impedance, receiver have infinite input impedance, and termination resistors perfectly match transmission line impedance. We simply strive to limit undershoot at the receiver. Overshoot is within tolerance mostly for our low voltage systems.
- To minimize undershoot in a transmission line impedance with tolerance, termination resistor value should result in a change in impedance such that the wave going towards the receiver tends to an overshoot. HIGH->LOW for series, LOW->HIGH for parallel.
 - o Note that the reflected wave should be inverted, to be in phase with the incident wave. This means LOW->HIGH impedance for parallel superimposes to tend to an overshoot. Also, LOW -> HIGH is seen on reflected series signal, which tends also to overshoot.
 - o Undershoot degrades the logic level and is always harmful. Overshoot is harmful if it exceeds the voltage rating of a logic circuit.



- Place series termination resistors as close as possible to the driver output. We want the sum of the output impedance of the driver and the termination resistor to match the characteristic impedance of the transmission line.
 - o Distance from driver output to termination resistor, L, should be minimized.
 - o Termination resistor value should overcompensate in impedance matching, i.e., edge to the value to the higher tolerance of the transmission line impedance. Such that a high->low impedance is matched.
 - o This is to produce in phase forward propagation and 180° back-reflections that dampen and do not positively superimpose to increase the reflections.
 - o Note: the sum of the output impedance of the driver + termination should match and tend to the highest tolerance of transmission line impedance.
- When low input-to-output delay is desired, minimum output impedance (strongest drive setting) is applied in the series termination impedance at the driver.
- Series terminated signals should propagate at half amplitude due to HIGH impedance reflection at the receiver, ~doubling the receiver signal.
- Place parallel termination resistors anywhere at or after the receiver that satisfies transmission line layout convenience.

- Resistor value should undercompensate in impedance matching to the transmission line such that the termination resistor's value should match the lowest tolerance of the transmission line.



- Parallel termination and series termination can be used together for specialty logic.
 - Output signal level may need to be intentionally shifted down to a lower voltage
 - Suppress ground bounce by placing a series resistor for damping, but the reflection off the load is still suppressed with parallel termination.
- For parallel termination, it should be placed closest (or tending after) at the receiver, that is, the location of Hi Z. So, for array board, termination to clk in should be placed closest to TPs, not receiver.
- Qs: Why the reflection at receiver for parallel receiver doesn't double signal?
 - A: it seems to form a voltage divider
- Qs: It seems that a voltage signal simply has to have its field reach, electromagnetic wave things. Termination in series damps reflection, but not the propagating signal?
- [The Right Termination, Of The Right Size, At The Right Place](#)

RF:

- Purely reactive components, no resistance, strictly impedance.

Ground Bounce:

- The primary cause of switching noise and EMI.
- Causes ringing, see Ringing section below.
- Caused by the inherent inductance found in all circuits at any point, due to the closed loop nature of all practical circuits at any voltage rail, in our circuits.
- Found in most bipolar and CMOS transistor families.
- The quick slew rates of CMOS coupled with the rail-to-rail output swing, tend to generate more ground bounce noise, than BJTs, which have quicker slew rates, but lower output swing.

Idealistic and Intuitive Understanding of Ground Bounce:

- A real model is much too complex to understand practically, with high D.E.s.

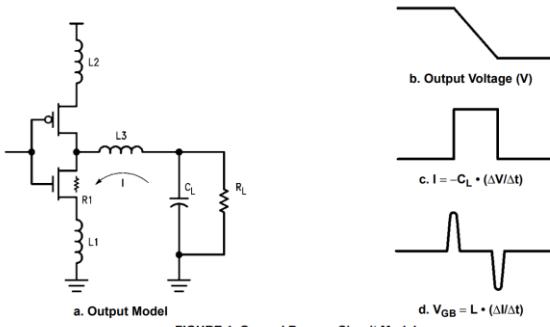
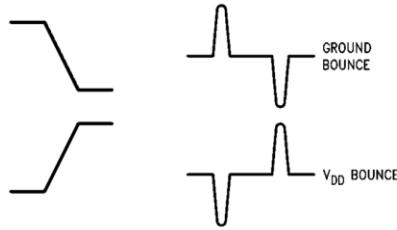


FIGURE 1. Ground Bounce Circuit Model

- B) The voltage across the load is switched from HIGH to LOW. The slew rate is dependent on L1, L3, C_L.
 - o When the pull down is turned on, current discharges from the load capacitor.
- C) The current across a capacitor is proportional to the change in voltage across it.
- D) A change in current causes an opposing emf by inductors, proportional to the change in current.
 - o This voltage at the inherent inductances, which exists at ground, changes, i.e. (internal device) ground bounce.
- *This shift in potential causes the device inputs and outputs to behave differently than expected because they are referenced to the internal device ground, while the devices which are either driving into the inputs or being driven by the outputs are referenced to the external system ground.*
- A high slew rate is detrimental here, as a high slew rate increases ground bounce and dV/dt .
- There exists ground bounce from LOW-TO-HIGH, at a much lower amplitude due to the larger gate capacitances and resistances of the PMOS p.u. transistors, yielding a lower slew rate and slower current change. $\tau = RC$; R and C increase. An increase in C decreases the rate of change of voltage, slew rate, by $\tau = RC$, although it increases current by $Q = CV$, overall, current is decreased.
 - o During a high-to-low transition, both the NMOS and PMOS transistors can momentarily conduct simultaneously, leading to a higher current spike
- **Higher C, in series with L, implies lower ringing noise by increased ability to store charge (capacitance), implies decreased rate of change in current).**
- V_DD bounce is the inverse of ground bounce, most prominent from LOW-TO-HIGH. Intrinsic from the inductances.
 - o Less concerned since it is the exact inverse of ground bounce and input HIGH noise margin is greater than input LOW noise margin, hence GND bouncing down is more dangerous than VDD bouncing up. Though both happen in the same period for a GND/VDD bounce.



- V_{DD} bounce (droop) is the voltage drop across the package
- Inductance (to V_{DD}) is caused by charging load capacitances
- V_{DD} bounce is less of a concern than ground bounce because TTL-level inputs have greater high noise immunity

FIGURE 2. Ground Bounce/ V_{DD} Bounce

- <https://www.eeweb.com/wp-content/uploads/articles-app-notes-files-understanding-ground-bounce-1326344987.pdf>

Design:

1. A poorly designed return path that is highly restrictive and narrow will increase discontinuity in the path and increase the inductance problem.
 - o A wide, continuous plane is desired for the return path.
 - o Small current loops with the return path close the signal path.
 2. Multiple signals on return path.
 - a. Noise of one signal with ground bounce will affect another signal sharing the path.
 - b. If only one signal on the return path, it is fine.
 3. dI/dT .
 - a. $V = L \frac{dI}{dT}$
 - b. Stagger I/O switching, use source series termination resistors, use more return paths, and use differential signals. Slew rate control and increase rise time if possible.
- W/ differential signaling, reduce mode conversion as much as possible. Mode conversion will create common current that will drive some ground bounce.

$$V_{gnd} = L_{\text{total}} n \frac{dI_{\text{return current}}}{dt}$$

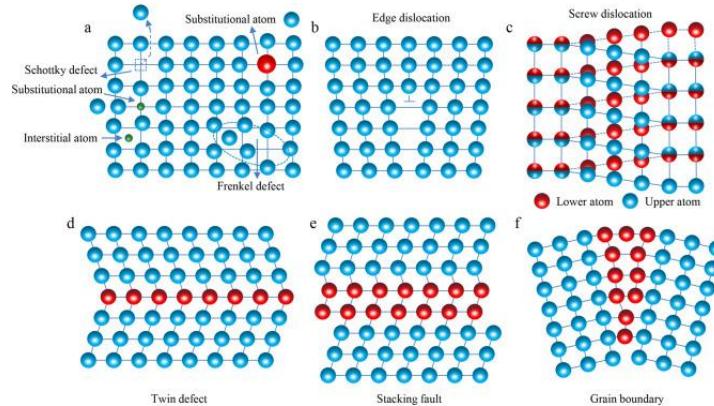
- Ground bounce can be minimized with bulk, bypass capacitors. The higher the (stray) inductance, yielding to more detrimental ground bounce, the higher the bulk, bypass capacitors should be.
- [Test Happens - Teledyne LeCroy Blog: The Causes of Ground Bounce and How To Avoid It](#)

Return Paths:

- The return path travels via GND (designated return path) and PWR paths.
 - o **DC Bias travels on path designated, the expected path. So the below applies to high-speed clocks and other critical traces.**
 - o AC signals can couple onto GND/PWR layers, GND is good. If PWR layer, the signal must return to GND (designated return path) through an increased current loop.
- It is the HF component of a signal that couples into other PWR/GND layers, increasing current loop, while having a critical return path.
- The amount of current in a path is inversely proportional to its impedance.

- The least impedance path of return current is on the closest plane directly under the signal. This minimizes resistance and inductance and maximizes capacitance.
- Interrupted conduction of HF return path directly under the signal path implies a larger current loop (inductance).
- When a HF signal switches layer through a via, the return path will still tend to the closest PWR/GND plane, if on the new layer, it is a PWR plane, the return current will return by adding a capacitor to GND. This increase current loop a lot since the current must go to the surface of the board where the cap is.
- Increasing interplanar capacitance between pwr and GND decreases the current loop of HF signals which couple into a pwr layer as its return path.
- Without a way for HF signals on PWR layers to return to the GND return path, Hi Z, the noise can radiate and couple through the board unpredictably.
- Ideally, if switching layers for a signal, the return path, closest plane are always a GND plane. This allows controlling of the HF return signal. In this case, use a stitching via close to the signal via to limit loop size , inductance.
- Due to the skin effect, HF signal current traveling through a conductor resides in travel in opposite sides
 - o This is why we sandwich signal layers with GNDs
 - o If we do not have 2 reference planes. We place a signal via through the signal plane and the return signal passes through the via to both currents of a signal, due to the skin effect.
- See Henry Ott resource.

Crystal Defects:



Impedance Measurement:

- When displayed in the frequency domain, the impedance is the total, integrated impedance of the entire DUT at each frequency. When displayed in the time domain, it is the instantaneous impedance at each spatially distinct point on the DUT that is displayed

Impedance Analyzer:

- 4-terminal instrument operating in frequency domain.
- 2 terminals inject a generated constant-current sine wave to the DUT.
- 2 terminal measure the sine-wave voltage across the DUT.

- $V / I = Z$.
- Frequency sweep from low (100 Hz) to high (40 MHz).

Vector-Network Analyzer:

- Measuring instrument of impedance operating in frequency domain. The output impedance typically of VNA outputted sine wave is 50 ohms.
- Frequency sweep from low (kHz) to high (50 GHz).
- At each frequency, incident & reflected voltage amplitude and phase is measured, and impedance is calculated from reflection:incident ratio. reflection coefficient ratio or something.
 - o This is why VNA output impedance is important to be considered.
- This ratio is one of the S-parameters of VNA, S11.
 - o $S11 \& (50 \text{ ohm})$ source impedance \Rightarrow impedance of DUT at frequency.

$$\frac{V_{\text{reflected}}}{V_{\text{incident}}} = \frac{Z_{\text{DUT}} - 50\Omega}{Z_{\text{DUT}} + 50\Omega}$$

where:

$V_{\text{reflected}}$ = the amplitude and phase of the reflected sine-wave voltage

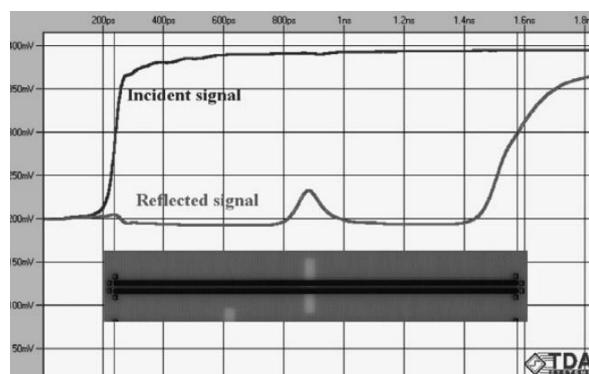
V_{incident} = the amplitude and phase of the incident sine-wave voltage

Z_{DUT} = the impedance of the device under test

50Ω = impedance of the VNA

Time-Domain Reflectometer:

- Operates in the **time-domain**.
- Outputs a fast rise-time signal (35-150 picoseconds) and measures reflected (voltage) signal amplitude.
- Knowing the reflected voltage, the impedance of DUT can be calculated, by some ratio or reflection coefficient.
- Since in time domain, the impedance is the instantaneous impedance and hence the TDR can continuously map out the impedance profile of a transmission line.



Transmission Line Effects from Inductance:

-

Power Supply Etiquette:

- ESD and wrist strap before contacting the board.
- When connecting the power leads, ALWAYS connect GND (black) first.
- When disconnecting the power leads, ALWAYS disconnect VCC (red) first.
 - o Always turn off before taking out any leads.

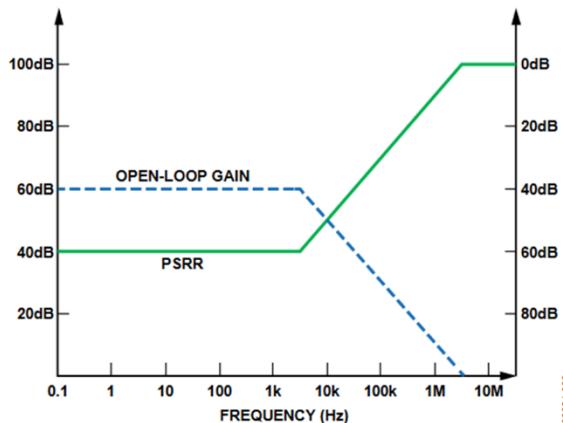
Power Supply Rejection Ratio:

- The higher the PSRR, the better the noise response of the component.
- Ratio of the change in supply voltage to the equivalent output voltage [dB].
 - o Ideally infinite.

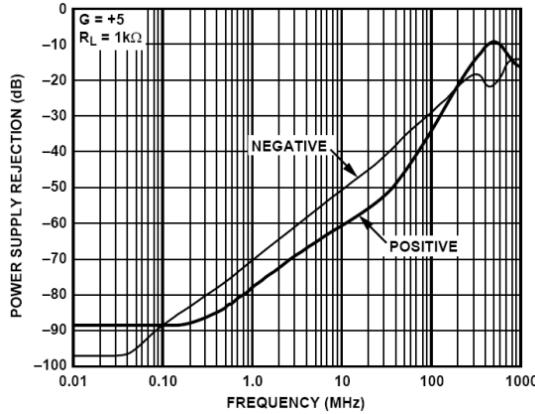
$$\text{PSRR[dB]} = 10 \log_{10} \left(\frac{\Delta V_{\text{supply}}^2 A_v^2}{\Delta V_{\text{out}}^2} \right) \text{dB}$$

where A_v is the voltage gain.

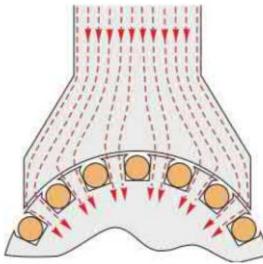
- The PSRR is the ratio of the input power supply **noise/ripple** and the amount that is transferred to the output of the regulator in decibels (dB)
- PSRR is frequency dependent



- For a chip, without decoupling, PSR drops rapidly at higher frequencies due to more energy coupling from the power line to the output.
 - o **HF energy can be decoupled w/ caps and beads** to maintain a more constant frequency response.



Motors:



- $F_m = BII$
- Unless an exotic cooling system is employed, most motors (induction, d.c., etc.) of a particular size have generally similar magnetic & electric loadings, regardless of type. So, similar torque capabilities.

$$T = (\overline{BA}) \times (\pi DL) \times \frac{D}{2} = \frac{\pi}{2} (\overline{BA}) D^2 L$$

- The magnetic loading is a measure of the (average) magnitude of the radial magnetic flux density over the the entire cylindrical surface of the rotor. The electric/current loading is a measure of the average axial current per metre into the circumferential area.
 - o For B, higher B at teeth, hence average over cylinder SA [B/m^2].
 - o For A, higher current along conductor, but assumed spread over cylinder SA, *about a certain length into the cylinder* [A/m].
- Higher current means that magnetic flux may saturate, higher magnetic density with thinner teeth, mean current might be too high. Opposing nature.
- For loading, the volume effectively doesn't matter, hence it is the **materials** used and the **cooling system** which effect loading.
- $F_m = BIA$ effectively. Equation for total torque on the surface of the rotor. torque shows that the magnetic and current loadings are scaled by the proportion to the motor's volume.
 - o This means that while we generally know that magnetic & current densities/loadings are constant for any given size and current and field strength for a normal cooling system due to current-heating and magnetic saturation, increasing rotor volume does increase torque.

- Generally, the overall volume of a motor is determined by the torque it has.
- Work is force \times distance. Torque is force \times radial distance. For a circumference arc of angle θ , $a = r\theta$. Work by tangential force on a circle is $F \times r \times \theta = T \times \theta$.
- Power is Work/time, implies power of motor is $T \times \omega$.

$$P = \frac{W}{t} = \frac{T \times \theta}{t} = T \times \omega \quad P = T \omega = \frac{\pi}{2} (\overline{BA}) D^2 L \omega$$

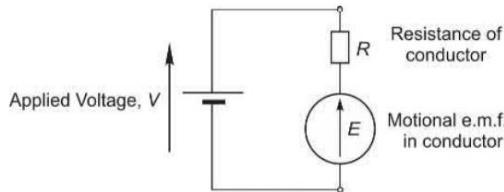
- This implies that the Power density is:

$$Q = 2\overline{BA} \omega$$

- o By Volume = $\pi r^2 h = \pi(D/2)^2 L$. This value implies the power of the motor relative to its volume; effectively the representation of power if volume wasn't a factor.
 - Increasing rotor velocity is very important in increasing power of motor.

$$\text{Electrical input power (VI)} = \frac{\text{Mechanical output power (EI)}}{\text{Copper loss (I}^2R)}$$

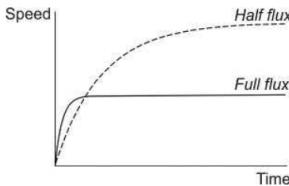
- Intuitive and from $V = E + IR$; KVL.



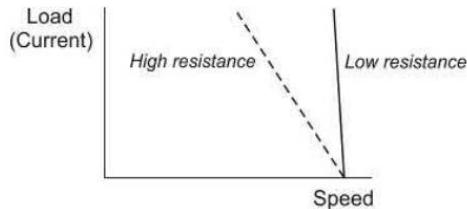
- In all real world scenarios, a load exists on the motor (friction), hence the current through the inductor will never be 0, at steady state. There will be power loss in the conductor resistance and power loss through the mechanical force.
 - o Only if no load exists and no friction exists can the steady-state current be 0.
- Crucial relationships:
 - o EI represents the power by the work done on the motor load.
 - o A higher load means a lower E.M.F force since the net force on the load will be lower in the direction of the magnetic force on the conductors, and hence the power = EI will be lower. Since I is dependent on E, and E is independent, E will be lower with a higher load.
 - I will be higher when E is lower.
 - o Intuitively, a higher load means a lower speed that the rotor will move by lower power dissipation.
 - o Higher speed means higher emf means lower current. Higher load means lower speed means lower emf means higher current.
 - o A higher E.M.F. (E) implies the load is at a higher velocity, for a constant load; proportionality.
 - o The steady state speed is inversely proportional to the magnetic flux density. A lower magnetic flux density implies a direct higher steady-state speed of the conductor/rotor.

$$E = V = Blv_0, \text{ i.e. } v_0 = \frac{V}{Bl}$$

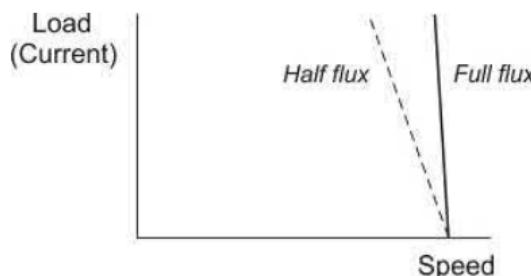
- For an non-ideal conductor with friction, @ steady state, there is current. But still, $E = V - K$ for V/Bl applies. And lower B implies higher v **at steady state**.
- At steady state is important, because it means no acceleration and that all acceleration to speed has been contributed.



- For the opposing force on the rotor, the load. The larger it is, the larger the current and lower the EMF, the difference $k = V - E$ is greater.
- A lower magnetic flux means higher velocity at the steady state. Steady state is when current in the conductor is 0, and $VI = EI + I^2R$.
- The higher the resistance of the conductor, the higher the speed decreases as the load increases. The lower the resistance of the conductor, the lower the speed decreases as the load increases. This is because the E.M.F. would have a smaller range if the resistance is higher, implying faster drop to steady state velocity.



- Interestingly, although lower magnetic flux density is known to increase steady state speed. Lower flux density does obviously imply a lower electromagnetic force. This lower force means that the power on the load by the motor decreases – EMF decrease -, hence current increases. Flux scales quadratically with speed. So a lower flux by 2, decrease speed by 4x.
 - Effectively, the lower flux means lower power generated by the motor initially, and only tends to higher steady state speeds due to inherent properties.



- Increasing the voltage of the source increases efficiency if the current stays equal, i.e., the mechanical power of the motor also scales with the increased voltage in some relationship.

- Basically if we can increase the proportion of the power of the conducting circuit to mechanical power : resistive heating, efficiency increases.
- **Energy conversion is more efficient at higher speeds when the motor does more work and at lighter loads. And with higher magnetic density. And at lower resistances. And with higher voltages to increase total headroom of EMF vs. IR relationship.**
- A larger motor will be more efficient... as it will have higher B, lower R, and higher current carrying abilities.
- A motor's efficiency applies in the same way as a generator with the back EMF. Where the EMF is the source, the IR resistive heating still applying, and voltage (and current) to the source as the power generated.
- Principles:
 - The max speed that the motor can run at is determined by the applied voltage as this tells us the maximum E.M.F. that can be generated.
 - The E.M.F. / current that the conductor circuit produces is determined predominantly by the mechanical load, amongst other smaller things like resistance, magnetic field, injected current.

Motional e.m.f:

$$V_2 - V_1 = Blv = E$$

$$\text{Electrical input power} = \frac{\text{Rate of production of heat in conductor} + \text{Mechanical output power}}{\text{Rate of production of heat in conductor} + \text{Mechanical output power}}$$

Deduced from

$$\text{i.e. } V_2I = I^2R + (BlI)v \quad (1.18)$$

- The magnetic field is simply the catalyst for the force on the conductor. No energy is required from the magnetic field to power the motor.
 - Once the B field has been established (when the magnet was first magnetised and placed in position), no further energy will be needed to sustain the field.
- The only electrical input power required is that needed to drive the current through the conductor.
- If the conductor is not accelerating, this means that the current in the conductor is a function and can be deducted from the load.
- If no motion occurs, no work is done, implies no power loss/generation.
- Whenever energy is being converted from electrical to mechanical (motion occurs) form, the induced e.m.f. always acts in opposition to the applied (source) voltage.
 - Can occur even if the back e.m.f. is induced in a circuit without existing current/voltage.
- **With a constant load, the current is the same at all steady speeds, the voltage being increased with speed to take account of the rising motional e.m.f..**

Motor Principles:

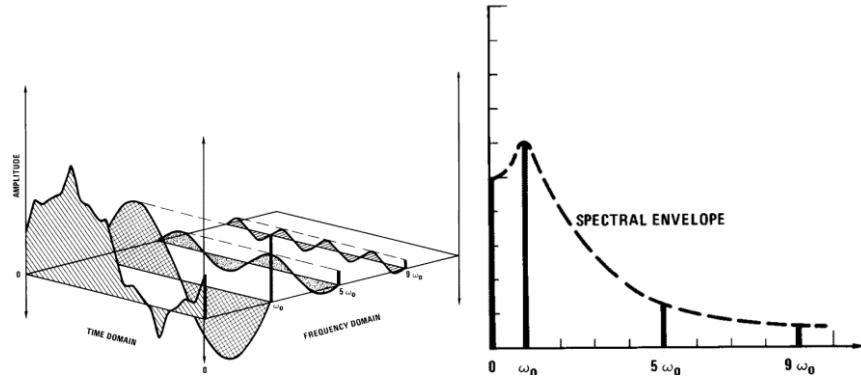
- The limiting factor / characteristic of motor power is current capacity. Current is limited by the cooling system and by the conductor insulation class.
 - Prominently, the temperature rise in the windings
 - Class F: temp rise of 100K

- Class H: temp rise of 125 K.
 - Torque per unit volume. A larger rotor volume (means a larger motor volume) will provide a larger torque. In the formula D^2L scales linearly with $V = \pi r^2 h$.
- $$P = T\omega = \frac{\pi}{2} (\overline{BA}) D^2 L \omega \quad Q = 2\overline{BA} \omega$$
- Generally speaking, magnetic and electric loading stays the same with motor size/volume as flux and current density are directly scaled to size.
 - The torque scales quadratically with the square of the diameter $\rightarrow r^2 \rightarrow V$.
 - Speed: **higher speed** means **higher output power** (per unit volume; means that if volume was constant, higher speed means higher power) and **efficiency**.
 - A smaller motor, will have higher speed capability since the angular velocity can be higher for a given torque. But a smaller motor may not be always fortuitous, as above.
 - A higher speed means more energy on mechanical power relative to IR heating \Rightarrow higher efficiency.
 - There are many complex relationships, but: A larger motor is generally better, it contains the merits of much higher electric loading, magnetic loading (somewhat higher), and higher torque capability.
 - The higher torque of larger motors means higher efficiency. More energy/torque on mechanical power, rather than I^2R heating.
 - Motor design is flexible. Changing the amount of current and voltage is invited and motors can generally be overloaded for certain periods of time without damage.
 - The magnitude and/or duration of the current may exceed ratings dependent on thermal time constants and temperature reached.
 - Thermal time constants range from a few seconds for small motors to many minutes or even hours for large ones.
 - Temp sensors to maximize motor power and overload it strategically.
 - MMF = $N \times A$ (excluding reluctance) can be altered by the N, A parameters.

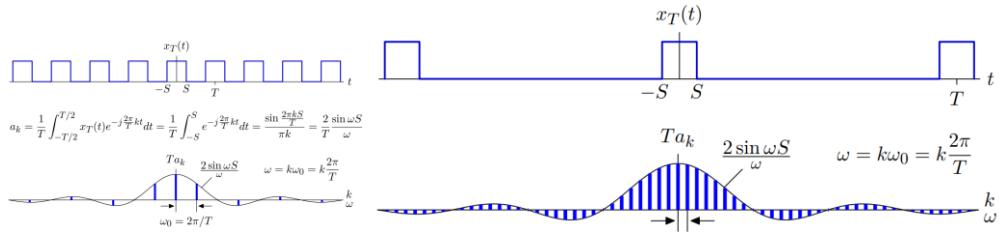
Power Spectrum:

- Spectrum: A plot of the magnitude vs frequency. Hence, power [Voltage/current squared] vs frequency for power spectrum.
- Fourier Transform: function that transforms a function in the time domain [magnitude vs time] to its correspondent in the frequency domain [magnitude vs freq.]. $f(t) \rightarrow F(\omega)$

$$F[x(t)] = \int_{-\infty}^{\infty} x(t) e^{-j\omega t} dt = X(\omega)$$



- Note: Doubling period doubles # of harmonics in given frequency interval.
 - o As $T \rightarrow \infty$, synthesis sum \rightarrow integral.



- Units of power (J/s) can be represented simply as V^2 or I^2 and energy (J) as $V^2 * s$ or $I^2 * s$ since the constant impedance value to evaluate to power or energy can be multiplied/divided with at the end.
- Instantaneous power can only be calculated through the time domain (see av. Power below), by the square of $f(t)$, $f(t)^2$ [A^2 / V^2].
- By the Fourier Transform, Parseval's theorem allows us to calculate the total energy in the system of $f(t)$ in the time domain:

$$\int_{-\infty}^{\infty} f_1(t)f_2(t) dt = \int_{-\infty}^{\infty} F_1(f)F_2(-f) df \quad (4e)$$

A corollary to this theorem is the condition $f_1(t) = f_2(t)$ then $F(-f) = F^*(f)$, the complex conjugate of $F(f)$, and

$$\omega(t) = \int_{-\infty}^{\infty} f^2(t) dt = \int_{-\infty}^{\infty} F(f)F^*(f) df \quad (5a)$$

$$= \int_{-\infty}^{\infty} |F(f)|^2 df \quad (5b)$$

- o $|F(f)|^2$ is the energy density, spectral density, or power spectral density function. [$V^2 * s$ or $I^2 * s$]
- o Average power can be calculated by dividing energy by $T_2 - T_1$.
- [Power Spectrum Estimation](#) (very good) [Lecture 16: Fourier transform](#)

PCB Layout:

- Generally, minimizing trace length is always desired, though which points must be minimized more, with respect to others, is the consideration,
 - o Data write lines close.

- To minimize the inductance of any via connecting to ground it is useful to have a thin dielectric thickness between the signal layer and ground.
 - o Using multiple vias will reduce the inductance further, by parallel inductors.
- Do not split the ground plane (for ringing and noise purposes); stitching vias can be implanted.
- Keep N/P signals parallel, and in close proximity.
- Guard traces (GND?) are sometimes needed parallel to N/P signals to avoid leakage from otherwise close HV traces.
- Do not route through vias to minimize copper/solder thermocouple (Voltage) effects.
- Place chips as close as possible to their sensors to limit parasitic capacitance and inductance noise.
- Worse noise generators: Voltage sources/traces, CRTs, Clock generators, memory buses, ISA/PCI buses.
- Leakage current produces offset and error.
- Route differential signals in parallel and in proximity, twisted for long cabling (or for particularly noisy environments).
- Use wide traces, narrow ones are more inductive and pick up radiated noise.
- Short traces with uniform width for uniform impedances.
- Copper can't be used as an EMI shield, and only ferrous materials, such as steel, work well.
- Floating pins cannot tolerate high capacitances (50 Pf), to avert risks of signal errors
- Place decoupling capacitors as closed as possible to chips for signal sources.
- PCB layout can heavily minimize radiated and conducted CM EMI from switching.
- Prepreg: dielectric material, often fiberglass reinforced with resin, as insulation layer between copper layers or core layers to create a robust and insulated multilayer PCB.
- Try to avoid power planes under switching inductors. The prereg power plane doesn't really matter since another level of filtering exists in filtering noise coupled into the plane.
 - o Stagger plane placement to avoid this or just do efficient design.
- Place higher current power supplies closer to the load since higher current loads have greater voltage drop over transmission lines. Generally, must consider the inherent voltage drop (real impedance) of all transmission lines (lossy and lossless), see eqn in calculating characteristic impedance for proof.

Copper Electroplating:

- Electrolytic cell: electrochemical cell that uses an external voltage (electrical energy), non-spontaneous reaction, to catalyze a chemical reaction which otherwise wouldn't occur.
- Voltage applied to electrolyte solution that is between cell's electrodes.
- In a galvanic cell, the electrolyte solution does not require an external source of (electrical) energy, implying a spontaneous reaction with negative Gibbs free energy.
- The part to deposit copper is cleaned and then immersed into an electrolyte solution to function as the cathode.

- The anode is the copper and copper ions flow through the electrolyte solution to create a current from the applied voltage.
- Positive copper cations dissolved at the anode through oxidation and are deposited to the cathode by transporting through the electrolyte solution.
- At the cathode, the copper ions are reduced to metallic copper by gaining electrons. This causes a thin, solid, metallic copper film to deposit onto the surface of the part.
- [Copper electroplating - Wikipedia](#)

Copper Pour:

- Filling unused space on PCB with planar copper. Costs more but has merit.
- A dry film is applied to section off non-plating sections that do need a copper pour. The PCB is then placed in plating solution with copper ions to undergo electroplating w/ a fixed a current.

Copper Balancing:

- In high level PCB layout, we do copper balancing to make component placement and PCB thicknesses even and flat.
- This means symmetrical vias and copper (traces/planes) under a component.

Stack-up:

- Power planes are used for high-current carrying capacity, thermal distribution, and emi purposes through interplanar capacitances.
- Thinner dielectric layers between multiple power planes can enhance heat dissipation, especially when paired with a well-planned via network.
- Symmetry of the stack up is greatly desired.
- The outer layers or surface microstrip layers are subject to many process steps that can result in substantial trace width variation and the associated variations in impedance that make them undesirable for high speed signaling. I use the outer layers for redistribution and “non-critical” signals only.
- Signal planes are generally surrounded by ground planes (or outside air for top and bottom layers)
 - o This limits parasitic inductive effects caused by current coupling into Power layers, which then have to go through some decoupling cap or component connected from Power to GND.
 - o This can result in an extremely high impedance return path except for extremely fast digital signals or very high frequency RF signals due to a very small capacitance to the next PCB ground plane layer.
 - o [Power Plane and Ground Planes: Should You Use Your PCB Power Plane as a Return Path? | PCB Design Blog | Altium Designer](#)
- Characteristic Impedance of signal layers (adjacent to grounds on both sides) can be controlled with adjacent dielectric thicknesses. Lower dielectric thicknesses imply higher capacitance and lower impedance, and vice versa.
 - o Wide or narrow traces imply lower or higher inductances, increasing or decreasing impedance, respectively.

- Can create Signal/power planes to limit the number of planes while keeping interplanar capacitances present.
- Power layers are generally closer to the top and bottom of a stack up, with signal layers closer to the centre due to better heat dissipation of the high current power layers and better (external) emi shielding for the signal layers from outer power/ground layers.
- The volume of the copper, i.e. the current carrying capacity of a conductor does not scale linearly with its dimensions.
 - o With length, current carrying capacity is invariant.
- Reference GND plane adjacent to all signals and power since:
 - o Return Path for Current: High-speed signals generate return currents that flow in the nearest reference plane. If there's no nearby plane, the return path becomes long and noisy, increasing EMI and crosstalk.
 - o Controlled Impedance: The impedance of a trace depends on its distance to the reference plane. Without a nearby plane, impedance becomes unpredictable.
 - o Signal Integrity: A nearby reference plane helps contain the electromagnetic field around the trace, reducing radiation and susceptibility to noise.
- 1. A signal layer should always be adjacent to a plane.
- 2. Signal layers should be tightly coupled (close) to their adjacent planes.
- 3. Power and Ground planes should be closely coupled together.
- 4. High-speed signals should be routed on buried layers located between planes. In this way the planes can act as shields and contain the radiation from the high-speed traces.
- 5. Multiple ground planes are very advantageous, since they will lower the ground (reference plane) impedance of the board and reduce the common-mode radiation.
- Generally, don't want high speed signal traces on top and bottom layers to prevent picking up emi and to prevent emi propagation (antenna), with the caveat that a trace becomes an antenna at $\frac{1}{2}\lambda$ or λ transmission line length.
- At top and bottom layers, less shielding of EMI, and one less return path (GND) since the other side is air, this can potentially cause common mode noise to radiate due to higher impedance return path, though this is minimal effect.
 - o Controlled impedance better in internal layers, due to etching variation and mechanical damage.

Routing:

- Apply transmission line models when the trace length is more than 1/10th of the wavelength of the highest frequency component on the trace.
 - o These long traces' impedance will decrease voltage over trace.
 - o For traces shorter, it is safe to assume that the voltage level is the same over the entire trace.
- [AN0046: USB Hardware Design Guidelines](#)

Relationship: Temperature, Frequency, Voltage:

- Temperature and voltage are proportional to the acceleration of life of an integrated circuit.
- Temperature:
 - o Higher input voltage, and therefore power, is required when operating a chip at more extreme temperatures, at the same operating conditions (frequency).
 - o Higher frequency of the device (better performance) is realized at less extreme temperatures.
 - o The above two points imply that higher voltages allow a higher bandwidth of operating frequency, i.e., performance.
- It was seen that power consumption increases exponentially to temperature.
- The effect of power dissipation with frequency does not change at higher temperatures. That is, the difference in power dissipation at different frequencies is constant across temperature.

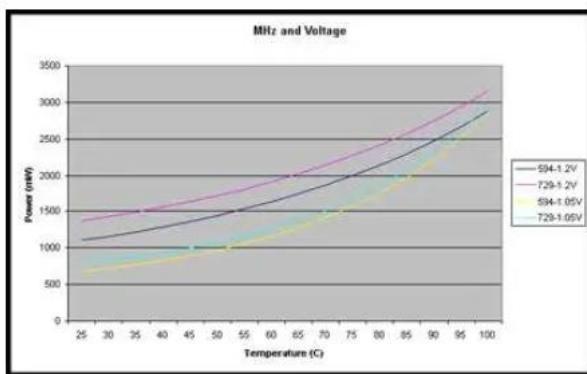
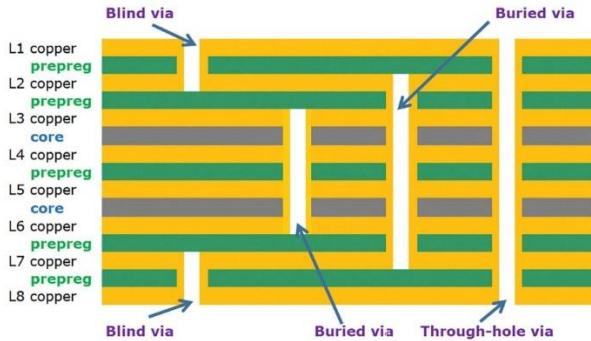


Fig. 3: Power consumption versus case temperature shows a constant difference between the two that corresponds to the 'dynamic' power dissipation between them.

- At higher temps, power consumption is increased. At a constant power consumption, CPU frequency (performance) decreases as compensation.
- There is a balance of reliability and performance, with higher frequencies at higher voltages, reliability decreases.
- [Go beyond the datasheet, Part 2: Understand the considerations - EE Times](#)

Vias:

- Using multiple vias will reduce the inductance further, by parallel inductors.
- Can implement stitching vias to connect sections of the ground plane to ensure uniform grounding.
 - o Spacing between them dependent on LF ($\lambda/20$) / HF ($\lambda/10$) design
- Electrical connection, mechanical support, thermal support.



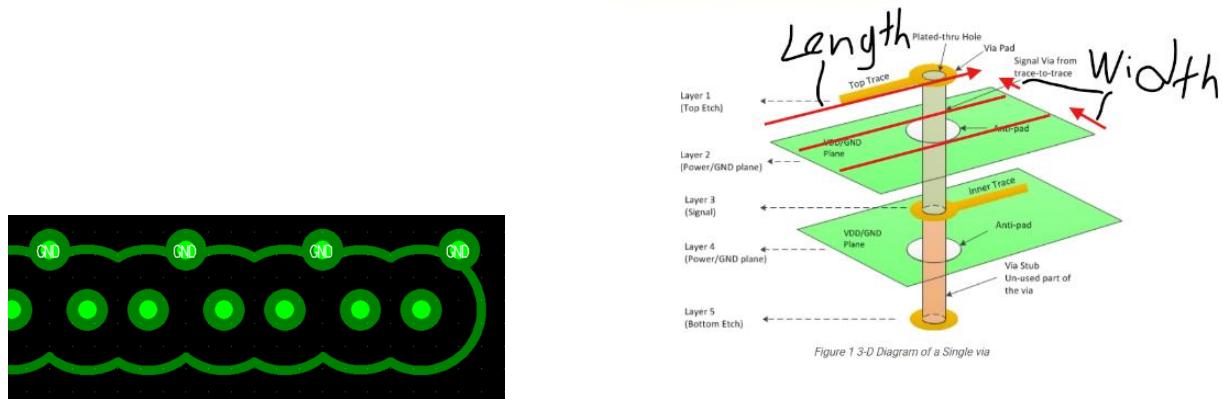
- Vias introduce parasitics, hence try to minimize number of vias.
 - o Especially for high-speed PCBs, the effects of the parasitics are magnified.
- Any dielectric between two signal paths yields a capacitor; any current loop yields an inductor. A via creates capacitors and increases current loop size, by adding 2^*w .
 - o See Parasitics section.
- Larger vias have lower impedance.
- Small note: [How to Avoid Parasitic Effects in High-Speed PCB Via Design - TechSparks](#)

Via-In-Pad:

- A more expensive operation where the cost of using 1 is the same as using any free amount.
- Manufacturing requires an epoxy fill of via so that the SMT pad is even and good for placement.

Stitching Vias:

- Layer transitions in digital circuits and RF circuits need to have a clear ground reference to control signal propagation along an interconnect in a PCB.
 - o They are used to provide a low impedance path (higher capacitance) for return current that is coupled onto lines beside and along the edge of the stitching via.
- Stitching vias placed near the signal via help maintain a tight return path, minimizing these problems.
- Generally, if you place a stitching via array in a PCB, there is likely to be a stitching via near a layer transition through a signal via.
 - o When making a layer transition, a nearby via in a stitching via array can perform the same function as the ground plane below a trace.
 - o With high-speed digital and RF, the situation is different and you need to have a purposefully designed stitching via array near the signal via.
- Typically, of stitching vias. When designing differential pairs, **merged circular antipads** refer to a single, shared clearance area around two closely spaced vias instead of separate antipads for each via. This approach helps reduce parasitic capacitance and improves signal integrity by maintaining a more controlled impedance

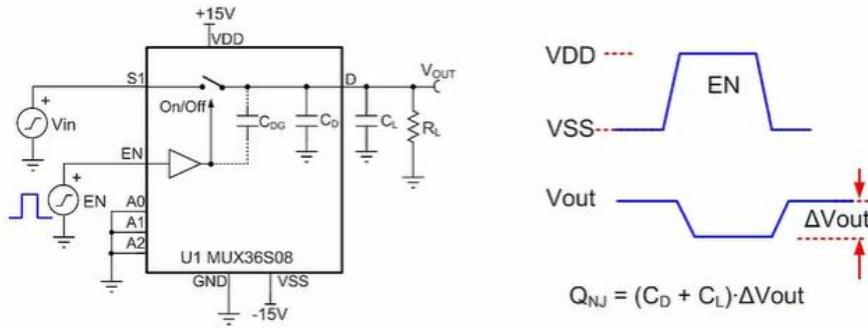


- Of differential vias, when we bring the stitching vias closer, we see that the localization frequency increases, but there is no change in impedance. This means the stitching vias are playing a role in confining the electromagnetic field around the vias, but not much else.

Charge Injection:

- $Q = CV$. Charge is proportional to capacitance and voltage.
 - o Redistribution of charge from one capacitor to another(s) causes a voltage decrease across all (if parallel).
- Since parallel capacitors increase capacitance, and for the case of charge injection, the charge stays constant per clock cycle, then the voltage across the capacitances decrease.
 - o This results in a decrease in output voltage since the reference voltage, i.e. one side of the capacitance is grounded and set.
- A charge/voltage distribution facilitated by capacitors occurring when a change in potential difference across an arrangement of parallel caps occur.
- The capacitance between the gate and nodes of the transistors in a switch causes the parasitic capacitance between the gate and the drain to shunt charge to and from the load by a change in the gate/control voltage.
- Charge injection: A coupling of the switch control signal through a parasitic cap.
 - o When the control line to the gate changes, the p.d. between the charge on the parasitic capacitance C_{gd} changes accordingly.
- For fast switchings, charge injection gets more pronounced, so choose lower C specs
- Specifics:
 - o Higher C_{gd} , implies high Q to be redistributed and a higher voltage offset, by $Q = C(\Delta V)$.
 - Imply use the smallest MOSFET device that still has a low enough ON resistance for the signal being switched.
 - o Lower C_{Load} , implies higher offset voltage since Q to be redistributed is constant.
 - o Error ($\Delta V_{out,error}$) = $Q_{injected} / C_{load}$. C_{load} are parallel capacitances beyond C_{dg} .

- Charge injection minimized by CMOS Switch.
- [Precision labs series: Understanding switches and multiplexer's features and parameters | TI.com](#)
- [AN-874: Operating the ADG12xx Series of Parts with \$\pm 5\$ V Supplies and the Impact on Performance | Analog Devices](#)



Heat:

- Convection is heat transfer through fluids. Radiation is heat transfer through electromagnetic waves.
 - o Plastic is better at radiation due to lower permeability.
 - o Copper is best metal for conduction dissipation.
 - o Increase surface contact with air to increase convection.
- Higher resistance, and thus power dissipation, at higher temps.
- **Joule's Law:** $P = IV = i^2R \rightarrow \Delta T = kRI^2$. $\Delta T = kRI^2$. $\Delta T \sim KI^2$. Temperature rise is proportional to the square of the current.
- ΔT is inversely proportional to wire volume. $1/V \sim \Delta T \sim KI^2$. To be used with knowledge on application and what is kept constant/changed!

Ground:

- The external system ground: the stable reference at which all electrical components of a larger system are ideally referenced to.
 - o E.g. ground connection on power supply connected to building's supply.
- The internal device ground: the reference point within a specific device used internally. It is ideally stable and equal to the external system ground.
 - o Typically connected to the external system ground with possible filtering or isolation.
 - o More sensitive and susceptible to noise, hence additional filters.
 - E.g. The ground plane on motherboard, referencing internals.
- A node of a circuit maintained at a steady potential that is equal, but not directly connected to GND.

Bridge Circuits:

- A bridge circuit is an electrical circuit that connects two nodes by means of a path between them.
- Half-bridge implies that two switches are used in connecting the 2 nodes. Full bridge, 4 switches.

Low side and High side:

- For half bridge circuits, one may have a switch that connects to some power (high voltage) and then after this switch is the load. Then after the load is a switch that connects to some lower voltage (e.g. GND). The high side switch and low side switch terminology is used.
 - o See Switching Section for more info on specific switches.

Bootstrap Circuit:

- Circuit used in half-bridge configurations to generate high-side bias to drive the gate of the high-side FET.
 - o The high voltage of the source at the output, where $V_{\text{source}} < V_{\text{drain}} = V_{\text{HV}}$, where $V_{\text{source}} \sim V_{\text{drain}} = V_{\text{HV}}$, implies that V_{gate} must be driven to be higher than a supply voltage.
- This gate drive circuit is provided by a bootstrap circuit using a capacitor, diode, resistor, and bypass cap..

High level basic operation:

- The gate of the low-side switch can be turned on and off trivially due to its source voltage of GND (0 V).
- During charging, the low-side switch is ON and facilitates charging of the Bootstrap capacitor. The forward biased diode and resistor drops some voltage, nevertheless, the capacitor reaches a voltage near the supply.
- The voltage at the bootstrap while charging does not turn on the highside switch, with it's source at GND, since there is probably some internal circuitry within the line from the boot strap to the high side gate that turns on/off accordingly when the low side switch turn on / off.

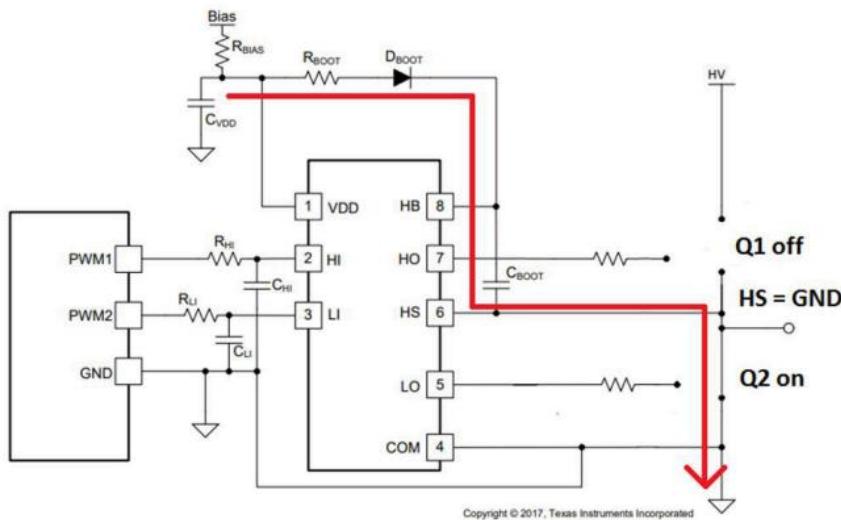


Figure 2-1. Bootstrap Charging Path

- Turning off the low-side switch, and subsequently turning on the high side switch (through some internal switches), the transistor somehow turns on. (This may be done by keeping the source at

GND for a short period, but nevertheless the transistor turns on with the voltage at the charged bootstrap cap.).

- The capacitor then provides a V_{gs} that turns on the high side.
- My inference that the low-side switch stays on for a fraction of a second, and some internal circuitry at HB that turns on, to turn on the high side switch seems to be valid.
- Once Q1 is ON, and Q2 off, first we must recognize that the voltage at C_BOOT and at the bias is now floating.
- Since the source of Q1 is now at $\sim HV$ w.r.t. GND, the floating supply of C_Boot takes on HV + V_boot w.r.t. GND. This floating voltage can now turn on the high side switch!

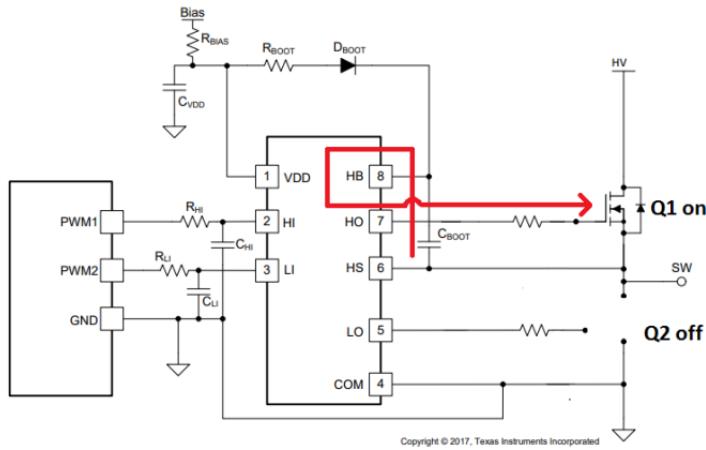


Figure 2-2. Bootstrap Capacitor Discharging Path

- This bootstrap cap should be at least 10 times greater than the gate capacitance of the high-side FET
- bypass capacitor should be sized to be at least 10 times larger than the bootstrap capacitor so that it is not completely drained during the charging time of the bootstrap capacitor.
- *"When the HS pin (switch node) is pulled to a higher voltage, the diode must be able reverse bias fast enough to block any charges from the bootstrap capacitor to the VDD supply. This bootstrap diode should be carefully chosen such that it is capable of handling the peak transient currents during start-up; and such that its voltage rating is higher than the system DC-link voltage with enough margins."*
- The resistor is essential in limiting the peak currents through the bootstrap diode at start-up and limiting the dv/dt of HB-HS? (high-side floating supply to the return high-side floating supply).
 - Tune $RC = TAU$ (time constant).
- [Bootstrap Circuitry Selection for Half Bridge Configurations \(Rev. A\) UCC27710 620-V, 0.5-A, 1.0-A High-Side Low-Side Gate Driver with Interlock datasheet \(Rev. B\)](#)
- [an296220-bootstrap-supply.pdf 8372.AN-6076.pdf](#)

Floating Voltage:

- A floating voltage is any voltage that is not connected to a fixed voltage.

- Imagine a 12 V power supply. Until it is connected, it is floating. This 12 V supply can supply an infinitely high voltage depending on the voltage reference it is connected to, e.g. "Grounded" at infinite.
- Just imagine a voltage that is not connected to a fixed voltage as (floating), and as a voltage supply, that is absolute and independent of what its connected to.

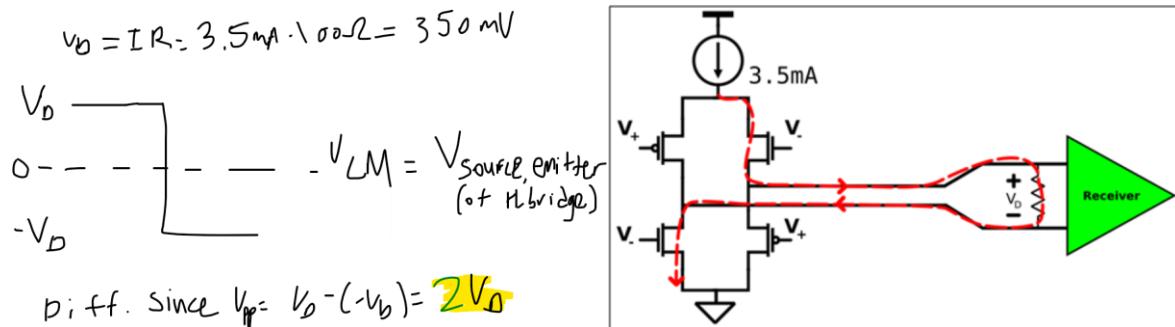
Oscilloscope:

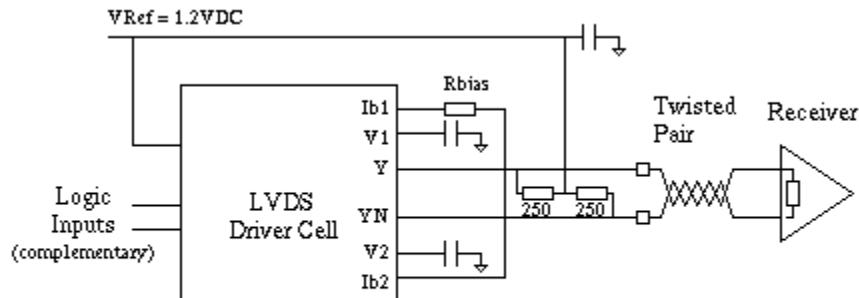
- Set triggers to set the signal at a certain trigger point to remove scrolling, yielding good signal reads.

Differential Signaling:

- Headroom => 2x.
- A balanced line uses two balanced conductors to become less susceptible to common mode noise with close conductors and possibly twisted pairs. Both lines have equal impedance to ground.
- Differential signaling uses complementary/ "a-difference-of" voltage signals to increase headroom for signaling, this increases digital threshold, which decreases noise interdependency.
- The difference from the 2 complementary signals is read as the signal.
- Driver(transmitter)-Receiver Pair on PHY layer.
- In differential signaling: Skew is the misalignment of the two sides of a differential pair as they arrive at the receiver.
- Parallel termination resistor value is determined by the geometry and spacing of the two conductors, the dielectric material, and the return path. For a tightly coupled pair, the differential impedance is typically: $Z_{diff} \approx 2 \cdot Z_{odd}$
- o Z_{odd} is the impedance of one conductor when driven differentially (with the other conductor carrying the opposite signal).
 - Implies $Z_{odd} = 50,60$ for lvds.

LVDS:

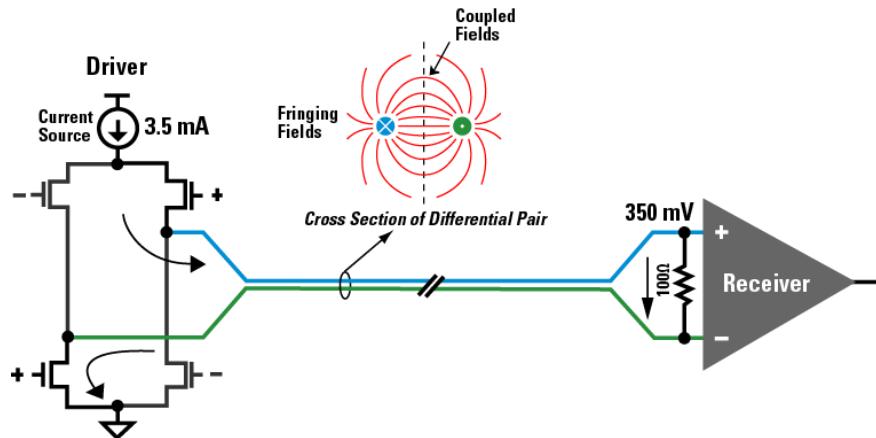




LVDS Driver – Application Example

- A technical standard, not a communication protocol.
- The LVDS driver includes a constant current source that provides a steady current of approximately 3.5 mA.
 - o $VD_{drive} = 3.5 \text{ mA} \times R_t - VSS$ (GND in the right photo).
 - o The common mode voltage is the VSS.
 - The above statement doesn't appear to be true.
- Low-voltage differential signaling (LVDS) is a signaling method used for high-speed transmission of binary data over copper. It is well recognized that the benefits of balanced data transmission begin to outweigh the costs over single-ended techniques when signal transition times approach 10 ns. This represents signaling rates of about 30 Mbps or clock rates of 60 MHz (in single-edge clocking systems) and above.
- LVDS is less noisy than saturating CMOS logic.
- The termination resistor (stub) should be placed as close as possible to the receiver to minimize the stub length.
- **Termination resistance provides voltage drop-differential** for differential signaling (with driver current).
- Low voltage difference/swing (350 mV) implies low power consumption.
- Bandwidth of 1 Gb/s at 10-15 m.
- For typical implementation: Tx at 3.5 mA from a push-pull current mode driver, reaches termination resistance of 100-120 to reduce reflections.
- Receiver input of high impedance, so “all” current flows through termination resistor.
- Receiver input can tolerate $\pm 1\text{V}$ ground shift between driver and receiver
 - o Low common-mode voltage (the average of the voltages on the two wires) of about 1.2 V.
 - o Receiver will have a common mode range of 0.2-2.2 volts. Even with different ground potentials from different power supplies of transmitter and receiver, signal can be received properly.
 - o Receiver threshold of $\leq 100 \text{ mV}$ (implies any difference greater than 100 mV can be read in diff. signaling). Implies 6 dB of loss possible from original 350 mV (from traces, etc.).

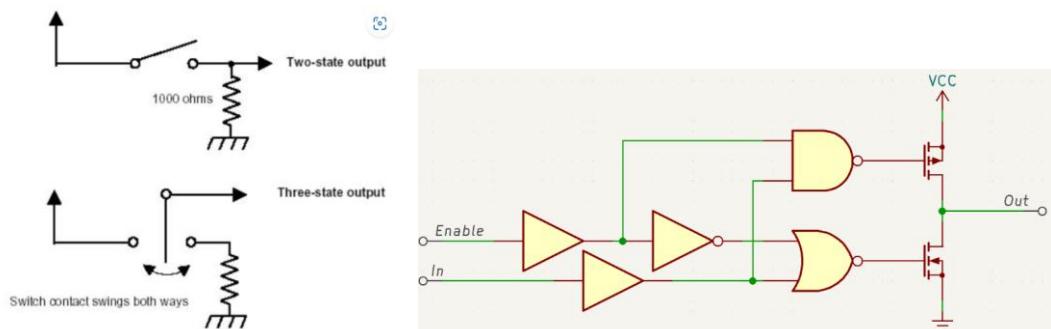
- Balanced line with tight electric- and magnetic-field coupling reduces the generation of electromagnetic noise. This noise reduction is due to the equal and opposite current flow in the two wires creating equal and opposite electromagnetic fields that tend to cancel each other.
- For LVDS and CAN, a reflection dissipator resistor is placed that is approximately 100 ohms. This matches the characteristic impedance of twisted pairs (and creates differential).
- Impedance matching decreases reflections which increase the integrity of the signal.



- [https://youtu.be/nngsse6AO8 An Overview of LVDS Technology](https://youtu.be/nngsse6AO8)
- [Understanding LVDS \(Low Voltage Differential Signaling\) - HardwareBee](#)

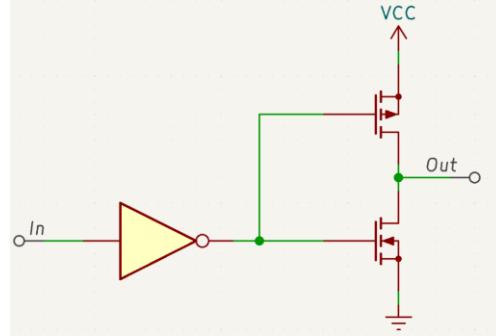
LVC MOS:

Three-state Logic:



- A type of digital buffer with 3 states: HIGH output, LOW output, high impedance.
- Used for bus-based systems where multiple devices connected to a bus, hence the need to separate interference of outputs and inputs from each unit on the bus.
- When a device transmits, it sends its digital signal, receives, or in the HI-Z state to allow other devices to access the bus.

- A standard **push-pull** output, but both the high side and low side output transistors are separately controlled to let them either output a signal in push/pull mode or keep both off; requires some coordination.



- In the high-impedance state, the output of the buffer is effectively disconnected from the output bus, hence no interference of buffer output to other signal outputs.
 - o High-Z state prevents short circuits if one device drives high and one low on the same bus.
- Tri-state logic provides input, output, HI-Z. The input state is independent from the output state.
- Can be implemented using transistors, good design challenge.
 - o BJTs / MOSFET implementation.
- Frequently, CS and OE pins are used to put the output to High-Z, although in different forms.
 - o See more in Oscillator section.
- [Three-state logic - Wikipedia](#)
- [digital logic - What is the advantage of a tri-state output? - Electrical Engineering Stack Exchange](#)

Charlieplexing:

Table 1. The MAX6951 Driver to LED Display Connections

	DIG0/SEG0 Pin 6	DIG1/SEG1 Pin 5	DIG2/SEG2 Pin 4	DIG3/SEG3 Pin 3	DIG4/SEG4 Pin 14	DIG5/SEG5 Pin 13	DIG6/SEG6 Pin 12	DIG7/SEG7 Pin 11	SEG8 Pin 10
LED Digit 0	CC0	SEG dp	SEG g	SEG f	SEG e	SEG d	SEG c	SEG b	SEG a
LED Digit 1	SEG dp	CC1	SEG g	SEG f	SEG e	SEG d	SEG c	SEG b	SEG a
LED Digit 2	SEG dp	SEG g	CC2	SEG f	SEG e	SEG d	SEG c	SEG b	SEG a
LED Digit 3	SEG dp	SEG g	SEG f	CC3	SEG e	SEG d	SEG c	SEG b	SEG a
LED Digit 4	SEG dp	SEG g	SEG f	SEG e	CC4	SEG d	SEG c	SEG b	SEG a
LED Digit 5*	SEG dp	SEG g	SEG f	SEG e	SEG d	CC5	SEG c	SEG b	SEG a
LED Digit 6*	SEG dp	SEG g	SEG f	SEG e	SEG d	SEG c	CC6	SEG b	SEG a
LED Digit 7*	SEG dp	SEG g	SEG f	SEG e	SEG d	SEG c	SEG b	CC7	SEG a

- CC implies common ground

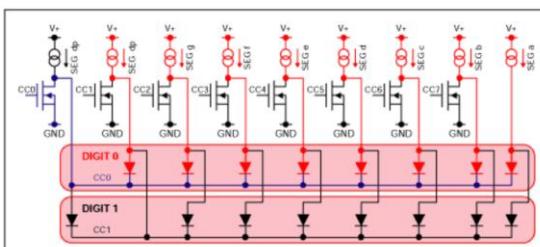


Figure 3. The MAX6951 current flows during digit 0 multiple cycle.

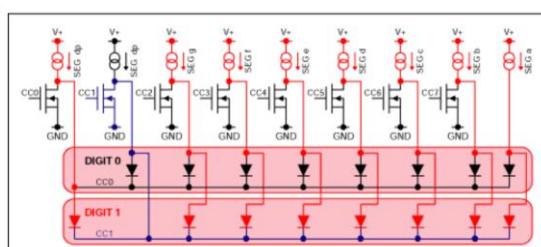


Figure 4. The MAX6951 current flows during digit 1 multiple cycle.

- Maximum reverse bias rating of LED should be greater than or equal to the supply voltage for proper reverse biasing.
- I'm assuming for each digit layout, we replace the segment that doesn't turn on with a higher V_RWM diode, such that it doesn't turn on.
 - o WRONG. A segment can be left off by ensuring that the corresponding pin is set to a high-impedance (Hi-Z) state.
- n drive pins can be used to drive n digits each with n-1 segments
- [Charlieplexing - Reduced Pin-Count LED Display Multiplexing - Application Note - Maxim](#)
- [Charlieplexing - Wikipedia](#) -interesting TBR.

Transmission Lines:

- Interconnects for voltage signals.

Lossy:

- Rise time degradation caused by increased dielectric losses with higher frequency due to dipole movements and increased resistance losses due to the skin effect with higher frequency.

Capacitance:

- Longer transmission lines have higher resistance and capacitance, resulting in slower rise/fall times, which can fall below acceptable/standard.d
- Due to line conductors having a voltage difference from the phase conductors. The phase conductors have a voltage difference between the ground. These conductors are separated by a dielectric like insulation or air.
 - o Gauss's Law: Total electric flux leaving the closed surface = total charge within the volume enclosed by the surface. -> surface integrals = Q_{enclosed} .
- Electric field inside perfect conductor is 0.
- Neutral wire is conducting wire that returns the current back to the source. Ground wire grounds neutral wire.
- Transposition is the exchanging of position of conductors when the spacing between 3-phase conductors are unequal, resulting in unequal flux linkages -> unequal inductances in conductors.
 - o Each phase connector occupies each three positions for 1 third of the line, resulting in equal flux linkage and inductance.
- Switching supplies have a lot of noise due to parasitic capacitance and inductance in effect when switching occurs.

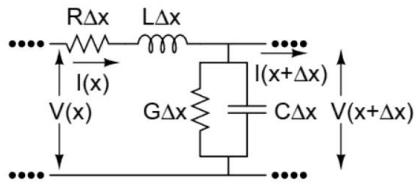
Impedance:

Characteristic Impedance:

- The impedance of a transmission line. The length of the transmission line should not matter since it has been effectively nullified?

$$\frac{\partial V(x)}{\partial x} = -(R + j\omega L)I(x) \quad (1)$$

$$\frac{\partial I(x)}{\partial x} = -(G + j\omega C)V(x) \quad (2)$$



$$Z_0 = \frac{Z_s \pm \sqrt{Z_s^2 + 4Z_p Z_s}}{2} \quad (8)$$

Equation (8) terms of R, L, G and C

$$Z_0 = \frac{(R + j\omega L)\Delta x}{2} \pm \frac{1}{2}\sqrt{[(R + j\omega L)\Delta x]^2 + 4\frac{(R + j\omega L)}{(G + j\omega C)}} \quad (9)$$

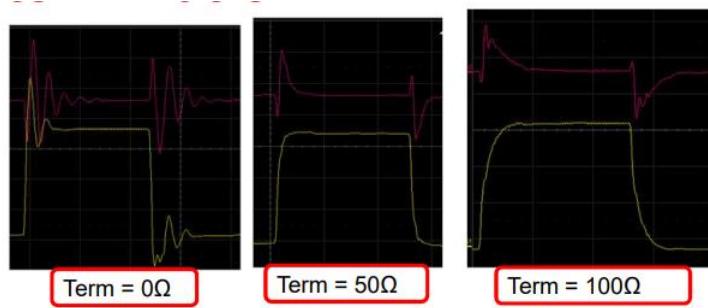
Putting $\Delta x = 0$ in equation (9)

$$Z_0 = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \quad (10)$$

- The characteristic impedance is not dependent on length and represents the “the impedance seen by a wave front traveling down the line”.
- The telegrapher’s equation describes the relationship between voltage, current and the impedance constants of a transmission line.
- In the circuit representing a transmission line above, when $x = \infty$, the series circuit and the parallel circuit are in series. This is used to calculate the characteristic impedance (when $\Delta x \rightarrow \infty$). But then we set $\Delta x = 0$ for some reason to nullify it.
- A lossy transmission line has both resistance and reactance.
- An ideal, lossless transmission line is purely resistive. As transmission lines are modeled to have very low loss, resistances. The characteristic impedance of most transmission lines is effectively resistive. And this is how we add termination resistances (real) to match impedance.
- In PCBs we just assume a lossless 50 ohm real impedance.
- Negative impedance implies voltage and current are inversely proportional; it’s a power source (a component which provides a certain power).
- The characteristic impedance is the sum of the forward and return path impedances of the transmission line.
- A real Z_0 doesn’t mean energy is lost. It means energy is transferred down the line without reflection or storage in reactive elements.
-

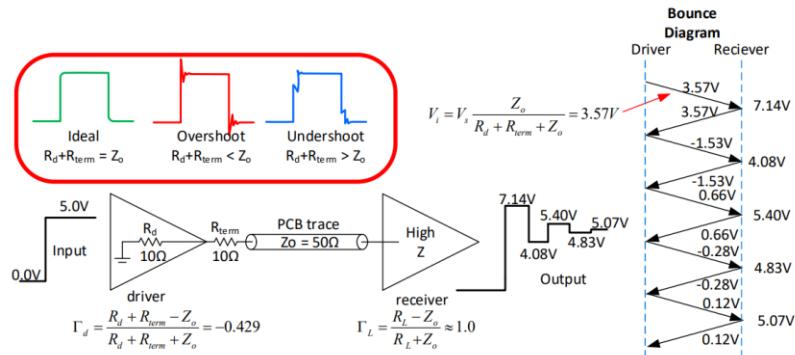
Termination Matching:

- The termination resistor ($Z_{load} + Z_{term}$):
 - o If less than the characteristic impedance, overshoot occurs
 - o If equal to the characteristic impedance, no over/under shoot should occur
 - o If greater than the characteristic impedance, undershoot occurs, this is seen in the form as a lower slew rate.



- When impedance matching with a termination resistor, generally the receiver is the gate of a MOSFET, so very HI Z. At infinite Z, a reflection WILL occur, and the voltage will double. By matching impedances, the MOSFET gate receives ½ of the source voltage, which when reflected will equal the source signal voltage.
- An unmatched termination resistance to the characteristic impedance will cause a reflection whenever the signal crosses this discontinuity. Reflection back to the driver can be assumed to be shunted to ground. Maybe its shunted to ground due to a push-pull topology.
- Reflection to the receiver will not be exactly ½ V_{signal}, so there will be overshoot/undershoot.
- After this ringing of over/under shoot the signal approaches its desired V_{sig}/2 value, since the signal is effectively “dampened” by the R_{term} and Z₀ which produce an over then under signal which oscillates to the nominal.

Transmission line

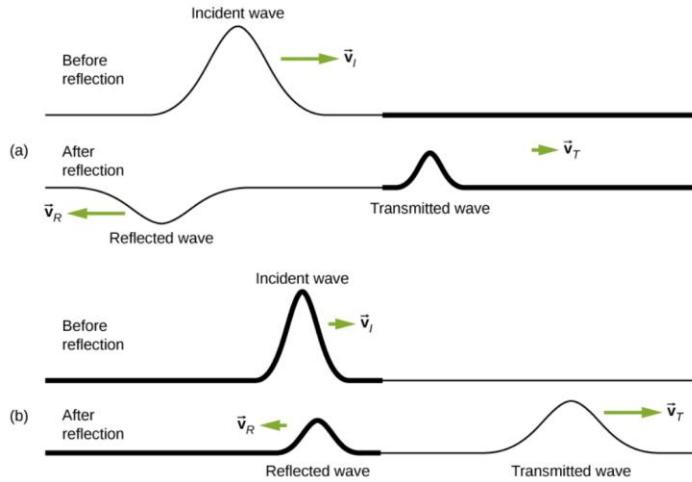


I/O Impedance:

- A low (zero) output impedance is desired so that a change in current doesn't cause a change in voltage, a big voltage drop, across the output impedance.
- A high (infinite) input impedance is desired so that low power dissipation is seen and for better low-frequency response.
 - o Measure of the loading effect.
- Calculated just like R_{thevenin}. Input impedance is in parallel with receiver, and output Z in series, now termination resistors make sense of correcting the I/O impedances to match the characteristic impedance of transmission line.
- The source output impedance is the impedance from the load looking back into the source direction.
- The load input impedance is the impedance from the source looking into the load.

- R_{source} should be accounted for, for R_{out} , by placing the resistor in series with the source.

Reflections



- When an open circuit is met, the voltage (emf) at the open circuit is 2x the source voltage, by superposition, while the current is 0, by superposition.
- If the transmission line ends in an **open** circuit, infinite impedance, all of the incident voltage is reflected. The entire reflected voltage amplitude, EM field energy is reflected and adds to the incident voltage level. This results in double the voltage at the open circuit end of the line.
- If the transmission line ends in a **short** circuit, zero impedance. The reflected voltage subtracts from the incident voltage. All of the energy in the EM field reflects back and subtracts from the incident voltage yielding zero volts.
- See above inverted/non-inverted reflections for impedance changes.
- Applies to both dc and ac currents. Both dc and ac are sinusoidal but, dc is uni-directional and has negligible amplitude.
- Smith chart for impedance matching.
- Basic wave propagation theory

AC/DC:

- 100-240 V for “high voltage” Mains voltage.
- Almost all electronics operate at low voltage DC, <12 V.
- DC voltages aren’t concerned with reflections since they are symmetrical for all time.

OSI Model:

- Differential signaling, LVDS, RS 232, RS 422, are all on the PHY layer of TCP/OSI in transferring data, to process these PHY protocols, high level digital processing is required.

Crosstalk:

- The superposition of signals causing 2 or more signals and receivers in proximity to be imposed on each other or imposed on another's receiver.
- Crosstalk is a feature of copper cables only – fiber-optic cables do not experience crosstalk.
- Higher frequencies and circuit density increases crosstalk.

Parasitic Capacitance and Inductance:

$$C = \frac{\epsilon A}{d} \quad L = \frac{N^2 \mu_0 \mu_r A}{l}$$

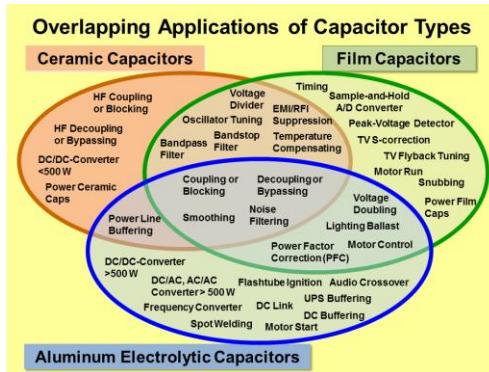
- Parasitic capacitance is everywhere, providing a path for frequencies above the cut-off to be coupled from one conductor to another.
- Parasitic inductance is everywhere, providing HF impedance and voltage offsets in a circuit.
- A longer current path always leads to higher parasitic inductance.
 - o PCB w/ more layers, higher diameter vias.
- The smaller the distance of the dielectric between two signals, the greater the parasitic capacitance.
- Longer wires (unshielded) have more parasitic capacitance, since Area of parallel plates effectively increases, which decreases the current.
- Increased radius of conductor decreases induction. Similar note above.
 - o This is why cable bundling is used.
 - o similar to decreased diameters of vias.
- Increased frequency increases stray/parasitics; miller capacitance. Intuition from high pass filters.
- Surface mount components reduce the effects of parasitics.

Coupling/Decoupling Capacitors (filters and stabilizers):

- Decoupling capacitors filter Voltage rails not data signals.
- "Filtering Technique Isolating Analog/Digital Power Supplies in PLL-Based CDC"
- The value of the capacitor should be such that its resonant frequency is matched to that of the ringing of the voltage spike to create a low impedance AC path to ground for this high frequency noise.
- In parallel from the supply to GND; angular orientation does not matter since parallelism.
- The typical ESL of a decoupling capacitor is on the order of 200nH.
- Capacitors with smaller capacitance should be positioned near noise sources
- Acts as a local charge reservoir that controls sudden changes in voltage and current stabilize.

- Decoupling caps stabilize during a current surge. Acts as a voltage source and current stabilizer.
- Decoupling capacitors filter unwanted frequencies and prevent transients.
 - A change in voltage causes current to flow “into” a capacitor, i.e. charge to be stored in a delayed manner, minimizing the high current damages.
 - The capacitors also delay/stabilize the voltage surge in an exponential manner by releasing the stored charge slowly.
 - When current surges occur from high power loads, the voltage reaching the load(s) is lower, by $V = IR$ & source impedance. Decoupling capacitors decrease the change in current (protecting circuitry) by providing a stabilized voltage (transient protection) charge/discharge!
 - Question: what if voltage stays constant, but current surges? A cap wouldn't charge/discharge? But it would, voltage would drop, and the cap would discharge at a slower current rate than no cap, since $V_C = V \left(1 - e^{\frac{-t}{RC}}\right)$, hence the voltage is less than the nominal voltage.
- A capacitor acts a HP filter, a resistor [RC Network pair] is not needed to filter and shunt HF to GND for filtering
- **Local decoupling cap:** Decoupling capacitor for individual ICs or components that stabilize rapid, HF, lower amplitude current changes caused by switching.
 - Help maintain stable voltage for IC power pins.
 - Minimize ripple.
- **Bulk decoupling cap:** Decoupling capacitor for the overall system power. Provides lower frequency current change stabilization
 - Power supply ramp up and ramp down smoothening
 - Recharges local decoupling and smooths out larger variations.
- A capacitor of higher capacitance stores more charge and by Z_C , has a lower impedance. Therefore, only very low frequencies signals are blocked, and it effectively acts as a High pass filter. The inverse applies to lower capacitance caps..
 - Inherently, bulk caps filter out HF, pass LF noise
 - Inherently, local caps filter out LF, pass HF noise.
 - Therefore include other capacitor values for full filtering.
- Higher frequency implies more reactance by the reactance of a cap, therefore lower capacitances are needed to effectively filter.
 - A capacitor with ESL will resonate at high frequencies due to the effect of capacitance being minimized, with respect to the inductor.
- Electrolytic capacitors have more capacitance, ESR and ESL (decreasing life) than ceramic capacitors. This increases “stability” and damping. Higher ESR means lower frequency decoupling. Lower ESR means higher frequency decoupling.
- A large electrolytic serves as bulk current storage or low-frequency suppression
- Ceramic capacitors are used to reduce interference in the 10MHz to 100MHz range.

- A capacitor in the pico-Farad range is used to limit the higher radio frequencies.
- Ceramic capacitors have low ESR and ESL and can decouple higher frequency noise.



- Coupling capacitors block frequencies below the cut-off frequency as at lower frequencies, the capacitor does not have enough time to charge or discharge these signals, blocking them (given that the time constant is high enough).
- A capacitor can be used to **block quiescent dc** voltages present. Such as on the base or collector from the external circuitry. The capacitor essentially helps in keeping circuitries biased at the desired voltage. It essentially keeps a voltage reference level (w.r.t. gnd).
 - o The cut off frequency is the frequency at when the signal across the medium, like capacitor, becomes attenuated, most commonly, when the signal is attenuated by -3 dB, or to half-power, i.e. a voltage ratio to a fall of $\sqrt{2}$ / 70.7%.
 - o Cut off should be below the lowest frequency to be transmitted.

Determining Custom Values:

- Identify frequency content of noise in the circuit using a spectrum analyzer or Oscilloscope with FFT capabilities (for time->freq domain).
 - o After determining EMI frequency, follow up with Impedance analysis using network/impedance analyzer to find self-resonant frequencies of various decoupling caps.
 - o Select caps with desired impedance properties for noise.
- Modeling using SPICE somehow, when noise is not theoretically predictable.
 - o Model PDN
- Educated trial and error for (further) optimization.
- Noise figure measurement using noise figure meter and Y-FACTOR / GAIN METHOD for noise-frequency spectrum.

Specification details:

- **LIMIT THE CURRENT LOOP [INDUCTANCE] OF THE DECOUPLING CAPS!**
- Large loops emit more RF signals/EMI as well.
- Also, longer distance to a decoupling cap means the signal will get noisier and more polluted
- Place caps as close to the power supply to minimize current loop -> inductance.
 - o Connection inductance is crucial

- With layers, the loop inductance can only be minimized to $2*C$. It is highly affected by trace length, since the length of the via is the most minimized current loop size.
 - Place vias within or near cap pad. To limit connection ind..
 - Place planes as near as possible to (local) decouplers.
- Each active device should have a local decoupling cap; each power voltage a bulk.
- Placing n local decouplers is better than $1 \text{ } nxC_i$ cap since lower overall inductance and better HF filtering.
- Decoupling caps should be greater than the capacitance between the power and ground planes.
- Local decoupling caps have variable, vicinity placement since the ground plane is equidistant from the local plane, hence inductance similar.
- Number of decoupling caps is \sim inversely proportional to the connection inductance of an active device.
- At higher frequencies, the inductance of local decouplers is far more critical than their capacitance.
- For, generally power lines that are electrically long, decoupling caps are more needed due to higher “source” impedance.

Resistors, capacitors, inductors:

- HOW FILTERING WORKS. Resistors and capacitors are filtering/attenuation agents by their ability to stabilize and oppose changes in voltage and currents. By Ohm's law, voltage and current are proportional. Hence:
 - A capacitor uses current to stabilize voltage
 - An inductor uses voltage to stabilize current.
 - By $V = IR$, both voltage and current are stabilized if one is stabilized
 - The resulting stabilization of the line, decreases the oscillatory nature of the signal. Implies how caps and inductors act as filters.
 - Where does this energy go? Energy is stored and released in caps and inductors in this filtering/attenuating/energy storing effect. Ideally, they energy is perfectly stored => no reactive power dissipated, and the energy is released and stored in the components stabilization effects.
 - Power is dissipated through imperfect resistances in the component and the transmission line.
- A capacitor impedance is $-j*XC$ and an inductor impedance is $j*XL$.
- For capacitors and inductors, their real impedance, with ESR and ESL is one where the ideal impedance approximately follows the real impedance during the initial monotonic stage, respective to an inductor or capacitor. The ideal curves will be logarithmically linear, and the real curves will exhibit an approximation of that logarithmically linearity in the beginning monotonicity.
 - Used this knowledge in determining L, or C from *real* L, C impedance curves.

- Resistance causes voltage changes (drops), reactance causes phase shifts. Hence, we use the complex plane to represent phase shift, w.r.t. the imaginary value of a reactive device. No reactance implies no phase shift!

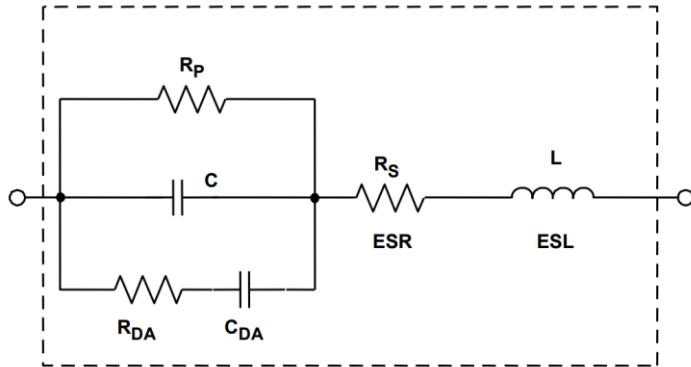
Capacitors:

- A DC level voltage causes the inverted voltage to appear on the opposite plane. Since it is negative, a delta V occurs and current would seem to flow, but the open plate of the capacitor blocks dc level current
- AC level voltages have a 180-degree phase shift on opposite plates. This effectively means no phase shift, as this would just mean a time delay, which is arbitrary to the signal. The AC signal would have a ref. to the EoA of the signal. So current goes through in that charge is going through!
- Current flows into and out a capacitor whenever the voltage changes on each plate; voltage is not driven on to any plate.
- Capacitors store charge and have a voltage smoothening effect. This charge stored has voltage (emf) by $q = cv$. The larger the current the quicker the voltage charging since more charges are stored and thus a greater voltage is being generated as well.
- To store charge and discharge this must be current flow.
- Ac current passes through due to low impedance.
- High capacitive loading causes high inrush currents during start-up.
- Can not have instantaneous change in voltage, implies no infinite current from capacitor.
- When the capacitor is charging, there is a short circuit.
 - o Charge is the number of electrons, capacitance is the capability of the electric field of the capacitor and the ability to store charge and r , and voltage is the emf applied to the capacitor.
 - o In frequency signals, - voltage lags current due to electric field
- Voltage/emf inversely proportional to capacitance because if capacitance high, the more charge required per voltage increase.
 - The voltage at a capacitor always approaches the steady-state (infinite) value

$$V_C = V \left(1 - e^{\frac{-t}{RC}} \right)$$

- A higher capacitance has a slower change in voltage, by $\tau = RC$; though a higher capacitance has higher current flow by $I = C dv/dt$.
- The ESR of a capacitor is inversely proportional to the temperature.
- Aging of a capacitance results in a decreasing of capacitance and a change in leakage current.
- Capacitors decrease bandwidth and slew rate the number of frequencies through filtering and smoothening effects through voltages.
- An RC circuit can act as a timer, with time based on $\tau = R \times C$.
- By the reactance formula and intuitively caps have low impedance to high freq.

- A multilayer ceramic capacitor (MLCC) with X5R, X7R, etc. type of dielectric material has a capacitance value that can drop significantly with dc bias voltage.
 - o Check derating curve.
- There exists a lot of stray capacitances between high-signals and ground (or any lower voltage). This is exacerbated at higher frequencies.

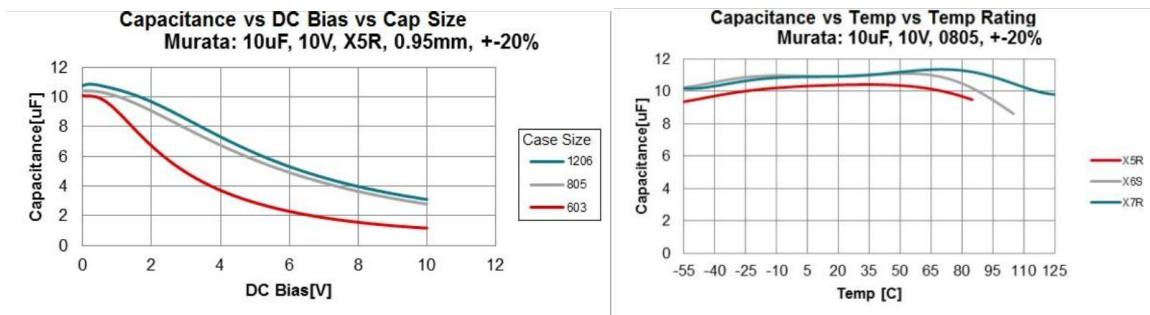


Understanding:

- The voltage on each side of a capacitor is equal and opposite. Hence ac passes, such as for a HP filter.
- The conundrum is then if for a DC bias on a HP filter, voltage on the output would seem to be constantly $-V_{in}$. The reason this is not true and proves that voltage on each side of a capacitor is equal AND opposite, and not just equal, as they assume, is because if the V_R is V_{in} (R to GND), even then, current would not flow, and since current does not flow V_{out} would get pulled to GND, not $-V_{in}$, as voltage 'travels' across 0 current resistor, not an open circuit (i.e. cap plates)!

Derating:

- Derate: (Of a component) to operate at or yield values lower than as rated specifications; for safety and appropriating.
- The derating of a capacitor means that the capacitor will supply a lower current in maintaining voltage (Bad).
- DC voltage biases derating:
 - o Certain dipoles of the dielectric become locked at an external dc bias. These locked dipoles do not react to changes in the electric field (changes in voltage), yielding to lower charge storing => lower capacitance.
 - o Locking proportional to electric field strength (bias voltage).
 - o Implies larger caps have lower dc voltage derating, since larger dielectric width implies lower electric field
- Temperature derating:
 - o Temperature derating is like a very wide, negative coefficient parabola.
 - o Temperature affects capacitance much less than the DC bias derating
 - o A capacitor with higher a higher dielectric coefficient, implies a higher capacitance value, and has a lower temperature coefficient of capacitance (TCC)



- [SSZT654 Technical article | TI.com](#)

Types:

Capacitor material	Pros	Cons
Aluminum	<ul style="list-style-type: none"> • Most commonly used as low-pass filters. • High capacitance available. 	<ul style="list-style-type: none"> • Polarized. • Large size. • Large equivalent series resistance (ESR) values. • May overheat. • Limited lifetime. • Large leakage currents.
Tantalum	<ul style="list-style-type: none"> • Small footprint. • Long lifetime. • Low leakage current. 	<ul style="list-style-type: none"> • Polarized.
Ceramic	<ul style="list-style-type: none"> • Nonpolarized. • Very small size. • Minimal ESR values. • Low cost. • Low tolerances. • Thermally stable. 	<ul style="list-style-type: none"> • Limited selection of high capacitance. • DC bias derating.

- Monolithic: (of a solid-state circuit) composed of active and passive components formed in a single chip
 - o Monolithic Capacitors: unified, one-piece structure. Tantalum, Aluminum, Ceramic dielectrics.
- Electrolytic:
 - o Can "dry out" over time, leading to increased ESR.
 - o ESR generally specified at 120 Hz since electrolytic caps are commonly used in power supplies, where the ripple frequency is often around 120 Hz (twice the mains frequency of 60 Hz).
- Ceramic:
 - o Wide temperature range, high capacitance, small size
 - o Piezoelectric nature.
 - o Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best inductor ripple current performance.
 - o This guide provides information on the temperature coefficients of ceramic capacitors. [Understanding Ceramic Capacitor Temp-Coefficients - Passives / Capacitors - Electronic Component and Engineering Solution Forum - TechForum | DigiKey](#)
 - o ESR generally specified at 100 kHz, relevant for high-frequency RF, digital circuits.
- Also consider voltage rating of cap.

- Stacked capacitors:
 - o Increased capacitance within small form factor.
 - o Multi-layer ceramic capacitor (MLCC)
- 3 terminal (or feedthrough) capacitors: Decreases the ESL such that the capacitor impedance more so behaves as an ideal capacitor up until a higher frequency. On a impedance vs freq plot, it shifts the minimum more so along the ideal cap. impedance line. Effectively creates a better filtering capacitor with higher insertion loss. Inductance impedance line shifted to the right and lowered (ROC) basically.
 - o Insertion Loss: The ratio of the signal level without the filter (component) installed to the signal level with the filter (component) installed.
 - o Shows the attenuation/filtering ability of a filter. higher is better.

$$\text{Insertion loss (dB)} = 10 \log_{10} \frac{|V_1|^2}{|V_2|^2} = 20 \log_{10} \frac{|V_1|}{|V_2|}$$

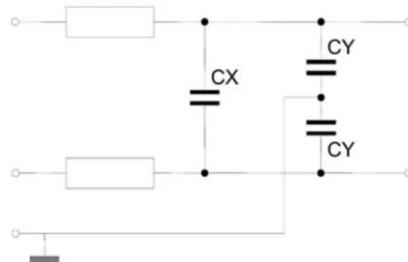
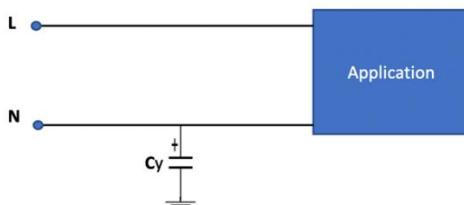
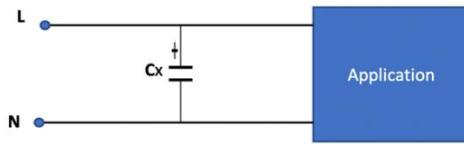
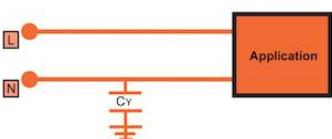
- X-Y Capacitors:
 - o X capacitors to filter our differential noise; y capacitors to filter common mode noise.

Safety Capacitor Classifications

Class X Capacitor (Line - to -Line)



Class Y Capacitor (Line - to -Ground)



- [Front.PM6](#) 3 vs 2 terminal cap. Very good!
- [The difference between monolithic capacitors and ceramic capacitors - Tempero Systems Shopping](#)

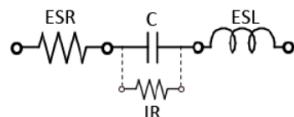
AC Coupling:

- Block DC, opposite side of voltage source is driven (usually a GND value).

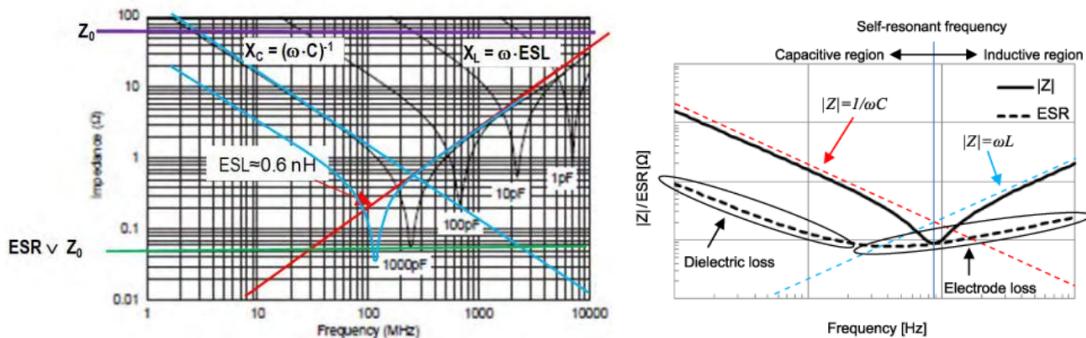
- Frequently used in multi-gigabit data links (PCIe , Ethernet) to offset incompatible common mode voltages between driver and receivers.
- PCIe:
 - o Each lane of a link between corresponding transmitter and receiver must be AC-coupled.
 - o The transmitter common mode voltage can be non-zero, but the receiver's DC common mode voltage must be 0V.
 - o Allows independent biasing of transmitter and receiver.
 - o The transmitter may use RC time constants to detect the presence of a receiver at the end of a lane, and to detect an insertion or removal of a receiver.
 - o Isolates the driver and receiver's grounds from each other
 - o 0402 sized caps are as big as you should go for PCIe blocking caps, package size and induction below.
 - o PCIeExpressElectricalInterconnectDesignfromIntelPress (2004)
 - o [high speed - Why place inline capacitors on PCIe traces? - Electrical Engineering Stack Exchange](#)
- It may be in vain looking for caps with high resonant frequencies (<10pF), while low frequency data preservation (0.1-4.7 mF), power supply decoupling caps and hope is sometimes all.
- [VPPD-02901.pdf](#)

Impedance:

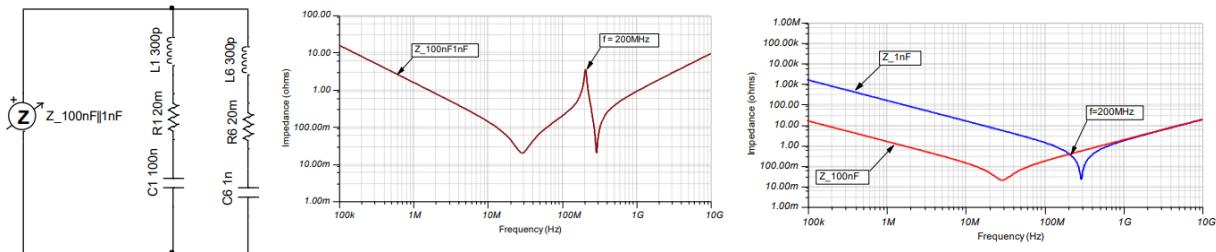
- Higher capacitance implies lower impedance (in the capacitive region).
- A real capacitor possesses an ESR and ESL, with the capacitance. Therefore, impedance of cap. is sum of ESR + ESL + $Z_C (1/j\omega C)$.



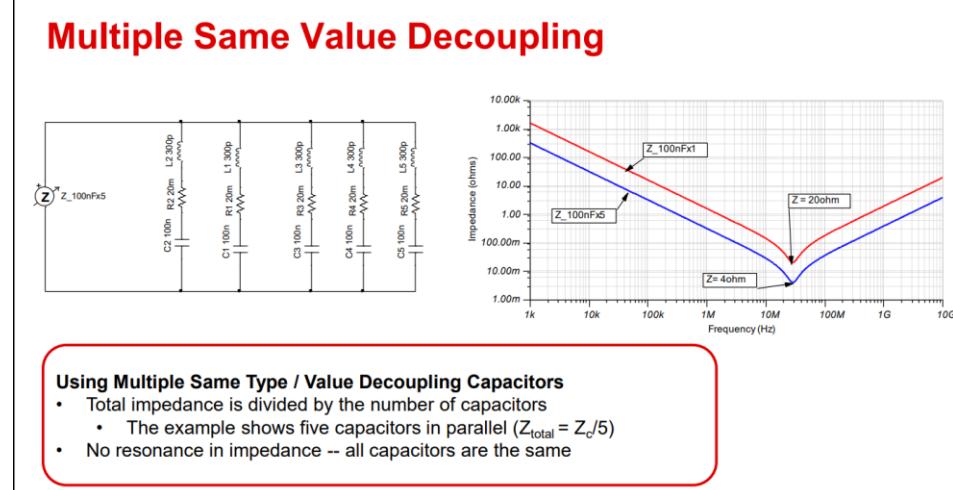
- The value of R is large enough to be unimportant (especially in ac signal)
 - o ESR is smaller relative to total impedance in ac signals.
- ESL is largely dependent upon package size and construction, not upon capacitance value.
- Both capacitance and inductance (ESL) are inversely proportional to the resonance frequency
- Impedance of Cap. determines the frequency response – noise suppression + filtering.

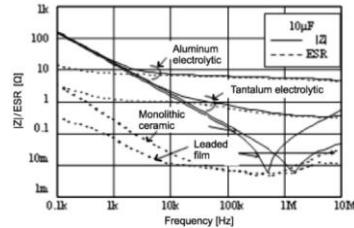


- Red: Impedance of Capacitor. Blue: Impedance of ESL. Black: Impedance of ESR.
- ESR: caused by dielectric and electrode impedance, which are “felt” only at threshold frequencies. Dielectric in capacitive region, electrode in inductive region.
- Low-frequency region: ESR is relatively high due to dielectric losses.
- Near the self-resonant frequency: ESR reaches its minimum value.
- High-frequency region: ESR increases again due to parasitic inductance the loss of its electrode metal.
- At the **minimum**, the capacitor is at the **self-resonant frequency**; $|Z|$ (Impedance) = ESR.
- The region below the self-resonant frequency is called the capacitive region and the region above is called the inductive region.
- Impedance is small over a wide frequency band in SMD-type MLCCs, making them best-suited capacitors for high-frequency applications. Right line in plot below.
- At lower frequencies, the ESR is dominated by dielectric losses, at higher frequencies by the skin effect.
- Using different valued capacitors can cause a resonance peak.

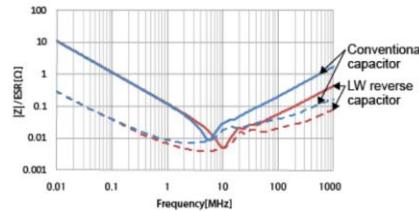


- Using same value decoupling shifts the impedance down. ESR decreases in parallel. Higher C, implies impedance from capacitance decreases, shifts to the left. Lower L, impedance from inductance decreases, implies inductance shifts to the right. So, a vertical translation down occurs.





- Film capacitors and ceramic (or MLCC) capacitors exhibit low ESR, due to metallic electrodes.
- An LW reverse capacitor with a short length l and large width w has even minimal ESR.



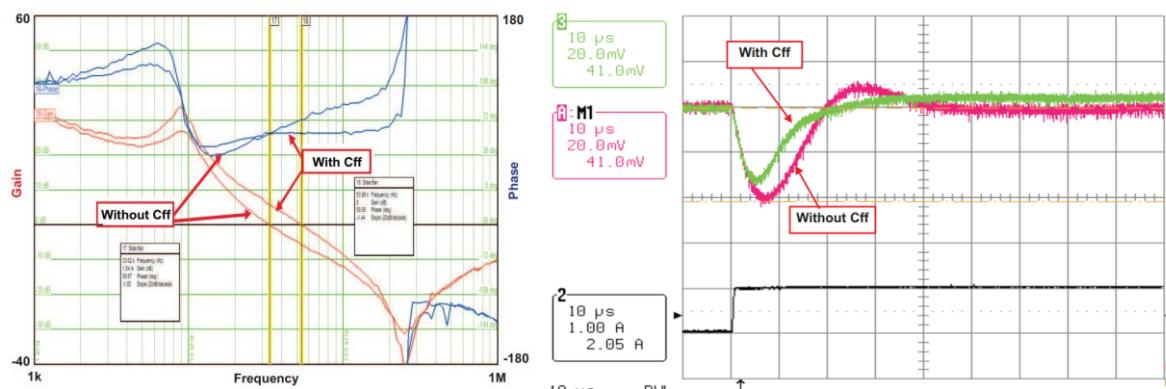
- Skin and proximity effect
- [What are impedance/ ESR frequency characteristics in capacitors? | Murata Manufacturing Articles](#)

Calculating ESR:

- [Calculating capacitor ESR from Tan\(δ\)- Passives / Capacitors- DigiKey TechForum- An Electronic Component and Engineering Solution Forum](#)
- Described at a certain frequency, typically 100 kHz for SMPS.

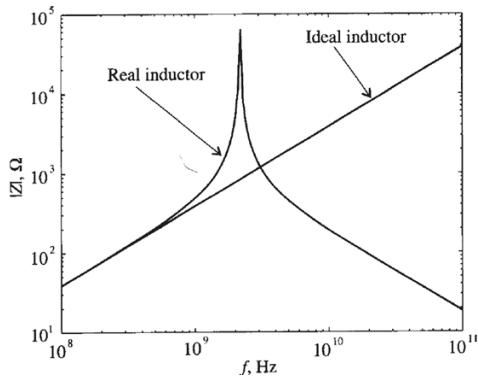
Feedforward Capacitors:

- Look into more if using it.
- Capacitor place in parallel to high side resistor for a feedback network.
- Based on capacitor and resistance, one can alter the response and stability.
 - o Phase margin and bandwidth improves.



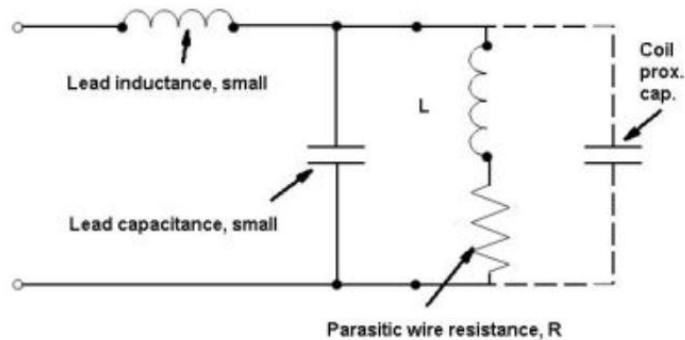
- [Feedforward Capacitor to Improve Stability and Bandwidth \(Rev. A\)](#)

Inductors:



- “The self inductance of a wire is about 25 nH/inch.”
- Current lags voltage due to magnetic field.
 - o This lagging of reactant elements is due to the phases of increasing and decreasing frequency signal.
- When current is increasing, emf being stored in magnetic field, hence an opposition.
When current decreases, emf released, yielding voltage.
- Can not have instantaneous change in current, implies no infinite voltage.
- Inductance is proportional to inductor size. Rate of change of current across an inductor is inversely proportional to inductance; inductance represents the strength of opposition to current, can store more energy in magnetic field, v.v. for capacitors.
- Inductors have high impedance to high freq. current.
- A nonlinear inductance can occur due to saturation with direct current.
 - o The inductance value may drop noticeably with increased load current, especially for a ferrite bead type of inductor
- There exists a lot of parasitic/stray [inherent] inductance since, generally, any net or lead forms some sort of closed loop with itself and “GND”, i.e. some reference, in a circuit. Power, ground, output leads.

Equivalent circuit of a wire-wound inductor



- Inductors have losses through the DC resistance of the coil, the inductor core losses through eddy currents and hysteresis.
- When the temperature rises above the Curie point, the ferrite (a possible inductor core) loses its magnetic properties, and becomes paramagnetic, rendering it useless. The Curie point is material dependent, ranging from 120°C to 500°C.

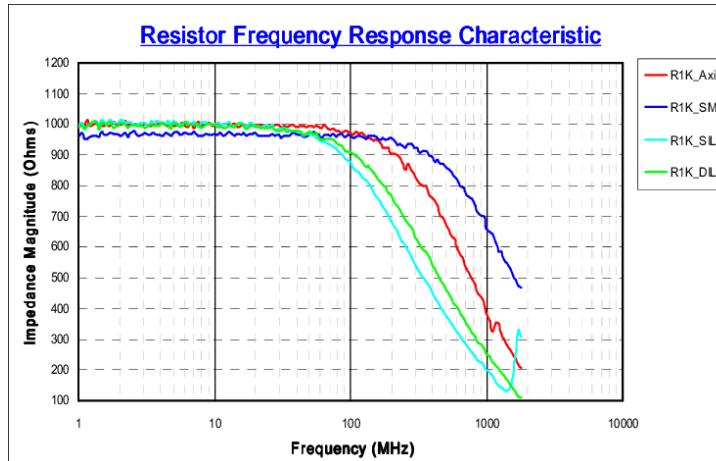
Shielded Inductors:

- As its name implies, a ferrite-shielded inductor consists of a coil wound around a ferrite core with an additional ferrite shielding layer around the whole assembly to contain the magnetic field. This approach gives the highest level of shielding.
- Shielded inductors shield the inductance and magnetic field of an inductor to prevent it from coupling to associated interconnects, limiting the inductance of a system, and therefore noise.
- [Do I Need a Shielded Power Inductor.pdf](#)

Saturation:

- Applied DC current drops an inductor's inductance below its measured value w/ no dc current.
- Operating an inductor beyond the saturation knee is dangerous because the inductive impedance drops significantly and an uncontrolled rise in current can occur.
- Caused by the core reaching maximum flux density. The magnetic domains become fully aligned and the permeability of the core is reduced, hence inductance decreases. In saturation, the inductor can store less energy and the ripple current increases, reducing efficiency.

Resistors:

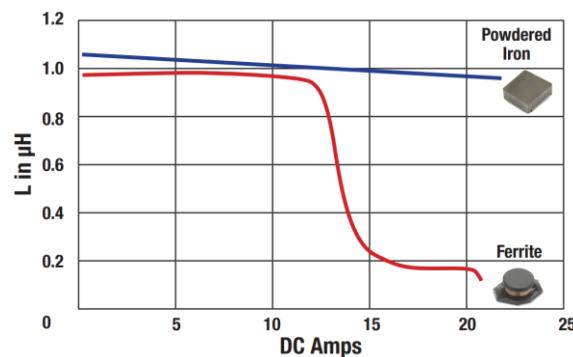


- An increase in resistance implies higher noise susceptibility and higher (thermal) noise.
- Resistors dampen oscillations by absorbing voltage and decreasing current. Resistors should be used in parallel with inductors for low-pass (DC) filters to help attenuate the signal and coincide with the inductor in decreasing the amplitude of the dc (full-wave) signal.

- Resistors are impedances that are constant over most of the frequency range.
- Resistor in series are less impactful if small value, large value for resistors in parallel.
- Pull down resistors are in parallel with the load, hence they don't prominently increase current draw from the source if high enough.
- Pull up resistors are in series with the load, hence they don't prominently effect the power transfer if low enough.
- I2C p.u./p.d. are a different realm of capacitive loading and speed due to high impedance input gates.

Current:

- Devices with negative resistances, such as those outputting constant power, have a decrease in current/voltage with an increase in voltage/current. This is important since most devices do not have a negative resistance; so, an increase in voltage/current generally leads to an increase in current/voltage.

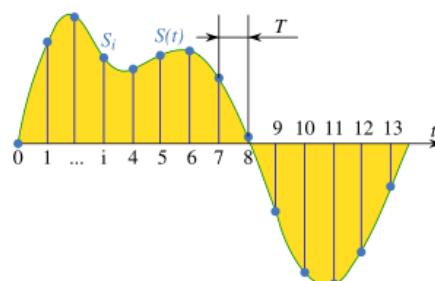


T-resistor Network:

- Provides a lower Thevenin resistance which means that the voltage gain on the offset voltage will be lower. This is better for achieving accurate output and one that does not saturate.
- Provides the same negative feedback current to the capacitor. The T network provides a high impedance, low current path, since there are parallel resistors with the higher one back to the cap and the lower one to gnd.
 - o Heat dissipation though!

Nyquist (folding) Frequency:

- A characteristic of a sampler, i.e. a continuous-time function \rightarrow discrete-time based function converter. Blue dots are samples.



- For a given sampling rate (samples/s), Nyquist frequency (cycles/s) is frequency at which the period is 2x the period of the sampling rate. Implies 0.5 cycle/sample.
- $2 \times \text{Nyquist Frequency} = \text{Sampling rate}$.
- When the highest frequency (bandwidth) of a signal is less than the Nyquist frequency of the sampler, the resulting discrete-time sequence is free of aliasing distortion. Implies *sample rate above Nyquist rate* for the signal.
- [Nyquist frequency - Wikipedia](#)

Filters:

Basics:

- An ideal filter has a fixed amplitude response of k for the frequencies of interest (*pass band*) and zero elsewhere (*stop band*).
 - o The transition from pass to stop is nowhere ideally instantaneous
- *Cutoff frequency*: the frequency at which the filter response changes from pass to stop.
- If a high-pass filter and a low-pass filter are cascaded, a *band pass filter* is created. The UNION of the two are the pass band. The complement is the *band-reject/notch filter*; takes the complement of the two.
 - o all-pole configurations (i.e. no zeros in the transfer function) will not have ripple in the stop band.
- **Each pole gives a -6 dB/octave or -20 dB/decade response. Each zero gives a $+6 \text{ dB/octave}$, or $+20 \text{ dB/decade}$ response**

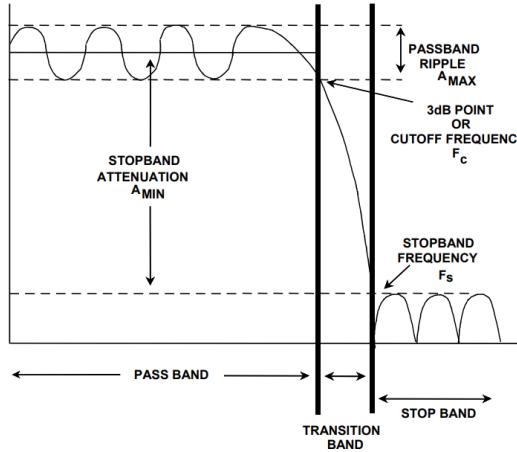


Figure 8.2: Key Filter Parameters

Application:

- The term "corner/cutoff frequency" refers to the -3 dB point on the frequency response curve.
- The impedance of a filter denotes a relationship with the amount of filtering in an inversely proportional relationship. That is, a higher impedance filter will filter less and vice versa.
 - o Higher impedance implies higher gain (undesirable for filter).
- The output impedance of the filter must be far lower than the input impedance of the SMPS to not modify the SMPS loop gain, i.e. to avoid oscillations (noise).

- More damping for a better frequency response, and reducing the peak output impedance/gain, increases the amount of components (bad).
 - o Good damping compromise between size and performance is $\zeta = 1/\sqrt{2} \rightarrow 3 \text{ dB}$ attenuation at corner/resonant frequency.
- Network of passive components, caps, inductors, resistors, that provide attenuation to signals within a certain bandwidth.
- Non linearity of passive components are seen, especially at higher frequencies
 - o At HF, the dielectrics of capacitors are nonlinear.
 - o Of magnetic materials, permeability is inversely proportional to frequency.
 - o B-H curve of electromagnetic is non linear.
 - o As a magnetic core approaches saturation, the demand for magnetising current increases significantly
- Demarcation (determination of boundary) of LF to HF is relative; defined: when the parasitic components cannot be ignored and become important enough to affect circuit operation.
- An n-th order filter will have a stop band roll-off at $n \cdot 20 \text{ dB/decade}$ or $n \cdot 6 \text{ dB/octave}$ as the operating frequency increases above the cut-off frequency, f_c .
- An **n-th order filter has n reactive components** and a maximum phase shift of $n \cdot 90^\circ$ degrees.
- [Microsoft Word - EDCh 8 filter.doc](#)
- [Input Filter Design for Switching Power Supplies](#)

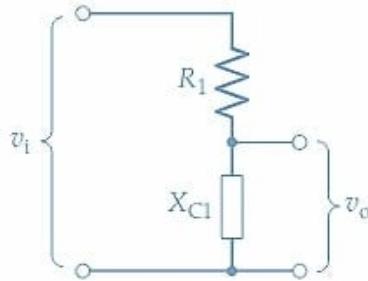
[Impedance:](#)

- A big proponent of filtering is in impedance control. The impedance of the filtering section should be much lower than the impedance of the load.
- Current takes the path of least impedance. Hence the load impedance must be higher than the filter (noise-current shunting) impedance – i.e. the parallel capacitor.
- For a series capacitor, for direct blocking, not shunting, of noise, the load impedance must be lower such that lesser of the series capacitance coupling of ac noise (changes in voltage) occur.
- Learned that noise will couple from the EMI filter to the load due to current taking the paths of least resistance, i.e. exploring all paths. No full shunting or blocking of noise.
- This is to prevent noise from coupling into the load and, by superposition, affecting the gain of the DC-DC converter in purpose.

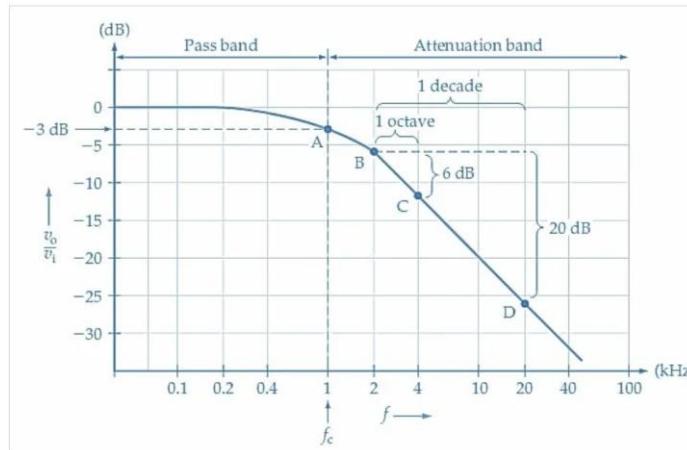
[Resonant Frequency:](#)

- The resonant frequency is when the feedback of the signal is in phase with the original signal causing the superposition and summation of the feedback and incident signal to sum and yield a positive gain. The positive feedback loop yields a gain of infinity if undamped.

RC Filter/Operations:

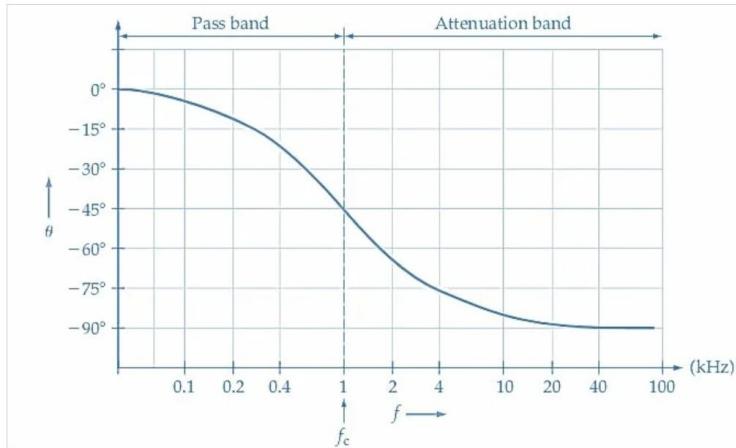


- This would be an RC-Integrator.
- $F_{-3\text{db}} = 1/2\pi RC$. The attenuation at a frequency f_a can be approximated by: Attenuation = f_a / f_c OR f_c / f_a depending on if f_a is smaller, or larger.
- The frequency response for RC filter is rather good, but the roll off is much less steep than an emi filter, thus for HF use emi filter!
 - o No resonance which is fortuitive.



(a) Gain/frequency response for low-pass filter

- Generally, speaker, a Butterworth filter is worth 5 RC filters.
- For a resistor-capacitor voltage divider, the phase shift at the divided output varies from 0 to -90 degrees depending on the Frequency, which affects the impedance level of the capacitor.
- Zero at low signal frequencies where $X_C \gg R$. As the signal frequency increases, the (lagging) phase shift gradually increases to -45° at f_c , and then continues beyond f_c to a maximum of -90.



- Considering the input & output impedance of an RC LP filter, just consider R. It is the worst-case input and output impedance. See impedance section on how to compute these impedances.
- RC filter rolloff is -6 dB/octave or -19.93 dB/decade since it is a first order filter with only 1 reactive component in the cap.

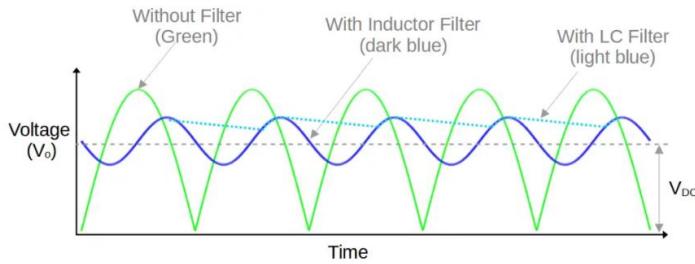
f_c :

- An important approximation is such that when you want to make dc gain of an op amp close to unity (with the noninverting amp config), this is fortuitous in only causing ac gain.
- When $f = 1/2\pi RC$, $Z_R = Z_C$, since the cap is reactive Z_C would ideally (at high enough freq, for a 90 deg. Phase shift) be at $(Z_R / \sqrt{2}), \sqrt{Z_R} / \sqrt{2}$. This means that gain = $1 + \frac{1}{2}$ (noninverting amp config implies a unity in the gain) ~ 1 for DC.

LC Filter Learnings (about inductors and capacitors):

- Voltage and current are directly proportional (given that there is a resistance, which is guaranteed in the real world and with filters for a load).
- Something to understand is that frequency associated with forward voltage can be filtered by reducing the amplitude; hench the inductor filter!
- Alternating current signal have sinusoidal voltage and current. Due to the sinusoidal voltage, a sinusoidal current is generated because of this linearity above.
- Inductors have impedance to current (& voltage). If a change in current exists, the inductor will generate an emf to counteract this change. This emf will oppose the change in current and decrease/increase the voltage at the load/source. As a result of this generated voltage due to the change in current, the voltage at the load is attenuated.
- The voltage change across an inductor is proportional to the change in current. In a rectified signal which has an inductor-symbol shaped graph, the resulting voltage (& current) is a sinusoid.
- One must realize that voltage and current is directly related and proportional to realize how changes in current result in changes in voltage for an inductor and v.v. for a capacitor.

- A capacitor stores charge which results in emf (as that's what voltage is, a potential difference), when a change in voltage (& thus current) is seen, the emf of the cap shunts current and voltage to stabilize.
- Note that for inductors and capacitors in PURE DC, it will take time for them to even reach their steady state current/voltage, not only for ac signals with LC filters.



- [LC Filter - Electronics Reference , Low Pass Filter- Explained](#)

EMI Filter:

[EMI Filter Design](#)

Summary of Key Equations

Parameter	Equation
Cutoff frequency	$f_c = \frac{1}{2\pi\sqrt{LC}}$
Inductance	$L = \frac{1}{(2\pi f_c)^2 C}$
Damping resistor	$R = \sqrt{\frac{L}{C}}$
Attenuation at f_s	$A(f_s) = 40 \log_{10} \left(\frac{f_c}{f_s} \right)$

$$C = \frac{1}{\omega_C R_d} \quad L = \frac{R_d}{\omega_C}$$

- The above formulas have f_c or ω_c as the pole or frequency. The above formulas solve for a Butterworth type rolloff filter and are a crux of understanding the individual components.
- A Butterworth filter is not necessarily a Pi filter.
- To use lower valued, smaller components (/ 2):
 - o can change structure from single-ended to balanced L.
 - o can change to a Pi filter structure.
- Used to reduce conducted emissions (typically), or limit inrush current (voltage collapses) and suppress voltage transients (ESD).
 - o Most effective filter for KHz to low MHz noise.

- For a switcher, PWM power supply, there exists an incremental negative input resistance to the input of the overall switching circuit.
- Key factors that will impact the filter in terms of performance, characteristics of source and load, filter size and weight, cost.
 - Form factor limitations and mechanical constraints
 - Mounting types/packaging needs
 - Environmental conditions (temperature, shock, vibration, moisture)
 - Electrical characteristics (voltage, current, capacitance, insertion loss)
- Before EMI filter design, understanding the harmonic composition of the switching current can be done with a simulation model to obtain a frequency spectrum sweep. Then use this spectrum with the dB amplitude limit requirements to search for the insertion loss.
- The dB_{uV} scale is typically used for EMI filters, because it provides the best scale for small-signal noise.
 - $1 \mu\text{V} = 0 \text{ dB}\mu\text{V}$
 - $1 \text{ mV} = 60 \text{ dB}\mu\text{V}$
 - $1 \text{ V} = 120 \text{ dB}\mu\text{V}$
- The (negative) resistance of a switching regulator is $R_n = - |V_{in} / I_{in}|$.
 - Negative since power is kept constant, thus inverse rel. between V & I.
- If the pole-q (cutoff) frequency is too low to be feasible for a n-pole structure, an N-pole structure is used ($N = n + 2a$).
- The harmonic current can be defined through the **fundamental peak amplitude**. Where I_{pk} is $2 * I_{av}$ for a square wave at 50% duty cycle. Where I_{av} is just the average current draw by V_{in} and P_{out} , and with efficiency divided (since voltage is constant, current must increase for constant power).

$$I_{av} = \frac{P_{out}}{V_{in}\eta} \hat{I}_p^F = \frac{2}{\pi} (I_{pk})$$

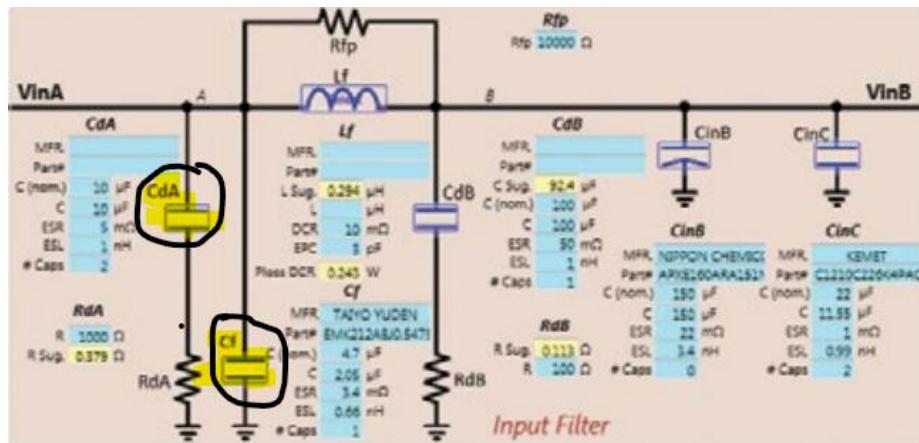
- With the above harmonic current value, attenuation at a certain frequency can be determined, with the known current harmonic desired, by calculating the dB gain/att. Value.
 - We're taking the max harmonic and calculating the attenuation to the desired value s.t. the filtered harmonic now has a max harmonic value at the desired. Effectively a vertical shift.

- The characteristic impedance of the filter should be less than impedance of SMPS, and is

$$|Z_o| = \sqrt{\frac{L}{C}}$$

determined by , since it consists of ideal passives. This value would represent the filter impedance when calculating L, C.

- The
- A dual L pi filter is **the most effective filter for KHz to low MHz noise**
- Filters can take 25% of electronic system. EMC standards and noise-sensitive components require noise filtering.
- Before switching:
 - o Reduces conducted EMI from the switching components (transistor, switching inductor, cap) from reaching back to the power supply.
 - This noise can travel in both directions: towards the load and back towards the power source.
 - o Filters HF noise caused from switching before reaching power supply, and then to others.
 - o Effectively, noise is either absorbed by the inductor or always shunted to ground by the capacitor. And the differential/common mode noise doesn't reach the load, only traveling in its own loop.

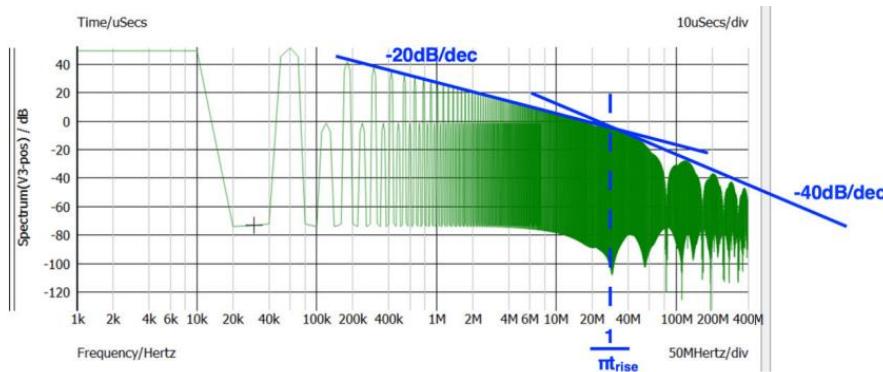


- In general, choose a damping capacitance, CdA, that is around two to four times the real filter Cf value.
- When adding an input EMI filter in front of a switch-mode supply, the filter output impedance, ZOF, can interact with the supply input impedance, ZIN, causing undesirable oscillation. To avoid this unstable situation, the magnitude of the EMI filter output impedance, ZOF, should be much lower than the magnitude of the supply input impedance, ZIN, with enough margin.
 - o $|Z_O| \ll |R_n|$.

- Note that R_n is the smallest under high load and low input voltage; can play around here is plausible.
- For filters with ≥ 4 poles, ensure each LC section has $Z < R_n$.
- Middlebrook extra element theorem.
- For high Q, the -3 dB cutoff frequency is approximately the resonant frequency. At lower Q, the cutoff frequency is at a higher f than the resonant frequency.
- Insertion loss formula (trivial): Same as all gain/att. Formulae.

$$IL_{dB} = 20 \log_{10} \left[\frac{V_1}{V_2} \right]$$

- After switching:
 - Filters EMI to ensure cleaner output power to sensitive loads.
- $1/\pi t_{rise}$ is the frequency at which the filter insertion loss/ attenuation changes from x to y, e.g., from -20 dB/decade to -40 dB/decade.



- The Q factor and Zeta are inversely related by the following equation.
 - Q representing how underdamped a system is; Zeta representing the damping (how overdamped).

$$Q = \frac{1}{2\zeta} \quad \text{or} \quad \zeta = \frac{1}{2Q}$$

- The actual power supplied to the device through the filter is restricted to the fundamental frequency.
- The shorter power lines start taking on their characteristic impedance at much higher frequencies, due to lower losses. The characteristic impedance of power lines vary significantly; characteristic impedance varies with frequency and is not as constant as that of coax, twin lead, and twisted pair. The characteristic impedance of the open wire-type typically varies between 50 and 180 ohms due to the spacing between the conductors and the diameter of the wire.

- [AN-2146 Power Design for SDI and other Noise Sensitive Devices \(Rev. A\)](#)

Calculating Pole-Q (-3 dB Cut-off) Frequency:

$$\alpha = 10 \log_{10} \left[1 + \frac{\omega_s}{\omega_c} \right]^{2n} \triangleq 20 \log_{10} \left[1 + \frac{\omega_s}{\omega_c} \right]^n$$

- Attenuation (alpha, NOT IN DB, in unitless *factor*) value should be known already from above steps. Where ω_s is the frequency of interest (switching frequency). Where n is the order of the filter; ω_c is the half-power [-3 dB] pole-Q frequency, as desired.
 - o Formula based on Butterworth design.

$$\alpha = 20 \log_{10} \left[\frac{f_{-3dB}}{F_{pwm}} \right]^2 \triangleq 40 \log_{10} \left[\frac{f_{-3dB}}{F_{pwm}} \right] \Rightarrow f_{-3dB} = \left[\frac{F_{pwm}}{10^{\frac{\alpha}{40}}} \right]$$

- Where F_{pwm} : F_{sw} , order of filter: exponent (for us 2nd order here), a (alpha): attenuation in dB.
 - o The attenuation should be positive since we are designing for a -3 dB cut off.
- The cut off frequency may be equal to the resonant frequency: $1/(2(\pi)\sqrt{LC})$.
- This pole-q freq. value for thus calculating L, C.
- What broke down why resonant and cutoff frequency is “equal” is since: “At the resonant frequency, the filter will have a voltage gain such that the output voltage is Q times the input voltage”. At -3 dB cutoff, power is halved, or voltage/current is divided by $\sqrt{2}$. That means Q should be $1/\sqrt{2}$, this precisely matches the critically damped Q! So, in our Frame of Reference of a Butterworth, this is extremely fortuitous.
 - o **When a filter is critically damped, the resonant frequency = -3 dB cut off frequency.**
 - **Implies a Butterworth filter.**

Q:

- Q factor represents how underdamped a system is.
- Inductor:
 - o The filtering inductor, i.e. the low pass element. Q assumes a real model of an inductor with a series ESR.
 - o It is a ratio of inductor reactance [inductance] to resistance, which are in series in real model.

$$Q = \frac{j\omega L}{r_{DC}}$$

- The Q of a capacitor is the, $Q = \text{Capacitor Reactance} / \text{ESR}$.
- Accounting for both L and C of an LC EMI filter gives a system Q of:

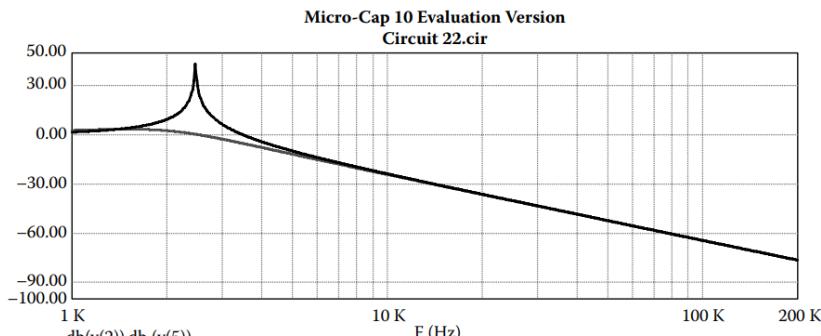
$$\frac{1}{r_C + r_L} \sqrt{\frac{L}{C}}$$

- Where the reactance is represented by the characteristic impedance. Simply a ratio of reactance/resistance, hence, represents damping.

Damping:

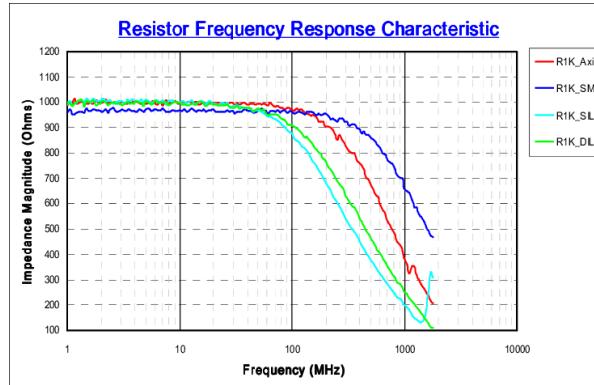
- Typically, we want to aim for a filter Q of 1 or less.
- At the resonant frequency, the filter has a voltage gain that the output voltage is Q times the input voltage, and this may create overvoltage issues with power conversion circuits.
- Input and output impedances are also affected by filter-Q. If Q is greater than 1, the input impedance will be lower than the characteristic impedance of the filter. Furthermore, the output impedance of the filter will be greater than the characteristic impedance. In both cases, the mismatch in impedance relative to the characteristic impedance is a factor of Q. These factors necessitate that the filter be suitably designed for optimal Q where $Q \leq 1$.
- Implies: the input impedance of the filter is the **Filter Characteristic Impedance / Q**. The output impedance is **Filter Characteristic Impedance * Q**.
 - Want $Q \leq 1$. Implies want input impedance to be greater/equal to filter characteristic impedance. Want output impedance to be less/equal to filter characteristic impedance.
- Relating to the pole-q frequency, the cutoff frequency is equal to the resonant frequency. This can be problematic at high Q, which is present inherently in passive LC filters, since it is the resonant frequency. As a result, we need damping components to bring down Q.
- In altering Q, the impedance of the filter will change by the added passives. This tells me that we must work around our known L, C to accommodate the existing cut off frequency while adding L, C to specifically damp and lower Q.

C-R:



- Shunt series RC network in parallel with filtering cap.

- The idea is to add a capacitor with a capacitance 3-5 times higher than the filtering capacitor, and a resistor, before the capacitor, of resistance equal to the characteristic impedance of the LC filter (without the added damping cap).
- The idea is:
 - o A high capacitance will have a lower impedance to HF signals.
 - o The higher capacitance with the existing filtering caps will increase the overall capacitance.
 - This shifts the resonant frequency of the circuit to a lower frequency.
 - This is actually good since then the added damping capacitor will have less impact on the lower resonant frequency.
 - o At lower freq., the RC network will have higher ac impedance due to the damp resistor, hence not altering the resonant frequency unexpectedly.
 - o At higher freq., the RC network has low ac impedance and effectively shunts and damps the HF noise; see below plot on attenuation of a resistor.

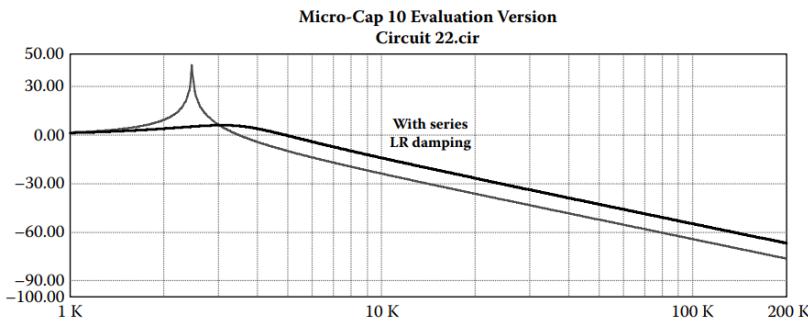


- o By making the damp capacitor large, and since we have the resistor, we basically are able to damp HF noise, and not affect the signal at LF, but the resonant frequency is nonetheless shifted to the left.
- Note: with above steps the damping takes effect at a frequency below the resonant/cutoff frequency, so there *is* a bit of alteration to the cutoff frequency.
- Angular freq. which the rc network takes effect is:

$$\omega_d = \frac{1}{R_d C_d}$$

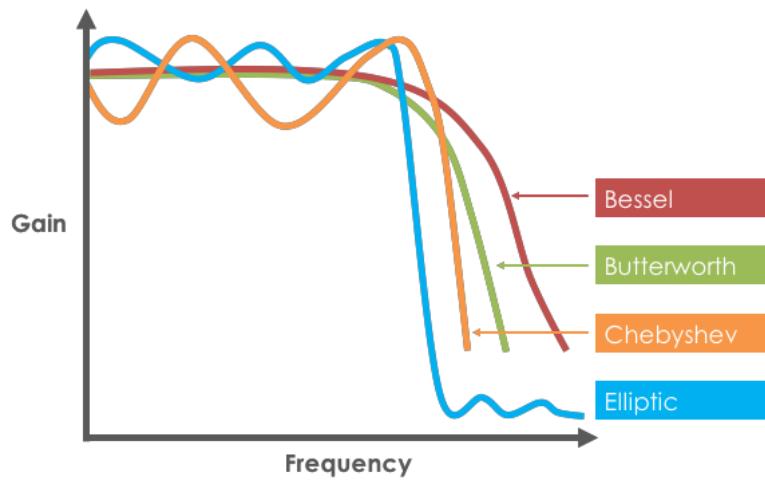
- The problem with RC damping is such that a large cap is required which requires space & +cost, and thus is unideal => LR damping!

$L // R$:



- To allow the parallel R_d to damp the filter, inductor L_d should have an impedance magnitude that is sufficiently smaller than R_d at the filter pole-Q frequency (cutoff frequency).
- The damping resistor must have a DCR much greater than the ESR of the filtering L. **10 – 100 X.**
- Idea (equivalent to RC damping):
 - o The damping inductor in parallel decreases the overall inductance/impedance of the filter network. This will increase the resonant frequency to the right.
 - o The idea is to block LF with the damping resistor and shunt HF through to damp HF.
 - o The damping resistor is chosen such that its R is much higher than the filter inductor's parasitic R , and hence, LF noise will see Hi Z at the RL network and pass through the filtering inductor, not the damping inductor.
 - o The damping inductor is low such that HF noise can shunt through to be damped by the damping resistor and RL network.
 - o Why put the damping inductor then? And that is why we don't have one in our Topologies!!!

EMI Filter Topologies:



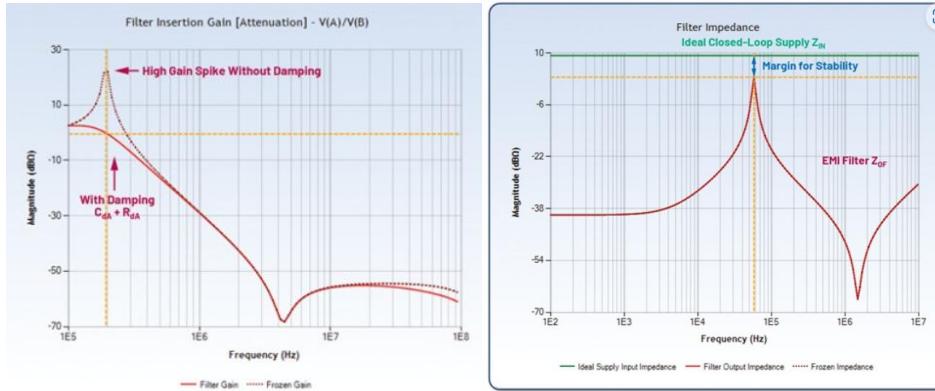
- A maximally flat response, or Butterworth shows that $Q = \zeta = 0.707$.
- A Butterworth filter has $Q = \zeta = 0.707$, by definition.

CMC:

- Impedance = $2(\pi)F_{swL}$. Find frequency and impedance in graphs to solve for L of CMC.

Resonant Frequencies (of LC circuits):

- At (and approaching) the resonant frequencies of an LC circuit, the LC circuit's ability to attenuate signal SIGNIFICANTLY decreases while the impedance SIGNIFICANTLY increases.
 - o Make sure the input impedance to the load is lower than the (output) impedance of the emi filter.



- To attenuate this resonant peak, a pair of optional **damping components** CdA and RdA can be added in parallel with the filter capacitor Cf.
- [Speed Up the Design of EMI Filters for Switch-Mode Power Supplies | Analog Devices](#)

Diode vs. transistor; reverse-current controller:

- The forward voltage drop of the Schottky diodes results in significant power loss at high currents and increases the need for thermal management using heat sinks and a larger PCB space. Forward conduction loss and associated thermal management reduces efficiency and increases system cost and space.
- This leads to using mosfets as ideal diode controllers. Though current can flow both ways through a mosfet inherently, as opposed to one for a Schottky diode.
- [Basics of Ideal Diodes \(Rev. B\)](#)

Transients:

- Inductive (voltage) transients caused by parasitic inductance and capacitance and switching supplies. A diode can be used to shunt the current and voltage by the inductance.
- It is generally not the voltage in a transient that causes damage, but the excess current. This can be seen in transistors and how decoupling capacitors both source current and delay voltage surge in voltage transients.
- A current transient, due to the source impedance, the voltage at the load drops. This dangerous drop in voltage is prevented and subsidized by a decoupling cap..

- Must use a diode to dissipate voltage transients in inductor and transistor systems to avoid the transistor reaching the breakdown voltage, as these inductive transients can reach very high.
 - A TVS.
- This application note explains the voltage + currents of transients: [tvs-diode-overview-application-note](#)

Corona discharge:

- caused when Electric field > dielectric strength of air, causing an electrical discharge and ionization of air.

Arcing:

- Electricity jumping across typical insulators due to p.d. and created connection.
 - The degradation of insulation materials due to environmental factors like heat, moisture, or chemical exposure
 - High humidity can lead to condensation on electrical components, creating a conductive pathway for arcing.
 - Dust accumulation can also act as a conductor, bridging gaps between contacts
- Induced currents can cause voltage spikes such as with EMI currents.
- [Understanding and Preventing Electrical Arcing: Causes and Types - DesignHorizons](#)

Backplane board:

- A carrier board which allows insertions and has connectors for edge computing and integration of different System on Modules.
- The motherboard of a computer
- Hot insertion/swapping
 - Risks: False clock edge generation. If SCL hi on backplane, initial inrush current will fill parasitic capacitance of slave. This may cause the slaves' clock to become out of sync due to this additional clock edge.
 - Risks: Based on the power-up ramp-up requirements of I2C devices, the parasitic capacitance/inductance between the connected slave and backplane may have a ramp rate outside of the required Vcc ramp rate to power up properly. (Not in min, max range). This may result in the slave powering up to an unknown state, e.g. SDA low, SCL locked.
 - [I2C Solutions for Hot Swap Applications \(Rev. A\)](#)

Nets & Buses:

- The net is all the continuous connection between all nodes within the connection. It is all the metal that is connected in a system, including the return path.
- Net: A connection between two components
- Netlist: A representation showing all the nets between all the components of a circuit.

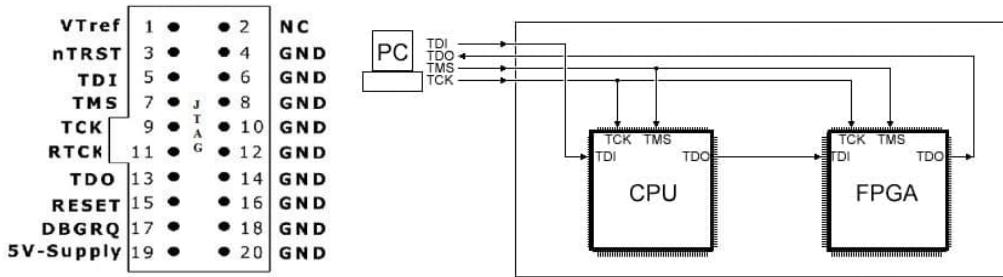
- Essentially, a representation of an electronic circuit. Schematic -> layout.
 - Physical arrangement not considered.
 - Used for simulation.
- Schematic Netlist: netlist derived from circuit schematic for layout
- Structural Netlist: netlist derived from lower-level components like transistors and FFs.
- Electronic Bus: “For All”. A connection for the transport of a group of signals.
 - Parallel: Signals/bits are divided into lines and pins for their own purpose.
 - **Problem:** all lines must arrive to a component (of a single CLK) within the appropriate time interval with the CLK. Implies equal signal propagation time or delay-logic implementation.
 - Bus width grows with signals used.
 - This increases the number of pins + traces, EMI, and the PCB size.
 - Serial: Signals/bits can be processed in series on one line of a bus.
 - Variation in signal propagation aren't problematic
- The instances (components) used in circuitry and how and what nodes they are connected to.

PCI Express:

- Based on high-speed LVDS connections.
-

JTAG (Joint Test Action Group; IEEE 1149):

- A boundary scan test that tests the interconnects between different components – chips- on a PCBA.
- JTAG builds functionality into the IC to assist in testing PCBAs without using test probes.
- Boundary-scan cells (w/ muxes and latch circuits) embedded in the chip to capture and force data from the pins.
- JTAG TAP (Test Access Port) controls the signals and shifts in and out the serially data and asserts test results.
- Tests BGA faults, which are difficult to detect and diagnose without JTAG. Data is serial.
- JTAG is used for everything from testing interconnects and functionality on ICs to programming flash memory of systems deployed in the field and everything in-between
- BSDL (Boundary Scan Description Language) led to fast, automated test development.
- Consist of test program generator for test development and test program executive for running test and reporting results.
- [JTAG Tutorial](#)



Types of Resets:

- System Reset: the SRST hardware signal resets all chips connected to the JTAG adapter.
- JTAG TAP Reset: the TRST hardware signal resets the TAP controllers connected to the JTAG adapter. Invisible to the rest of the system; resetting a device's TAP controller just puts that controller into a known state.
 - o TRST is an optional pin in the JTAG interface. The Test Access Port (TAP) can be controlled completely via the TMS and TDI pins, and for simpler chips, this is all you need. TRST simply provides a quicker way to put the TAP controller into a known state for more complex chips.
- Emulation Reset: many devices can be reset through JTAG commands. These resets are often distinguishable from system resets, either explicitly (a "reset reason" register says so) or implicitly (not all parts of the chip get reset).
- Other Resets ... system-on-chip devices often support several other types of reset. You may need to arrange that a watchdog timer stops while debugging, preventing a watchdog reset. There may be individual module resets.
- [Reset Configuration \(OpenOCD User's Guide\)](#)

Packaging:

- Chip Scale Packages (CSPs) can control impedance.

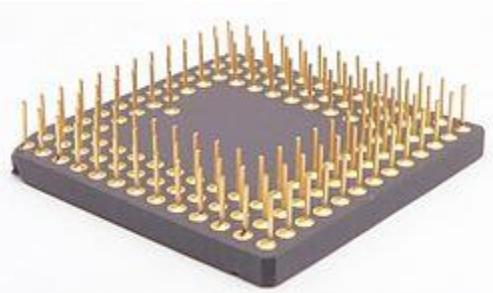
Lead Frame:

- A metal structure inside a chip package that carries signals from the die to the outside.
 - o The die sits on a pad in the lead frame
 - o The leads, the metal conductors branch out from the die. The leads are cut and bent into the desired shape depending on the packaging.
 - Copper, gold, aluminum.
 - o Small wire bonds connect the die to the leads through bond pads on the die and lead.
- A plastic case is molded around the lead frame to protect the wire bonds and expose only the desired leads to be connected to outside.
- Lead frame structure doesn't imply leads sticking out, but implies the structure that which the die can be connected to outside.

Pin-Grid Array:

- Type of IC packaging with pins on the underside of the package in an array (pitch is usually 2.54 mm / 0.1 inch)

- Usually mounted through through-hole holes-mounts.
- Allows higher pin counts (than DIP)



Ball-grid Array:

- Chip packaging technology used in high-technology, compact, high pin-out chip designs with a grid pattern of solder balls at IC base. high pin count (>300).
- Provides heat dissipation.
- Short (think parasitic cap and ind), spherical connection points at base save lateral-surface space and allow for cavities for heat dissipation.
- BGA package variants alter the substrate of the chip. Substrate: The material that is the layer in between the PCB and IC silicon die. It provides layers, vias to distribute signals.
- Epoxy overmold,
- Substrate can provide heat dissipation.
- [Microsoft PowerPoint - Freescale PBGA Presentation-Q1'08.ppt What Is BGA \(Ball Grid Array\) Packaging? - TechSparks](#)

Quad Flat Package (QFP)

- a surface-mount IC package featuring "gull-wing" leads/pins extending from all four edges.
- Standard in large-scale and very large-scale integrated circuits. With the pin count being over 100
 - o Very efficient and reliable -> ideal for packaging central processing units.
 - o Tiny parasitic parameters, making them ideal for high-frequency applications.



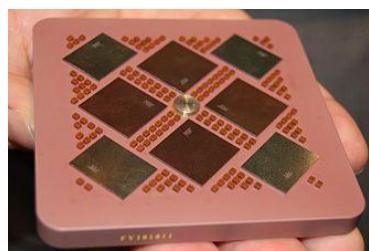
Quad Flat Package No-Lead (QFN):

- [QFP vs. QFN: Difference Between QFP and QFN – PCB HERO](#)

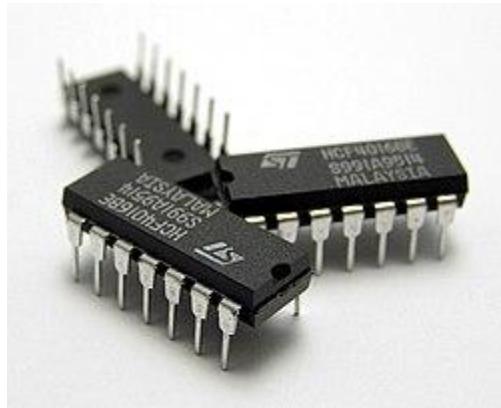


Multi-Chip Module (MCM):

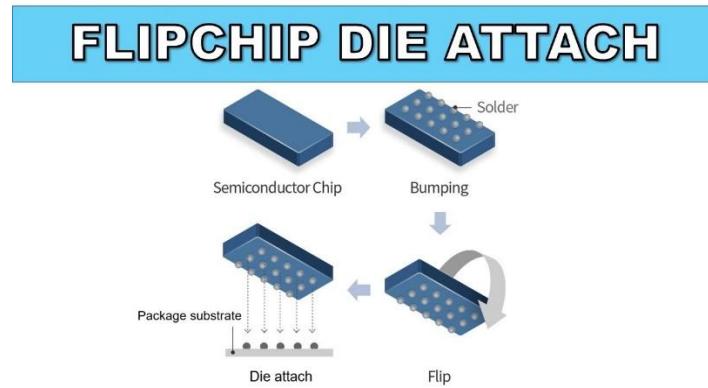
- An electronic assembly where multiple integrated circuits, semiconductor dies and/or other discrete components are integrated, usually onto a unifying substrate, so that in use it can be treated as if it were a larger IC for modularity and/or to improve yields over a conventional monolithic IC approach.
- May use flip chip technology



Dual In-Line Package:



Flip Chip Attach Process:

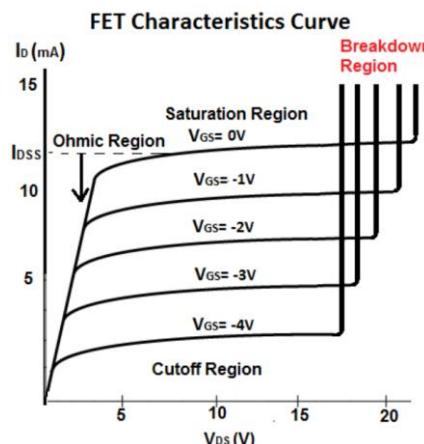


LGA (Land Grid Array)

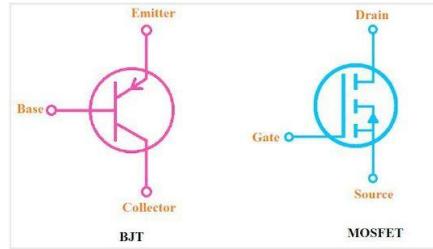
- Uses a grid of contact pads, or lands, to connect the IC package to the PCB, not have solder balls.
- The connection between the package and the PCB is achieved through a compression force applied by a socket or a clamping mechanism.
 - o Soldering not needed.
 - o Replacement is easier
- Improved thermal conductivity and heat dissipation compared to BGA.

Transistors:

- Mosfet transistors can have adjustable V_{DS} saturation voltages through transistor sizing while in Bipolar transistors the saturation voltage is fixed
 - o Implies equal/unequal common mode voltage ranges from V_+ and V_- of supplies of Bipolar vs cmos designs of amplifiers.
- Breakdown voltage is the voltage across terminals where the transistor may break or cause an exponential increase in leakage current across the junction, if current capacity is exceeded, the transistor will be burned. Generally nondestructive, only increase current can overheat junction.



- NPN AND nMOS have greater conductance than PNP and pMOS, due to lower resistance and smaller sizes.
- Bipolar junction transistors are bipolar in that there are two currents Emitter-Base and Emitter-Collector that facilitates the switching and amplification. FETs are unipolar transistors in that there is 1 current Source-Drain that facilitates switching and amp..



BJT:

- The V_{BE} vs I_{CE} relationship (diode; Ebers-Moll), emitter-base internal resistance, the amount of DC bias of the input signal play a major role in the final voltage amplification ratio.
- h parameters, current gain, is very sensitive to temperature changes. E.g., in common emitter configuration, h_{FE} can increase by 60% if the temperature climbs from 25 to 100 degrees.

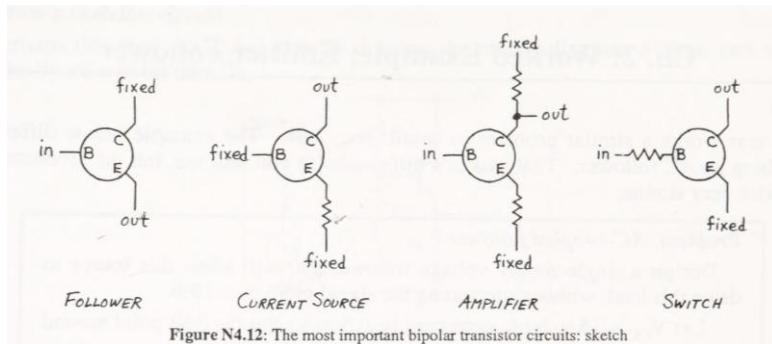


Figure N4.12: The most important bipolar transistor circuits: sketch

- Feedback affects DC levels, but not circuit gain, the signal response, since the seemingly low output impedance of function generator to the base is still way higher than the (high impedance) feedback signal.
- Principles:
 - o Works because of the physical geometry and doping.
 - o A reversed bias p-n junction will increase in its depletion layer size if the voltage across it increases due to higher carrier combination to create matching terminal voltages.
 - o A lower doped p-n junction will have a larger depletion region due to the lower potential difference formed by the diffusion current of the p-n junction to form an opposing drift current to reach equilibrium, i.e. a depletion layer. In both reversed & forward biases, since both have a depletion region.
 - o Transistor power can be calculated as: $P = V_{BE} * I_B + V_{CE} * I_C$.
 - $I_B \ll I_C$, so $P \sim + V_{CE} * I_C$.
 - $|V_{BE}|$ typical is around 0.6 to 0.7 volts for silicon BJTs.

■ Voltage drop: $V_{BE} + V_{BE} = V_{CE}$. I_E , total = $I_B + I_C$

- Think of superposition of small base power and larger amplified EC power.

- Collector:

- The collector is larger for better heat dissipation and transistor performance/durability.
- The collector is less doped than the emitter for a larger depletion region. This decreases the size of the base. And increases the ability of the depletion region to withstand a higher electric field (V_{CB}) due to the larger distance created by the dep. layer, allowing a higher maximum voltage before breakdown.

- Base:

- Thin and lightly doped for higher current amplification (beta value).
- A smaller base current implies a larger collector current.
- Base current is caused by recombination of emitter electrons and base holes; recombination takes some time, especially since hole number is less.
- The p-typed base is electron rich in BJT.
- Thermal diffusion causes electrons to diffuse towards CB depletion region junction when electrons exist and unrecombined in the p-type base.
- There exists a large p.d. from the depletion layer that heavily attracts and forces the electrons in the base to the collector region, if the electrons random-walk to the edge of the CB depletion layer, thus creating the collector current.
- Diodes in reverse bias, produce a current if charge carriers of the opposite sign are placed in a p or n junction e.g. electrons in p-type region.
- Depletion region acts a vacuum region with an intense e-field only repelling the default carriers.
 - Hence, like a triode vacuum tube.

- Emitter:

- Highly doped region for higher current amplification (beta value).

- Saturation:

- 'saturation' refers to the limit of how many base charge carriers flow into the collector region. Majority of collector current is from emitter region, but some from base. Beyond a certain amount of base current, there won't be an increase in the charge carriers crossing the B-C junction, hence saturation.

- [bjt - How do I saturate an NPN transistor? - Electrical Engineering Stack Exchange](#)

- [transistors - Why can current flow through the reverse biased base-collector junction \(N-P junction\) in a BJT with a forward biased base-emitter junction? - Electrical Engineering Stack Exchange](#)

- [transistors - What are the reasons that the emitter is heavily doped in an NPN BJT? - Electrical Engineering Stack Exchange](#)
- [What is the largest region of a Bipolar Junction Transistor \(BJT\)?](#)

Modes:

Saturation:

- Using Ebers Moll model, both junction diodes are forward biased and an increase in base current (called biasing), doesn't increase collector current.
- Saturation occurs due to negative feedback of $R_{\text{collector}}$ and V_{cc} with transistor.
 - o The emitter is tied to ground without an intermediary resistor to ensure V_{be} is more predictable.
- As you increase I_{be} , I_{ce} increases, implies $V_{\text{R}-\text{c}}$ increases implies, V_{ce} decrease, i.e. V_{c} decreases. Implies at some point V_{c} decreases so much that V_{bc} becomes forward biased and an equilibrium is reached where further increases in I_{be} , which increases I_{ce} , decreases V_{c} even more, causing more forward biasing of BC junction, enforcing equilibrium.
- A 'constant' current is present, which can be used as an ON state.
- Occurs when the base current drive is too high, where further increases in base current, through voltage or sourcing, does not increase $I_{\text{C}}/I_{\text{E}}$.

Cut-off:

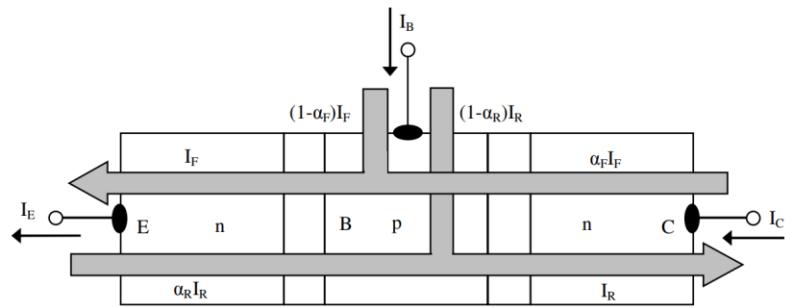
- Both junction diodes are reverse biased and the BJT is not conducting.

Active:

- An increase in $I_{\text{be}} / V_{\text{be}}$ causes and increase in I_{ce} . Amplification.

Reverse Active Mode:

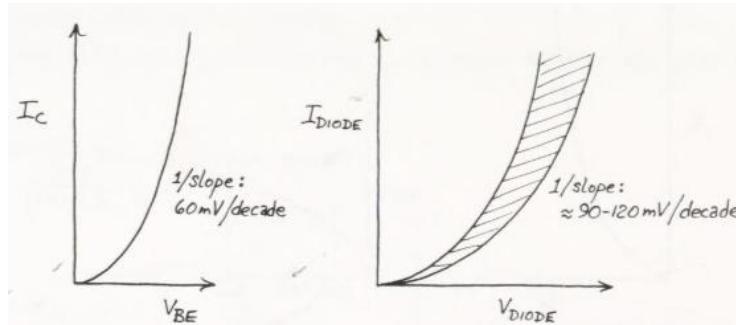
- Forward active mode is the setting of a BJT where the Base-Emitter is forward biased and the Base-Collector is reverse biased. Reverse active mode is when Base-collector is forward biased and base-emitter is reverse biased.
- Forward active mode has a much higher transconductance/gain than reverse mode.
- βR is much smaller than βF due to the relative doping of C and E.
 - o Forward: I_B generally is $(1-a)*I_{\text{CE}} = 0.01*I_{\text{CE}}$; implies a gain of approximately 100.
 - $a = 0.98-0.99$
 - o Reverse: I_B generally is $(1-a)*I_{\text{CE}} = 0.75*I_{\text{CE}}$; implies a gain of approximately 2.
 - $a= 0.1-0.5$.



Combined B-E and B-C Junctions

Ebers-Moll Model:

- Models BJT as 2 diode junctions.
- Models BJT collector current I_C according by the voltage across the base and emitter, V_{BE} ; just a diode.



- Uses an exponential relationship for I_C vs V_{BE} . An 18 mV increase in V_{BE} tends a double in I_c
- r_e , intrinsic resistance in series with the emitter that has a dynamic resistance proportional to the derivative of an exponential $\Rightarrow k\alpha^2 V_{BE}$, since $r_e = V_{BE} / I_C$ is exponential (above).
- The dynamic r_e can vary from -50% to 100% based on the I_C vs V_{BE} relationship (curve). Note: a lower r_e implies a higher I_C and lower voltage gain, since a bigger voltage drop across R_c . Diminishing this variation with a resistor is below.
- This model describes saturation of transistors by the diode that is the forward biased base-emitter junction.

Evidently the value of r_e varies with I_C . Specifically, here's our rule of thumb:

$$r_e = 25 \text{ ohms}/(I_C \text{ (in mA)})$$

- **VT≈25 mV at room temperature.**
- **In the perspective of common emitter, voltage amplification, $G = -R_C / r_e$. Since r_e is dependent on the I_C , the current going through the BJT, by the Eber-Molls modeling I_C as having a dynamic, exponential relationship to V_{BE} , then of it is intuitive that r_e changes.
 - o Voltage gain varies a lot depending on the input voltage at a given time, due to the corresponding change in current, or voltage across R_c .
 - o *This can be solved with placing a resistor at the emitter, increasing r_e so that fluctuations in r_e due to the changes in I_C are made relatively negligible. $\alpha + C \approx C$, for $C \gg \alpha$.

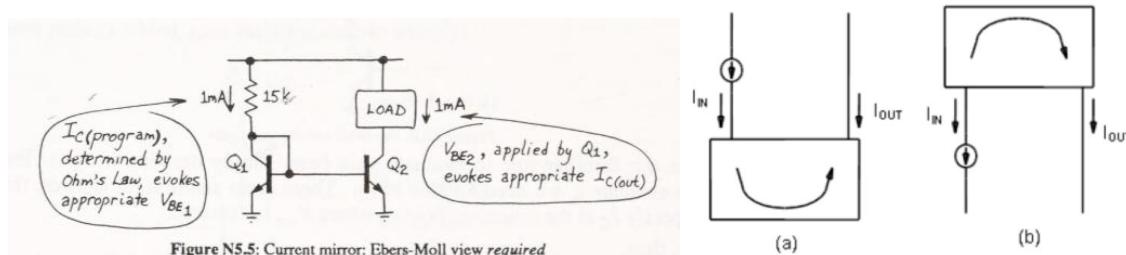
- This perspective is only seen through Ebers-Moll model.
- [Microsoft Word - 2 The Ebers-Moll BJT Model.doc](#)

Temperature:

- Exponential relationship: I_C grows at 9%/C, at constant V_{BE} . $I_C = 1.09^T$.
- At constant I_C , temperature increase causes a decrease in V_{BE} of ≈ 2 mV/C to compensate.
- Although the Ebers-Moll equation implies an inverse relationship, the effect of temperature on semiconductors has a greater effect over the equation that is not visible in the EB eq..
- Similar to the above of an emitter resistor increasing voltage gain stability, an emitter resistor increases $I_C (V_{BE})$ temperature stability by the MAGIC of negative feedback.
 - The difference is that in voltage stability, the emitter resistance is seen as r_e , increasing it, so the effect is seen after R_e .
 - Here we are essentially splitting the node of ground and the emitter such that an increased temp \rightarrow increased $I_C \rightarrow$ increased V_E (V_B fixed) \rightarrow decreased I_C .
 - Current gain scales with voltage, V_{BE} ; Ebers-Moll.

Current Mirror:

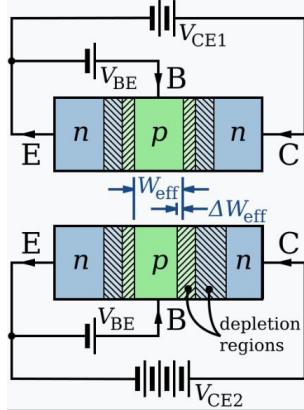
- [By the Ebers-Moll Model.](#)
- Conceptually, an ideal current mirror is simply an ideal current amplifier with a gain of -1.
- A current mirror is supposed to mirror current from a reference to a "loaded" circuit.
- Typical current mirrors are susceptible to the Early Effect. V_{CE} across the load transistor is dependent on the impedance of the load (relative to the ohmic CE junction)
- Combatting the Early Effect consequences on current mirrors, the clever Wilson Current Mirror is invented.



Early Effect:

- With respect to the Early Effect & V_{CE} . Temperature and Early Effect tend to make I_{OUT} larger than $I_{PROGRAM}$ in a current mirror.
- The reverse-biased, collector-base depletion-region size is inversely proportional to the collector-base voltage.
- CB depletion region size increases proportionately with CB voltage, due to reverse bias nature.
- The p-type base size and hole count decreases and the CB depl. layer increases in size.
- Hence:
 - Smaller p-type base region implies lower holes for recombination from I_{EB} .
 - Larger depletion region means larger p.d. and size which can pull more electrons from base into collector, inverse of above point.
 - The larger depletion region implies a larger p.d. across it. This p.d. crosses to the base and the V_{BE} voltage and current increases. Implies V_{EC} increases as well.

- Therefore, collector current increases proportionately with V_{CB} .
- When V_{CB} reaches a certain device specific value, the BE depletion region boundary meets the BE depletion region boundary. Therefore no base, no current (gain = 0).



CE, CC, CB BJT Topologies:

- $h_{fb} = IC / IE$ (current gain in CB), $h_{fe} = IC / IB$ (current gain in CE) and $h_{fc} = IE / IB$ (current gain in CC). Therefore, $h_{fc} > h_{fe} > h_{fb}$.
- Germanium: $V_{BE} = 0.3V$ and Silicon: $V_{BE} = 0.7$ volts
- Good for impedance matching due to high input impedance, low output impedance.
- CE/CB: load at collector, CC: load at emitter.
- Common emitter and common base topologies are very similar, the only difference is such that the return current is shared in common base, but separate in common emitter, hence the small current gain CB.

Common Base:

- The two external power supplies share a common node at the base node.
- As usual, the base-emitter is forward biased, base-collector reverse-biased.
- Since, $I_E = I_B + I_C$, of the common base topology, where the load is on the emitter side, the current will be less than that at the collector. This allows current attenuation; $0.9 < h_{fb} < 1$.
- Topology provides voltage amplification. Non inverting amplification since input and output signal in phase.
- Since ground is connected to the base of the transistor, the output signal is unlikely to be fed back to the input circuit. Effective grounded screen (for HF applications).

Common Collector (Emitter Follower):

- The common node between the 2 external supplies (circuits) is at the collector.
- Highest current gain factor, h_{fe} . High input impedance, low output impedance.
- non-inverting; $V_E = V_B - V_{BE}$.
- Can be used in voltage regulators due to the emitter voltage following, and with a diode at the base to clamp voltage $\leq V_Z$, or to V_Z when operated $> V_Z$.

Common Emitter:

- Most common transistor topology due to higher power amplification (voltage + current amplification).

- Current gain less than that of CC, but typically said to have almost same gain.
- **Inverting amplifier.**
- **Inverting due to effect of r_e ; so the voltage before and after the transistor is opposite due to voltage division by r_e (current controller). High voltage before r_e implies high r_e , implies low voltage after r_e . Implies phase inversion!!**

Basic circuit	Common emitter	Common collector	Common base	Cascode
Voltage gain	high	less than unity	high, same as CE	high, same as CB
Current gain	high	high	less than unity	high, same as CE
Power gain	high	moderate	moderate	highest
Phase inversion	yes	no	no	yes
Input impedance	moderate $\approx 1\text{k}\Omega$	highest $\approx 300\text{k}\Omega$	low $\approx 50\Omega$	same as CE, $\approx 1\text{M}\Omega$
Output impedance	moderate $\approx 50\text{k}\Omega$	low $\approx 300\Omega$	highest $\approx 1\text{M}\Omega$	same as CB, $\approx 1\text{M}\Omega$

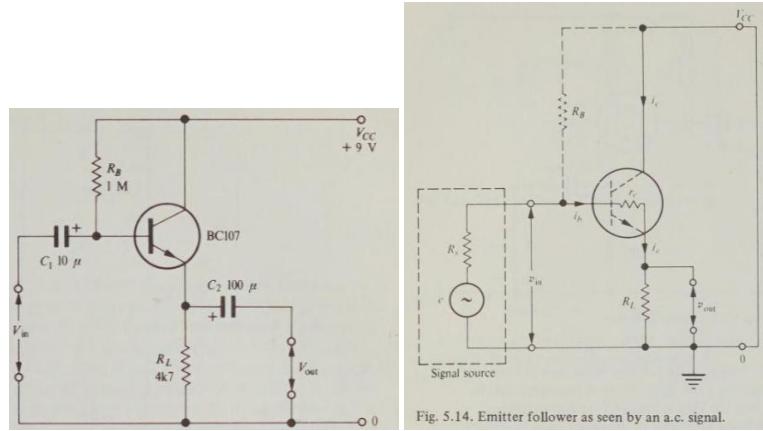
	Common Base	Common Emitter	Common Collector
Input Impedance	Low (about 50Ω)	Medium ($1-5\text{K}\Omega$)	High ($300-500\text{K}\Omega$)
Output Impedance	High ($500\text{K}\Omega-1\text{M}\Omega$)	Medium (about $50\text{K}\Omega$)	Low (up to 300Ω)
Current Gain	Low (<1)	High ($50 - 800$)	High ($50-800$)
Voltage Gain	Low (about 20)	High (about 200)	Low (<1)
Power Gain	Low (about 20)	High (up to 10000)	Medium (about 50)

BJTs (npn)

- Lightly doped base, heavily doped emitter. Reverse biased collector-base, forward biased emitter-base.
- Base-Emitter is low-impedance due to forward bias, Base-collector is high-impedance due to reverse bias.
- The reversed bias collector-emitter relies on the minority carriers for current from emitter to collector via base, from the p.d.. Minority carriers for reversed bias.
- $I_E = I_B + I_C$. For common base and common emitter.
- The voltage and current gain or the BJT topologies are self-explanatory, the input and output impedances are derived from this.
 - o The input impedance of emitter follower is high due to negative feedback...
 - o The input and output impedances of the different topologies are derived via $V = IR$ and $I_E = I_B + I_C$.
- Low impedance and high impedance input and output can be used for impedance matching to ensure maximum power transfer, low noise figure, and maximum signal transfer.

- [BJT Emitter-Follower - Working, Application Circuits - Homemade Circuit Projects](#)
- [Emitter Follower : Working, Characteristics and Its Applications - Semiconductor for You](#)
- [Different Configurations of Transistors - Common Base, Collector & Emitter](#)

Emitter Follower Topology (includes some facts in other topologies):



- Bias resistance provides a current bias.
- R_L provides a bias voltage at which an ac input voltage may fluctuate from, the new setpoint; bias.
 - o Capacitors are something I need to explore more
- The emitter follower gets its name from the small voltage drop between the base-emitter. This gives a near-unity voltage gain and hence emitter-voltage follower.
- Deduced by $V = IR$, KCL, and similar values (derived from relatively large/small values),

the input impedance is

$$R_{in} \approx R_L h_{fe}.$$

in parallel with R_B

$$R_{in} \approx \frac{R_B R_L h_{fe}}{R_B + R_L h_{fe}}.$$

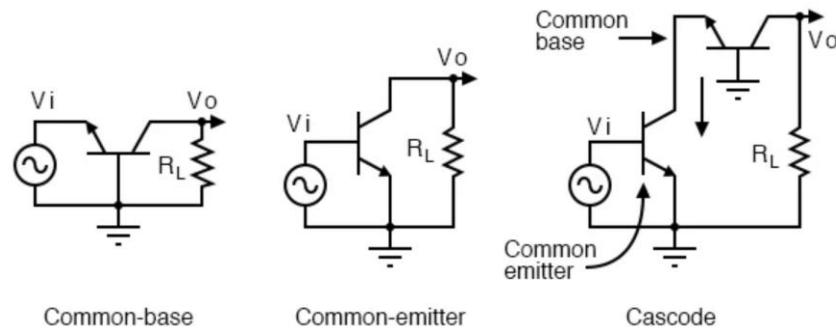
- o The input impedance is relatively quite large.
- o R_B is considered in parallel since ac superposition principle, dc src -> gnd.
- The output impedance is deduced using thevenins theorem. Considering how the output and input voltage are similar in a emitter follower circuit, the open circuit voltage is obtained. The short circuit current is obtained from the output current, i.e. input current \times gain, with the base-emitter resistance ignored.

$$Z_{out} \approx \frac{R_s}{h_{fe}}.$$

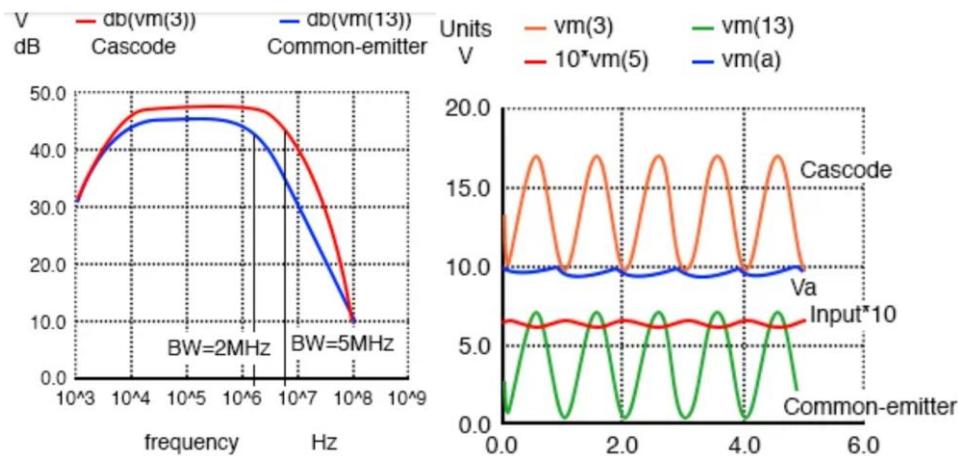
Miller Effect:

- The $(1 + h_{fe})$ increase in capacitance between the collector-base junction of a transistor, especially in common-collector topologies where the **inverted** input-output signals generate very high capacitances.
- The small C-B capacitance appears $(1+|Av|)$ times larger than its actual value.
- C-B capacitance is actually smaller than the E-B capacitance without signal.

Cascode:

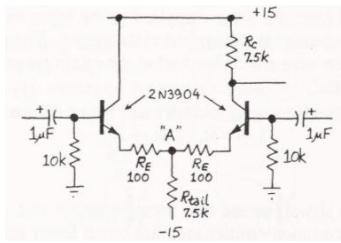


- Decreases the impedance at the base of the transistor whose collector is the output.
- A transistor topology that fights the Miller effect. Effectively, it increases the operational bandwidth.
- A Common emitter + a common base topology.
 - o The common base properties of:
 - Low input impedance due to the high coupling of the input and output current yielding an amplification being only less than unity. 10s of ohms 50.
 - Same voltage gain of common emitter is used.
 - The output voltage is seen at the CB load.
 - o A common-base configuration is not subject to the Miller effect because the grounded base shields the collector signal from being fed back to the emitter input. Thus, a C-B amplifier has better high frequency response. To have a moderately high input impedance, the C-E stage is still desirable. The key is to reduce the gain (to about 1) of the C-E stage which reduces the Miller effect C-B feedback to 1·CCBO.



- [The Cascode Amplifier | Bipolar Junction Transistors | Electronics Textbook](#)

Differential Amplifier:

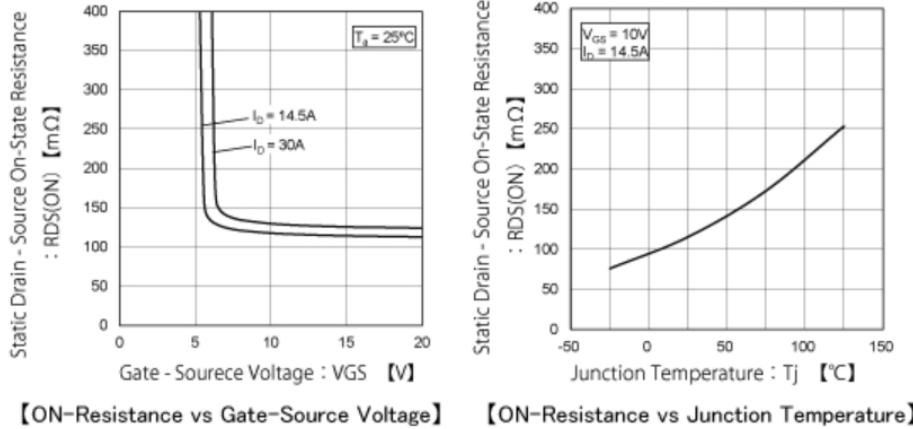


- For a differential signal, $(+V, -V)$, the voltage at node A is constant, as the voltage at A is a median-dependent value. By Eber's-Moll the current through both would be the same, causing A to compensate to a median value, which is constant in differential signals since the voltages would differ to the median or something, i.e. (A). My intuition.
- A common mode signal would skew A, as to amplify the common-mode signal, this is undesired, hence diff. amp.
- Diff. gain: $G_{\text{diff}} = R_C / 2(r_e + R_E)$
- CM gain: $G_{\text{CM}} = -R_C / (r_e + R_E + 2(R_{\text{tail}}))$
 - o Increase diff gain, without cm gain by increasing R_{tail} , hence a current sourc, (ideal infinite impedance).

FETs:

- Characterized by V_{GS} , V_{DS} , $\rightarrow I_D$.
- Relationships
 - o I_{ds} vs. V_{gs} is a quadratic model too solve with.
 - o Transconductance is approximate to the square root of I_d since I_d can be modeled by $(V_{gs} - V_t)^2$ and V_{gs} modeled as $V_{gs} - V_t$.
 - o Transconductance is approximate to $2(V_{gs} - V_t)$ for V_{gs} modeled as $V_{gs} - V_t$, since $I_d \approx (V_{gs} - V_t)^2$, implies a linear derivative, or transconductance, I/R , of $2(V_{gs} - V_t)$.
 - o The ohmic, linear region of I_d vs V_{gs} is (considerably) larger for a FET than for a BJT.
 - o At high I_{ds} , the I_d current saturates due to the balancing of increased field strength, but a longer channel (increased resistance).
 - o **I_d vs V_{gs} is linear, ohmic when $V_{ds} \leq V_{gs} - V_t$; saturated for $V_{ds} > V_{gs} - V_t$.**
 - o JFET: A current source is plausible through negative feedback and the tying of gate to source since JFET operates in depletion mode.
- For a voltage amplifier, with output tied to drain, the voltage oscillates about the quiescent at an amplitude determined by the quiescent voltage drop across the source resistor.
- A FET is a current source in Saturation, with sufficient V_{ds} , w.r.t. V_{gs} , and a resistor at lower V_{ds} ; see above highlight.
 - o While linear, ohmic, R_{ds} is calculated by Ohm's law, while saturated, R_{ds} is constant.
- The transconductance of a FET represents the inverse of an inherent resistance at the source of the FET, before the source node (so, inside the FET).
 - o Since g_m is approximated to vary linearly with V_{gs} , this is how the voltage follower works, in that increased input voltage, implies increased g_m , implies decreased ' r_e ', implies increased V_{gs} . This voltage following will differ by V_{Th} .

- Note: the inverse of g_m is the FET's ' r_e '.
- Generally, the larger the chip size (surface area) of the MOSFET the smaller the ON resistance.
- $R_{DS(ON)}$ has a positive temperature coefficient, meaning it increases with rising temperature.
 - Unlike a semiconductor p-n junction
 - When R_{ds} saturates, it takes on its most recent unsaturated value, approximately.



Saturation:

- Caused when the proportion between V_{gs} and V_{ds} is such that $V_{ds} > V_{gs} - V_t$ so that further increases in V_{gs} doesn't increase the current going through the FET, i.e., $R_{ds(on)}$ doesn't decrease, by the channel become both longer and pinched off.
- In theory, I_{ds} increases quadratically with V_{gs} ($-V_t$). In practice, there are limiters like *velocity saturation, thermal limits, and oxide breakdown* that limit max I_{ds} to V_{gs} .

Current Sources:

- A

Capacitance:

- Assume an inductive load (SMPS) with 2 (NMOS) transistors (high and low side) that switch to examine the inductive load behavior of mosfet gate charging & capacitance.
 - We will also refer to the high-side Mosfet.
- There exists capacitance $C_{iss} = C_{gd} + C_{gs}$, representing input capacitance
- The linearity of V_{gs} implies constant current. Constant current implies no reactive components. But there exists the C_{iss} , this means the capacitor is not in play and it already fully charged.
 - So, the capacitor charges during the miller plateau in establishing equilibrium. Before and after, it is already in equilibrium with its equal and opposite side and doesn't charge. Hence linear V_{gs} .
- Note: $C_{rss} = C_{gd}$ of a Mosfet.
- Initially, V_{ds} is clamped because of the body diode in the Mosfet(s). The clamping is caused by the continuing current caused by the load inductor's stored energy that goes through the low side mosfet.
 - It's not so clear though.

- The plateau V_{gs} is caused by the decreasing V_{ds} that makes the drain side more negative of C_{gd} , as a result, the gate side needs to become more positive. This effectively implies a capacitor where the charge will go into C_{gd} / C_{rss} , instead of charge on the gate to increase V_{gs} , hence the plateau.
- The reason the plateau starts when the voltage starts decreasing and when the current is max is because when the current is max, the diode isn't in play anymore and all current goes into the FET. This means that V_{ds} will not be clamped and will start decreasing, hence Q_g starts storing in the miller capacitance and causes the plateau.

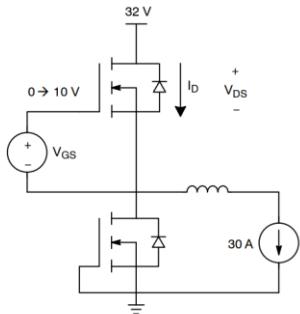


Figure 2. Inductive Switching

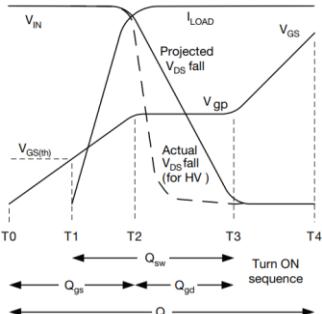


Fig. 7 - Gate Charge Components and Timings

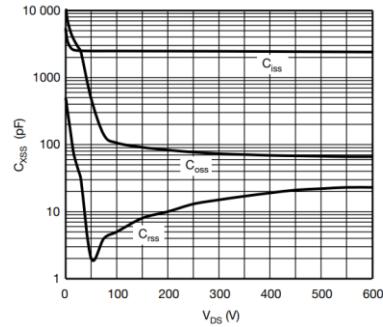
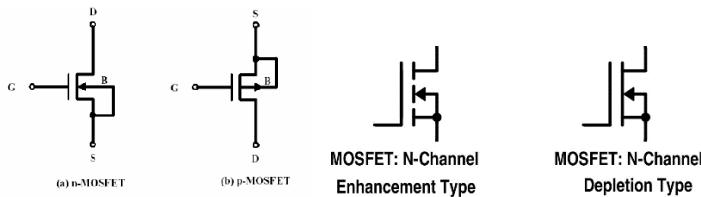


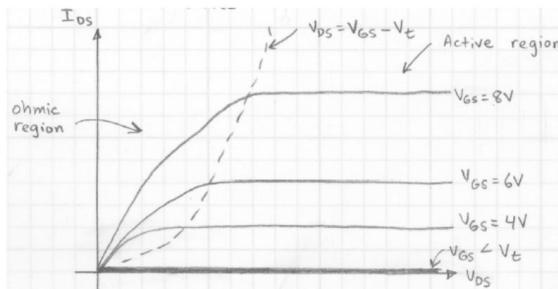
Fig. 8 - Capacitance Variations w.r.t. Applied V_{ds}

MOSFETS:



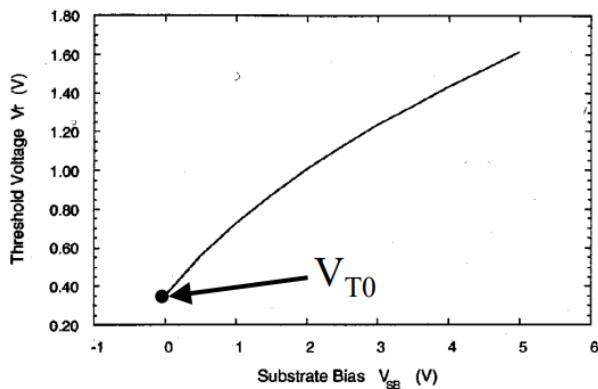
- Arrow always connected to source side and arrow denotes electron flow.
- Primarily used in low voltage applications. Can be switched quickly (relative to BJTs and IGBTs) but are limited by voltage ratings and thermal properties.
 - o <150 kHz switching
 - o Rise time: 1 – 10 ns.

HiBuS® Technology

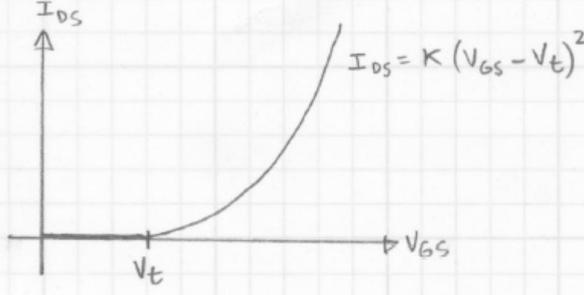


- $R_{ds(on)}$ provides resistance, not a sc.
- Bidirectional current since symmetrical. Drain and Source are interchangeable.
- may replace diodes for lower power dissipation for an ideal reverse current protection.
- Cut-off region: $V_{gs} < V_{th}$, the drain current is 0.

- Depletion region forms, no carriers in channel.
- The Body effect implies that the higher the V_source-to-bulk, where the bulk is the substrate, the higher the V_th becomes.



- I_{ds} is proportional to V_{gs} , implies r_{on} is inversely proportional to V_{gs} .
 - For higher I_{ds} and lower R_{on} , increase V_{gs} , as seen in characteristic curve
- Drain current varies quadratically with gate-source voltage V_{GS} (in Saturation)



- For $V_{gs} > V_{th}$, an inversion layer forms.
- If $V_{gs} > V_{th}$ and $V_{DS} < V_{GS} - V_{th}$, the MOSFET operates in the triode/ohmic region.
 - Current is linear with V_{ds}
 - Inversion region increase proportionately as V_{ds} increases.
- If $V_{gs} > V_{th}$ and $V_{gs} - V_{th} = V_{ds}$, the MOSFET is in saturation.
 - The channel begins to become pinched off, i.e. pinch off point is exactly at the drain junction.
 - Thus, it acts as a current source, with "constant" I_{ds} .
- Electric field (Voltage) between G-S creates inversion region. Since the source-bulk is forward biased, Hence, the triangular inversion region shape from the source. The voltage between D-S actually pushes/pulls the inversion region away due to competing with the G-S voltage.
- If $V_{gs} > V_{th}$ and $V_{DS} > V_{GS} - V_{th}$, implies constant I_{ds} .
 - As V_{ds} increases, pinch-off point moves closer to source.
 - Pinch off works by changing the p.d. along V_{gd} (or gs since interchangeable for a MOSFET).
 - Pinched-off region becomes a depletion region.

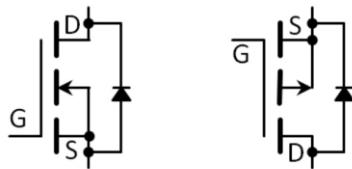
- It is the **high electric field from V_{ds}** that accelerates electrons towards drain.

MOSFET type	$V_{GS} = +V_{th}$	$V_{GS} = 0$	$V_{GS} = -V_{th}$
NMOS Enhancement	ON	OFF	OFF
PMOS Enhancement	OFF	OFF	ON
NMOS Depletion	ON	ON	OFF
PMOS Depletion	OFF	ON	ON

- Breakdown voltage of a FET is the gate-drain voltage at which the resistance of the p-n junctions of the transistor decreases dramatically, causing the drain current to drastically increase.
 - can occur whether the FET is on or off.
- $R_{ds(on)}$ is the resistance of the MOSFET when it is in saturation. Maximum current without breaking down basically.
 - Remember than when in saturation, the MOSFET does not behave linearly, (although called linear region), hence $V=IR$ doesn't apply.

MOSFET Body Diode:

- Mosfet semiconductor-diode structure implies a parallel diode.

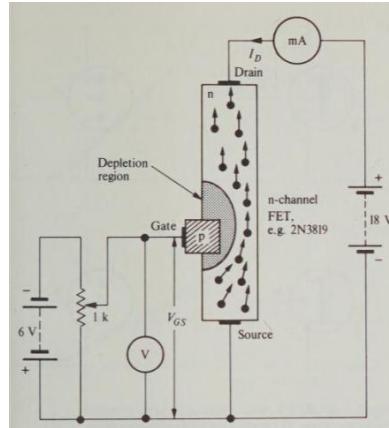


MOSFET schematics, complete with body diodes.

- This diode leads to forward voltage drops and forward currents when the diode forward conduction voltage is exceeded, leading to power losses
- [What is the MOSFET body diode?](#)

JFET

- The JFET conducts with 0 gate-source voltage, and the channel is cut off with negative gate voltage. The mosfet conducted with positive voltage and is cut off at ≤ 0 voltage.
 - o JFET => depletion

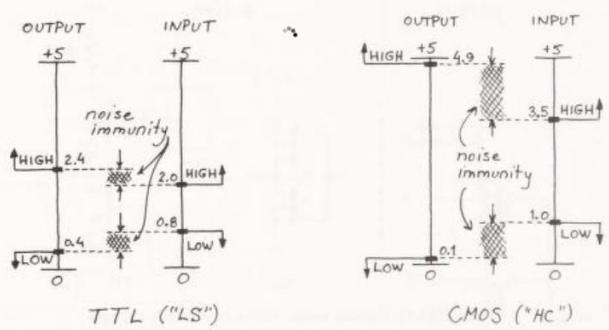


- MOSFET/IGFET => enhancement
- Enh/dep n-channel mosfets available, while dep p-channel mosfets are not readily available.
- Depletion mode implies that the transistor is normally on (i.e. channel on) with 0 (or less) gate-source voltage. For MOSFETS this can be made possible by trapping positive ions in the SiO₂ layer under the gate or by diffusing impurities into the p-type (uncommon). Depletion mode n-channel MOSFETs are the most common.
- NOTE: the forward biased region/side of the MOSFET transistor has a wider channel. While for a JFET, the forward biased side is smaller due to its overall negative charge, whilst seemingly positive (but electron flows to drain, overall expressing voltage difference). So electrons like to reside on the positive side more?
- Mosfets have a higher gate impedance than Bipolar transistors.
- A Darlington pair (bipolar) has a ~50% voltage signal lost due to the similar input and output impedances of the emitter and base. While the higher output impedance of a mosfet gate yields to much better signal integrity.
- Bipolar transistors are susceptible to both 1/f and shot noise, JFETs very little shot noise and 1/f noise, but MOSFETs practically only 1/f noise, due to the high gate impedance. On top of thermal noise.
- The 1/f noise of MOSFETs are considerably higher than, 100x than JFETs.
- The main advantage of using MOSFETs is their low ON resistance, which implies low switching losses.
 - IGBTs are similar to MOSFETs in terms of ON resistance, but they have the added advantage of being able to block high voltages.
- BJTs have a higher ON resistance than MOSFETs and IGBTs, but they are less expensive and easier to control.

Comparison:

- Both are transfer resistors (transistors) that modulate, amplify a larger current flow through a current OR voltage at the base OR gate.

- BJTs' bases couple into the emitter by means of the necessary current flow I_{be} . The coupling means a lower noise immunity of BJTs, compared to FETs, since noise transfers from the input to the output...
 - o The thresholds of TTL's output is super large and a HIGH output has a large range which is unfortunate. If an output drives an input, there's only a noise immunity of 0.4 V, as seen in this picture.



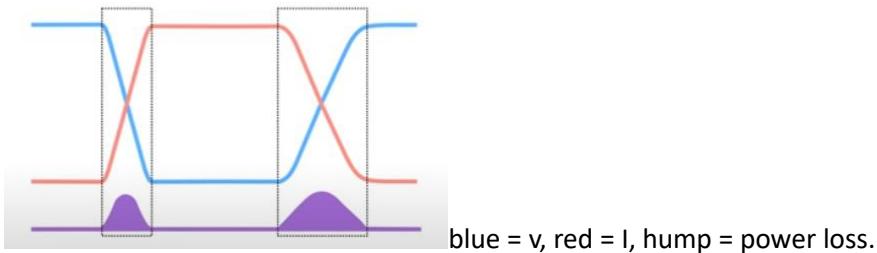
- TTL inputs float high. Since they are current controlled, a preexisting voltage must be present in order to bias the BJTs at any input signal. So, this HIGH level bias, connected to the base (input) of TTL BJTs, pulls floating input high. In FETs, this input voltage would be user-determined.
- TTL consumes much more power, due to inherent current flow at all times, even at output LOW. At any output, TTL passes current.

IGBT:

- IGBTs have a tail-current, limiting their switching speed and switching frequency.
 - o Typically, switching frequency limited to about 60kHz.
- IGBTs possess much lower power loss and higher switching speed than other topologies..

Switching Losses:

- Ideal switch has no power loss; assumes zero and infinite impedance => zero voltage drop and zero current, respectively.
 - o By $P = IV$, $P = 0$.
- Ideal switch has instantaneous transitions between on and off.
 - o Power is mostly loss in switching transitions. Due to non-ideal, non-zero transition time, there exists a time where both voltage and current are greater than zero, implies power lost during transitions.
 - o Faster transitions (high slew rate) imply lower power loss e.g. wide bandgap materials. This due to smaller integral, as seen in diagram.
- Switching loss = turn on loss + conduction loss + turn off loss + non-conduction loss.
 - o To measure use oscilloscope, voltage, and current probe for $P = IV$.
 - Sufficient bandwidth and range and properly deskewed.



Negative Feedback:

- Seems to be the phenomenon of setting some value so that the other (desired, important) factor can vary (oscillate) to a desired more dependent on the set value.
- Negative feedback is when you set up a system such that a desired opposition occurs so that the system stays in the desired response. This opposition occurs as the resultant effect of something else occurring at the same time, something implemented or another effect. This balances the system to the desired response.
- Generally, with BJTs (and probably everything), implementing negative feedback reduces gain due to the opposition to variability.

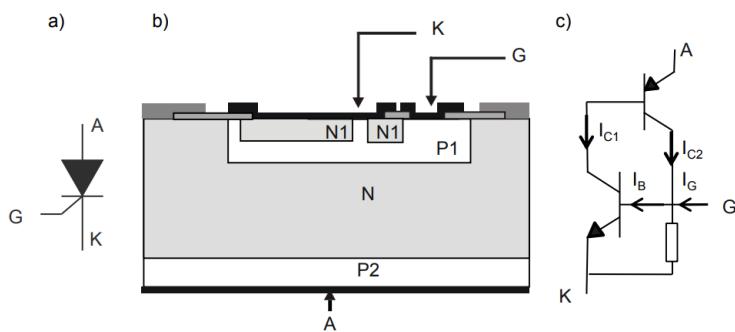
TTL:

- Digital logic made of BJTs on DC pulses.
- TTL ICs have TTL logic gates fabricated on an IC, numbers typically beginning with 74 or 54.
- Fundamental gates (AND, OR, NAND, NOR) still used in digital logic in VLSI.
 - o Flash memory from nand, nor.
- Transistors provide switching, turning on or off in response to input signals.
- Resistors limit current and help optimize voltage levels (biasing) for the transistors.
- Diodes ensure current flows in only one direction, helping to stabilize the circuit.

CMOS:

- CMOS slew/edge rates are generally slower than Bipolar logic devices; advancements have made CMOS slew rates comparable.
- CMOS outputs swing almost rail to rail, while bipolar outputs swing from GND to approx. 3.0 V.
- In the bipolar world, the trade-offs are between speed and power; in the CMOS world, the tradeoffs are between speed and ease of use.

Thyristor:



- Assume A is a HIGH level and K is a LOW level and G biases the NPN transistor.

Switches:

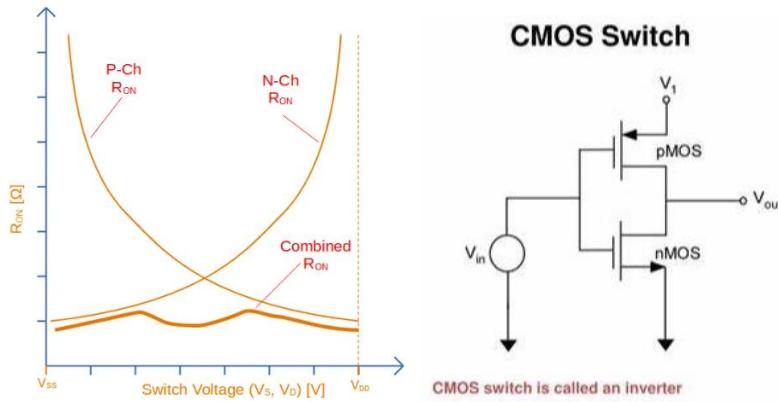
- [Basics of Power Switches \(Rev. A\)](#)
- ON/OFF Switches with HIGH and LOW dual-outputs can be implemented with 2 transistors (NMOS & PMOS or Enh. & dep.) Push-Pull configuration, 1 transistor Open-X configuration with a p.u. or p.d. resistor, tri state logic.
 - o A CMOS switch is actually a push-pull topology; unique since VCC can be adjustable.

Push-pull:

- A push-pull output (often used for SPI communication) has complementary NMOS and PMOS transistors that drive the output high or low.

CMOS Switch (Inverter):

- Uses an NFET and PFET to ensure an entire input range can be switched on/off.
 - o Threshold limits of an NFET/PFET can be contributed by the other.
 - o Bidirectional current flow
- NFET and PFET in parallel use opposite polarity signal which cancel out the charge injection from each other. Dependent on gate cap matching.
- R_{ds} contributed by both FETs, determines the output voltage by $V = IR$.
- CMOS switch inverts about the common mode voltage, V_{cm} , due to almost constant resistance (voltage divider).



- Capacitances at gate and around FETs create a loading time.
- Read some app notes when time abides.
- <https://www.youtube.com/watch?v=h8ad1-Sy39A>

Open Drain / Source (Collector / Emitter):

- Open X configuration implies the X terminal of the transistor is connected/exposed as the output signal and pin for NPN and nMOS technologies.
 - o Mosfet and bjt topologies both apply.
- In these Open X configurations, the source voltage is VCC and the drain voltage is GND.
 - o This is reversed for PNP topologies.
 - o Open outputs using PNP and pMOS transistors will use the opposite internal voltage rail used by NPN and nMOS transistors.
- In these configurations, when the transistor is conducting (LO-Z), the output voltage signal is not floating
- When the transistor is not conducting (HI-Z), the output voltage is floating and pull up and pull down transistors are used, for open drain and open source configs, respectively.
- The data rate is proportional for an Open X configuration is proportional and dependent on resistor rating.
 - o Lowspeed => 1.5 kOhm.
 - o Can put resistors in parallel to alter/increase data rate transmission.
- [Open collector - Wikipedia](#)

SerDes (check Wikipedia page for more info) [SerDes- Wikipedia](#):

- Parallel in Serial out (PISO) & Serial In Parallel out (SIPO), and full duplex, generally.
- Parallel data has >power consumption, emi, and clock timing skew.
- Generally, a parallel bus interface, such as SoC, FPGA, ASIC. Serial data stream used with coaxial or twisted pair cable and a clock.

- Phased Lock Loop (PLL) is feedback-control system sensitive to freq and phase that acts a reference clock for PISO and SIPO to serialize and deserialize data.
- PLL clock signals can be scaled up by factors of the clk signal.
- To deserialize the data, a shift register and counter may be employed.
- Very different SerDes architectures out there for additional exploration.
- [What is SerDes \(serializer/deserializer\)? | Definition from TechTarget](#)

OTP (One Time Programmable) Memory:

-

NAND Flash with eMMC:

- Flash is non-volatile memory and doesn't need a power supply to retain data. It is finite; cells will fail...
- eMMC (embedded Multi Media Card): MMC soldered permanently onto devices, with a built in controller for I/O operations, using NAND flash.
 - o More power efficient due to single NAND gate.
 - o MMC -> SD. SD has higher storage, speeds, and security, but more expensive.

Phased Lock loop:

-

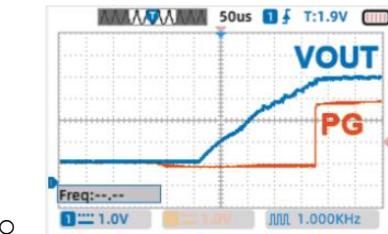
Camera Link High Speed (CLHS):

- Camera Link, built on Channel Link, a LVDS serial communication for close devices, is a standard for connecting cameras and frame grabbers.
- Channel link comes in configuration of 3,4,8 parallel data transfer lanes + clock. Each lane has 7 serialized bits, except for 6 for the 8-laner.
 - o Camera link use the 4 lane, 28 bit channel link version, and up to 3 channel link transceiver chips, i.e. 3x.
 - o 28 bits: 24 bits of pixel data, 3 for video synchronization, and 1 spare.
 - o 4 lanes of LVDS data and 1 LVDS clock for 5.
 - o Due to the serialization factor of 7, a 7x clock can be generated by SERDES-PLL.
 - o Camera link has a clk rate up to 85 MHz for total throughput of 2.38 Gbit/s.
- Different clhs configurations exist.
- How color and value of data bits are assigned are yet to be fully discovered.
- [Camera Link - Wikipedia](#)

Schematic terms:

- DNP: do not populate. Empt pad.
- OR zero ohm resistor.

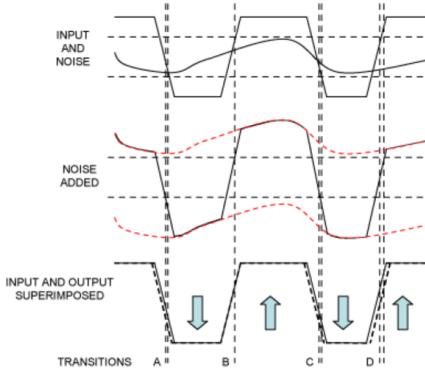
- A 0-ohm resistor used as a removable connector and to prevent reverse engineering.
- X: connection
- Q: transistor
- J: connector
- U: IC
- AG -> Audio ground.
 - Sensitive analog circuits are sensitive to switching noise into their grounds
 - To have same dc potential, a CMC (common mode choke) has low dc resistance, high ac resistance, to get less noisy AG.
- On page 6, many unknown pin, e.g. ak am an,ad, af;
- Power Good: A logic level signal provided by a power supply that indicates the output voltage is within specification to ...
 - internal self-tests and the outputs have stabilized
 - Used for sequencing DC-DC converters; PG to EN.



- An open-drain (for LDOs) output that signals the output voltage has almost reached its target value.

Noise:

- Four families of noise problems: reflections, cross talk, rail collapse in the power distribution network, and EMI.
- Noise floor: The sum of all the noise sources and unwanted signals within a system
 - Indicates the smallest noise measurement that can be taken with certainty.
 - No measured amplitude of noise can be “on average” less than the noise floor.
 - Commonly lowered with system cooling, limiting thermal/johnson noise.
- Generated from **high dv/dt and di/dt switching nodes**.
- Mostly generated from high-frequency, fast switching devices.
- Analog and digital signals both are noisy w.r.t. to each other.
- Analog noise to digital signals, even if within thresholds, produce errors and time-based error jitters, due to superposition of waveforms and slope changing.



- [Well Grounded, Digital Is Analog | Analog Devices](#)
- Noise: Always present, random voltage fluctuation. The limiting agent in electronic instruments.
 - o Being random, noise can be any frequency.
 - o Noise power produced by circuit is proportional to the frequency bandwidth of circuit.
- At higher frequencies going through transistors (and amplifiers), the input noise current increases due to the capacitive coupling from the channel to the gain of MOSFETs. This increase in current, implies that a low optimum signal source impedance is required for a low noise figure.

Current Noise:

- The phenomenon of current noise increasing with frequency is well known to IC design engineers and circuit designers.
- Caused by

SNR

- SNR measures intelligibility of signal in an amplifier relative to noise. Signal power to noise power.

$$\text{S/N ratio} = \frac{P_s}{P_n} .$$

It is commonly stated in decibels:

$$\text{S/N ratio} = 10 \log_{10} \frac{P_s}{P_n} \text{ dB.}$$

- For same input impedance from signal and noise to a load, by $P = V^2/R$, snr can be calculated in terms of voltages.

$$\begin{aligned}\text{S/N ratio} &= 10 \log_{10} \left(\frac{V_s}{V_n} \right)^2 \text{ dB} \\ &= 20 \log_{10} \frac{V_s}{V_n} \text{ dB.}\end{aligned}$$

Types of Noise

- Thermal/Johnson/white noise: Any interconnect produces electrical noise from thermal agitation; arises from resistance.

Nyquist showed from thermodynamic principles that the r.m.s. noise e.m.f. V_n across a resistor R is given by

$$V_n = \sqrt{(4kTR\Delta f)}, \quad (5.9)$$

where k is Boltzmann's constant ($k = 1.380 \times 10^{-23} \text{ J K}^{-1}$), T is resistor temperature in K ($= 273 + {}^\circ\text{C}$), Δf is the frequency bandwidth of the measurement circuit (Hz); R is the resistor value (Ω).

- Shot noise: current carriers crossing a barrier/junction cause a transient current surge. Power spectrum is proportional to current and its effect is greatest when the junction has high internal impedance such as that with a reverse biased junction.
 - o Occurring in semiconductors as carriers cross a PN junction.
 - o Current flow is not constant/continuous in PN junctions
 - o Does not vary with frequency (random), although a higher bandwidth will still increase shot noise; intuitive.

$$i_n = \sqrt{2qi_b}$$

- Flicker/1/f/pink noise: noise from (surface) crystal defects in semiconductors and random variations in diffusion processes of transistor.
 - o Intuition says that since crystal defects tend to volume of a crystal, crystal defects increase capacitance. Hence at higher F , more coupling occurs.
 - o Proportional to bias current amount
 - o power spectrum is inversely proportional to frequency \rightarrow mostly low frequency energy.
 - o 1/f noise is dependent on device geometry, device type, and semiconductor material. Hard to create mathematical models \Rightarrow empirical testing.

- Devices with buried junctions, such as bipolar transistors and JFETs, tend to have lower 1/f noise than surface devices such as MOSFETs.
- Burst/popcorn noise: low frequency noise associated with ionic contamination. Abrupt, fast changes in I & V.
 - Random. Proportional to current, inversely proportional to f^2.
 - Virtually eliminated by cleanliness of modern semiconductor processss.

Noise Figure (> unity):

by the *noise figure* (NF) of the amplifier, which is defined as the ratio of signal-to-noise power in the input signal (P_{si}/P_{ni}) to the signal-to-noise power at the amplifier output (P_{so}/P_{no}), i.e.

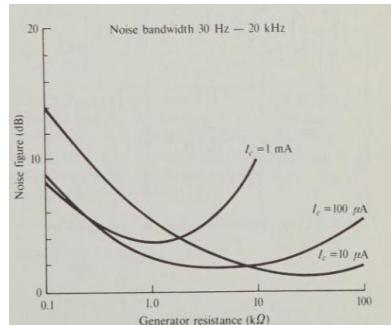
$$NF = \frac{P_{si}/P_{ni}}{P_{so}/P_{no}}$$

$$NF = \left(\frac{V_{si}/V_{ni}}{V_{so}/V_{no}} \right)^2 \quad NF = \left(\frac{V_{no}}{A_V V_{ni}} \right)^2$$

- Noise Figure measured with a bandwidth of 1Hz is called the spot noise figure.
- Noise is proportional to the bandwidth of the amplifier. Higher bandwidth implies higher noise signals capable of generating.
- For minimum NF, i.e. the most effective amplifier with the higher output and least noise:

$$R_{s(opt)} = \left(\frac{e_n^2}{I_n^2} \right)^{1/2}$$

- The lowest noise figures (in bipolar transistors) are obtained at very low collector currents \rightarrow less shot + flicker noise, this results in high optimal source resistances to minimize noise figure.



Ripple:

- Voltage ripple is a function of the inductor ripple current, the switching frequency (FSW) and the output capacitor's ESR

Ringing:

- An oscillation seen in signals occurring when signal transitions occur e.g. HIGH to LOW. Seen mostly in digital circuits as noise.
- Caused by ground bounce or impedance mismatch.
- Oscillation of a voltage/current signal that is ideally stable, particularly in the step response, i.e. state transition.

- Ringing can be undesirable because it causes extra current to flow, thereby wasting energy and causing extra heating of the components.
- Ringing/ripple may be the result of overshoot and settling time of signals, such as that in the PID step response.
 - Realization: a damping resistor can be used to reach/tend to steady state, i.e. ideal state, faster. If the ringing is not inherently damped either, the resistor acts as this damping.

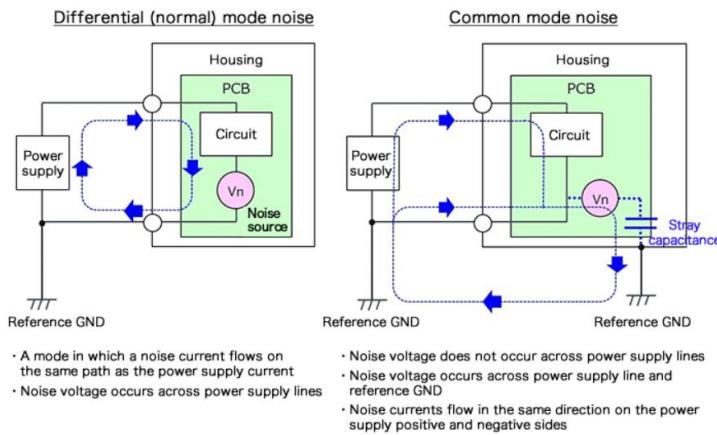
Causes:

- Long trace (digital signals): round trip propagation time from source-load-source is around the signal rise time.
- Long trace (analog sine signal): round trip propagation time is greater or equal to the period / 8.
- Impedance mismatches: Reflections cause ringing
 - In long traces.
 - Match characteristic impedance to the load impedance (terminated load) for minimal reflections
 - Damping needed (especially for long traces) even with characteristic and load impedance matched, in practice.
 - Damping resistors to minimize ringing effects.
 - Want critically damped.
- Ground bounce; parasitics – inherent.
 - In short and long traces.
 - Caused by increased impedance in lines.
 - Add series (to signal line) termination resistor (at source end) and parallel (to signal line) termination resistor (at load end). The values are calculated such that: $Z_0(\text{char.}) = Z_{\text{src}} + Z_{\text{series}}$ and $Z_0(\text{char.}) = Z_{\text{load}} \parallel Z_{\text{parallel}}$.
 - See ground bounce for solution.
- [Ringing \(signal\) - Wikipedia](#)
- [How to Reduce Ringing in Your PCB Designs | Sierra Circuits](#)
- [impedance matching - Causes of ringing in a PCB - Electrical Engineering Stack Exchange](#)

Radiated and Conducted Noise:

- Radiated noise is essentially noise that was too high frequency for conduction?
- Radiated EMI: Interference traveling through the air, requiring no physical contact, produced from electromagnetic energy from an electric field.
 - Generated by high dv/dt noise at switching nodes produced by switching voltage ringing and spikes.
 - Industry standards for radiated emissions usually cover the frequency band from 30 MHz to 1 GHz
- Every conductor/pin is an antenna that receives and transmits signals.
- For **radiated noise**: only ac signals can propagate from antennas since time invariant signals do not create the electromagnetic fields necessary for radiation.

- Non-ideal DC sources, with low ac superposition, has weak propagated wave since power transmitted is directly related to amplitude.
- Conducted EMI: Interference transferred from a source to receiver via a direct route; circuit noise. Capacitive coupling included. Generated from rapid changes in **conducted** input current.
- Basically, parasitic capacitance and inductance,
 - Standard industry limits from 150 kHz to 30 MHz.
- **Common-mode Noise:** The difference between the common-mode voltage vs theoretical common-mode voltage.
 - Dv/dt.
 - Generally, higher frequency.
 - Noise current leaked through stray capacitance that passes through ground and return to the supply. The direction of noise currents are in the same direction for both the + and – side of the line.
- **Differential-mode Noise:** Noise source appears to be in series with the power supply line. And hence the noise current flows in the same direction as supply current and in opposite directions from the + and – sides of the line.
 - Generally, lower frequency.
 - Di/dt. Apparently more predictable by software.



- [Differential \(Normal\) Mode Noise and Common Mode Noise—Causes and Measures | What is EMC? | TechWeb](#)
- Radiation due to common mode noise is far greater

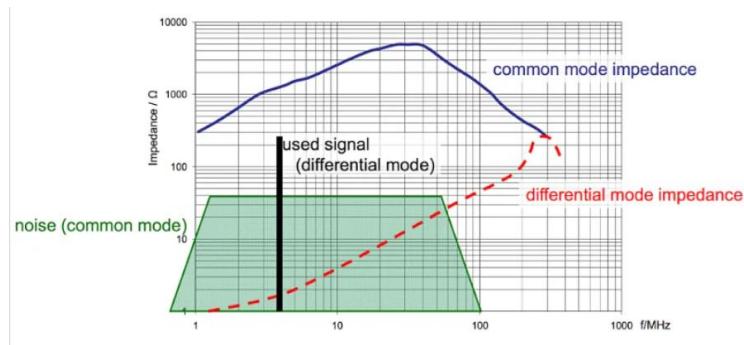
Electromagnetic Compatibility:

- Proper EMC ensures electronic devices operate efficiently without causing or experiencing interferences from other devices.
- Emission: generation of EMI must comply with regulatory standards for emissions to ensure devices don't cause interference to other devices in operating environment.
- Immunity: Ability of an electronic device to resist EMI from other devices in operating environment.
- CISPER 16-1-2, MIL-STD-461 standards:
 - C

- [What is electromagnetic compatibility \(EMC\), and why is it important in electronic devices?](#)

Common Mode Chokes and Ferrite Beads:

- An inductor which acts as an impedance to certain rejection frequencies (noise).
- CMCs:
- Two or more coils of wire wound on a common core
- The thing is, is that signals are always differential signals that drive in opposite directions from the supply.
- CMCs attenuate common mode noise, and some differential useful signals; must find balance.

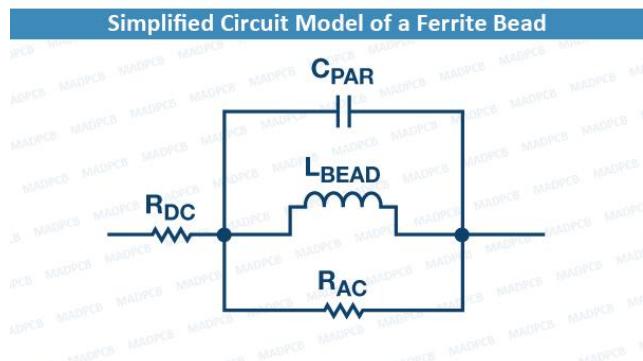


- One can use a CMC to determine between common vs differential noise. Using the power supply + and – wires, attach the choke. If CMC decreases noise, implies common noise, if small attenuation, differential noise. This is because of the equal and opposite noise canceling out in the magnetic field of the choke, implying no noise impedance which the inductor would otherwise provide

Ferrite Bead:

- Also, an inductor, but provides noise attenuation for differential signals.
- Dissipative by its own nature and best suited for higher (dozens of MHz frequencies)
- Not so clear on the difference.

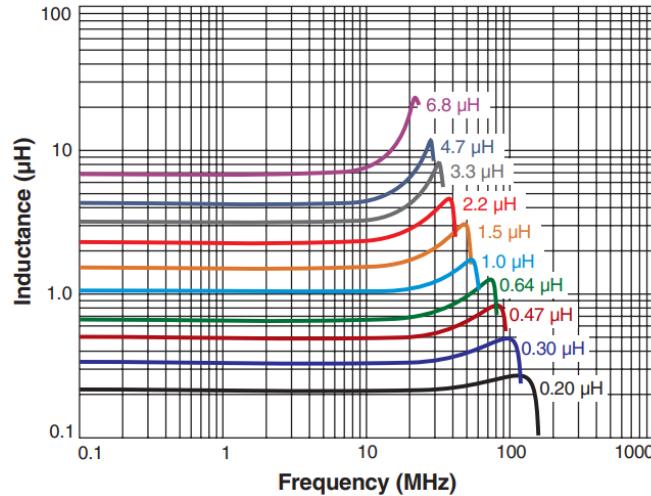
Ferrite Bead:



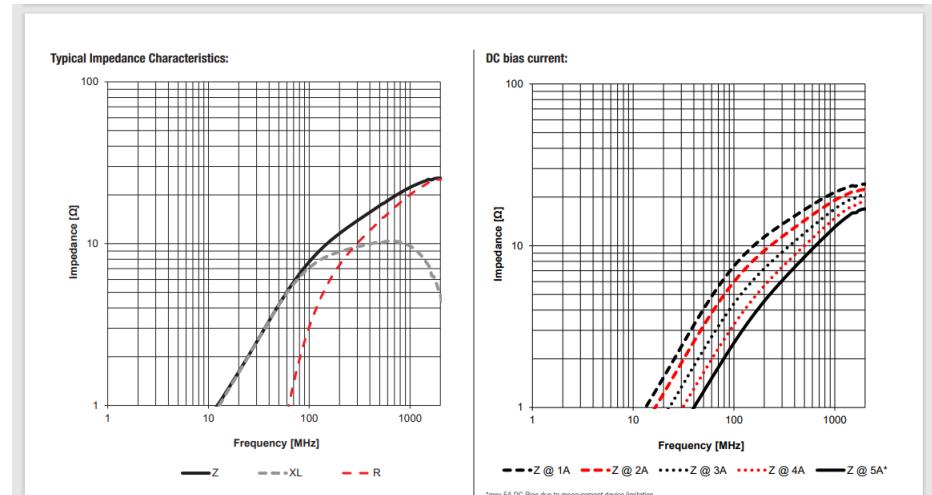
- An inductor with a (much) higher dc resistance / series resistance. A ferrite bead filters HF noise by dissipating it through the resistor, while an inductor stores HF energy in its magnetic field for filtering.

- Ferrite bead is lossy and this feature of filtering unwanted energy through dissipation without storing the energy in a magnetic field is more simple and can prevent further emi issues with inductor fields.
- Higher series resistance and much higher capacitance (parasitic) through the inductor wirings.

Typical L vs Frequency



-Inductor with low ac losses



-ferrite bead with much higher resistance and capacitance (decreasing the impedance at HF). Impedance should increase in a f^*e^f manner, but it's flat. Implies the capacitance is much higher for ferrite bead.

LISN (Line Impedance Stabilization Network):

- “Artificial Mains Network”
- Effectively keeps the source impedance constant by reflecting emi due to measuring instrument of constant impedance of 50 ohms rather than an unknown, variable source impedance.
- Stable Line impedance:

- Impedance looking into mains varies heavily. To view conducted emissions on an EUT, mains impedance should be constant, for reliable emissions testing.
 - LISN provides a constant impedance (generally 150 kHz to 30 MHz conducted noise).
- Measures the conducted emissions from an EUT.
- Conducted noise emission are generally conducted in or out of a device via its AC (main) power cord.
 - Can enter to another device
 - Can become radiated emissions
- Provides a stable *50-ohm* impedance to the spectrum analyzer from mains and blocks RF noise on mains from entering EUT.
- A measuring instrument is attached to the port to measure emissions. If not measuring instrument, add a 50-ohm impedance.
 - Generally, the measuring instrument will have a 50-ohm impedance. Thus, the LISN matches it, minimizing reflections and maximizing power transfer.



- Configured by an LC circuit; inductor (value) affects frequency-impedance and max. current. Capacitor decouples the rf noise from the mains.
 - Inductor determines the impedance and frequency response; caps are for filtering.
 - LC -> low pass filter to block HF rf noise and pass LF mains signal. This is the inductor-frequency response.

Frame Grabber (pixel to image):

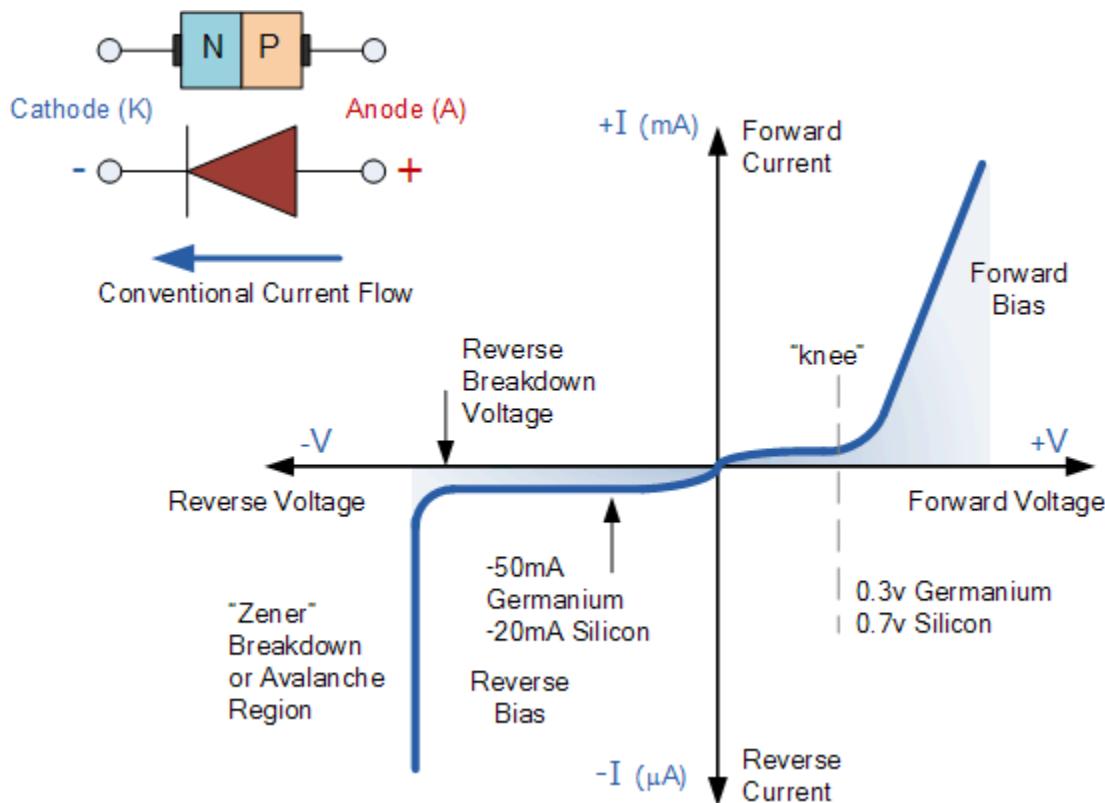
Power Dissipation:

- The ability of a component to dissipate heat is proportional to $\Delta T / R_{T,A}$, where ΔT is the difference in temp between the component and the ambient environment and $R_{T,A}$ is the thermal resistance between the component and the ambient environment.

Perovskite:

- True Perovskite CaTiO₃. A perovskite structure: ABX₃ and same crystallography as CaTiO₃.
- “colossal magnetoresistance” - their electrical resistance changes when they are put in a magnetic field
- Superconducting properties
- Ferroelectricity, charge ordering, spin dependent transport, high thermopower and the interplay of structural, magnetic and transport properties

Diodes:



- Most fundamental nonlinear circuit element
- Forward and reverse voltages are equivalent in meaning implying the minimum voltage between the electrodes to cause some specific current, in forward or reverse bias, respectively.
- (TVS) diodes fail due to excess current rather than excess voltage.
- The voltage drop across a diode, $V_f = [\text{breakdown voltage}] + [\text{current through diode}] * [\text{resistance of diode}]$. Hence the voltage and power across a diode is related to the current passing through it and the diode's inherent resistance.
 - o $P = V_f * I$.
- Forward/Breakdown voltage: Voltage difference between the anode and cathode in forward bias of the diode at which some/significant conduction (1 mA) occurs and further voltage increase causes exponential increases in current.
- [Reverse Working Maximum]/[Maximum reverse standoff] voltage: the voltage below which no significant conduction occurs, single digit nano-amps.
- Leakage current: the amount of current conducted when voltage applied is below the maximum reverse standoff voltage or current uncalculated for in ideal diode behavior. **REVERSED BIAS CURRENT**.
- Clamping voltage: the voltage that the diode sees at the input node. Usually used when the diode conducts significant current due to a forward voltage above the breakdown voltage. $V_{CLAMP} = V_{BR} + I_{Pass} \times R_{DYN}$

- I_{PP} (Peak Pulse Current): maximum surge current that can be shunted before the diode itself will overheat and fail. Derates over temperature.
- Dynamic Resistance: Diode intrinsic resistance.
- Parasitic capacitance: The nonconducting diode behaves like a capacitor, which can distort and corrupt high-speed signals.
- Amount of energy it can absorb.

Thermal Diodes:

- Semiconductor junctions vary vigorously to temperature changes.
- Diode forward voltage is inversely proportional to temperature. As temperature increases, the diode voltage drop decreases.
- This voltage is measured and from calibrations, the temperature is sensed.

Varactor Diode:

- Uses the reversed bias depletion region as a dielectric to form a capacitor. Different voltages across the diode, change the size of the depletion region and the capacitance. Voltage and capacitance is inversely proportional since depletion region increases with increased voltage, decreasing capacitance, for reverse bias.

Schottky Diode:

Zener Diode:

- Zener diodes for voltage clamping.

TVS (Transient Voltage Suppression) – Avalanche- Diode:

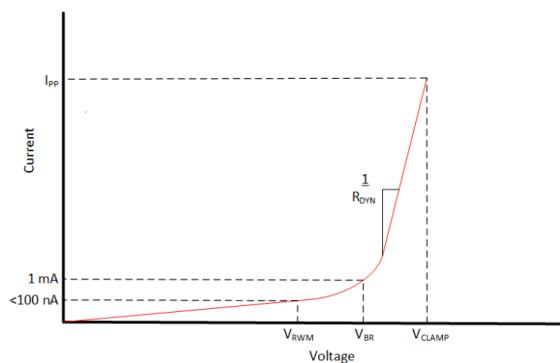


Figure 2. TVS Diode I/V Curve

- A passive component, diode to dissipate fault energy by shunting surge current and clamping surge voltage to a safe level. Efficient solution.
 - o Metal oxide varistors, gas discharge tubes, spark gaps, RC filters can also shunt current

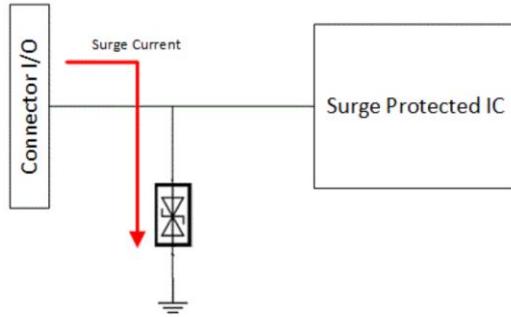
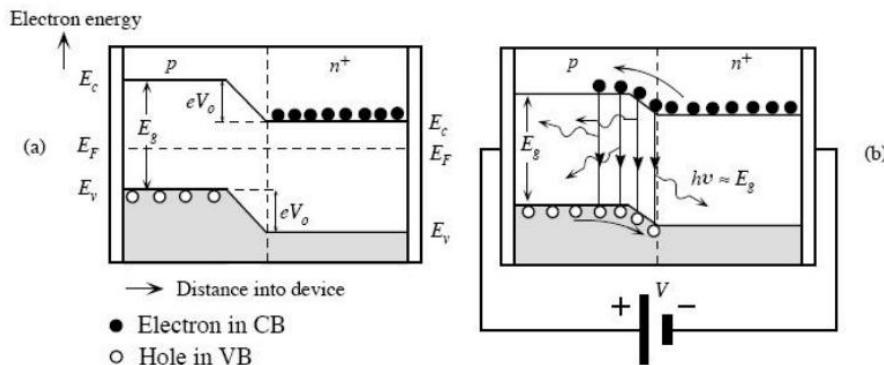


Figure 1. TVS Diode Functionality

- Ideally, should have no impact at nominal operation, i.e., $V_{RWM} > V_L$. Only impacts during transient overvoltage and overcurrent.
- $VCLAMP = VBR + ISURGE \times RDYN$
- Must have $V_{Clamp} < V_{Max\ Load}$, so that voltage seen at load is not harmful; implies minimize R_{DYN} .
- Bidirectional and unidirectional, depending on the load's input voltage working range.
- Made and tested to handle very large peak currents, relative to regular avalanche diodes.
- Useful for protection against very fast and often damaging voltage transients.
 - o In practical circuits the inductance of wires leads to slower voltage-transient prevention response.
 - o Clamping, full current shunting, can occur in roughly one picosecond.
- [How to select a Surge Diode](#)

LED (Light Emitting Diode):



(a) The energy band diagram of a $p-n^+$ (heavily n^+ -type doped) junction without any bias. Built-in potential V_0 prevents electrons from diffusing from n^+ to p side. (b) The applied bias reduces V_0 and thereby allows electrons to diffuse or be injected into the p -side. Recombination around the junction and within the diffusion length of the electrons in the p -side leads to photon emission.

Figure 1: p-n+ Junction under Unbiased and biased conditions.

- Brightness is determined by the amount of current going through the diode.
- A resistor is placed in series with the LED to control the current through the LED.
- Doped electrons are in the conduction band; doped holes are in the valence band.

- Injection electroluminescence: when conducted electrons combines with hole to release energy.
- $E = h\nu$ (nu) for a photon.
- Photons should be allowed to escape from the device without being reabsorbed
- Wavelength of the light emitted, and color, depends on the band gap energy of the materials forming the p-n junction
- Direct recombination: The spontaneous recombination in materials where the min of conduction band and max of valence band are at the same momentum. i.e., conduction and valence band have a minimized difference between them for all momenta.
 - o GaAs

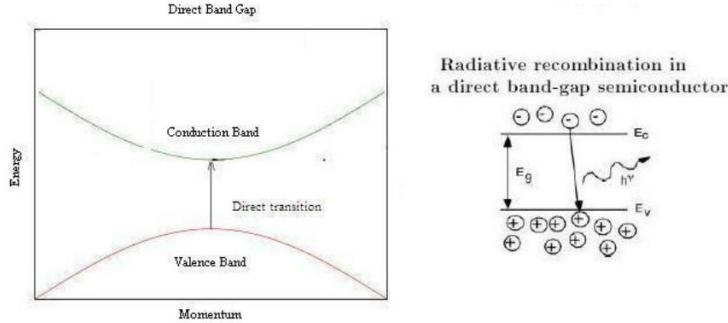


Figure 2: Direct Bandgap and Direct Recombination

- Indirect recombination: When there exists a k-vector difference in momentum of the valence & conduction bands s.t. max & mins do not exist at the same momentum. Hence, electron hole recombination is less probabilistic, and more probable at a higher E_g (blue).
 - o Dopant materials are added which form donor states where higher energy (free) electrons are captured and a momentum shift is provided for a (indirect) recombination.
- Due to 'unmatched' momenta, E_g is released in a photon and phonon.

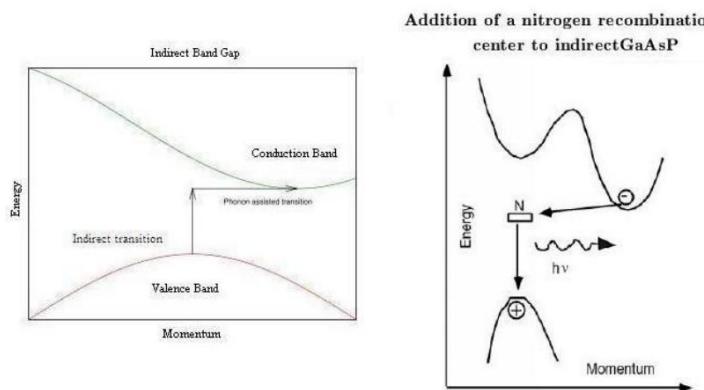
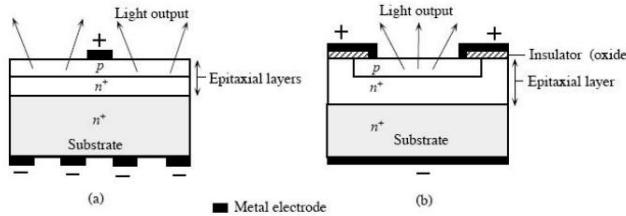


Figure 3: Indirect Bandgap and NonRadiative recombination

- Two differently doped semiconductors that are the same material is called a homojunction. When they are realized using different bandgap materials they are called a heterostructure device(see Appendix 7). A heterostructure LED is brighter than a homoJunction LED.
- LED has to be structured so that the photons emitted are not reabsorbed.
 - o Thin p-layer
 - o Recombinations should take place on a surface close to the light media (air).



A schematic illustration of typical planar surface emitting LED devices. (a) p -layer grown epitaxially on an n^+ substrate. (b) First n^+ is epitaxially grown and then p region is formed by dopant diffusion into the epitaxial layer.

- Generally an n-type substrate, with electrodes attached to p-type surface layer.
 - o Many commercial LEDs, especially GaN/InGaN, also use sapphire n substrate.
- external quantum efficiency η_{ext} : $P_{out(optical)} / IV$
 - o $\sim 1\%$ for indirect bandgap semiconductors; substantial for direct semiconductors
- η_{int} = rate of radiation recombination/ Total recombination
 - o Expresses the LED material and structure's ability to form light emitting recombinations.
- Ambient temp, over currenting; heat reduce performance and life of LED.
 - o Dim over time, not abrupt,
 - o Fast turn on
 - o On-off cycling not as sensitive as fluorescence lamps
 - o Efficient

Energy Levels:

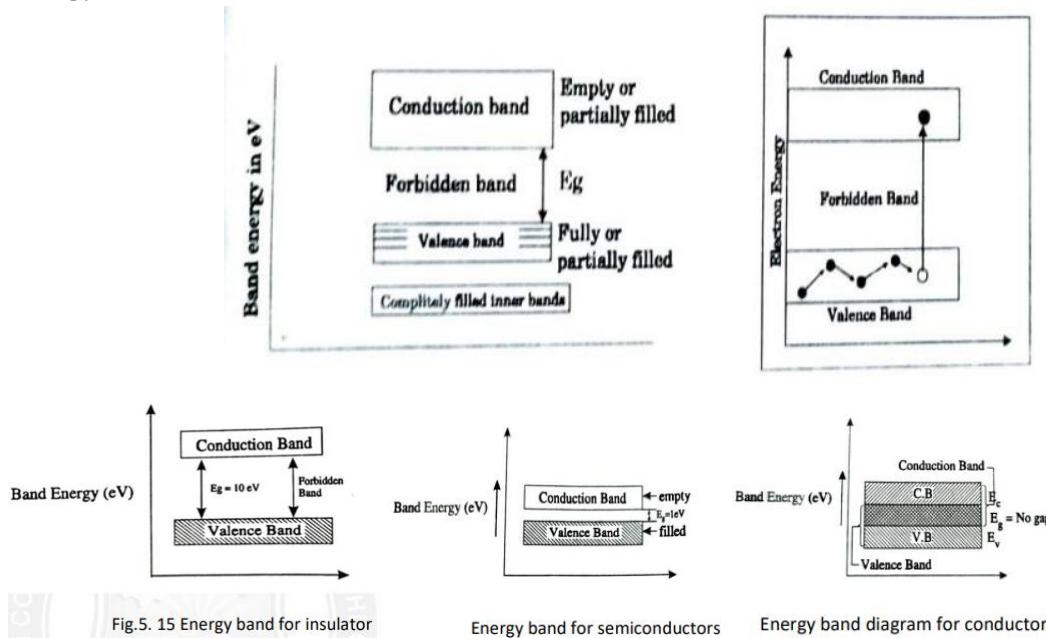


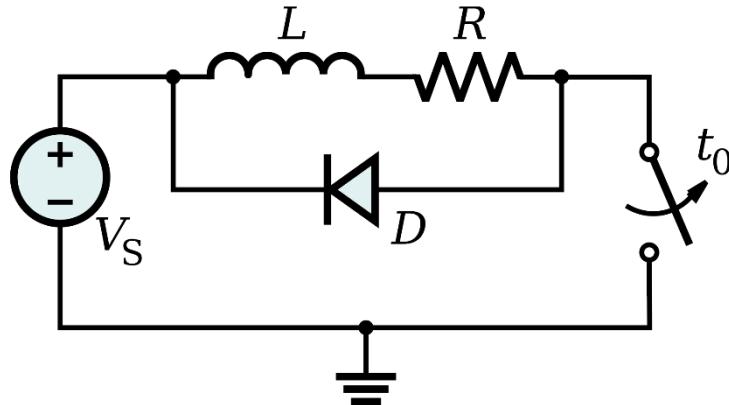
Fig.5. 15 Energy band for insulator

Energy band for semiconductors

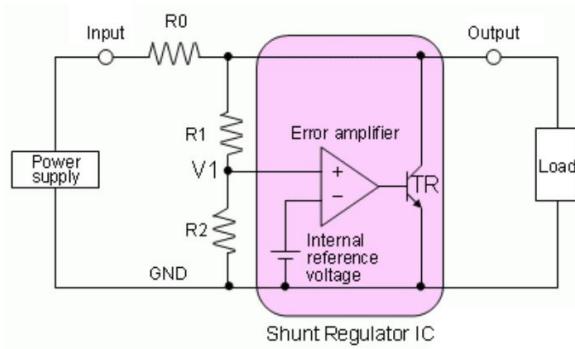
Energy band diagram for conductor

- Shows why temp increases semiconductor conduction; decreases for conductor due larger number of collisions with ions.
- The most important fact in conductors is that due to the absence of forbidden gap, there is no structure to establish holes. The total current in conductors is due to only the flow of electrons.
 - o Can't create vacancies as electrons are inherently conductive; no E_f to jump.
- ΔE_f , semiconductor = 0.5 eV to 1 eV .

Flyback Diode:



Shunt Regulator:

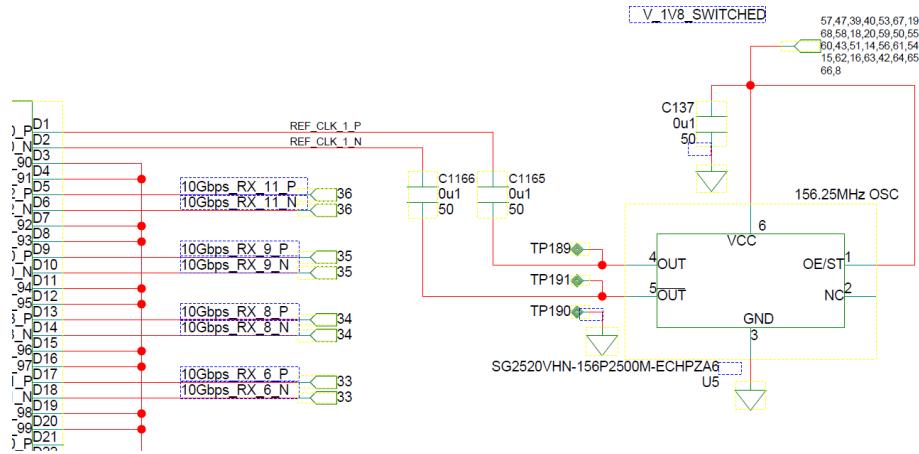


- Shunt regulator minimizes current variation of power supply, and thus voltage, and hence named “shunt” regulator. Ensures that V_1 is always equivalent to the internal reference voltage; set by a Zener diode.
- Maintains a constant voltage over voltage and current fluctuations under a maximum voltage fluctuation by adjusting current flow through the BJT.
- Altering the base voltage levels changes the BJT I_{CE} , and opposes the change in voltage by increasing or limiting current in the opposing manner.
- Detects output voltage variation via a voltage divider and an error amplifier and controls a transistor connected in **parallel** to the load to keep the output voltage constant if the load fluctuates.
- A basic limitation of shunt regulators, they cannot tolerate more fluctuations of current flowing in the load than the difference between the min. level and the max. level of the current flowing in the transistor.
- When the output voltage drops due to a variation of the load, the voltage applied to resistors R_1 and R_2 drops. This then lowers the voltage of V_1 , which is the output voltage divided by R_1 and R_2 . In other words, the input voltage of the error amplifier's non-inverted pin (+) is also lowered (below the internal reference voltage). As a result, the error amplifier causes the voltage applied to the base of transistor TR to drop, which suppresses the current flowing to the TR collector.

This in turn raises the output voltage, stabilizing it. Think of the BJT as a current-source application. And vice versa.

- [How does a shunt regulator work? | Renesas Customer Hub](#)

Oscillators:



- The output of the oscillator if probed will have an increasing DC bias and constant AC signal for Positive LVDS, and decreasing for Negative LVDS due to capacitor.
- May have Output enable (OE) or Standby (ST) pin.
 - o When LOW (generally, or HI), this tri-state pin become HI-Z. No Output from oscillator.
 - o OE does not stop the oscillations inside the component, only the output becomes HI-Z.
 - To resume, turning the output back to LO-Z, startup time in ns.
 - Oscillator input current on supply line almost the same as normal operating current.
 - When performance and speed is critical.
 - o ST stops all active circuitry within the oscillator; shut down. Supply line current becomes almost zero.
 - To restart, oscillator must go through start up period again. Start up time in the ms (long).
 - For decrease power consumption, battery powered applications.
- [Differences Between Standby and Output | DigiKey](#)

Q-Factor:

-
- [Q factor - Wikipedia](#)

Battery:

- Important terminologies on batteries: [A Guide to Understanding Battery Specifications](#)

Op-amp:

$$V_{out} = A(V_+ - V_-)$$

- Positive/negative feedback w.r.t. closed loop gain. Voltage is always compared w.r.t. to non-feedback terminal.
 - o Negative feedback → FB to inverting terminal: non-inverting terminal hold constant voltage. If $V_- = kV_O > V_+$, i.e. $V_- - V_+ > 0$, the output voltage increases, if $V_- - V_+ < 0$, output voltage decreases.
 - o Positive feedback → FB to non-inverting terminal: inverting terminal holds constant voltage. If $V_+ - V_- > 0$, output voltage increases to saturation, and v.v.. It goes in the opposite direction for equilibrium.
 - o [Positive and Negative Feedback in Op-Amps Circuits and their Practical Applications](#)
- Inverting and non-inverting op amps with negative feedback.
- Op amps have an Open-loop gain roll off of -6 dB/octave / -29.93 dB/decade, like a 1st order filter. (An op amp's A_{ol} gain seems to be going through a low-pass filter, since it is going through an RC filter! There is a capacitance inside the op amp)
 - o The cutoff frequency of this roll-off...
- Schmitt trigger and op amp with open loop gain (no feedback) as comparator to hit rails.
- Input Offset Voltage (V_{OS}): is the inherent error in the offset voltage of the input terminals, i.e. is the voltage that if applied would make the op amp output voltage = 0; mV, uV.
 - o Affected by the common-mode and supply voltages and inherent from differences in input transistors.
 - o Offset error based on ratio of offset voltage to common-mode voltage.
 - o Offset voltage drifts based on temperature and time.
 - o Lower offset voltage is traded for bandwidth and speed.
- Input Bias Current (I_B): Current flowing into inputs of an op-amp. Ideally, 2 input bias currents would equal and equate (cause no error since cancel out). Greater for bipolar rather than fets, $Z_{base} < Z_{gate}$.
 - o Input offset current is $I_{1,b} - I_{2,b}$, diff between I_B .
 - o Bias current can be decreased greatly using bias current cancellation circuits, I_b can be bidirectional.
 - o For FETS, bias current mainly due to ESD protection diodes, since high impedance gates.
 - o For Bipolar, the input bias current vs temperature increases at a higher T and less rapidly than for FETs.
 - o Bias currents go through the transistors and have the same offset voltage. Therefore, the current doesn't directly affect the error. Since current always flows in a closed loop, if the supply of the bias current forms a loop where resistors are present, such as for negative feedback, a voltage drop, i.e., an offset voltage, will

be apparent, since V_{out} is effectively the source of the bias current. By $V = IR$, an error voltage is to be summed w.r.t. the output voltage.

- Common Mode Voltage (V_{CM}): average voltage between op amp input terminals.
 - o Common-mode input voltage range/swing is the common mode input voltage range for normal, linear of op amp. Relative to +/- of supply.
 - o Output voltage swing: the range of output voltages that allow for linear operation of output signals. Relative to +/- of supply.
 - o Determine clipping/saturation of an opamp based on whether input/output voltage range/swing is within ratings.
- Operational amplifiers (op-amps) do draw current from their power supply.
 - o Ideally: Infinite open-loop gain $G = v_{out} / v$.
 - o Infinite input impedance R_{in} .
 - o And so zero input current

Input range:

- Transistors in op amps are operated in the saturation region, by using the supply voltages, so to ensure constant drain-source current, i.e. bias current. The common mode input voltage ranges are the ranges to restrict Cut-Off of the transistors.
- Common-mode Rejection Ratio (CMRR): The ratio of differential gain to common mode gain. Basically, it represents how much error is accumulated from the common mode voltage signals. CMMR effectively describes how much calibration is present to combat crossover distortion from the transition of CMI voltage.
- Rail-to-rail amplifier has input voltage range greater than supply voltage range.
- Single supply vs dual supply configuration has input voltage range depending on 1 or both supplies.
- Bipolar Op amp topologies generally have symmetric input voltage ranges, while not necessarily for CMOS due to transistor sizing adjusting Saturation V_{DS} in MOSFETs, but not for bipolar.
- For a rail-to-rail amplifier one may use 2 sep. p-channel and n-channel bipolar transistors. The PCH can cover to slightly BELOW supply, and ABOVE for NCH.
 - o This results in a “transition zone” and since the input offset voltage between the pairs are usually unequal, the transition results in an abrupt change in offset voltage => crossover distortion.
- To decrease distortion, one may also use a charge pump w/ one diff. transistor pair. Basis involves increasing V_{DS} , to adjust V_{gs} from CMI voltage. Or offset voltage calibration can increase CMMR and decrease distortion.
 - o charge pump noise from capacitor switching.
 - o If 2 diff. pairs are used, there will be offset voltage and voltage transition distortions from crossover of rail to rail amp.

Output Range

- Classic bipolar output stage has an open loop gain insignificantly effected by capacitive loading and it has a output impedance. Output range strictly reduced by $V_{sat} + V_{BE}$ from supplies.
- Slam limit: The maximum output voltage the amplifier can provide at saturation and nonlinear behaviour.
- Claw Curve: the curve representing the slam limits of output voltage swing. From the linear region to the slam limit, the voltage changes with lower gain (not linear). The linear region is usually indicated by a cutoff region with high gain, > 120 dB. The claws at the end are the op-amps short circuit protection, which at high output currents, the op amp increases its inherent output impedance somehow. To read the claw curve, calculate the output voltage, w.r.t. the op amp gain and calculated the current using ohm's law with the load resistor, match this (output) current on the claw curve to determine the slam limits. Notice how the linear region is always within the slam limits of the claw curve?

Valuable Info:

- The output current limit on an op amp means the maximum current that the op amp can source due to the transistor saturation. The op amp will clamp the output to this current, if exceeding it is attempted. This max current rating is a "can't" not "don't" -exceed value.
 - o (Current saturation, is saturation.) Saturation in a transistor is caused by R_c and I_{be} for bipolar transistors, V_{gs} and V_{ds} , to affect $R_{ds(on)}$, for FETs.

Offset Voltage & Bias Current:

- Like offset current, offset voltage is the voltage diff between two terminals.
- For smaller signal gain, the offset voltage presents a higher percent of the error seen at the output.
- For higher (open-loop) gain op amps, the offset voltage produces a greater error magnitude at the output.
- V_{os} drift is the coefficient representing the increase in offset voltage produced by an increase in temperature added to an initial ambient temp.
 - o Assumes linearity, which is not always the case.
- BJTs: V_{os} produced from V_{be} difference between differential BJT pair.
 - o Lithography, doping, packaging stresses processes
- FETs: V_{os} from V_{gs} threshold difference between differential FET pair.
- Bipolar V_{os} drift is predictable in its linearity. V_{os} drift directly proportional to temperature
 - o So, the V_{os} drift coefficient changes linearly with temperature. Implies a quadratic V_{os} relationship with temp.
 - each millivolt of offset yields about $+3.3\mu V/C$ of offset drift.
- FET V_{os} drift is non linear and no proportionality is present.
- Trimming internal resistors ($R_{1/2}$, $R_{os1/2}$) to compensate for offset voltage
 - o Laser trimming thin film resistors at wafer level.
 - o Bipolar resistor trimmed at one temperature due to linearity, FETs at multiple
 - o Bipolar resistor trims $R_{os1/2}$, FET requires trim of $R_{1/2}$ in trim calculation due to complexity.

- Voltage (resistor) trimming changes I_q , gain, Saturation of transistors and these have to be considered before trimming.

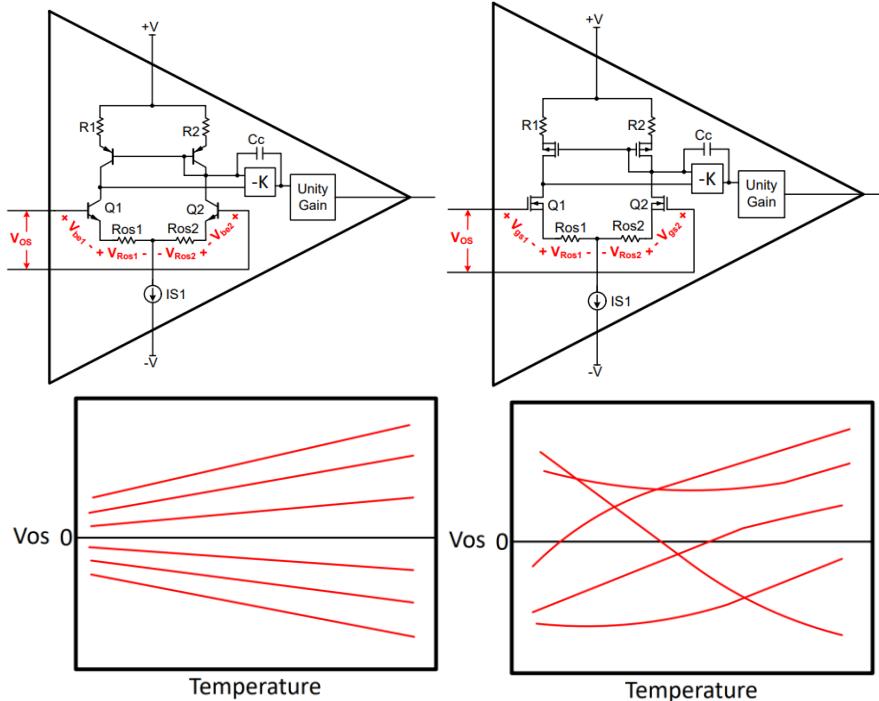


Figure 1-7. Bipolar V_{OS} vs Temperature

Figure 1-8. CMOS V_{OS} vs Temperature

Integrator:

- The capacitor stores charge and the output voltage is equal to opposite that of the charge stored on the input side.
- DC biases are completely blocked by the capacitor. By superposition principle, these biases would have a gain of the open-loop gain of the integrator, hence provide negative feedback to the output by feeding back to the integration capacitor at the input side to reduce appropriately and DC gain can be limited to a finite value by inserting the $R_{feedback}$!
- Additionally match impedances at the inverting and non-inverting side to minimize input bias offset currents (which generate offset voltages).
- Errors caused by a continuous, unsymmetrical offset error or bias current increase V_{out} . With V_{out} connected back to the input side of the capacitor, the error is undone.
- A large resistor is used, so that minimal feedback current returns, as minimal error was generated initially; better feedback equilibrium.
- For an integrator:

In some applications it is necessary to refer the offset error to the output in order to derive meaningful results. In this case the output error is a drift rate which is given by,

$$\frac{de_o}{dt} = \frac{e_{o1} + R i_{o1}}{RC} = \frac{e_{o1}}{RC} + \frac{i_{o1}}{C}$$

Again, we see that output drift rate is minimized by using the smallest value for R and the largest value for C. This follows since the drift rate due to offset voltage is fixed by the gain of the circuit ($1/RC$) whereas the drift rate due to offset current is reduced by using a larger C.

The practical limits on the choice of R and C are as follows:

1. Source impedance sets a minimum value on input impedance which is equal to R.
2. The physical size, price and quality are all serious problems in using large value capacitors particularly when greater than 1 to 5 μ F.

- The large feedback resistor unfortunately:
 - o Creates an inverting amplifier offset voltage at the output
 - o Leakage current through R creates voltage drop?
 - o At LF, cap it Hi Z, so “leakage” and “amplified offset voltage” are problems. At HF, these aren’t problems since R is Hi Z compared to cap.
- [Operational-Integrators.pdf](#)
- [Op amp integrator - Wikipedia](#)

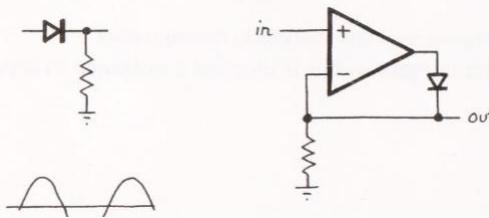
Differentiator:

$$dV_{out}/dt \ll dV_{in}/dt$$

- Want the above, as the above implies that V_out will be a square wave.
 - o If dV_{out}/dt is small implies almost horizontal line behaviour of $dV_{in}/dt = V_{out}$
- Note: a differentiator has RC positions reversed to that of an integrator. Uses $I = CdV/dt$.

Rectifier:

- Generally, passive rectifier has undesired diode voltage drop offsets.
- Active rectifiers remove diode offset by feedback
- Simple active rectifier saturates at high V_in and doesn’t represent V_in when V_in is high.



- Complexer active rectifier never saturates since always feedback, i.e., linkage to output to prevent Hi V_in saturation. Low V_in blocking is not a problem since rectifier!

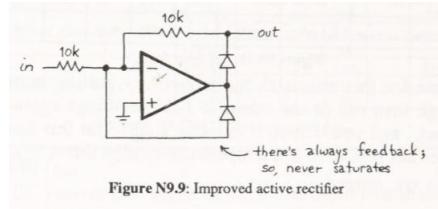


Figure N9.9: Improved active rectifier

Schmitt Trigger:

- An input signal with a slow slew rate fed to a MOSFET, can lead to an oscillatory output signal due to noise and resultant voltage drops (caused by increased currents), leading to bad data.
- Schmitt Triggers are buffers used for digital-data-signal receivers that receive a low slew rate signal, which would otherwise cause unpredictable state changes in the switch, and hence output signal, to produce a clean square wave output signal.
- Uses hysteresis [: the dependence of the state of a system based on its history], to reject noise and state changes.

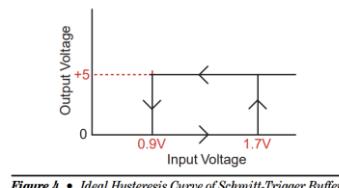
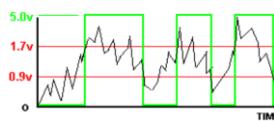
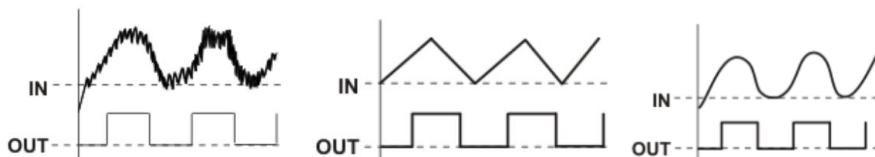


Figure 4 • Ideal Hysteresis Curve of Schmitt-Trigger Buffer



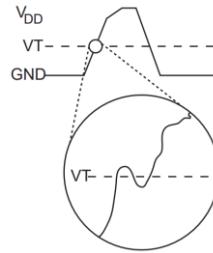
- Schmitt trigger input has the switching threshold adjusted where the part will switch at a higher point (V_{t+}) on the rising edge and at a lower point (V_{t-}) on the falling edge. The difference in these switching points is called Hysteresis ($^{\Delta}V_t$). A non-Schmitt trigger has $V_{\text{Threshold}}$, i.e., $^{\Delta}V_t = 0$.
- A Schmitt trigger can transform any signal that reaches its thresholds to a square wave using hysteresis theory.



- [Understanding Schmitt Triggers \(Rev. A\)](#)
- [Using Schmitt Triggers for Low Slew-Rate Input](#)

Noise

- A finite slew rate will be susceptible to finite noise; an infinite slew rate will only be susceptible to infinite noise.
 - o A slow slew rate effectively allows noise to cause a state changes, by the slew rate not being fast enough to counteract the absence of noise.



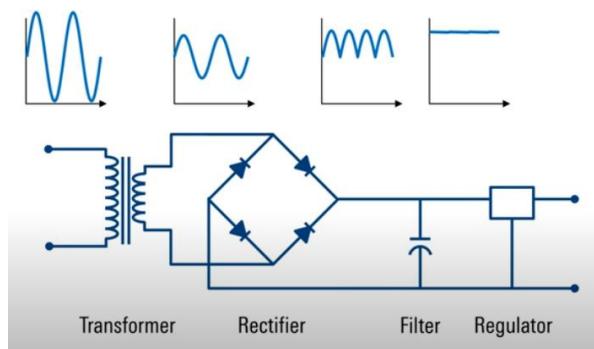
- The peak-to-peak amplitude of the noise should be always less than the difference between the threshold voltages. If the input signal is already in the range between the threshold voltages, the noise should always be less than the difference between the next threshold voltage and the current input signal voltage.
- As said above, a slow slew rate essentially cannot overcome the inherent noise and hence the noise causes state changes.
- When an input signal reaches the threshold of the MOSFET switch, the output signal's current, sourced from VCC, also increases. By $V = IR$, the voltage at the drain of the switch, i.e. VCC, will be lower, from the source impedance. Since VCC (drain) is lower, V_{gs} increases, the low slew rate (of the gate voltage), although slowly, still increases. But due to the low slew rate, any noise fluctuation can cause the input voltage to droop, turning off the MOSFET, and repeating this oscillatory cycle. Since noise is so prevalent, this oscillation can occur many until the low slew rate eventually leaves the threshold voltage area.
 - o Rising and falling edges.

Power Supplies:

- Converts HV mains AC into stable, LV DC
- Power Management Integrated Circuit (PMIC)

Linear:

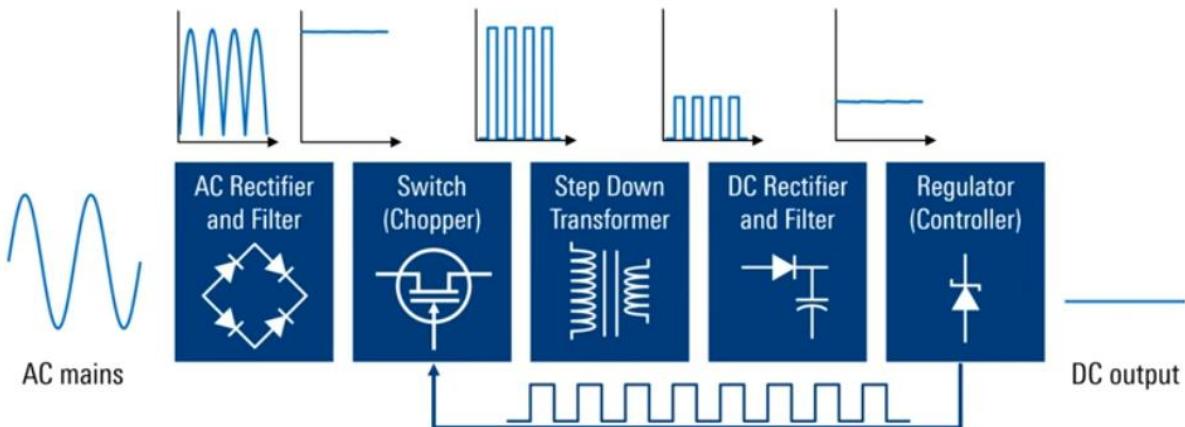
1. Transformer steps down ac voltage.
2. Rectification using diodes.
 - a. [Full-bridge diode]/[half-bridge diode w/ center tapped transformer] full-wave (absolute) vs half-wave (positive).
3. Filtering using caps and inductors which store energy. Output voltage will have some ripple.
 - a. A smaller capacitor or larger load impedance causes more ripple due to quicker discharge.
4. Regulation controls output voltage ripple, independent of filters and load.



- Cheap, simple, low emissions, though large, heavy (ac s.d. transformer), and inefficient.

SMPS:

- Ac-dc and dc-dc converters.
- 1. Full-wave rectification using diodes; full bridge diode preferred.
- 2. Full eave output filtered using caps and inductors - > HV DC.
- 3. Switches the HV DC into square pulses using a power transistor MOSFET (Chopper),
 - a. HF 10 kHz – MHz gate signal applied.
 - b. FET has high efficiency as a chopper with low switching losses.
- 4. Step down transformer for HV, HF pulsed DC.
 - a. HF pulses can yield to a smaller transformer and filtering components.
 - b. Electrical isolation
- 5. Filtering of LV, HF pulsed DC using diodes, caps, and inductors; smaller size due to HF.
- 6. Regulation of output voltage independent of load impedance and source voltage by changing duty cycle w/ a reference point. PWM.
 - a. Opto isolator for electrical isolation without stepdown transformer.
- Smaller, more efficient, flexible, but complicated, expensive, and higher emissions.
- Higher slew rate is more desirable.



Voltage Regulators:

LDO:

- DC Voltage regulator or filtering component.
- High PSRR to reject/filter/attenuate AC EMI [V], switching noises, to generate a clean DC rail.
 - o High PSRR over wide bandwidth desired.
- If used as a filter, optimize PSRR and note that the LDO needs input & output decoupling capacitors to function properly.
- The PSRR characteristics: The first region depends on the internal reference and internal filtering of the LDO. The second region depends on the open loop gain of the LDO error amplifier. Lastly, the third region depends on the total parasitic elements and output capacitance of the LDO.

Larger amounts of output capacitors allow more noise to be shunted to the system return path and result in an overall lowering of the output noise.

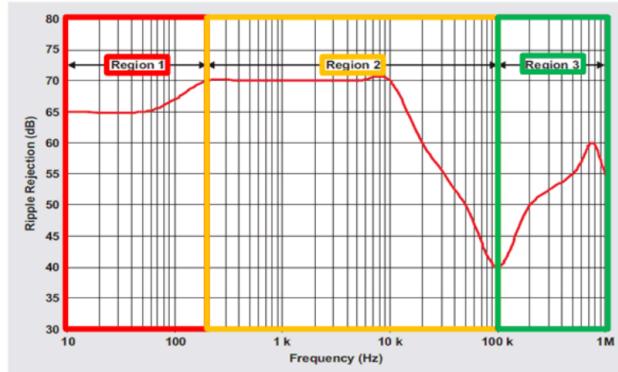
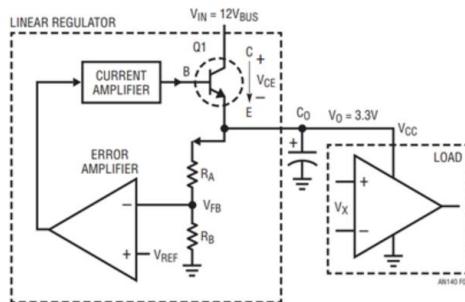


Figure 10. Different Regions of a LDO PSRR Plot

- Pass transistor is in high-dissipation, on-state, in linear region, allowing resistor-like power dissipation and control.
- High bandwidth.
- Require heat dissipation, increasing unit size. Not efficient, though at low dropouts, become more efficient; high light load efficiency. Only step down.
- Voltage regulation through using feedback through op amp and altering the transistor gate/base voltage/current in transistors linear region.
 - LDOs may be in non-linear region, which may be harder to control.



SMPS:

- Uses an inductor and the current regulation of inductors using an emf force with a capacitors ability to store emf to control current and voltage.
- Switching Regulators:
 - Pass transistor switches between low power dissipation, *full-on and full-off* states.
 - Duty cycle is varied for voltage regulation.
 - Higher efficiency. Low light load efficiency.

- Transformers' power handing capacity is proportional to frequency (provided that hysteresis losses are minimized) and thus is inversely proportional to frequency. At the higher frequencies of a SMPS, the transformer size is minimized.
- Noisy
- Buck Converter:
 - Step-down voltage regulator
 - Inductor based switching control. Output voltage is equal to input voltage x duty cycle.
 - The total energy being transferred is 0. The increase of stored energy in the inductor during the ON time of the switch is equal to the energy discharged into the output during the OFF time of the switch, ensuring steady-state operation.
 - Ccm vs dcm conduction modes. [Topic 3 Lynch.pdf](#)
 - Briefly, DCM mode has all the energy in the inductor discharged in each switching cycle/period, as opposed to CCM, which (may) does not have the inductor completely discharged when the switch is OFF.
 - In DCM all the energy discharges in a time shorter than 1-D, where D is the conduction charge time, since there has to be some dead time (I presume for something). So the peak current in the diode and when the switch is OFF is higher; hence more noisier.
 - the RMS losses will be greater in a DCM converter than in an equivalent CCM converter.
 - EMI Filters need to be more curated for DCM and more emphasized.

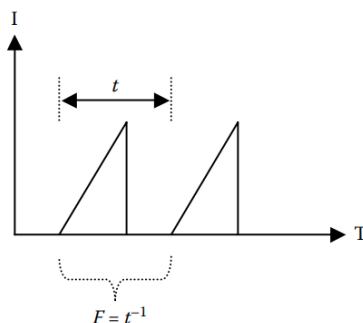


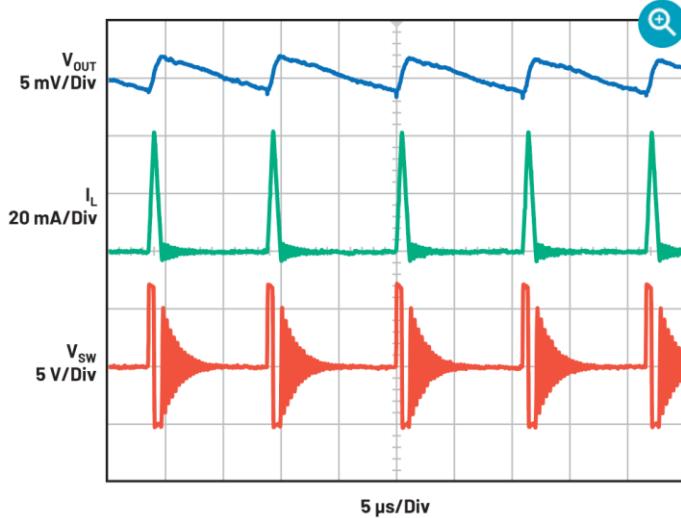
FIGURE 19.2 PWM discontinuous current signature for power converter.

- [AN-140: Basic Concepts of Linear Regulator and Switching Mode Power Supplies | Analog Devices](#)
- [*Switching regulator fundamentals \(Rev. C\)](#)

Application:

- The rising edge of the switching node, and the rising time of the output voltage is much noisier (ringing) due to the increase parasitic inductance (current loop size) of the switch on.

- Switching voltage is the voltage seen across the switch (of a SMPS); it is the voltage denoting the SW node/pin.
 - o It is caused by the switching inductor back e.m.f.s.



- Above, one can see the effect of the output voltage, switching inductor current, and switching voltage for a single switch of the power MOSFET node.
 - o Picture shows one pulse by a Burst Mode SMPS.
 - o In Burst Mode, the switching is paused and resumed at certain output voltage thresholds.
- [When Pulses Are Omitted in Switch-Mode Power Supplies | Analog Devices](#)
- The current through the inductor, I_L : when the switch is on, a constant voltage is across the inductor and by the DE of $I_L = Ldv/dt$, the current is positive linear. When the switch turns off, the change in current generates a back e.m.f. whose value depends on the change in current of the switch. My hypothesis is that first the current is linear negative and then quadratic linear. The switching time is linear, the (fully) OFF is quadratic.
- Therefore, knowing the current through the inductor, the voltage at the output capacitor can be inferred to be something similar, but smaller in ripple.
- Inductor back e.m.f. is proportional to the change in current, although current can increase, if the change in current is constant, the back e.m.f. stays the same.
- The SYNC pin takes an external clock signal and allows synchronization/locking between the phase of the input clock and the power-MOSFET-switch-gate-driver oscillator. This allows multiple regulators to operate in phase, reducing noise, and efficiency in parallel.
 - o Decrease beat frequencies and THD.
 - o [Reducing Noise by Synchronizing Switching Regulators | Analog Devices](#)
- Note: A larger input capacitance is required when a lower switching frequency is used to increase the charge time/storage of the caps.
- Note: A higher switching frequency decreases the output current ripple since inductive filtering/impedance increases with frequency.
- Output capacitor filters the DC output, hence a low impedance at the switching frequency is desired.

HF and LF Noise:

- di/dt is proportional to input voltage difference, and inversely proportional to switching inductance, since $di/dt = V_L/L$.
 - o So, higher voltage $V_{in}-V_{out}$ difference will be noisier.
 - o Consider the following equations and how they relate to the above and for detail on the switching node current parameters.

$$\Delta I_L = \frac{(V_{in} - V_{out}) \cdot D}{L \cdot f_s} \quad I_{max} = I_{load} + \frac{\Delta I_L}{2} \quad I_{min} = I_{load} - \frac{\Delta I_L}{2}$$

- HF noise is dependent on di/dt , see above, and internals (parasitic inductances at switching node) of the switcher IC.
- A higher current load will generate higher LF pk-to-pk voltage ripple (noise) by Ohm's Law.
- LF noise pk-to-pk is modifiable dependent on switching inductor, capacitors, and switching frequency.

Considerations:

- A larger value inductor provides a higher maximum load current and reduces the output voltage ripple
- The higher the inductance the lower the (peak) current through the switching inductor, but the need for phase compensation arises. Vice versa, a higher saturation current inductor is needed.
- The higher the input/output capacitors, the lower the voltage ripples at the input/output, respectively.
 - o Capacitor temperature derating can be minimized with high dielectric constant.
 - o A larger capacitor exhibits less derating at higher voltages.
 - o That is, larger capacitance, implies less voltage derating.
- Long duration overload or short-circuit conditions, the inductor current RMS rating requirement is greater to avoid overheating of the inductor.
- The higher the output load the lower the efficiency of converter, a type of derating.
- Operating frequency is a trade-off between efficiency, component size, and input voltage range
- Size and cost of passive components, $L + C + R$, affected by switching frequency.
- Higher switching frequency implies higher coupling of switching signal through passive components to other parts of the PCB.
- Higher frequency:
 - o Implies smaller output stage inductor and capacitors can be used, since higher f implies more EM energy stored in passive components which can offset the loss of EM energy storage by higher valued/ bigger passive components.
 - o Lower efficiency and a smaller input voltage range.
- If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no-load input current to the converter. Hence limiting the current decreases the load and hence efficiency.
- To keep the efficiency high, the series resistance (DCR) should be less than 0.02Ω , and the core material should be intended for high frequency applications.

- Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability.
- Burst Mode:
 - o For high conversion efficiencies.
 - o The switching node switches once/a couple before changing over to a longer pause phase. During this pause phase, numerous functions of the switching regulator IC are put into a sleep mode in which only a very low amount of supply energy is needed.
 - o Usually, as many pulses as necessary are generated until the output voltage reaches a set upper threshold. This is followed by a pause that lasts until the output voltage falls below a minimum threshold.
 - o voltage ripple of the output voltage is higher during operation in Burst Mode, though lower in frequency. See “When Pulses...” link.
- Pulse skipping:
 - o Involves keeping the output voltage within a certain range and does not save any significant amount of energy. The conversion efficiency thus only improves slightly.

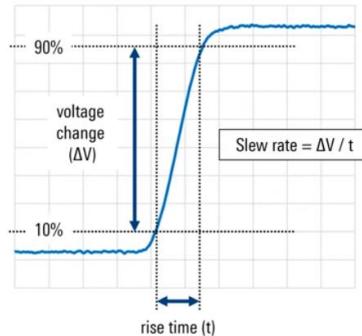
Equivalent input:

- The signal, mostly noise, of the output of a system, in the units of the system, isolated as a separate input to the data signal/

Slew Rate:

- Rate of change in voltage (or current) per unit time.
- Controlled by capacitors, inductors, and resistors, i.e. loading effects.
- Consequences:
 - o **Higher slew rate can lead to greater EMI** since faster rise times lead to higher frequency harmonics.
 - o High slew rates during operation (or start-up) cause transient spikes (EMI) ^ such as from Ground Bounce phenomenon.
 - o Inrush currents can be limited by reducing current slew rate.
- Application: The SLEW pin sets the slew rate for the FET driving the SW pin. For the fastest slew rate (best efficiency), leave the SLEW pin open. For a normal slew rate, connect the SLEW pin to VREG. For the slowest slew rate (best noise performance), connect the SLEW pin to GND.
- $\Delta V / t$; where the data considered for slew rate can be defined from percentage of max waveform amplitude. 10% - 90%, or 20/80.
- **Higher slew rate decrease switching losses but may increase level of transients at output.**
- Low slew rates are desired for EMI purposes. E.g., Soft-start for controlled, monotonic slew rate during startup.

- Limits the fast inrush currents caused by capacitive loads.
- Measured using scope and probes with sufficient bandwidth and range.
- A low slew rate is caused by **capacitive (and inductive) loading/charging and low drive capability** of the input signal. Increased current and decreased capacitance decreases the charge up time of caps, hence increasing slew rate.



Learn the LC parallel filter by learning slew rate and the Miller effect and TI videos on slew rate. Very non trivial.

What I need to learn next:

- Switching Regulators, crosstalk, SerDes (PLL) more, RC, RL, RLC, series and parallel circuits.
- Noise and the different materials and noise conditions
- OSI
- Design schematics
- Nand
- FMC
- [Practical Techniques to Avoid Instability Due to Capacitive Loading | Analog Devices](#)
 - What is capacitive loading of amplifiers and why does the phase shift cause oscillations, requiring the RL filter?
<https://www.bing.com/ck/a?!&&p=822b25ee049842af8e7f29d725e2eb8baf05d8e0efa000cbe570c3fbb2d201jmltdHM9MTczNzA3MjAwMA&ptn=3&ver=2&hs=h=4&fclid=03532bac-89c7-6b31-2325-3ec088546af4&u=a1L3ZpZGVvcy9yaXZlcnZpZXcvcmVsYXRIZHZpZGVvP3E9Y2FwYWNpdG12ZStsb2FkaW5nK2VmZmVjdHMmbWlkPTc4NkZBQzE2NDI0QzI0NjIxRkRCNzg2RkFDMDTY0MjRDMjQ2OTFGREImbWNpZD0xQUIyRDAzNzBERkY0MkY0QjQ5Mzg0RTJEOEM0MENDRCZGT1JNPVZJUkU&ntb=1>
- inductors

Learned about SMPS and inductors and buck converters. I understand the general operation and how the duty cycle determines the output voltage.

- Will have to look more into how boost converters work.

Learned about general op amp theory including how to read the data sheets, the offset voltage and bias current error and the common mode voltage cut off range.

- Briefly read over comparators but they are just positive feedback op amps.

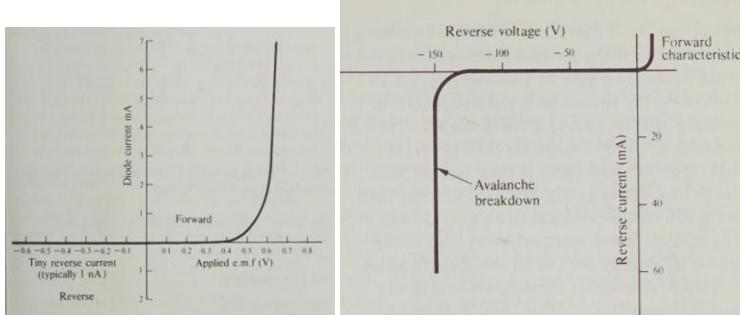
Trying to learn more on slew rate and op amp internals since so much of the chips are based on these. But its pretty complicated.

Trying to understand the LC parallel filter that reduces capacitive loading due to phase shifts cause oscillations, but the explanation brings be back to op amp properties.

Semiconductors:

- The conductivity of conductors decrease with temperature due to obstructive vibrations, while the conductivity of semiconductors increase due to increase electron-hole pairs generate to aid conduction
- Intrinsic semiconductor: Total negative charge carriers = Total positive charge carriers.
- Conduction of semiconductors in their pure form with defects form thermal energyis the intrinsic conductivity.
- Extrinsic conductivity is much higher by doping.
- Majority carriers: the charge carriers generated by doping,; extrinsic.
- Minority carriers: the charge carriers generated by inherent thermal vibrations; intrinsic.
- In forward bias, the depletion region and resistance of the junction dcreases.

Exponential increase in current by voltage.



- Reverse and forward bias due to the net neutral charge of semiconductors and how electron-hole drift and diffusion generate opposite charges on the terminal, essentially promoting or locking up the junction due to the electric fields.
- Breakdown voltage due to acceleration of electrons to become mobile and then collide with others.
- Higher doped p-n junctions result in thinner depletion region since more charge is present in p-n regions, yielding to more electron-hole pair recombination per area. This increases of electron-hole recombination, increases the drift voltage to match the voltage applied at the gates. This decreasing breakdown voltage and leading to Zener diodes.

- In reverse bias, higher doping implies smaller depletion region. And lower doping implies larger depletion region.
- The size of the depletion region is directly proportional to the voltage across it. Higher depletion region implies higher p.d., and vice versa. Therefore reversed bias depletion regions have a higher p.d.. This thought leads to the voltage gains of BJT topologies.

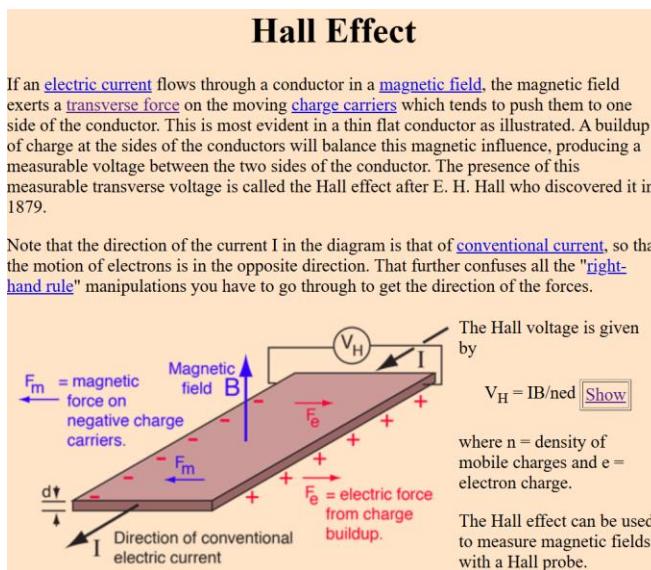
Silicon:

- The electrical resistance of silicon increases with temperature up to around 160 C, then actually starts decreasing, then decreases even more when the melting point of silicon is reached.
 - o Something to do with increased mobility of carriers.

Carriers:

- Charge carriers: either electrons (negative charge carriers) or holes (positive charge carriers)
- Negative/positive carriers only come from the respective N-type/P-type semiconductor.
 - o Hence, majority carrier in NPN are electrons since they move from emitter to base, and drain, with small recombination at the base, facilitating the minority carriers of the hole.
- Majority charge carrier: The charge carrier present in large(r)/most quantity; very simple.
 - o Mainly responsible for current flow
 - o Electrons for NPN, v.v..
 - o Holes for PNP, v.v..
- Minority charge carrier: The charge carrier in small(er) quantity.
 - o Carry a (very) small amount of electric current.
- It may seem confusing since only electrons actually move; any recombination of electron-hole pairs are both electron and hole movement, and the majority or minority carrier are simply based on quantity.
- Hence, BJTs are bipolar, as they have 2 currents, I_{EB} (minority) and I_{EC} (majority).

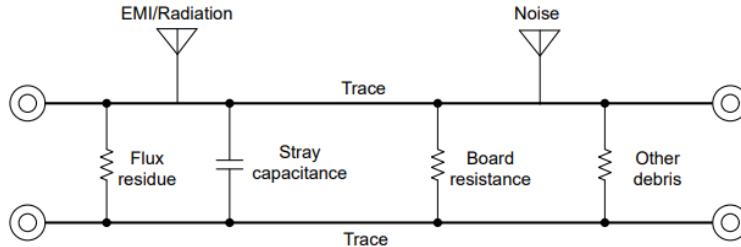
Hall Effect:



Current:

- Caused by voltage, e.m.f. force; charge.

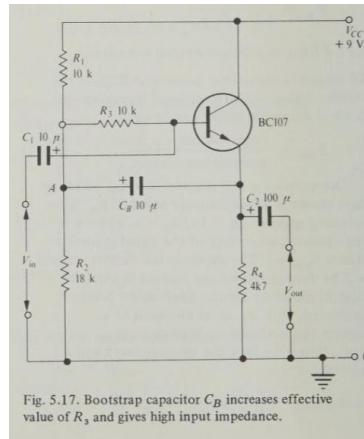
Leakage Current:



- With the guard ring and the net at the same potential, this effectively creates an incredibly small voltage delta between the trace and immediate surrounding area which drastically reduces the possibility of stray leakage currents leaking into this area of the PCB.
- Leakage increases with temperature
- Leakage current is due to a potential difference from “adjacent” traces which acts as a parallel circuit and a current source to the “known” circuit.
- This leakage-current, parallel circuit has the same voltage at the junction from which the leakage flows into the “desired” circuit.
 - o The extra current effectively changes the current of the real circuit, increase/decrease. Since resistance stay constant, by $V = IR$, the leakage changes the voltage of the real circuit.
 - o The leakage current effectively causes negative offset voltage by going against the original. Positive if going along the original.
 - o Leakage current produces more offset voltage If source impedance is higher.
- Non-infinite resistances imply (leakage) current flowing from different potential differences and forming a closed loop.
- Leakage current causes an offset voltage of $I_{\text{leak}} * R_{\text{source+on}}$ (such as in MUXs, due to high load impedance of amplifier).
 - o Assumed leakage current source a current source which causes the offset.
- Avoid leakage current by proper layout of chip and can add guard traces and guard planes or even concentric guards that minimize the p.d. between the signal trace and the side trace.
 - o A guard trace and plane (boxing ring) provides a 360 degree shielding in a way.
- Guard voltage must mimic the net voltage as close as possible
 - o Can use a high precision buffer.
- Bury sensitive nets within PCB to reduce possibility of debris or contamination.
- [Guarding in Multiplexer Applications](#)

Quiescent:

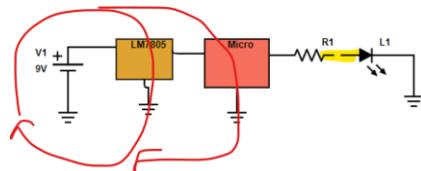
Quiescent Point:



- The DC operating conditions (current and voltage) set for an electronic component that processes AC time-varying signals with no input signal applied.
 - o Diodes, transistors, vacuum tubes.
 - o The AC signal applied to them is superposed on this DC bias current or voltage.
- Generally chosen at the center on the characteristic curve to maximize transistor's linearity, efficiency, and stability in the circuit.
- BJT:
 - o Voltage/currents at the terminals with no AC input signal present.
- MOSFET:
 - o V_{gs} and I_{ds} when no AC input signal is present on gate.
- This DC current or voltage required to operate correctly in the desired way
 - o For a transistor, it can be the gate bias voltage.
- [Biasing - Wikipedia](#)

Quiescent Current:

- Quiescent state is when the IC is in a no [load/switching] state and is defined by the voltages and currents present in the circuit when the power supply is on and stable, but no signal is applied.
 - o IC enabled still
 - o Paramount in energy efficiency

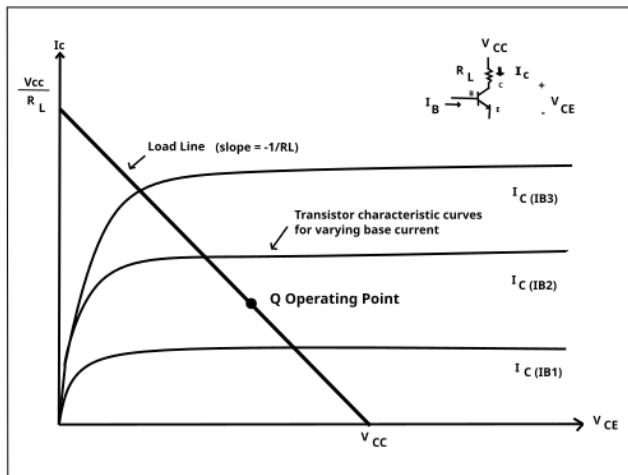


- Current through an IC when the device is active but no power supply is "on" (i.e., in low impedance). So the IC receives current only from diodes.

- Leakage Current: Current leak from diodes (forward and reverse) that can be thought as voltage suckers, or parasitic capacitance that takes voltage, e.g. from the gate of a MOSFET which decreases the true voltage on the gate, lower drain current. Higher leakage current implies lower resistance in compensation.
- Low leakage current of mosfets by high gate insulation means higher impedance gate voltages could be accepted. This risks static charges, so always short the gate when soldering a transistor. OR, use back to back Zener diodes shorted to GND.
- [Quiescent Current \(1\).pdf](#) (read if have time, unread).

Load Line:

- A load line is an I vs. V plot that represents the Quiescent point of a nonlinear 'system' (diode, transistor) as constrained by the linear part of the circuit, which is connected to the non linear part, in the circuit.
- It shows where the circuit thus must operate, i.e., be quiescent.

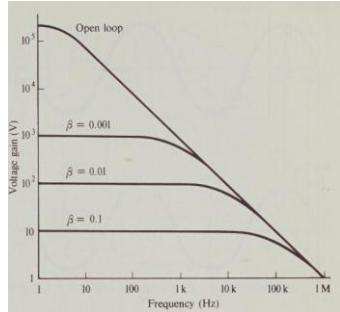


I/O Injection Current:

- Bidirectional
 - o Negative current is defined as current sourced by the pin.
 - o Positive current is defined as current source by a signal input
- Current entering I/O pins due to a signal input higher than V_{cc} or lower than GND. That is, below V_{ss} or above V_{dd} . Voltage can be lower than a GND if a floating power supply's GND is inputted.
 - o Current flows through input protection diodes to whichever supply is exceeded.
 - o V_{il} is input low level voltage
 - o V_{ih} is input high level voltage
- Injection current calculated by Ohm's law.
- I/O current injection causes ADC error.
 - o Non-zero injection current can affect ADC by 4-6 counts.
 - o >5 LSB TUE

- Due to the controller's pin ratings, voltage beyond GND – VCC causes more parasitic current via the pin, thus pin injection.
- *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*
- [pic - What does "injection current" mean in the context of a microcontroller datasheet? - Electrical Engineering Stack Exchange](#)
- [stm32f446ze.pdf](#)

Amplifiers:



- Frequency range of audio band: 20 Hz to about 20 kHz.
 - the open loop gain of amplifiers decreases at high frequencies, largely as a result of stray capacitance, this also limits the benefits of negative feedback.
 - Basically, for constant gain with negative feedback, want AOL > beta (NFB).
 - Infinite gain implies amplifier output signal with no input.
 - If excessive variation of gain with signal frequency, the amplifier has a poor frequency response, frequency distortion. To decrease variation, make open loop gain >> closed-loop gain (<1) for independent gain and frequency.
 - o Gain is independent of frequency when gain is not a function of any open loop gain?
 - The linearity (constant) gain with respect to frequency of negative feedback yields to lower gains but more constant, to achieve the same magnitude of gain as open loop, 2 negative feedback in cascade and return this high gain, with an optimal frequency response.
 - **Feed back** always improves the desired signal voltage amplification, decreasing distortion, but at the cost of lower gain.
 - Amplification of greater signals is (exponentially) more susceptible to distortion, thus using negative feedback which decreases distortion at the cost of gain, can be amplified yet again with little distortion due to now incredibly low biased signal.
- $$v_{\text{out}} = \frac{A_0}{1 + \beta A_0} v_{\text{in}} + \frac{D_0}{1 + \beta A_0},$$
- Amplifier oscillation occurs when open-loop and feedback gain equal 1; i.e. when total gain is infinity.

- At high amplification frequencies, the stray capacitance can cause a phase shift of 180° inversion. A large compensating capacitor keeps the open loop gain small... Nyquist stability criterion...

Common-Mode Rejection Ratio:

- The classification of a receiver to reject the signal common to both (two) of its differential input lines; common mode noise.
- $\text{CMRR} = \text{Noise attenuation factor} \times \text{Signal amplification factor}$.
- For an op amp, $\text{CMRR} = G_{\text{differential}} / G_{\text{common-mode}}$. That is, differential gain / common mode gain.
- Increasing CMRR could mean decreasing G_{cm} . G_{cm} is decreased by increasing the impedance of the emitter-side resistors. Maximum (infinite) impedance is realized when the R_{tail} resistance is infinite, i.e., a current-source at the differential tail.
 - o Increasing r_e is not viable, as it is the internal dynamic resistance of BJT dependent on I_C and V_{BE} .
 - o Increasing R_E wouldn't work as that would affect the differential gain.
 - o Only the tail impedance is variable since increasing R_E decreases differential gain at a higher rate than common mode gain. So actually decreasing CMRR.
 - o the "A" node voltage doesn't change under differential signals only.
- Note: $x 10^6 = 120 \text{ dB}$.

Multiplexers (MUXs):

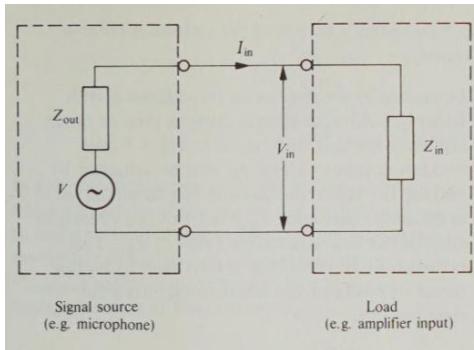
- Uses CMOS Switches to toggle between the desired states.
- Has leakage current. Leakage current varies by scenario, whether the CMOS MUX switch is ON or OFF.
- The higher the source impedance, the higher the offset caused by the leakage. To combat this, either decrease source resistance or leakage.
- $V_{LSB} = V_s / 2^{18}$
- $\text{OffsetError}[\text{Bits}/\text{codes}] = \text{OffsetError}[V]/V_{LSB}$
- Has charge injection. Charge injection caused by capacitance in the switching channels

Harmonics:

- Any repetitive waveform can be synthesized from sine waves at integral multiples of the original frequency, i.e. at various harmonics/frequencies, by Fourier analysis.
- First harmonic is the fundamental frequency. 2,3,...,n harmonics determine the amplitude and phase of the repeating complex waveform.
- When linear distortion arises, the amp is adding harmonics to original.
- The sine wave is unique because it contains only one frequency.
- Harmonic distortion measurement measures harmonics on the fundamental, by rejecting the fundamental.
- A wave analyzer uses a tunable narrow band filter picks out the individual frequencies/harmonics from noise to investigate harmonic distortion.

Impedance Matching (see noise for complementary info):

- Impedance matching is crucial in electronic circuits to ensure maximum power transfer and minimize signal reflection.
- Ensuring that maximum (or full) transfer of voltage signal occurs.
 - o Amplifiers, oscilloscopes, measure and amplify voltage!
- Thevenin's theorems state that any network of power generator and impedances between two output terminals is equivalent to a 1 voltage generator and 1 impedance in series.
- One can obtain the source impedance of a voltage generator by measuring the short circuit (can use a shunt resistor) current and open loop voltage. Subtracting the voltage generators voltage by the open loop voltage, and then dividing by the current yields the source output resistance (generally constant @ frequencies).
- For optimum voltage transfer, the source impedance should be minimized as much as possible with respect to the load impedance; i.e. the output impedance should be minimized w.r.t. the input impedance.



$$V_{in} = \frac{VZ_{in}}{Z_{out} + Z_{in}}$$

and $V_{in} \approx V$ if $Z_{in} \gg Z_{out}$.

- A good rule of thumb is $Z_{in} > 10 Z_{out}$.
 - o This is why sig. gen. have such low output impedance (< 100 ohm) and oscilloscopes have higher output impedances (1 Mohm).
 - o Think about every voltage signal as a voltage generator and a coupled resistance coming with it (wire), by **Thevenin's**. As to more understand why scopes are high resistance, one must think of every voltage signal as a generator with its own output impedance, otherwise other output impedances from various node interconnects will dilute a specific voltage node. Like if you want to read the voltage from the second note from a real voltage generator, one must make the 1st note and beyond equivalent to the voltage generator for the second note, otherwise, the output impedance of the first node will make irrelevant the effect of the second node to the source (input) impedance.
- For maximum power transfer from source to load, if $R_{in} = R_{out}$, this occurs. If reactive elements are present, it must be such that the reactive components' impedances cancel out to have maximum power transfer, i.e., just resistive impedances.
- The load impedance (input impedance) is matched with the characteristic impedance (source/output), such as with transmission lines, to eliminate reflections.

- It's strange how to provide maximum current transfer, the voltage transfer is minimized by decreasing output impedance the most (if input impedance fixed).
- If the input impedance is not high enough with respect to the output resistance such that voltage signal is loss/dissipated, by varying load impedances within the output impedance range, we will get varying voltage signals to the load. To obtain constant load voltage signals, to simulate a input/output impedance that is \gg , use an emitter follower. Case: Voltage transfer bad, noise figure good.
- A step transformer can be used to increase source impedance so that the optimum noise figure can be achieved. Case: Voltage transfer good, noise figure bad.

Transformers:

- Size is inversely proportional to frequency due to more change in current producing more transformed power per time unit. This means at a higher frequency, the same power can be transferred at a smaller size. Quite large.
 - o [Transformer size vs. frequency - Electrical Engineering Stack Exchange](#)
- Just a pair of coiled wires of different loop amounts.
- The inductances of the windings are infinite for 100% efficiency.
- Can be used for a.c. voltage scaling or impedance conversion.
- IDEAL Principles:
 - o $V_{out} = nV_{in}$; where $n = N_2/N_1$.
 - o Negligible power loss implies inversely proportional current to voltage scaling.
 - o Current reverses in direction (following schematic arrangement).
 - o Magnetic flux caused by secondary and primary current are equal and opposite \Rightarrow net flux = 0. No inductance produced by secondary current.
 - o No flux leakage
 - o The primary has a *reflected impedance* caused by n and the load resistance from the secondary. Can be derived from ohm's law and equivalent power.

$$R_{in} = \frac{R_L}{n^2}$$

- o
- The inductor performs an impedance changing function in converting high signal-low current to low signal-high current.
- [Transformer-Application-Note-Pt-2.pdf](#)

CFB vs VFB Op-Amps:

- Parallel capacitance for op amps.

Linear Systems:

- Superposition Principle that if $a = b + c$, for a signal, $f(a) = f(b) + f(c)$ for independent events/signals b, c .
 - o Property of linear circuits.

- As a result, DC voltage sources can be considered ground when considering ac signals, by superposition.

Closed-Loop:

- Describes a system that continuously compares the desired state with the actual, outputted state; and adjusts the systems output to minimize the difference between the two for precise control.
 - closed loop servo operating mode

Control Systems (basics):

PoleZero.dvi

- The transfer function provides a basis of the system response characteristics for an input without solving D.E. that represents the system.
 - Poles and zeros define system response.
 - Exists in the complex variable space, $s = \sigma + j\omega$, where ω is the frequency of input; rational function, where two polynomial functions exist, numerator and denominator.
- The polynomials factored, produce
$$H(s) = \frac{N(s)}{D(s)} = K \frac{(s - z_1)(s - z_2) \dots (s - z_{m-1})(s - z_m)}{(s - p_1)(s - p_2) \dots (s - p_{n-1})(s - p_n)},$$
- The characteristic equation is actually the [denominator polynomial] = 0 function.
- For $N(s) = 0$, s are called the zeros; for $D(s) = 0$, s are called the poles.
- All of the coefficients of polynomials $N(s)$ and $D(s)$ are real, therefore the poles and zeros must be either purely real, or appear in complex conjugate pairs.
- The system poles define the components in the homogenous response.
- The unforced response of a linear SISO (single input single output) system to a set of initial

$$y_h(t) = \sum_{i=1}^n C_i e^{\lambda_i t}$$

conditions is:

- C_i from initial conditions
- Eigenvalues are the roots of the characteristic equation, the [characteristic function] = 0 is actually $D(s)$.
- Thus, *the transfer function poles are the roots of the characteristic equation, and also the eigenvalues of the system A matrix.*
- The response of a system is defined by the response of the n components of the system.

$$\frac{d^2y}{dt^2} + 2\zeta\omega_n \frac{dy}{dt} + \omega_n^2 y = 0,$$

- An overdamped system has real poles in the left-half plane, where: $p_1, p_2 = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$.
- An underdamped system has complex conjugate pair poles in the left-half plane, where the poles $0 \leq \zeta < 1$.

- ζ is the damping ratio $p_1, p_2 = -\zeta\omega_n \pm j\omega_n\sqrt{1 - \zeta^2}$

Stability Criterions (Measuring the stability of feedback):

- The loop gain of a closed loop feedback system is the product of the open-loop gain and feedback system, with the sign of the type of feedback. It represents like the total gain of the feedback system and used as a stability factor for analysis.
- A loop gain of 0 dB, i.e. 1x, means the input and output signal magnitudes are equal.



Loop gain is not GH . Loop gain is $-GH$.

- Phase shift represents the time difference between the output relative to the input in phase [degrees]; since it is the difference between output – input, **phase shift < 0**.
 - o A -180 phase shift means the output, and feedback signal, is exactly out of phase with the input.
 - o Hence positive, oscillatory feedback, that amplifies error, rather than negative feedback to stabilize.
- Gain crossover frequency: The frequency at which the gain of the open loop response of a control system is 0 dB.
- Phase crossover frequency: The frequency at which the phase of the open loop response of a control system reaches -180 degrees.
- Phase Margin: The phase difference of the closed loop, loop-gain response, at the GCF (openloop), to – 180.
 - o A positive phase margin means the system is stable, while a negative phase margin means it's unstable. The larger the positive phase margin, the more stable the system is.
$$\angle LG(j\omega_{GCF}) + 180^\circ$$
- Gain Margin: The gain (dB) of the closed loop, loop-gain response, at the PCF (openloop).
 - o A positive gain margin indicates stability, while a negative gain margin suggests that the system is unstable. Larger gain margins imply greater stability.
 - o $0 \text{ dB} - 20 \log_{10} (|LG(j\omega_{PCF})|)$ Convert gain to dB, hence logarithm.

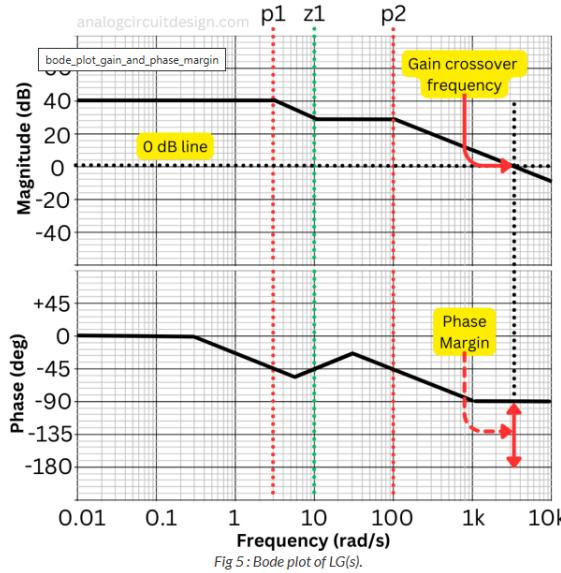


Fig 5 : Bode plot of $LG(s)$.

- Gain margin is $-90 - (-180) = 90$. Phase margin is $0 - \log(0) = \infty$.
- [Basics of Phase margin and Gain margin in Control Systems](#)

Homogenous (Natural) / Force Response:

- The homogenous response is the response of the system solely due to the initial conditions of the system, i.e. the input to the system is 0.
- The forced response is the response of the system to some input that is applied and is not an initial condition, i.e., may not be inherently present.
- Zero state and zero input.
- [analog - Why is a capacitor to ground a low frequency pole, instead of a high frequency zero? - Electrical Engineering Stack Exchange](#)

Pole-Zero Plot:

- The s-space, a complex space, has complex poles and zeros; complex s-plane.
 - o For $s_i \Rightarrow$ zeros, usually holes. For $s_i \Rightarrow$ poles, usually crosses.

Geometric Evaluation of Transfer Function:

- $H(s)$, the transfer function, can be evaluated for any complex value s_i . if s_i is complex, so is $H(s_i)$ (result).

$$|H(s)| = \sqrt{\Re\{H(s)\}^2 + \Im\{H(s)\}^2},$$

$$H(s) = |H(s)| e^{j\phi(s)} \quad \phi(s) = \tan^{-1} \left(\frac{\Im\{H(s)\}}{\Re\{H(s)\}} \right) \quad H(s) = K \frac{(s - z_1)(s - z_2) \dots (s - z_{m-1})(s - z_m)}{(s - p_1)(s - p_2) \dots (s - p_{n-1})(s - p_n)}$$

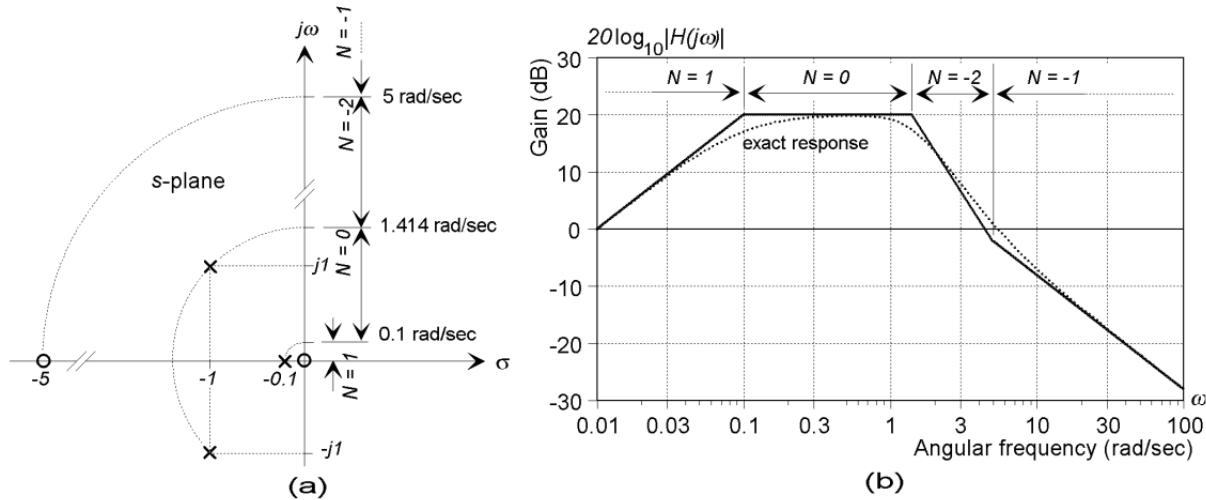
$$|H(s)| = K \frac{\prod_{i=1}^m |(s - z_i)|}{\prod_{i=1}^n |(s - p_i)|} \quad |H(s)| = K \frac{r_1 \dots r_m}{q_1 \dots q_n}$$

$$\angle H(s) = \sum_{i=1}^m \angle(s - z_i) - \sum_{i=1}^n \angle(s - p_i). \quad \angle H(s) = (\phi_1 + \dots + \phi_m) - (\theta_1 + \dots + \theta_n)$$

- The transfer function at any value of s may therefore be determined geometrically from the pole-zero plot, except for the overall "gain" factor K .

Frequency response (Bode Plot)

- Let $s = j\omega$ into $H(s)$ by above geometric evaluation. This gives the frequency response.
- $$|H(j\omega)| = K \frac{r_1 \cdots r_m}{q_1 \cdots q_n}$$
- $$\angle H(j\omega) = (\phi_1 + \dots + \phi_m) - (\theta_1 + \dots + \theta_n)$$
- One can draw the bode plot by varying ω , the frequency, and seeing how the magnitude and phase of the system changes, by Pythagorean theorem. See more details in link.
- The pole-zero plot of a system contains sufficient information to define the frequency response except for an arbitrary gain constant.
- Break frequencies: $\omega_b = \sqrt{\sigma^2 + \omega^2}$. On bode plot estimation, they are the piecewise termination points.
- $+20 \text{ dB}/\text{decade}$ at break frequencies.
- If there are Z breakpoints due to zeros to the left, and P breakpoints due to poles, the slope of the curve at that frequency is $20 \times (Z - P) \text{ dB}/\text{decade}$.
- Because all low frequency asymptotes are horizontal lines with a gain of 0dB, a pole or zero does not contribute to the magnitude Bode plot below its break frequency.



- Read the article.

Pole Location and Homogenous Response:

$$y_h(t) = \sum_{i=1}^n C_i e^{p_i t}.$$

- Homo. Response.

- negative implies on the left side, positive right side, of s-plane.-

1. A real, negative pole defines an exponentially decaying component.
2. A pole at the origin defines a component defined by the initial conditions; constant.
3. A real, positive pole defines an exponentially increasing component; unstable.
4. A negative, complex conjugate poles, $-\sigma \pm j\omega$, defines a component with a response that is a decaying sinusoid.

5. A positive, complex conjugate poles, $-\sigma \pm j\omega$, defines a component with exponential increase.
6. An imaginary pole pair $\pm j\omega$ generates an oscillatory component, with amplitude by initial conditions.
 - a. A system with ≥ 1 pole on the imaginary axis, without any on the right side of s-plane is defined to be **marginally stable**.
- The homogenous response is important here since it is the natural response with no input condition considered.
- In order for a linear system to be stable, all of its poles must have negative real parts, that is they must all lie within the left-half of the s-plane
 - o An nth order linear system's response is the **summation** of the n components' response.

Drive:

- A motor is a machine converting electrical energy to mechanical energy, v.v..
- A *drive* is something used to control the speed of an operating component/machine.
 - o Assembly line, fluid control
 - o A motor drive controls the speed of a motor.
- A variable frequency drive (VFD) is the system that controls that can control variably the speed of a machine.
 - o Speed adjustable, usually in discrete steps over a range.
 - o Variable: continuous speed adjustment.
- A VFD can be the PWM control for a motor. VFDs incur abrupt voltage transitions (slew rates), with high switching speed and low switching losses desired.
 - o High speed switching, dv/dt & di/dt , emit input stage and output stage, radiated and conducted EMI
- origin of noise from VFD operation is high dv/dt pulse-width modulated (PWM) output voltage which drive the motor, and couple through stray capacitance.
- surfa
- [Motor drive - Wikipedia](#)

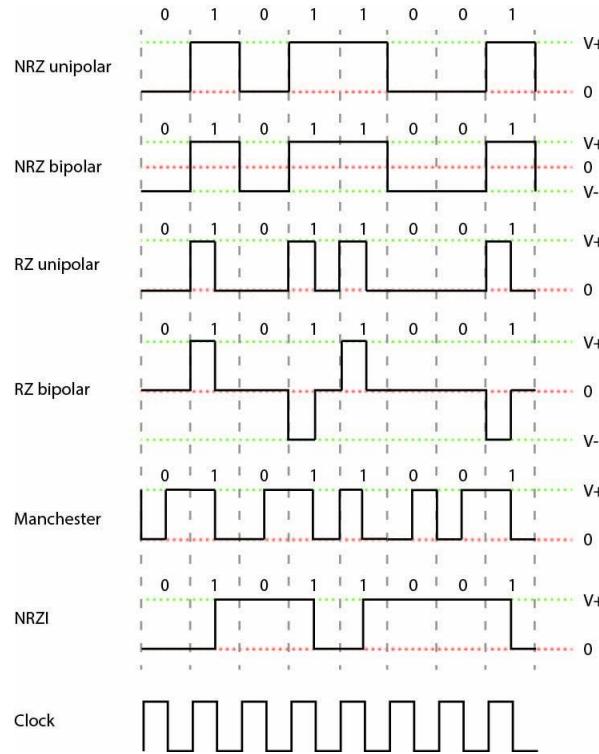
Connectors:

- Derating of connectors: Wurth derating of connectors [derating-of-connectors.pdf](#)
- Wafer connectors and xyz motion connectors.

Data Transfer:

- A "word" refers to a fixed-sized unit of data that a processor can handle or transfer at one time.

Encoding Techniques:



USB:

- [USB 101: An Introduction to Universal Serial Bus 2.0](#)
- [Microsoft Word - ANP024c EN The USB interface from EMC point of view](#)
- Bit stuffing for PLL offset.
- 48 MHz, 3V3, Full speed or High speed, Differential signaling, Pull up and pull down resistors for selecting modes on D+ or D- or to signal the start. ESD protection since USB is for hot plugging.
- The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.
- <https://electronics.stackexchange.com/questions/134684/why-use-stm32-hse>
- [USB On-the-Go Basics | Analog Devices](#)
- More depth: [AN65231 - USB On-The-Go \(OTG\) Basics](#) unclear now.

SPI (Serial Peripheral Interface):

- Push-pull configuration (CMOS) switching topology.
 - o Faster data transmission and better signal integrity compared to open-drain or open-collector configurations due to actively driven high and low states. Implies faster rise and fall times, by active driving.
 - o SPI communication is generally used when high-speed data transfer is required.
- The Idle State: period when CSB is high and transitioning to low at the start of transmission, and when CSB is low and transitioning to high at the end of transmission.
- The state when a master-slave pair is waiting a new instruction to be initiated by the next falling edge of the CSB line.
- SPI words can be of variable length. SPI slave supports 8-bit and 32-bit data granularity.

- Frame sizes: 8 (byte), 16 (half-word), or 32 bits (word).
- Consists of 3-4 pins: SCLK, SDIO, CSB (3-Wire, half duplex); SCLK, SDI, SDO, CSB (4-Wire, full duplex).
- SCLK implemented with a Schmitt trigger for best signal; pulled low by a 50 kOhm resistor to GND.
 - The maximum clock speed of the ADC SPI port is 25 MHz : 3.125 Megabytes/s
 - Synchronizes serial **reads** (OUTPUTS from Master) and **writes** (INPUTS to Master).
 - Input data (Writes) registered on rising edge. Output data (reads) registered on falling edge.
- The bus can turn around the state of the SDIO line in half an SCLK cycle
 - Implies the SDIO line can transition from output to input and v.v. within one half of a clock cycle. Therefore, at the next falling or rising edge, which is now used to read data from, can have data safely placed and read on the line.
 - If external controller cannot keep up with SPI CLK line, the external can stall the CLK line for additional time.
- CSB, an active low control, that gates read and write cycles; a high impedance line, pulled high by 50 kOhm resistor.
- CSB is tied low for a singular external device, implying SCLK and SDIO lines processed for selected device.
 - If pulled high, implies SPI function of device are in high impedance mode, device ignores info from SPI lines.
- If the CSB pin is tied high, the chip may allow control of other features on-chip which do not require SPI and otherwise could not operate if SPI was pulled low and on.
 - Output data format, duty cycle stabilizer
- CSB may stall high for multiple clock cycles to allow for additional timing for external device.
 - *If three or fewer words (not counting instruction information) are being transmitted through the interface at a time, CSB may stall high between bytes, including the bytes of the instruction information*
 - If, at any time, CSB stalls high in the middle of a byte, the state machine is reset and controller returns to idle, awaiting transmission of a new instruction. Fault detection Use.
 - Detected by serial clocks.

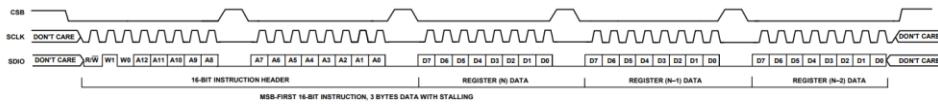


Figure 5. Most Significant Bit (MSB)-First Instruction and Data with Stalling

- Higher throughput than I²C, not limited to CLK speed.
- Simple hardware interfacing
- Without the SPI pins, one may use a switch or serial to parallel converter as in intermediary control to transmit the control signals from the GPIO of a uC to the a receiving SPI device.
 - The GPIOs of the uC are the control signal
 - This uses an extra switching or deserialization unit with 4xN lines.
 - With the SPI pins, an additional component is not needed for the SPI control lines and only extra CSB lines are required, slaves can share SDI/O and CLK.

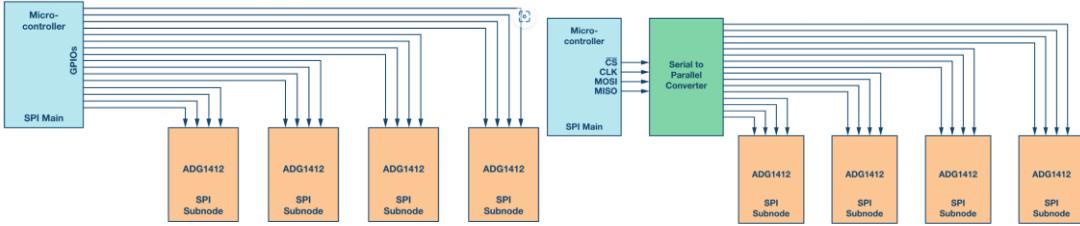


Figure 11. Multi-subnode switches using a serial-to-parallel converter.

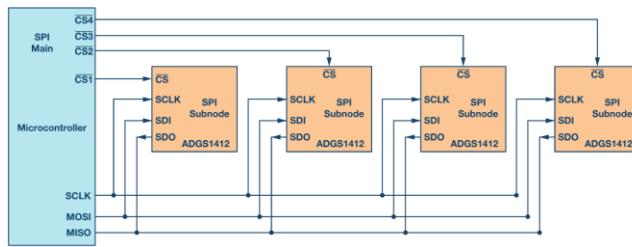


Figure 12. SPI enabled switches save up microcontroller GPIOs.

- One can daisy chain the SDO pin to save lines, but it may or may not be supported.
 - o Optimize the GPIO count with only 4 lines!
 - Uses 1 CSB line for everything, and one [through-all] SDO line.

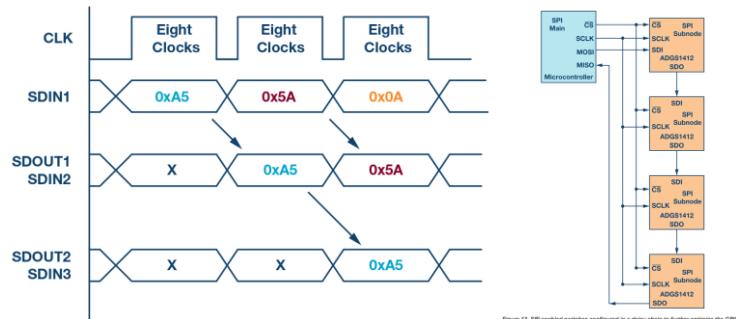


Figure 13. SPI enabled switches configured in a daisy chain to further optimize the GPIOs.

- Board space saving and simplicity is significant.
- External p.u.s and p.d.s may be needed. RTFDS.

Clock Polarity and Clock Phase Bits:

- CPOL bit sets the polarity of the clock signal during the idle state, and, hence transmitting state.
- CPHA bit sets the clock phase at which edge the data is sampled (received) and/or shifted (transmitted).

SPI Mode	CPOL	CPHA	Clock Polarity in Idle State	Clock Phase Used to Sample and/or Shift the Data
0	0	0	Logic low	Data sampled on rising edge and shifted out on the falling edge
1	0	1	Logic low	Data sampled on the falling edge and shifted out on the rising edge
2	1	0	Logic high	Data sampled on the falling edge and shifted out on the rising edge
3	1	1	Logic high	Data sampled on the rising edge and shifted out on the falling edge

- [AN-877 \(Rev. B\)](#)
- [Introduction to SPI Interface | Analog Devices](#)

Quad SPI:

- Half-duplex communication with $n = 4$ lines of communication in total; 2 MOSI, 2 MISO.
- [What are the Differences of Single vs Dual vs Quad SPI? - Total Phase](#)

I²C:

- Two-wire half duplex serial communication protocol supporting multiple targets and controllers on a bus.
 - o SDA and SCLK line.
 - o Generally lower speed communications.
 - Bus capacitance and Drive capability affect data rates
 - Stronger drivers for faster rise and fall times, high speed data controllers (Hi), write-only operation (UF).

I ² C Mode	Maximum Bit Rate
Standard-mode	100kbps
Fast-mode	400kbps
Fast-mode Plus	1Mbps
High-speed mode	3.4Mbps
Ultra-Fast mode	5Mbps

- Communication sent in byte packages to target address device.
- Requires the use of pull up resistors for its open drain switching topology.
 - o NMOS transistor

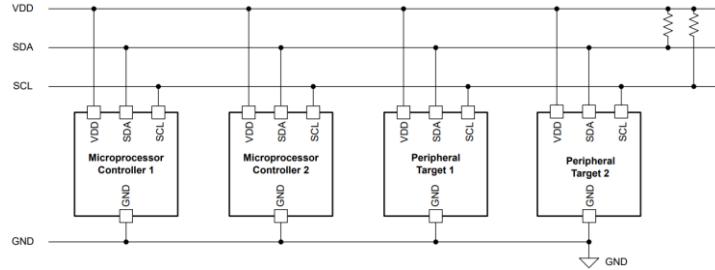


Figure 2-1. Typical I²C Implementation

- The transition from high to low is fast as it is actively driven by the NMOS. Speed determined by NMOS drive strength and bus capacitance.
- The transition from low to high is slower due to bus capacitance.
- The RC networks results in exponential capacitive settling time and lower transition speeds.
- Correctly sized pullup resistors provide a rise time fast enough for good noise immunity along with acceptable power consumption.
- A smaller pullup resistor has a faster rise time, but more power dissipation. A larger pullup resistor has a slower rise time, but less power dissipation.
 - o Due to increased current caused by decreased resistance and constant supply voltage, power increases.
- Bus contention does not put the bus into a destructive state in an open drain configuration
 - o if any output pulls the line low, the line is low. No shorts due to P.U. resistors.
 - o Wired-AND connection. Bus signal is the logical AND of all output signals.
 - o With Push pull config, the bus signal will be intermediate of the supply and GND when an output is on + off, due to resistance-voltage drop.
 - W/ pushpull, low impedance of NMOS and PMOS when an output is HI and another LO can yield significant current -> damage.

Procedure:

- I2C start condition: SDA -> LOW then SCL -> LOW => controller claiming I2C bus.
- I2C stop condition: SCL -> HIGH then SDA -> HIGH => releases bus and implies bus can be claimed

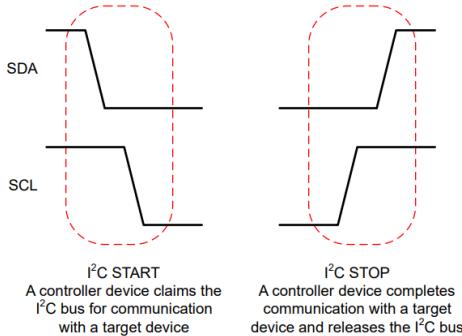


Figure 3-1. I²C START and STOP

- 1, 0s for serial communication. SCL times bit sequence for SDA data bits.

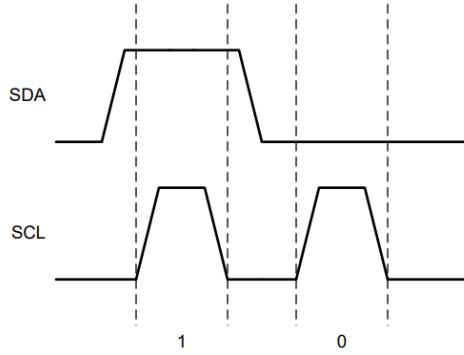


Figure 3-2. I²C Digital One and Zero Representations

- The ones and zeros are received when SCL is pulsed. For a valid bit, SDA does not change between a rising edge and the falling edge of SCK for that bit. **Changes of the SDA between the rising and falling edges of the SCL can be interpreted as a START or STOP condition on the I²C bus.** Notice the ridge orders.
- I2C frames:
 1. Controller STARTs
 2. Controller sends I2C 7-bit target address ($\Rightarrow 2^7$ unique addresses), R/NOT W bit + 9th ACK bit.
 - a. Read implies read data from target; Write implies write data to target.
 - b. Target device sends ACK bit, p.d. to verify communication.
 - 9th bit ACK verifies each byte of data sent in I2C.
 - For ACK, device pulls down - LOW - SDA during a SCL pulse to indicate successful data transmission, otherwise NACK, if HIGH.
 - For the data frames, each byte is preceded by an **ACK/NACK sent/pull downed by the device that the data is going towards.**
 - o E.g. WRITE implies target sends ACK; READ implies controller pulls down.
 - 3. N 1 byte data frames are sent, each with a preceding ACK bit.
 - 4. Controller STOPS
 - The ACK is a useful debugging tool.
 - Assumption: a NACK bit only throws error if programmed to, otherwise it is default ignored. Up to user debugging or program catch and response.

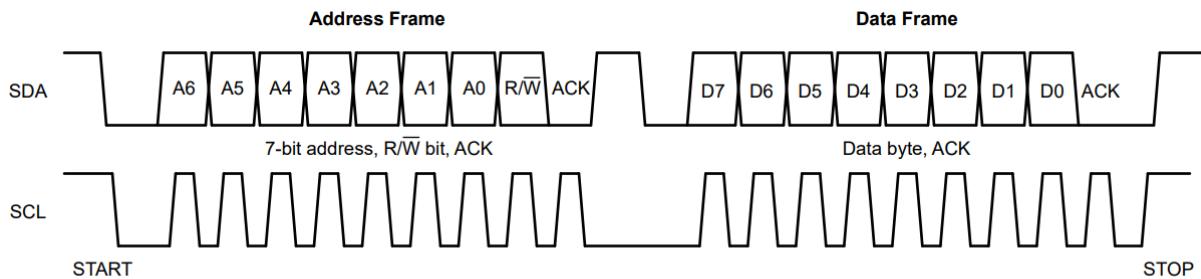


Figure 3-3. I²C Address and Data Frames

-
- [A Basic Guide to I²C](#)

SFP:

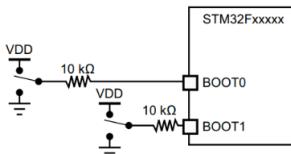
- A hot swappable transceiver with fast data and reliable signal transmission that uses photoelectric conversion.
 - o Small Form-Factor Pluggable
- Parts of the optical module:
 - o Housing: mini metal/plastic housing protecting the internals and provides the correct insertion size/interface into the network device
 - o Optical fibre interface/connector: connects the optical fibre transmission media to the module; lc/sc connector types.
 - [LC vs SC Connectors: Which to Choose? – VCELINK](#)
 - o Electrical interface: Allows electrical signal transmission by connecting the optical module and to whatever network/media. Generally, metal pins/sockets.
 - o Optical Transceiver: CORE PART of the module. Has photoelectric converters, converting optical signals into decoded electrical signals, and electro-optical converters, converting electrical signals into optical signal for transmission through fibre.
 - o EEPROM: chip to store ID info, performance info, and config data of the module, allowing devices to read and identify module's data.
- SFP: uses LC connector, smaller, 1.25 Gbps, shorter distance
- SFP+: same form-factor as SFP, with lower power consumption, higher data rate of 10 Gbps.
- SFP28: upgraded version of SFP+, 25 Gbps higher data rates and lower power consumption.
- Various specs: data rate (Gbps), wavelength (of optical signals) [nm], max transmission distance, fibre type ([Multi-mode fiber MMF or single-mode fiber SMF](#)), connector interface ([SC or LC](#)), compatible devices.
- [What Is Sfp Transceiver: Everything You Need To Know](#)

STM32:

- A microcontroller has one CPU that manages all the operations, including controlling the GPIO ports.
- CPU uses multiplexing to manage multiple ports and pins, allowing it to handle various tasks simultaneously.
- BOOT0:
 - o When STM32 is powered up (and RST released OFF), bootloader checks if flash is blank. If so, bootloader will enable (HIGH) and listen for peripherals (UART/I2C/SPI/USB) to flash the device.
 - If flash not blank, code in flash will start.
 - o If BOOT0 tied high, bootloader will assume flash is blank; always rewrite memory.
 - o Flashing uC can also be done via debugger (ST Link) through SWD/JTAG.
 - o *On STM8 MCU due to low pincount, the bootloader does not have a boot0 pin and instead the bootloader will be listening for communication for a single second after reset line is released.*
 - [Solved: Hi what is boot0 in stm32 - STMicroelectronics Community](#)
- Boot 0/1 Pins [STM32 Boot Modes | STM32 Boot0 Boot1 Pins](#)

Boot modes

Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space



- Pulled high/low using 10 kOhm.

DMA Controller:

- A hardware component that manages the transfer of data between the computer's memory and other peripherals without involving the CPU.

PWM:

- Pulse Width: The duration of the HIGH state of a pulsed signal.
- Duty Cycle: The ratio of the HIGH signal in a period of the signal waveform

Ports:

- A port represents all the pins of a certain associated register(s).
- N-bit architecture MCU implies ports and registers of N-bits. Usually 8, 16, 32 bits.
- Each pin corresponds to a bit in the register.
- Registers are a component of memory (RAM?). A port(s)'s register (pin memory) may be in the same memory as the processor (RAM). This implies the memory addresses for the pins are reserved and instructions on the RAM can work with the I/O memory/registers.
- [Pin and port in microcontroller - Electrical Engineering Stack Exchange](#)

Bit-Banging:

- A method of digital data transmission using general-purpose input/output (GPIO) instead of computer hardware intended specifically for data communication (e.g., UART, SPI, I²C).
- Tends to increase the runtime load on the controlling system – software and its host processor opposed to hardware protocols.
- Allows limited or no hardware changes and therefore can be a lower cost since changing software is typically less expensive than changing hardware.

Digital Signal Processing:

- Anti-aliasing: technique used to minimize distortion artifacts (aliasing), which are signal components at a too high frequency to be read, when converting a high-resolution image to a lower resolution.
 - o Essentially a blur/filter between adjacent pixels to achieve a lower resolution/frequency with minimized distortion.

ADC:

- Every additional 6.02 dB of noise floor corresponds to a 1-bit reduction of the effective number of bits of an analog-to-digital converter or digital-to-analog converter.
- An anti-aliasing filter for an ADC has a stop band frequency of the Nyquist frequency (1/2 sampling rate).
- Based on my knowledge

Data Rate Terminology:

- Baud: (named after Emile Baudot) One *symbol* per second. Where a symbol can be any n bits.
- Data rate is the theoretical maximum speed at which data can be transmitted over a communication channel, while throughput is the actual amount of data successfully transferred over that same channel in a given time.

Sensor:

FSI/BSI:

- [Back illuminated vs. front illuminated CCD-based imaging sensors and how it impacts Raman spectra](#)

Questions:

- How come on the block diagram, only PWR B is connected to the PLL Clock Generator, but in the schematic we have 3.3V and 1.8V
- Decoupling capacitors: How come there are so many capacitors of repeating values. I heard that the rule of thumb of capacitors differing by a factor of 10, is this true?
- Do you want me to use the same components

Need to answer if a higher storing Q capacitor is HP or LP filter. HF passing filter stores low f

Page 17 seems useful in selecting a deoculing cap.

Oscilloscope probing Notes:

- after a Schottky diode (U68 D32), voltage increased by 0.05 V, freq increased by 62 MHz, The prior voltage signal looked like a square waved with a parabola inside, the output voltage signal is more dc but with periodic voltage spikes.

Inductor took voltage signal and the output voltage -> to input voltage frequency is 105 MHz to 2 MHz. It also made the signal more equal where the voltage signal resided in a smaller peak to peak voltage from 230 mV to 130 mV. Average voltage stayed approximately equal.

Learn transistors common terminal configurations and leakage current.

Learn eeprom nand and sfp

To Learn:

- Watch
 - o Resonant frequency of LC circuits
 - o Cm chokes vs. ferrite beads
- Back to EMI filter
- forward feed capacitors
- Modern Computer Architecture and Organization: Learn x86, ARM, and RISC-V architectures and the design of smartphones, PCs, and cloud servers
- Finish impedance matching
- Learn layout and schematic design for real and how it actually interacts and works not just random stuff.
- LEARN PADS - > MAYBE START MY OWN DESIGN.
 - o Learn feed forward caps and filtering amplifiers (TI). Learn TI, read. EMI filter stuff.

Test sensors at high temperatures.

Write:

- Phase noise and the PLL
- Reading schematics
- Decoupling caps before not directly before load.

Internal vs external grounds, ground bounce, SPI, PLL, phase noise

Nyquist, root locus, TI precision labs, my book ...

I2C, then browse around my existing tabs and start learning digital circuits. Then learn some other stuff, CMOS Switch note, etc..

[Balance Resistors for Series Capacitors | VA1DER](#)

[Ferrite Filters: Types, Characteristics, and Applications | Advanced PCB Design Blog | Cadence](#)

[Film Capacitor | Capacitor Types | Capacitor Guide](#)

[Leakage Inductance: An Introduction | Advanced PCB Design Blog | Cadence](#)

[Skin effect - Wikipedia](#)

[Proximity effect \(electromagnetism\) - Wikipedia](#)

[the engineers practical guide to emi filters - web.pdf](#)

[Fractional/Integer-N PLL Basics](#)

[What is SerDes \(Serializer/Deserializer\)? – Why it's Important | Synopsys](#)

[Application Manual for Power Supply Noise Suppression and Decoupling for Digital ICs](#)

[automotive-electronics-clock-tree-design-consideration.pdf](#)

Impedance matching

[Decoupling Capacitor Calculations: What Size Should You Use For Digital ICs? | Altium Designer](#)

[transistors - How to calculate the quiescent current of a common emitter amplifier - Electrical Engineering Stack Exchange](#)

[How to Terminate LVDS Connections with DC and AC Coupling](#)

Loadline

[App Note - Output Voltage Trim by digital analog converter V2 Final](#) trimming resistors