CMOS IC Application Note

STEP-DOWN SWITCHING REGULATOR NOISE COUNTERMEASURES

Rev.2.0_00

This application note is a reference which explains board layouts for minimizing noise generated from step-down switching regulators (built-in FET type).
Refer to each product datasheet for details and specs.

Contents

1. How Noise is Generated

A magnetic field is formed as current passes through a conductor. According to the law of electromagnetic induction, an electric field is generated as the magnetic field changes over time. And as current changes over time, the magnetic field and electric field also change causing the generation of an electromagnetic field. This electromagnetic field is a so-called radio wave that may adversely impact electronic devices in the vicinity. This unwanted radio wave is noise.

1. 1 Noise generated by inductor (L)

In the following, we will describe the noise caused by L from the current and voltage aspect.

Figure 1 shows a circuit where L is connected to a current source (I). As shown in **Figure 2**, when a current change $(\frac{di}{dt})$ occurs in I, noise is generated in L.

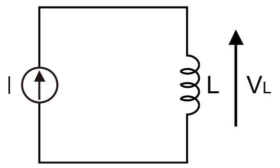


Figure 1

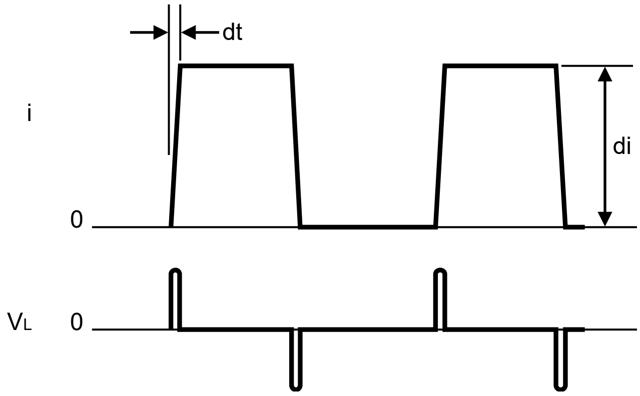


Figure 2

Figure 3 shows a circuit where a series circuit of L and a capacitor (C) is connected to a voltage source (V). As shown in **Figure 4,** when a voltage change $(\frac{dv}{dt})$ occurs in V, LC resonance occurs and noise is generated in L. Noise that oscillates in response to step-wise changes in voltage as indicated by V_L in **Figure 4** is called ringing.

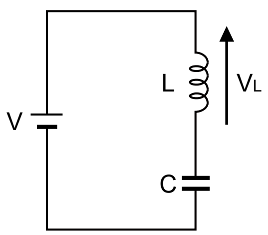


Figure 3

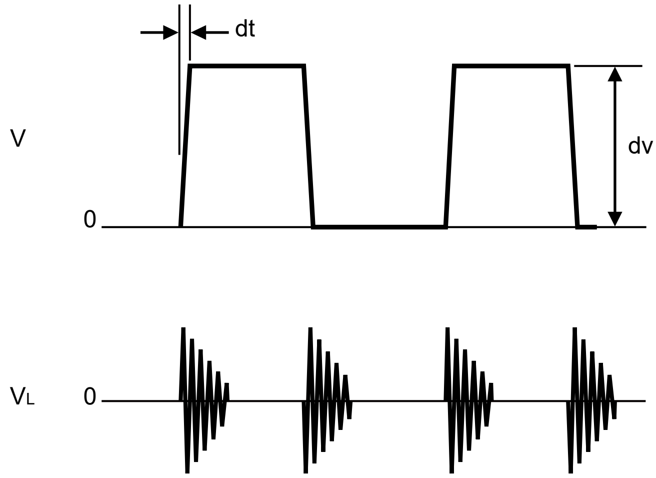


Figure 4

When current or voltage changes occur as shown, noise is generated in L. This is unwanted noise.

1. 2 Switching power supply noise

A switching power supply uses a switching element to constantly turn the power ON and OFF to supply the desired power to the output. For this reason, it can be assumed that switching power supply noise is caused when switching current flows through the board pattern and other areas where there is parasitic inductance.

In an actual switching regulator circuit, the L in **Figure 1** and **Figure 3** is the parasitic inductance of the board pattern and IC interior, and C in **Figure 3** is the parasitic capacitance of the switching element, the power MOS FET.

2. Parasitic Inductance and Noise Countermeasures in Current Path During Switching Operation

Figure 5 shows the current path when the high side power MOS FET (M_1) is ON. L_{p1}, L_{p4}, L_{p6} and L_{p7} indicate the parasitic inductance of the board and L_{p2}, L_{p3}, L_{p5} indicate the parasitic inductance inside the IC.

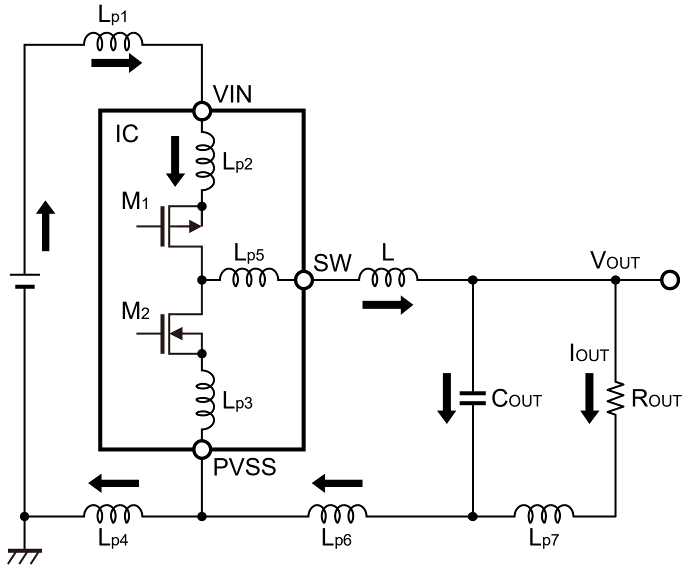


Figure 5

Figure 6 indicates the current path when the low side power MOS FET (M_2) is ON.

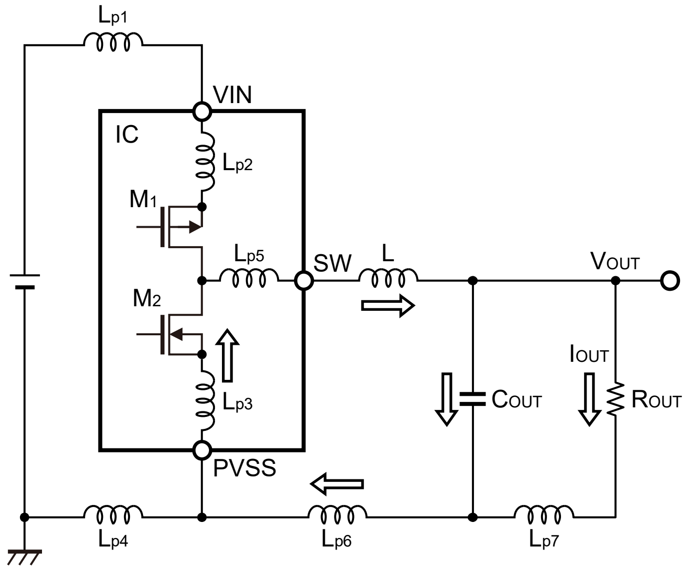


Figure 6

2. 1 Current path of continuous (steady-state) current

Continuous (steady-state) current like in **Figure 7** flows through the SW pin, inductor (L), output capacitor (C_{OUT}), load resistor (R_{OUT}) and parasitic inductance (L_{p5} to L_{p7}) in **Figure 5** and **Figure 6**.

A current change ($\frac{di}{dt}$) is small in paths where continuous (steady-state) current flows and the risk of serious noise in L_{p5} to L_{p7} is low.

Figure 7

2. 2 Current path of intermittent current

Current flows intermittently in L_{p1} to L_{p4} in **Figure 5** and **Figure 6**.

Figure 8 shows the waveform of current flowing through M_1 and M_2 during switching operation. The current flowing through L_{p1} to L_{p4} is identical to the current flowing through M_1 and M_2 and is therefore pulsating current. The pulsating current flowing through L_{p1} to L_{p4} causes large noise (V_{NOISE}).

Use the following equation to calculate V_{NOISE}.

$$V_{NOISE} = L_p \times \frac{di}{dt}$$

For example, assuming that $L_p = L_{p1} + L_{p2} + L_{p3} + L_{p4} = 10$ nH and the current change $(\frac{di}{dt}) = 1$ A/2 ns in t1 and t2 in **Figure 8**, noise as large as 10 nH $\times$ 1 A/2 ns = 5 V is generated. As a result, noise overlaps the rectangular wave SW pin voltage as shown in **Figure 9**. Parasitic inductance must be minimized to reduce such noise.

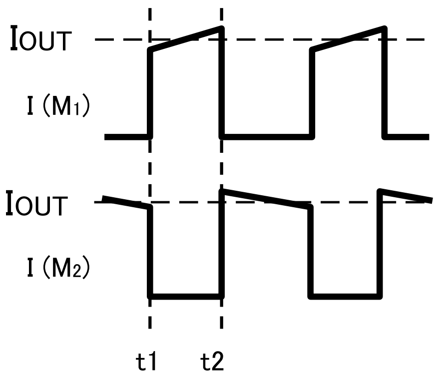


Figure 8

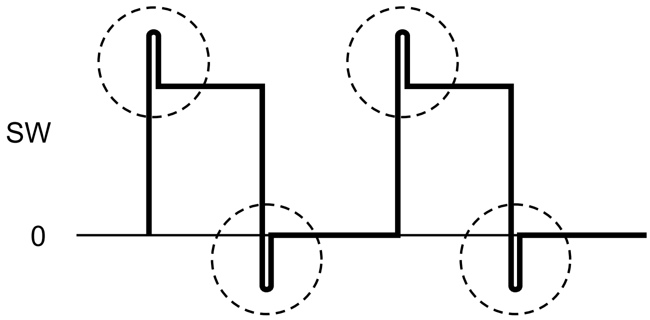


Figure 9

3. Ringing

3. 1 Cause of ringing in SW pin

As the switching regulator repeatedly turns M_1 and M_2 ON and OFF alternately, parasitic inductance and parasitic capacitance cause LC resonance generating ringing in the SW pin.

Figure 10 shows the parasitic capacitance (C_{p1}, C_{p2}) and parasitic inductance (L_{p1} to L_{p7}) in M_1 and M_2.

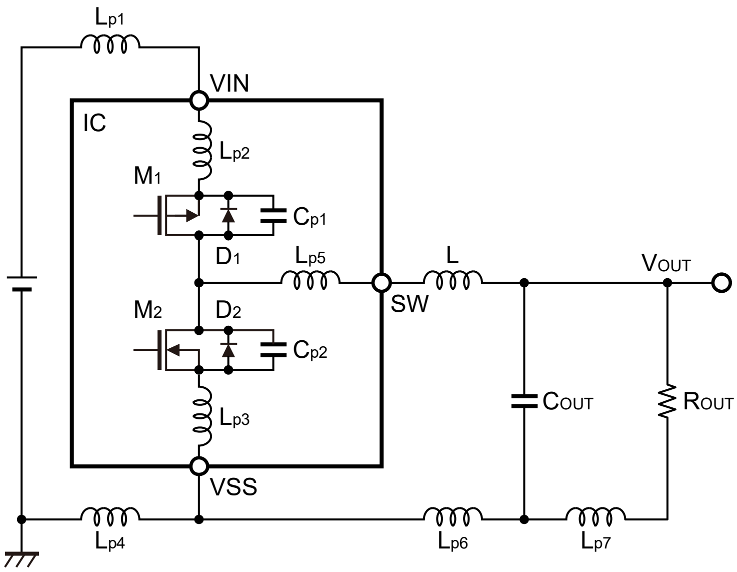
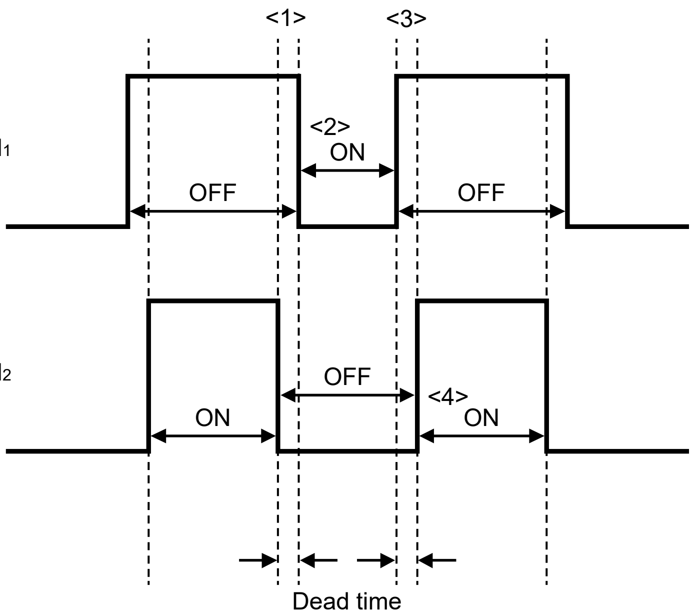


Figure 10

3. 2 High side power MOS FET (M_1) and low side power MOS FET (M_2) operation

M_1 and M_2 in **Figure 10** are operated so that they do not go ON simultaneously to prevent feed-through current.

Figure 11 shows the voltage waveform of the gate pin for M_1 and M_2.



<1> Both M_1 and M_2 are OFF. This time period is called dead time.
<2> M_1 turns ON after the elapse of dead time.
<3> Both M_1 and M_2 are again OFF and there is dead time.
<4> M_2 turns ON after the elapse of dead time.

In this manner, power is supplied to the load by alternately turning M_1 and M_2 ON and OFF after a dead time period.

Figure 11

3. 3 Ringing caused when M_1 is ON

Figure 12 is the observed waveform of the ringing waveform when M_1 is ON. The ringing frequency is approximately 300 MHz.
This is equivalent to the resonant frequency assuming that L_p = 5 nH and C_{p2} = 60 pF.

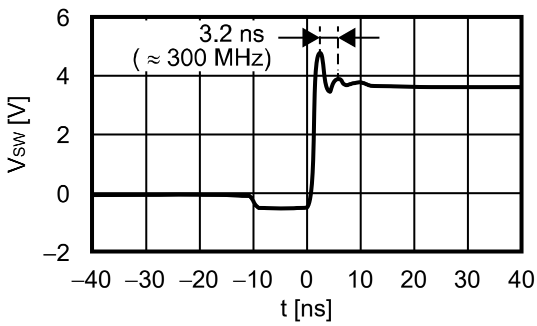


Figure 12

Since M_2 is ON in **Figure 12**, SW pin voltage (V_{SW}) is around 0 V. When M_2 turns OFF, the dead time indicated in <1> in **Figure 11** starts. When power is supplied to the load, current flows during dead time from the VSS pin in the direction of the SW pin to inductor (L) via the parasitic diode (D_2) of M_2. For this reason, the D_2 forward voltage causes V_{SW} to drop slightly below 0 V. When M_1 later turns ON, V_{SW} rises steeply to power supply voltage level ($\frac{dv}{dt}$) and parasitic inductance (L_{p1} to L_{p4}) and parasitic capacitance (C_{p2}) cause LC resonance that generates ringing. The ringing frequency is the L_{p1} to L_{p4} and C_{p2} resonance frequency. Since M_1 is ON, V_{SW} rises to the power supply voltage level.

3. 4 Ringing caused when M_1 is OFF

Figure 13 is also the observed waveform of the ringing waveform when M_1 is OFF.

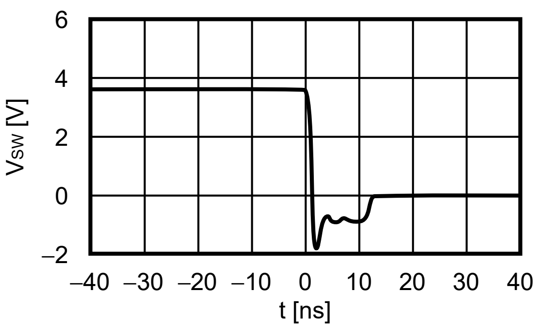


Figure 13

Since M_1 is ON in **Figure 13**, V_{SW} is about power supply voltage level. When M_1 turns OFF, the dead time indicated in <3> in **Figure 11** starts. When power is supplied to the load, current flows during dead time from the VSS pin in the direction of the SW pin to L via the D_2 of M_2. At this time, V_{SW} drops steeply from power supply voltage level ($\frac{dv}{dt}$) and L_{p1} to L_{p4} and C_{p1} cause LC resonance that generates ringing. The ringing frequency is the L_{p1} to L_{p4} and C_{p1} resonance frequency. During dead time, current flows from the VSS pin in the direction of the SW pin to L via D_2 of M_2, and the D_2 forward voltage causes V_{SW} to drop slightly below 0 V. Then M_2 turns ON, and V_{SW} becomes around 0 V.

3. 5 Impact of parasitic inductance on board layout and SW pin ringing

The characteristics of a step-down switching regulator are impacted by the parasitic inductance caused by the board pattern. For this reason, board layout must ensure that the parasitic inductance caused by the board pattern does not impact the characteristics of the step-down switching regulator circuits. A good example and a bad example of board layout are shown below.

Figure 14 shows that since the ceramic capacitors (C_{IN}, C_{INa}) are placed in the immediate vicinity of the power supply IC, there is virtually no parasitic inductance between the C_{IN}, C_{INa} and the power supply IC. Since the noise caused by L_{p1} and L_{p4} during switching operation can be reduced, the ringing of the SW pin is reduced as shown in **Figure 16**.

By contrast, **Figure 15** shows that C_{IN} and C_{INa} are placed away from the power supply IC. There is L_{p1} between C_{IN}, C_{INa} and the VIN pin making the feedback path to the VSS pin long and there is also L_{p4}. This increases the noise generated during the switching operation and also increases the ringing of the SW pin as shown in **Figure 17**.

Good example

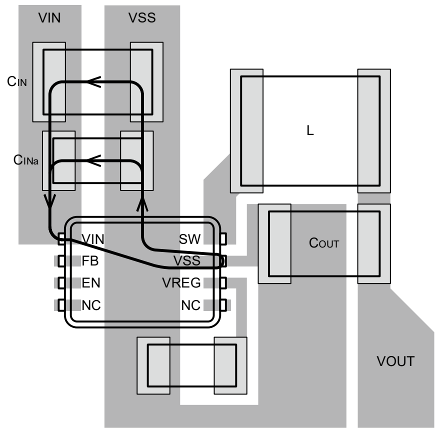


Figure 14

Bad example

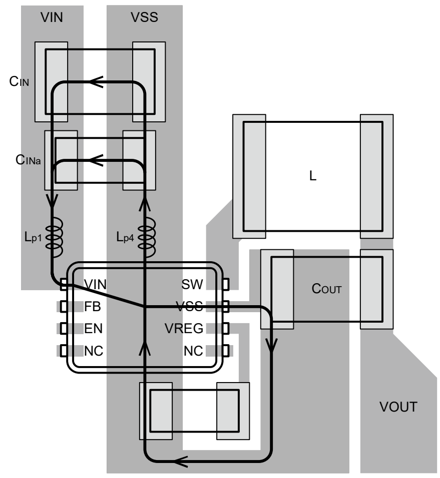


Figure 15

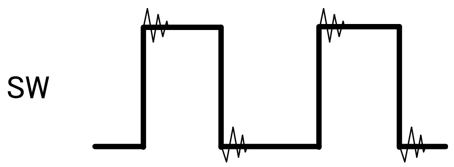


Figure 16

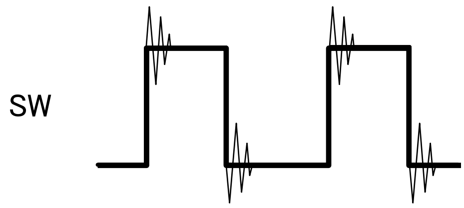


Figure 17

4. Board Layout Noise Countermeasures

Noise countermeasures are absolutely essential in a step-down switching regulator. Without countermeasures, noise may have an adverse impact on the electronic circuits in the vicinity. The input capacitor plays a major role in reducing noise. In board layout, the placement of input capacitors and VIN and VSS wirings are crucial. The input capacitors are of paramount importance and should be placed as close to the IC as possible and on the same surface layer.
C_{IN} is an essential capacitor to ensure stable IC operation and to suppress noise. C_{INa} is a capacitor of approximately 0.1 μF which is connected in parallel to C_{IN}. Add this capacitor as required to suppress mainly 10 MHz or larger noise.

4. 1 Placement and layout of input capacitor (C_{IN})

Figure 18 shows an example where ceramic capacitors (C_{IN} = 10 μF, C_{INa} = 0.1 μF) are placed in the immediate vicinity of and parallel to the VIN pin and the VSS pin. Be sure to select a C_{INa} with a capacitance smaller than C_{IN}. Place the low impedance C_{INa} = 0.1 μF capacitor closer to the VIN pin and VSS pin than the C_{IN} = 10 μF capacitor. This combination of capacitors will lower the impedance in the high frequency range, suppress noise during switching operation and minimize ringing.

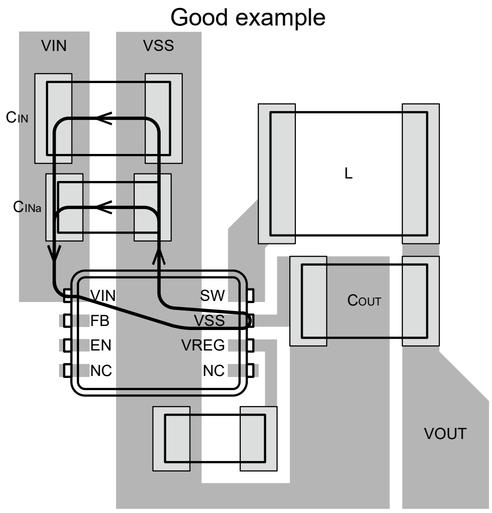


Figure 18

Figure 19 shows the frequency characteristics of C_{IN} impedance. The impedance of C_{IN} = 10 μF is minimized around 2 MHz.
Figure 20 shows the frequency characteristics of C_{INa} impedance. The impedance of C_{INa} = 0.1μF is minimized around 22 MHz.

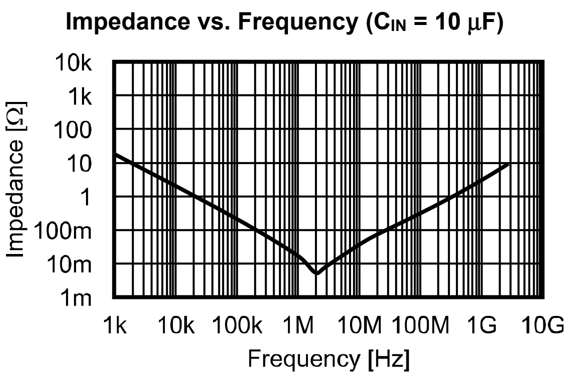


Figure 19

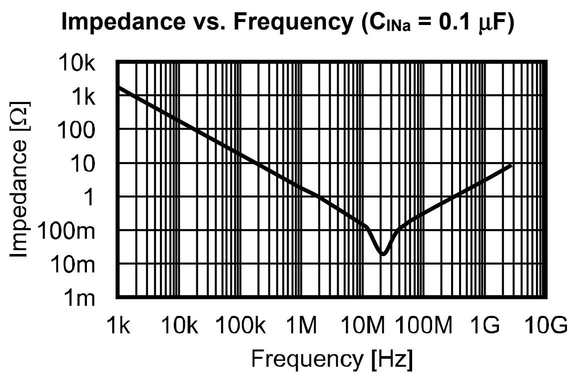


Figure 20

4. 2 SW wiring layout and inductor (L) placement and layout

The noise is an electromagnetic wave and propagates through space. To minimize noise, so called emission noise, that propagates through space, it is essential to minimize the distance between the SW pin and L and reduce the wiring length of the layout within the allowable current capacity range.
The rectangular wave voltage output from the SW pin contains high-frequency components, which could cause SW wiring to act as an antenna and thereby increase emission noise. In addition, as the high-frequency components in the rectangular wave voltage previously mentioned are transmitted from the SW pin to VOUT via the parasitic capacitance, SW wiring must be kept apart from VOUT wiring. Select a closed magnetic path L with low emission noise.

Figure 21 shows an example where the wiring area between the SW pin and L is reduced and the distance between SW wiring and VOUT wiring is extended.
By contrast, **Figure 22** shows an example where the SW wiring area is excessively large, the distance between SW wiring and VOUT wiring is short, and the parasitic capacitance is large.
If L heat generation is a concern, extend the SW wiring area to increase the heat dissipation effect. SW wiring layout must account for the conflicting requirements of controlling emission noise and reducing heat build-up.

Good example

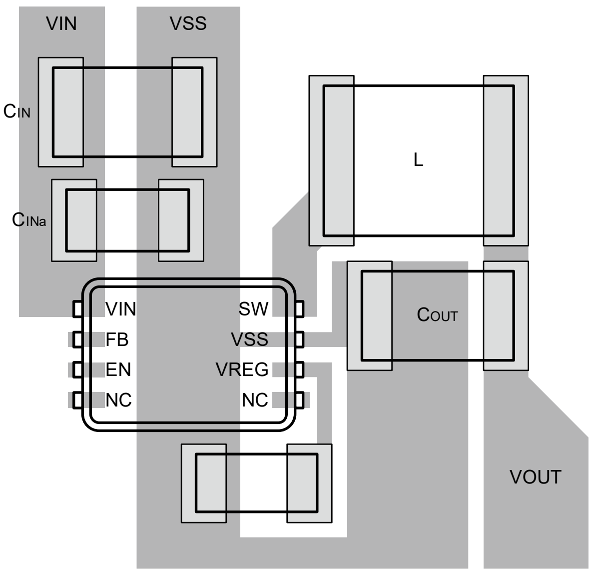


Figure 21

Bad example

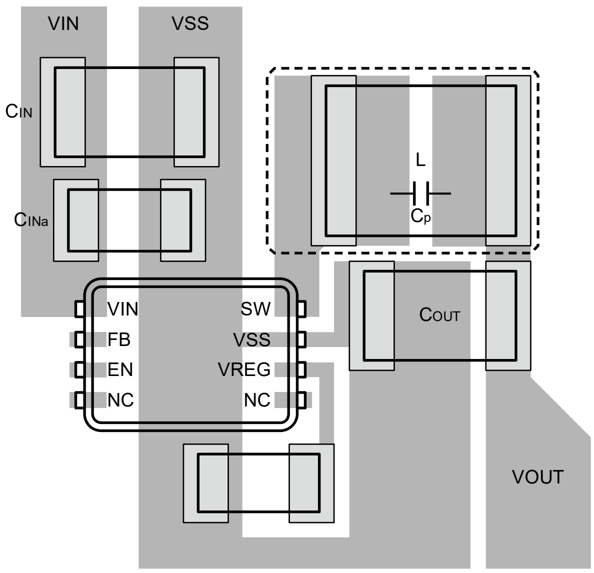


Figure 22

Figure 23 and **Figure 24** are cross sectional views of the L mounting in **Figure 21** and **Figure 22**, respectively.

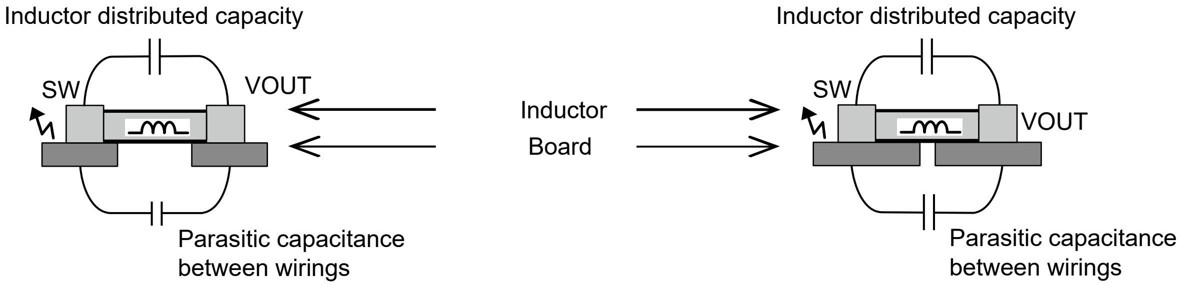


Figure 23

Figure 24

As the L land pattern shows in **Figure 21**, the distance between the SW pin and VOUT in **Figure 23** is longer. In contrast, as the land pattern shows in **Figure 22**, the distance between the SW pin and VOUT in **Figure 24** is shorter. The shorter the distance between the SW pin and VOUT, the larger the parasitic capacitance between the SW pin and VOUT becomes. For this reason, the parasitic capacitance in **Figure 24** is larger than that in **Figure 23**. A large parasitic capacitance will make it easier for noise generated in the SW pin during the switching operation to overlap VOUT.
The SW wiring area in **Figure 24** is large, which may increase emission noise. For this reason, make sure to provide sufficient space between the L electrodes in the board layout of the lower portion of L to minimize the emission noise dispersion area.
As shown in **Figure 21** and **Figure 22**, since L is connected to the SW pin, the presence of a small amount of parasitic inductance will have negligible impact on the inductance value.

Figure 25 shows a layout example of SW wiring and L placement. As shown below, if the SW pin cannot be wired to the bottom portion of C_{IN}, route the wiring through a thermal via and along the lower layer.

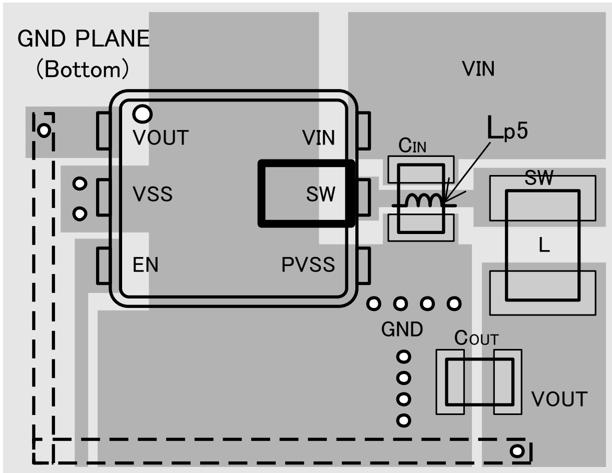


Figure 25

4. 3 Placement and layout of output capacitor (C_{OUT})

An output capacitor is essential in a step-down switching regulator for smoothing the output voltage waveform. During switching operation in a switching regulator, M_1 and M_2 are turned ON alternately and separated by dead time. When M_1 is ON, current flows to M_1, and when M_2 is ON, current flows to M_2. Since the current in L, M_1 and M_2 is the same, the voltage waveform near L fluctuates greatly. These voltage waveform fluctuations become noise that propagates through space. C_{OUT} smooths the voltage waveform and also absorbs the noise generated by the fluctuations of the output voltage waveform.

For that reason, place C_{OUT} close to the IC. If the area of the current path indicated by the bold line (SW pin → L → C_{OUT} → VSS pin) is reduced, the emission noise to be generated will be minimized. Be sure to pull out VOUT wiring after routing through the C_{OUT} land. If this is not the case, smoothing due to L and C_{OUT} is weakened causing high-frequency components in the rectangular wave voltage of SW pin to be conducted to VOUT. Similarly, when increasing the line width, pull out a wiring after routing through C_{OUT} land.

Figure 26 is an example where the current path area is narrowed. VOUT wiring is pulled out after routing through the C_{OUT} land.
By contrast, **Figure 27** is an example where the distance between the IC and C_{OUT} is long and the current path area is large. VOUT wiring is pulled out from L land without routing through C_{OUT} land. **Figure 28** is an example where VOUT line width is excessively increased before routing through C_{OUT} land.

Good example

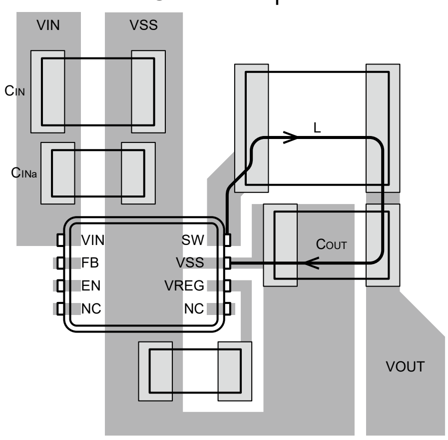


Figure 26

Bad example 1

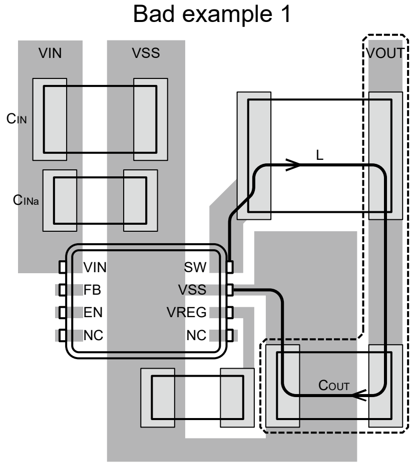


Figure 27

Bad example 2

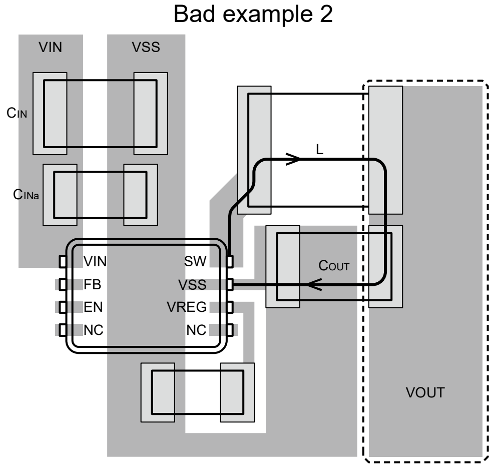


Figure 28

5. Precautions When Using Passive Voltage Probe to Measure Output Voltage (V_{OUT})

It is essential to pay attention to emission noise when measuring V_{OUT} of a step-down switching regulator circuit. Especially, when using an oscilloscope to measure V_{OUT} waveforms, the passive voltage probe must be provided with noise countermeasures. Otherwise emission noise will overlap the V_{OUT} waveform making it impossible to correctly measure the output voltage waveform. Emission noise overlapping the V_{OUT} waveform will propagate from the passive voltage probe through the ground lead of the probe. To reduce the noise overlapping the V_{OUT} waveform, the ground lead of the passive voltage probe has to be modified.

The following shows the difference in V_{OUT} waveform between a passive voltage probe with a regular ground lead and a ground spring. **Figure 29** and **Figure 31** show waveforms for the same voltage on the same oscilloscope.

5. 1 Measurements using regular passive voltage probe

Figure 29 shows a V_{OUT} waveform measured using a regular passive voltage probe shown in **Figure 30**.

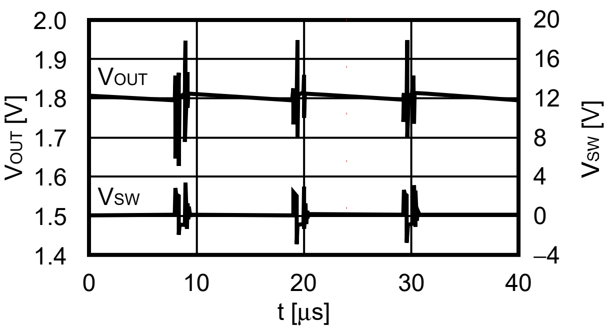


Figure 29

Figure 30

5. 2 Measurements using passive voltage probe with ground spring

Figure 31 shows a V_{OUT} waveform measured using a passive voltage probe with a modified ground spring shown in **Figure 32**. High-frequency noise does not overlap the V_{OUT} waveform in measurements made with this probe.

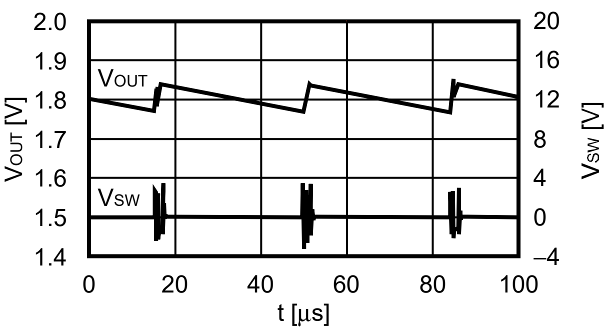


Figure 31

Figure 32

6. Precautions

- The usages described in this application note are typical examples using ICs of ABLIC Inc.
  Perform thorough evaluation before use.

- Do not apply an electrostatic discharge to this step-down switching regulator that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

7. Related Sources

The information described in this application note and the related product datasheets are subject to change without notice. Contact our sales representatives for details.
Regarding the newest version of the datasheet, select product category and product name on our website, and download the PDF file.

www.ablic.com ABLIC Inc. website

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07