MAZARITA_TEAM

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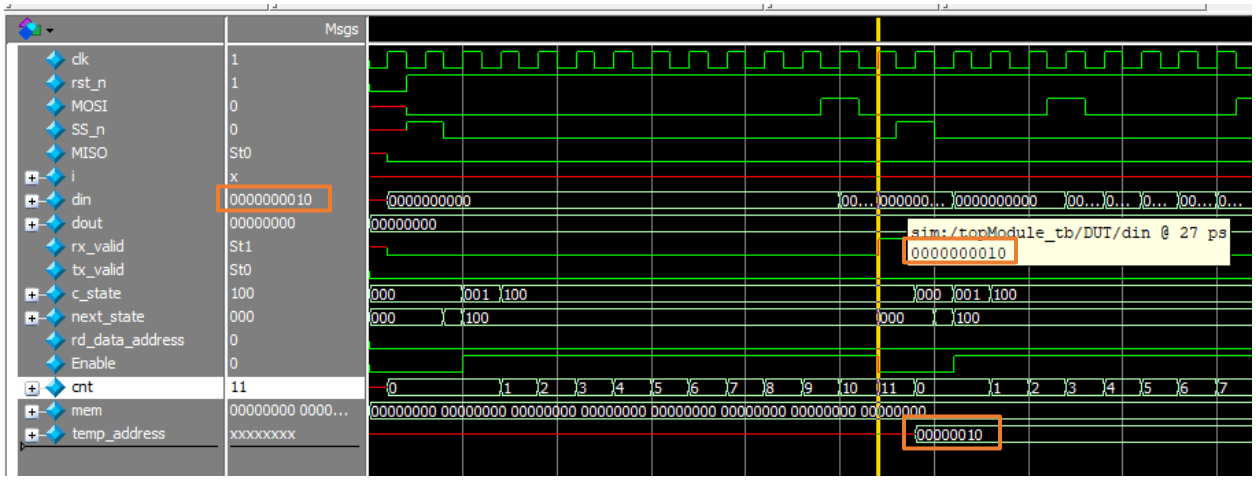
Contents

1) Design Files:

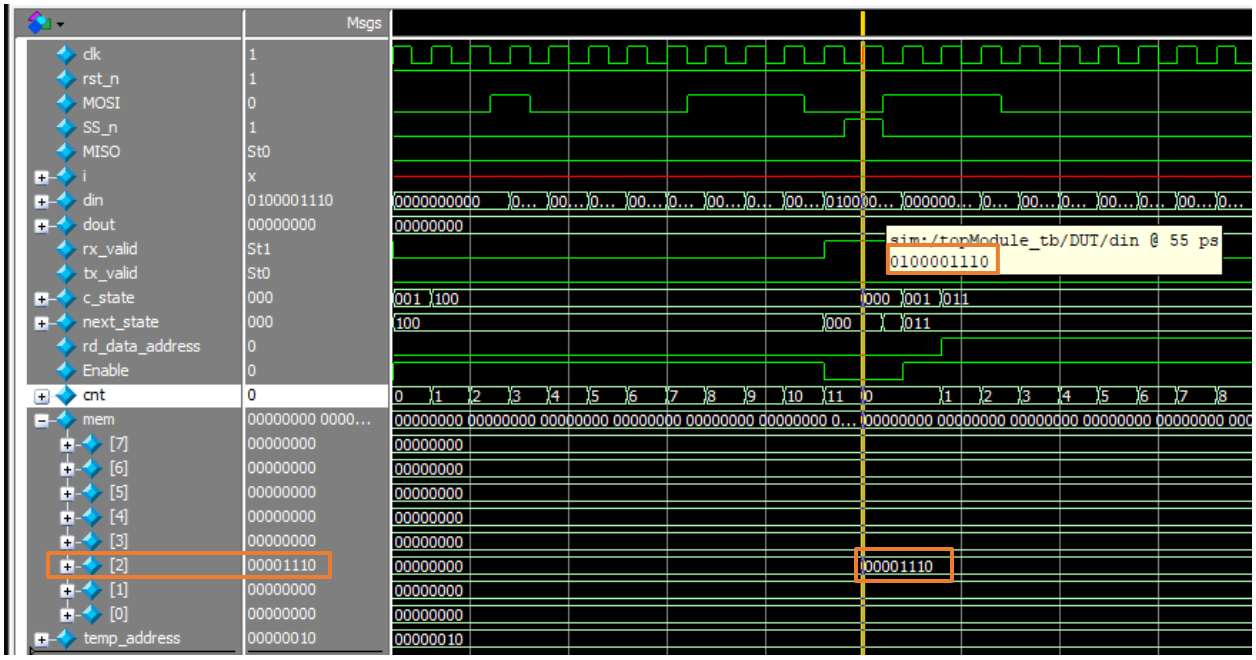
Link:
https://drive.google.com/drive/folders/1XNSKlNwFX5V1o6J_0B1wfRq-JrDrnDLf?usp=sharing

2) Snippets:

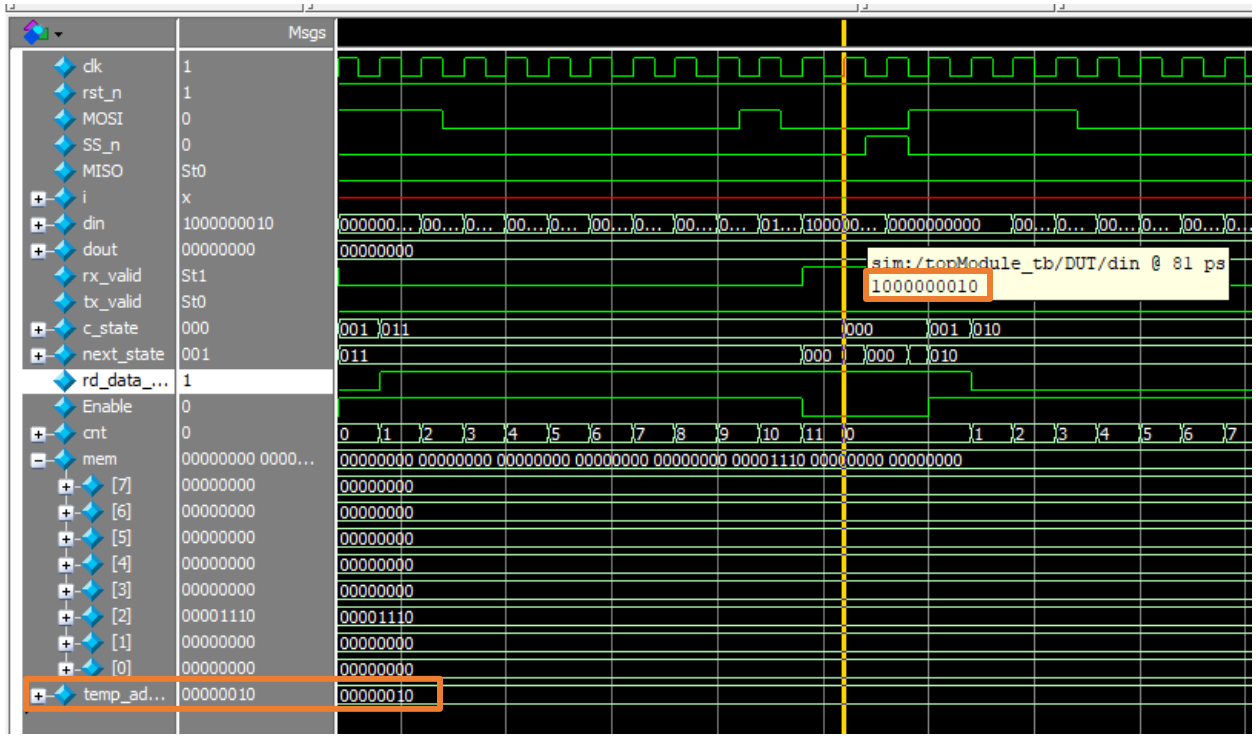
1. Two most significant bits of rx_data are [00],then write address state [the address I'll use to insert into RAM] in this case address is 8'b00000010 due to sequential output count from 2 not 1 so I'll get output at 11.



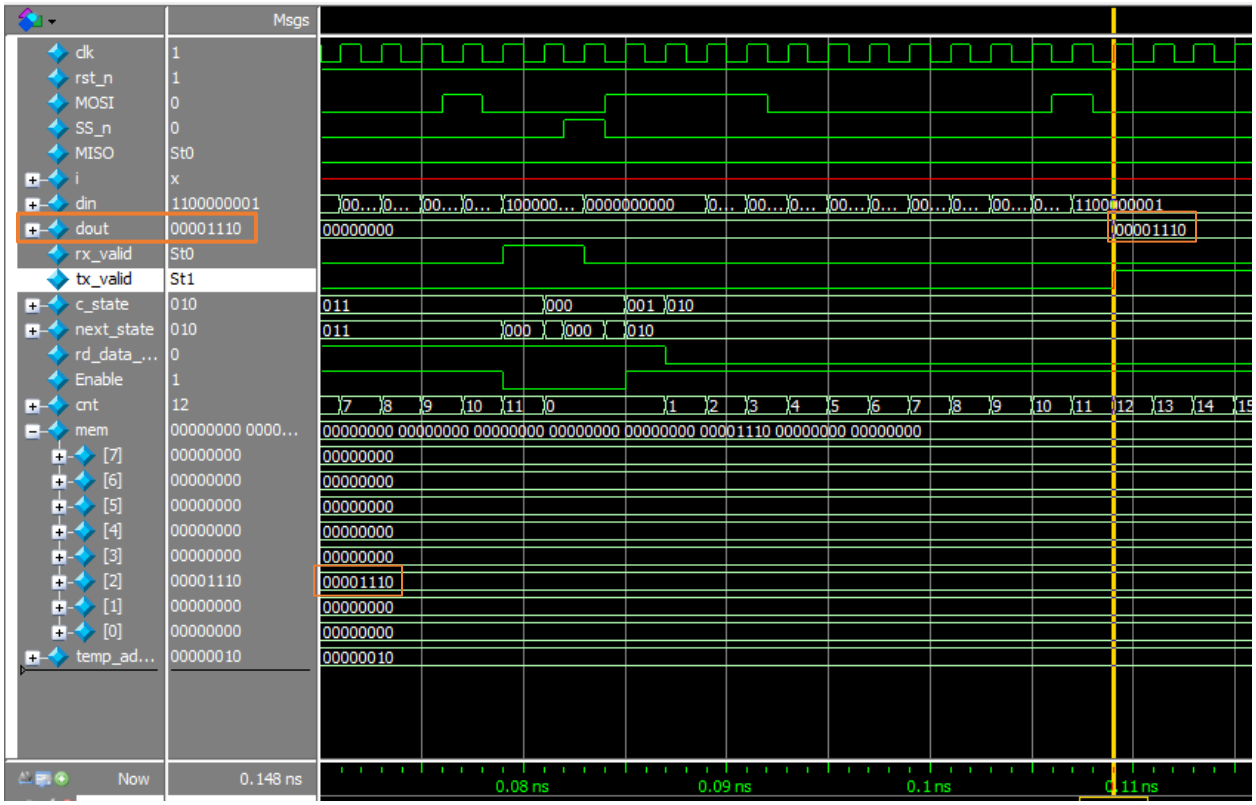
2. Two most significant bits of rx_data are [01],then I'll write data state with address from previous state which is 2 [8'b00000010] I stored it at temp_address ,hence I'll write my data [8'b00001110] into mem .



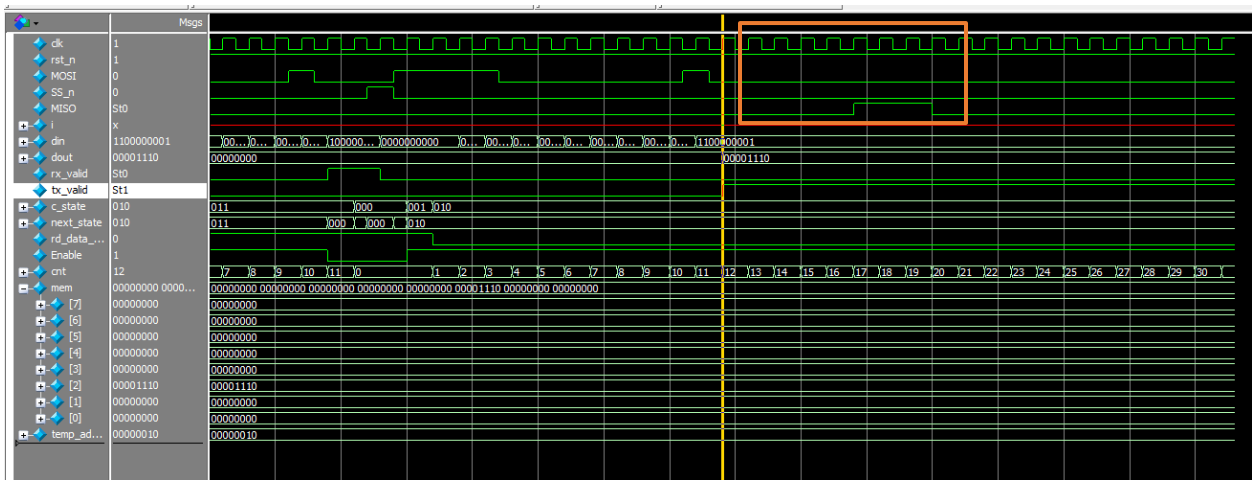
3. Two most significant bits of rx_data are [10],then I'll read address state and I supported same address memory I used to get same data from mem then my address is [8'b00000010].



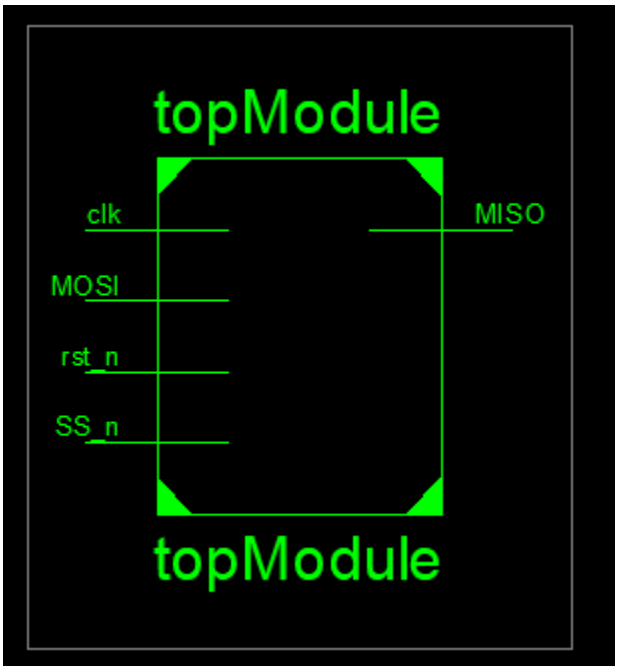
4. Two most significant bits of rx_data are [11],then I expected same data to be put on dout bus and this is read data state.

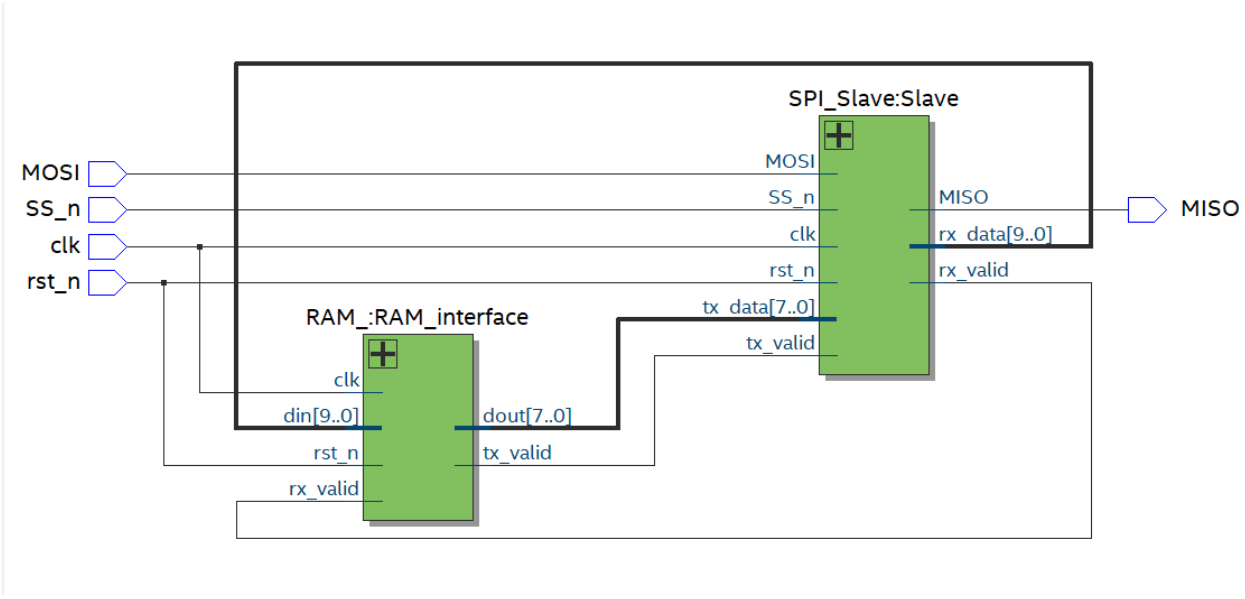


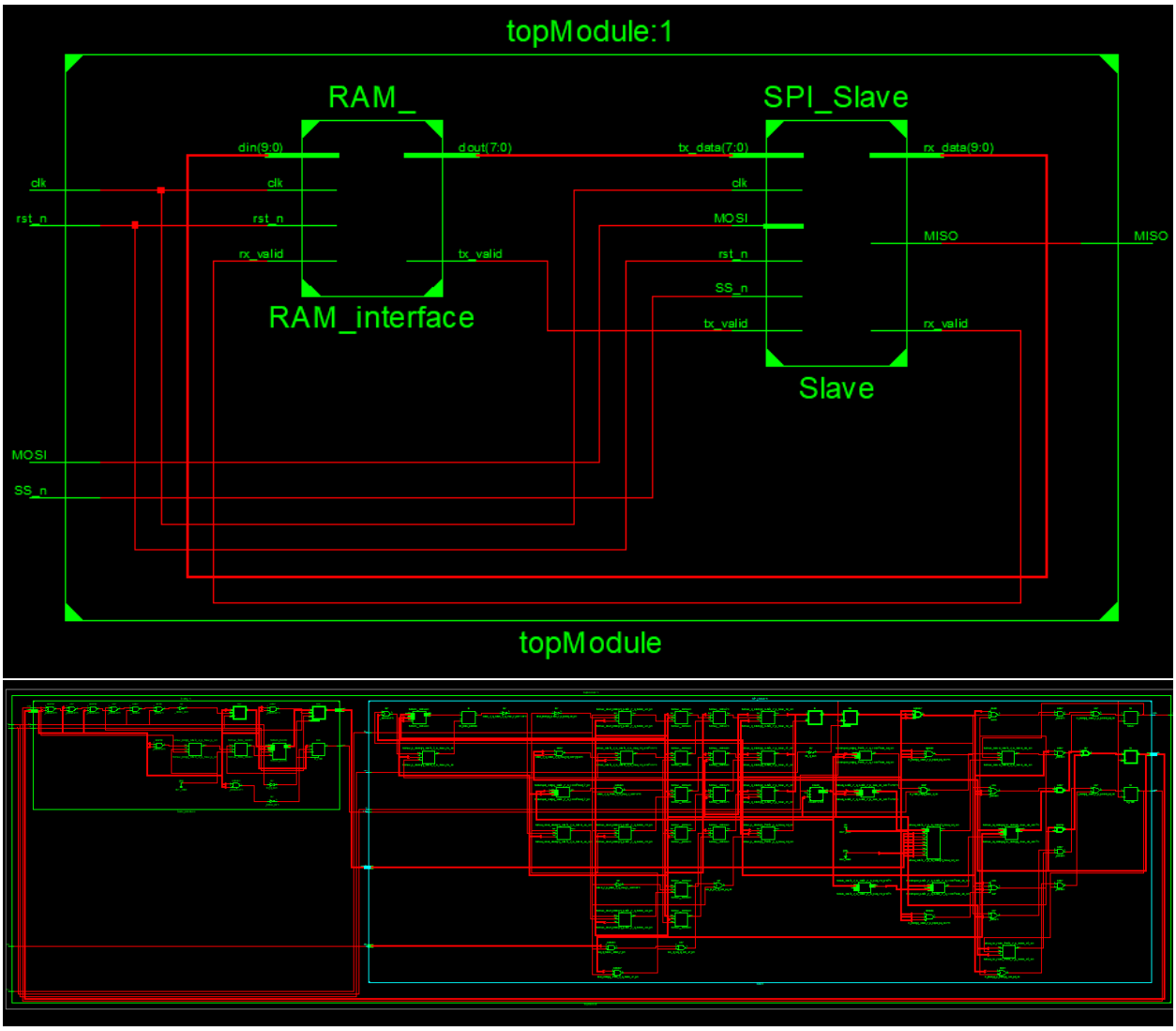
5. Finally I wait in Read Data state to export parallel data at single MISO bit [serial data].



3) Synthesis :


topModule
clk
MISO
MOSI
rst_n
SS_n
topModule


SPI_Slave:Slave
MOSI
SS_n
clk
rst_n
MISO
rx_data[9..0]
rx_valid
tx_data[7..0]
tx_valid
MOSI
SS_n
clk
rst_n
MISO
RAM_:RAM_interface
clk
din[9..0]
rst_n
rx_valid
dout[7..0]
tx_valid


topModule:1
RAM_
din(9:0)
dout(7:0)
clk
rst_n
rx_valid
tx_valid
RAM_interface
SPI_Slave
tx_data(7:0)
rx_data(9:0)
clk
MOSI
rst_n
SS_n
tx_valid
MISO
rx_valid
Slave
clk
rst_n
MOSI
SS_n
MISO
topModule

Thanks