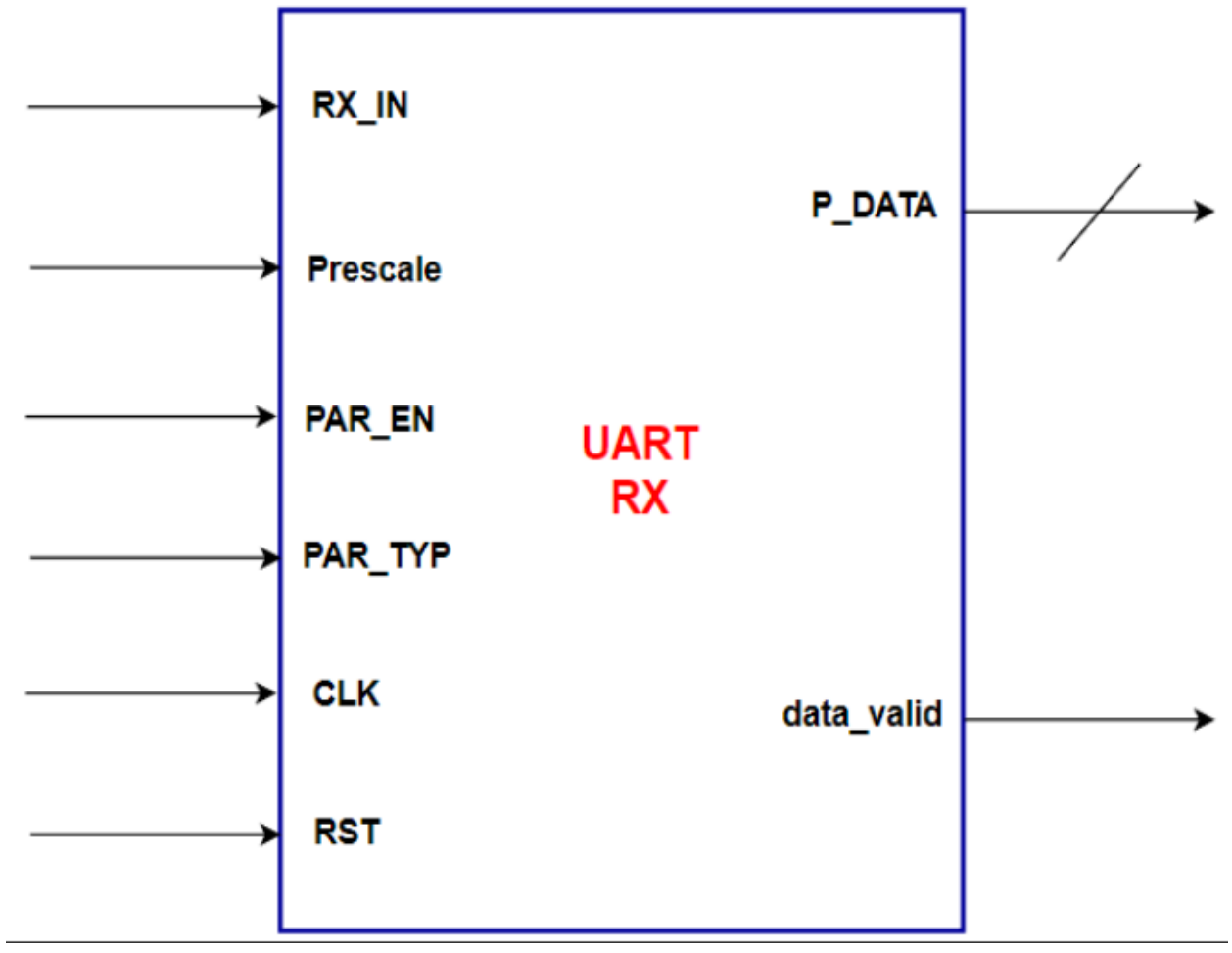
UART_RX

(Verification Plan)

- Block Interface :



- Configuration:
  - Parity type : 0 → even xor , 1 → odd xnor
  - F → F : consecutive frames
  - Frame [MSB:LSB]

- Test Cases :

#	Feature	RST	clk	frame	Typ	EN	scale	V(a)	V(e)	P(a)	P(e)	f→f
1	reset	0	1	x	x	x	x		0		0	0
2	start Glitch	1	1	11'b1xx_xxxx_xxxx	x	x	x		0		0	0
3	data	1	11*8	11'b001_1100_1111	0	1	8		1		8'hce	0
4	data	1	11*8	11'b010_0010_1101	0	1	8		1		8'hd1	0
5	data	1	11*8	11'b001_1100_1101	1	1	8		1		8'hce	0
6	data	1	11*8	11'b010_0010_1111	1	1	8		1		8'hd1	0
7	data	1	11*8	11'b000_0000_0011	1	1	8		1		8'h00	0
8	data	1	11*8	11'b011_1111_1101	0	1	8		1		8'hff	0
9	parity	1	11*8	11'b001_1100_1111	1	1	8		0		8'hce	0
10	parity	1	11*8	11'b001_1100_1101	0	1	8		0		8'hce	0
11	parity	1	11*8	11'b010_0010_1111	0	1	8		0		8'hd1	0
12	parity	1	11*8	11'b010_0010_1101	1	1	8		0		8'hd1	0

13	stop	1	11*8	11'b0xx_xxxx_xx00	x	1	8		0		xx	0
		Check all previous cases with no parity										
14		Check Consecutive Frames with no delays among frames										
15	data	1	11*8	11'b001_1100_1111	0	1	8		1		8'hce	1
16	data	1	11*8	11'b010_0010_1101	0	0	8		1		8'hd1	1
17	data	1	11*8	11'b001_1100_1101	1	0	8		1		8'hce	1
18	data	1	11*8	11'b010_0010_1111	1	1	8		1		8'hd1	1
19	data	1	11*8	11'b000_0000_0011	1	1	8		1		8'h00	1
20	data	1	11*8	11'b011_1111_1101	0	1	8		1		8'hff	1
21	parity	1	11*8	11'b001_1100_1111	1	1	8		0		8'hce	1
22	parity	1	11*8	11'b001_1100_1101	0	1	8		0		8'hce	1
23	parity	1	11*8	11'b010_0010_1111	0	1	8		0		8'hd1	1
24	parity	1	11*8	11'b010_0010_1101	1	1	8		0		8'hd1	1