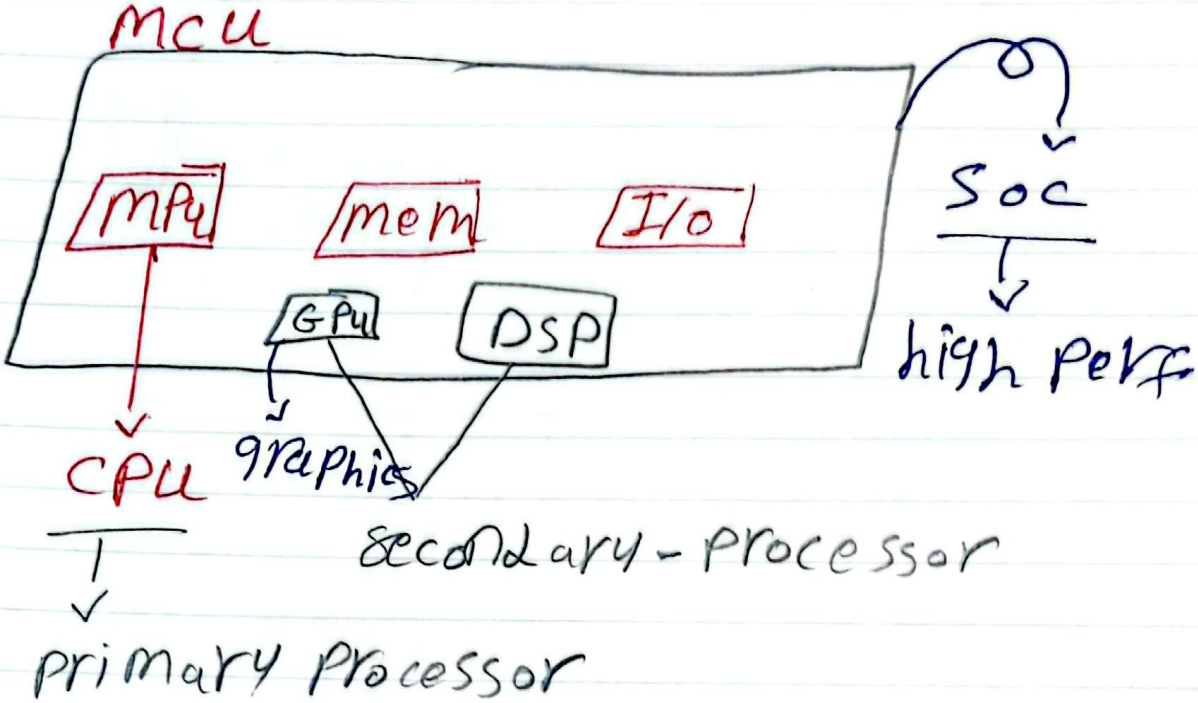
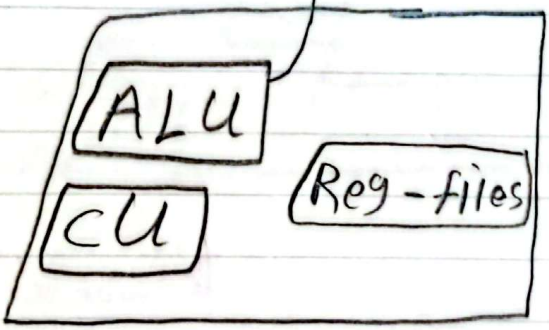
*MCU Micro ~~computer~~ controler unit "computing sys"



* MPU → Arithmetic Process



APP

SOC

Bereneta sw
APP
drivers
HW

OS APP
APP
kernal
drivers
H-W

	SB	SoC
size →	↑	↓
cost →	↑	↓
Power →	↑	↓
configurability	✓	X

configurability → development stage
✓ → Easy to upgrade

IC :- integrated circuit EX : 555 , OP-amp

* VLSI :- millions of Transistors

① size ↓ ② funtinality ↑

MP, Memory , SoC , RAM, Rom → Ic

* MPU

① Processor

16it ↔ 0 / 1

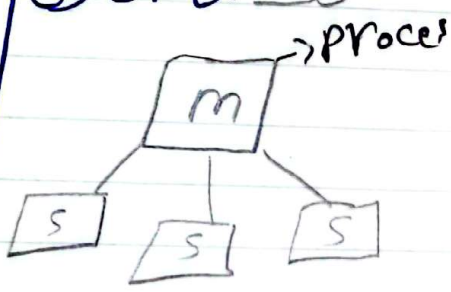
② micro processors

New Processors

→ Transistor

③ CPU

primary



introduction to Embedded systems

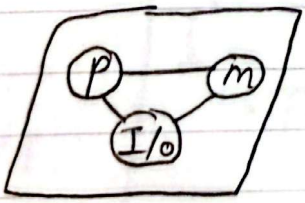
concepts :-

computing system → Processor, memory, I/O

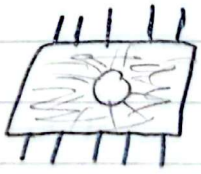
- General purpos
  - EX: Laptop
- Specific Purpos
  - EX: Embedded systems
    - constrains → ES challings
      - power
      - cost
      - size
      - speed / time

Embedded systems :-

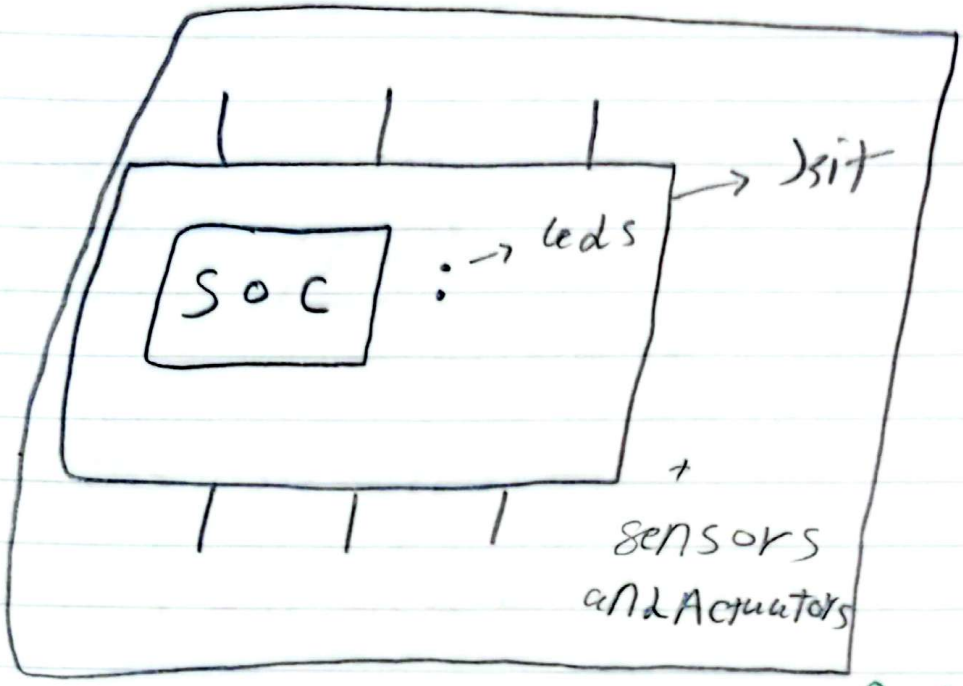
① system board

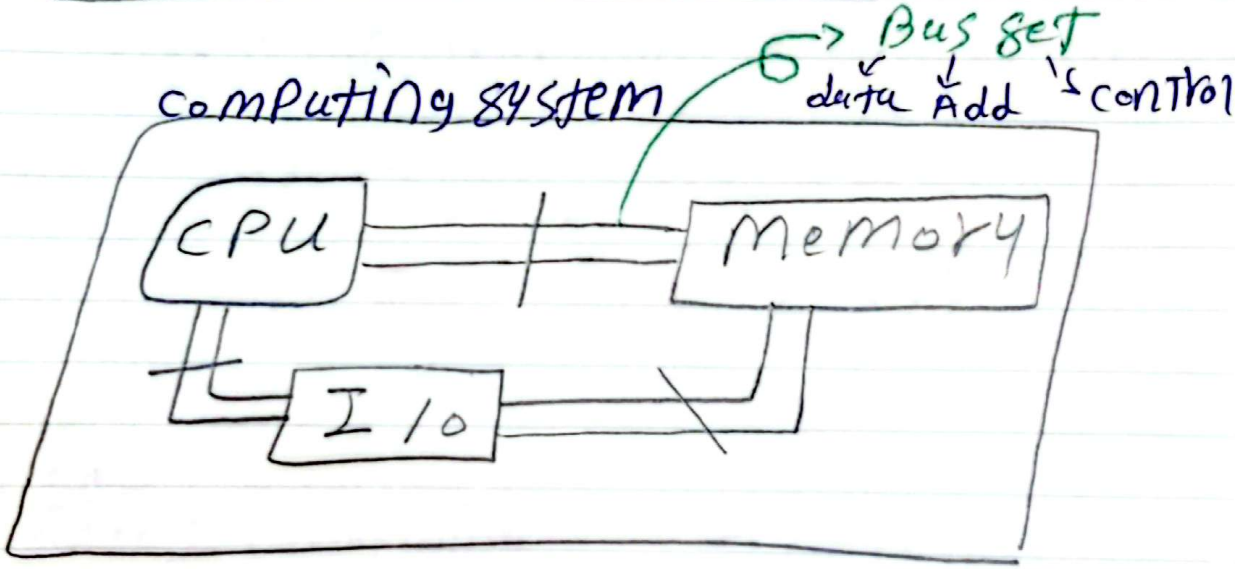


② system on chep



ECU Electrical control unit





* Processor :-

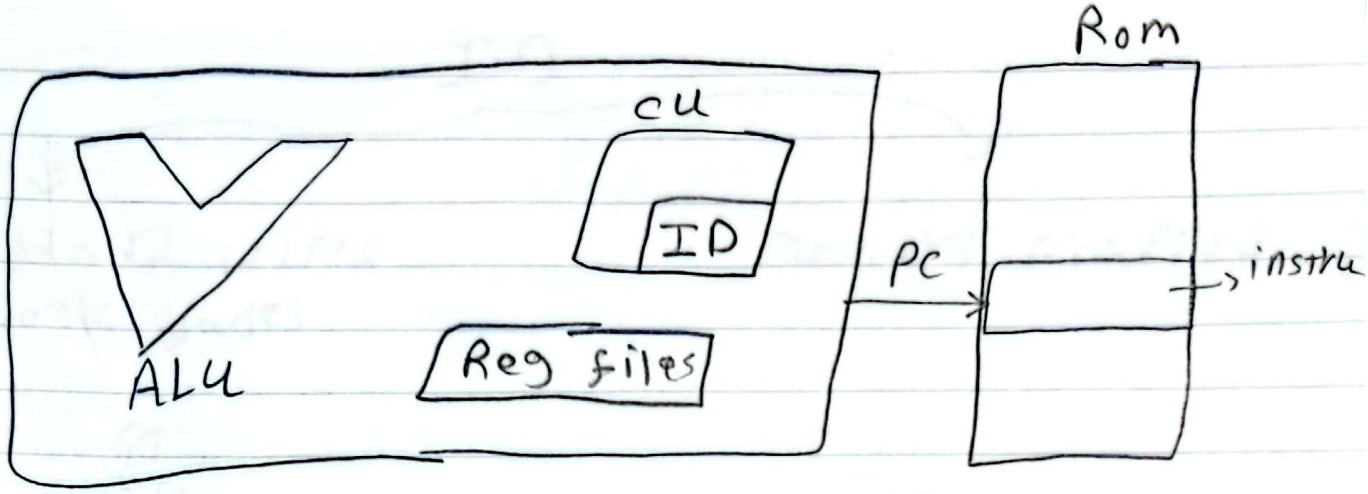
⇒ instruction life cycle

① fetch

CU fetch The instruction from rom to IR " instruction register

② Decode instruction decoder in CU decode the instruction

③ Execute

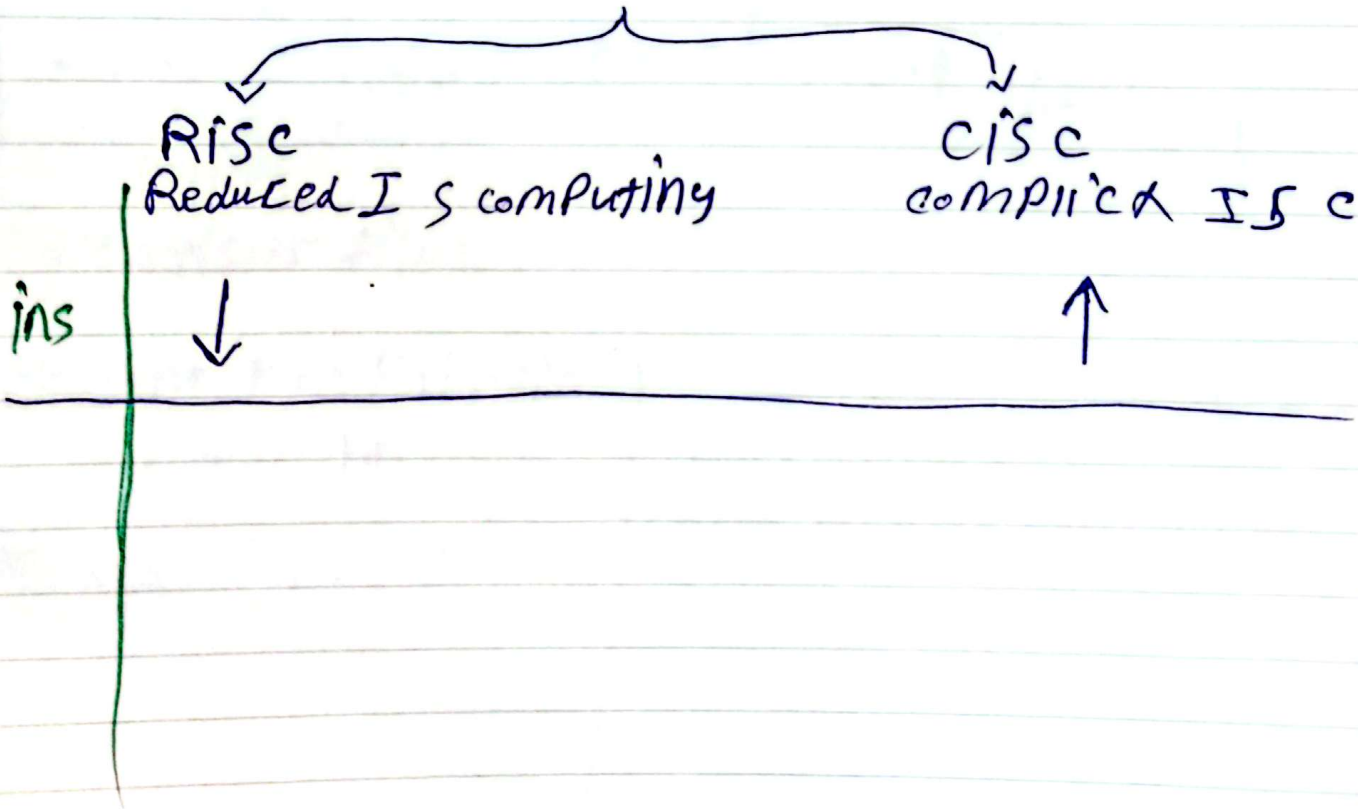


① CU fetch → instruction from Rom

② I D Decode instruction

③ After decoding instruction CU send signal to ALU Then Result store → Register files

* instruction set Arch ISA



ID

Hard wired logic gates

fast
simple
RICS

memory mapped

slow
CISC

	RISC	CISC
size	ALU↓, ID↑	ALU↑, ID↓
cost	SW↑, HW↓	SW↓, HU↑
Perform	=	
Power	ALU↓, IDT↑	ALU↑, ID↓

* Register files :-

① General Purpose
data store
temporary

② special Purose
Each register
has specific purpose

*Special Purpose Register

① PC → Program counter
↳ Next instruction

② SP → stack Pointer

③ ACC → Accumulator → result store temp

④ IR → instruction Register → store the instruction from memory

⑤ PSW → Process status word
↳ flags

*Memory : set of locations

① volatile → RAM

② Non volatile → Rom

③ Hybrid

Ram → Static → Transistor
→ Dynamic → Based on capacitor

① Dynamic Ram

Advantage

① simple H.W

② low cost per bit

③ High denisity

④ low power consumption

② Static Ram

faster, High cost

each bit has 6 Transistor

	S	D
Size	↓	↑
cost	↑	↓
Per	↑	↓
Power	↓	↑

Rom :-

① masked Rom → fixed code

② PRom "programmable rom" → one time programmable

③ EPRom old Erasable

④ EEProm settings storage

⑤ Flash Rom Rewritable firmware