Computer Architecture

Assignment 1 Verilog

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Group : 4

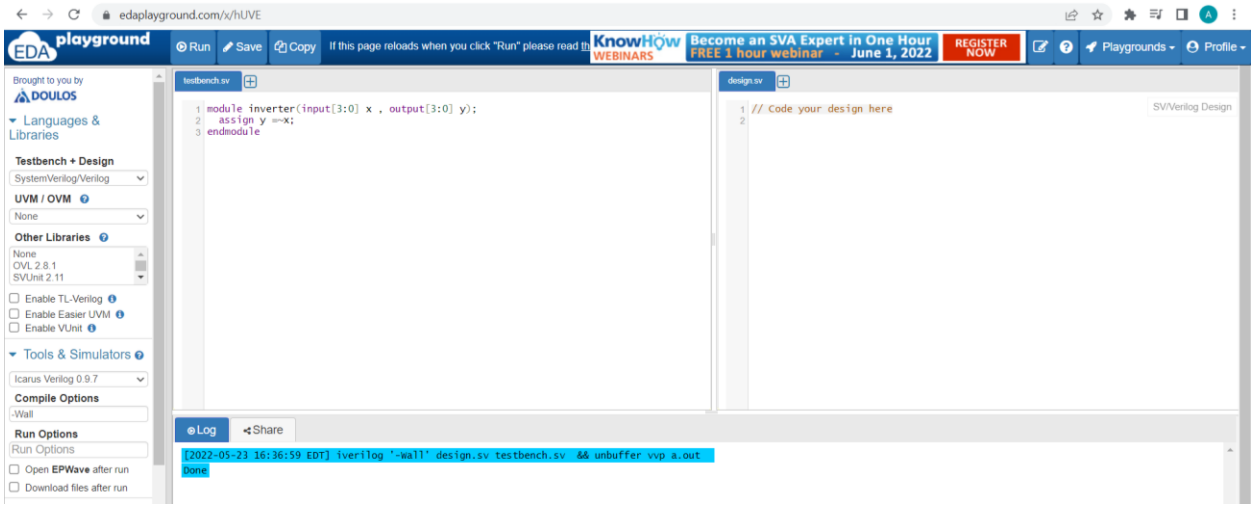
Section : 2

1-**INVERTOR**:

Code:-

```
module inverter(input[3:0] x , output[3:0] y);
  assign y =~x;
endmodule
```

Link:- https://edaplayground.com/x/hUVE



2-**Logic gates:**

Code:-

```
module gates(input [3:0] a,b,output [3:0] y1,y2,y3,y4,y5);
  assign y1=a&b; //AND
  assign y2=a|b; //OR
  assign y3=a^b;  //XOR
  assign y4=~(a&b); //NAND
  assign y5=~(a|b);  //NOR
endmodule
```

Link:- https://edaplayground.com/x/hUVE

3-**Multiplixer 2:1** :-

Code:-

```
module mux2(input[3:0] a0,a1,input[3:0] s , output[3:0] y);
 assign y = s ? a1 , a2 ;
endmodule
```

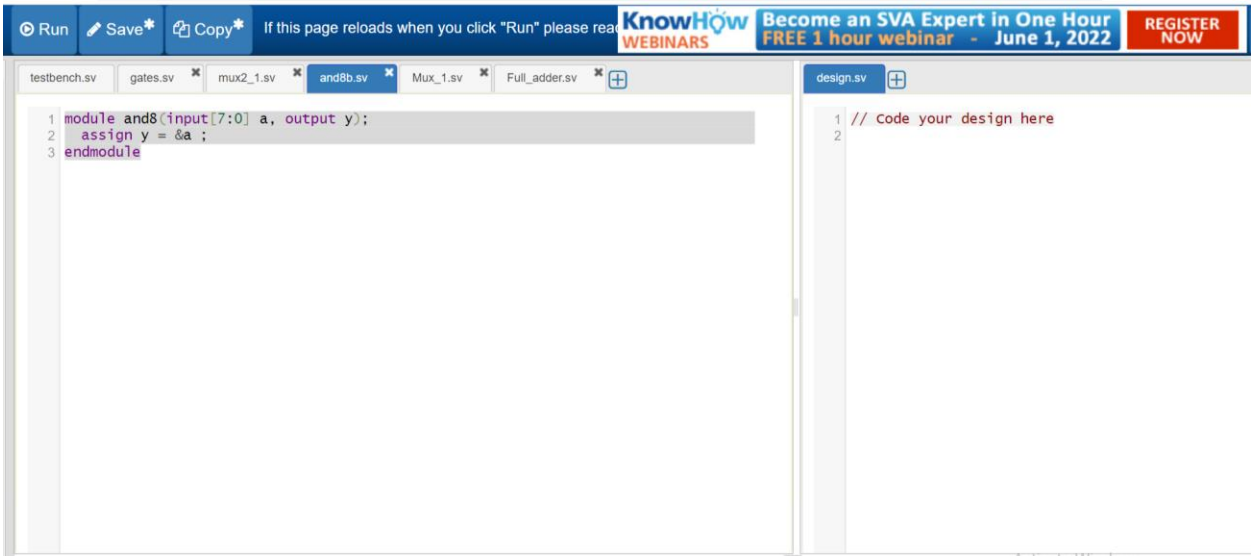
Link:- https://edaplayground.com/x/hUVE

4-**And-ing 8 bits** :-

Code:-

```
module and8(input[7:0] a, output y);
  assign y = &a ;
endmodule
```

Link:- https://edaplayground.com/x/hUVE

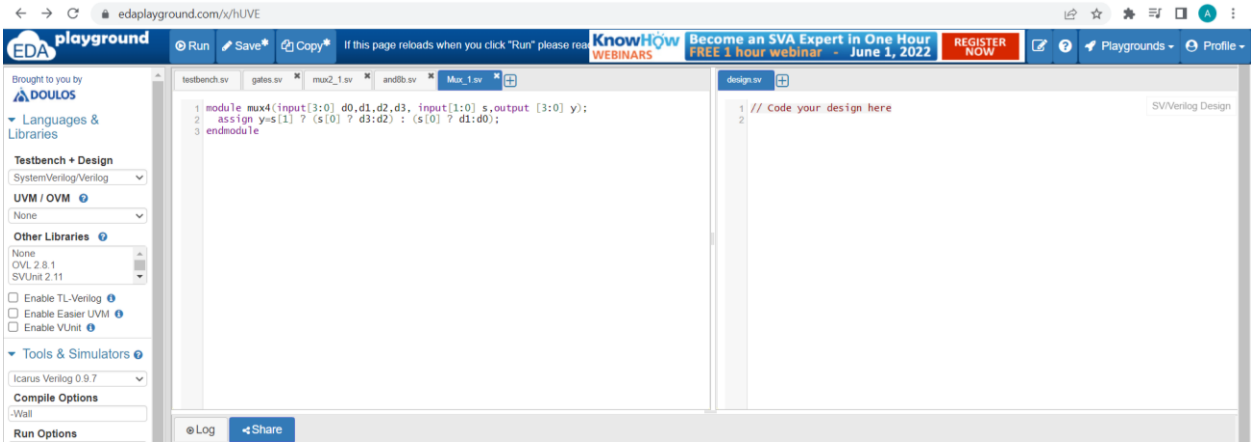


5-**Mux 4:1** :-

Code:

```
module mux4(input[3:0] d0,d1,d2,d3, input[1:0] s,output [3:0] y);
  assign y=s[1] ? (s[0] ? d3:d2) : (s[0] ? d1:d0);
endmodule
```

Link: https://edaplayground.com/x/hUVE



6- **Full Adder** :

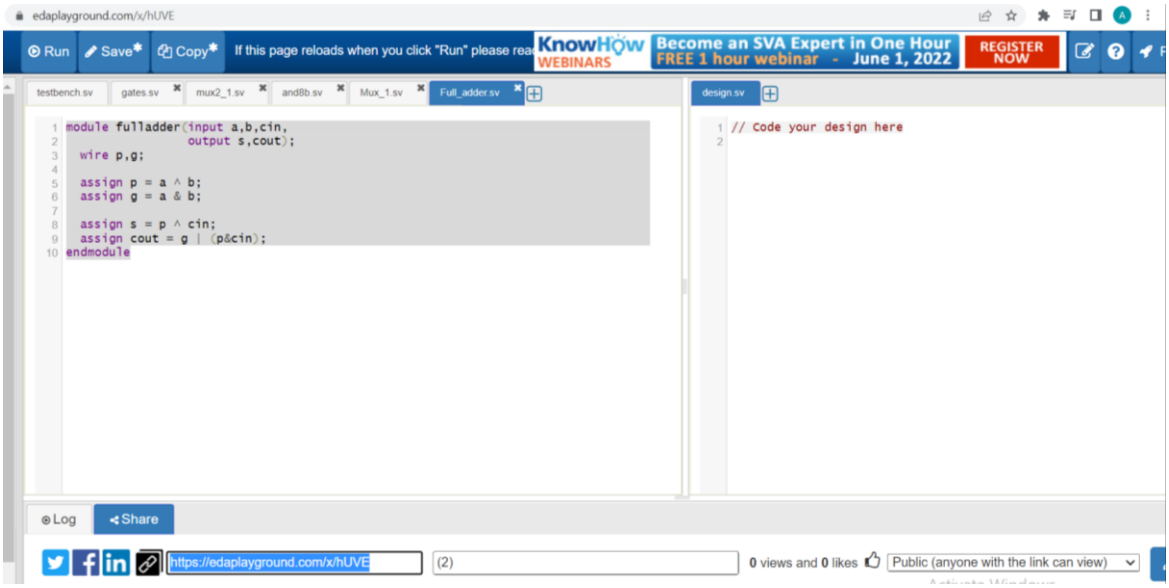
Code :

```
module fulladder(input a,b,cin,
                 output s,cout);
  wire p,g;

  assign p = a ^ b;
  assign g = a & b;

  assign s = p ^ cin;
  assign cout = g | (p&cin);
endmodule
```

Link: https://edaplayground.com/x/hUVE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gates.sv
mux2_1.sv
and8b.sv
Mux_1.sv
Full_adder.sv
design.sv
module fulladder(input a,b,cin,
output s,cout);
wire p,g;
assign p = a ^ b;
assign g = a & b;
assign s = p ^ cin;
assign cout = g | (p&cin);
endmodule
// Code your design here
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