EE 310 Hardware Description Languages
Spring 2018

Laboratory Assignment #2

Due Date: 29 March 2018

In this lab, you will design a sequential Future Video Coding (FVC) 4x4 Intra Prediction Hardware implementing the intra angular prediction mode with order 64 and angle 29. You will then write a behavioral Verilog model of this hardware.

A 4x4 block containing the pixels a1 to d4 and its neighboring pixels (R-H and R-P) are shown below. FVC 4x4 Intra Prediction Algorithm predicts the values of pixels a1 to d4 using the values of pixels R, A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P that belong to the neighboring blocks. The prediction equations used in intra angular prediction mode with order 64 and angle 29 are given in the attached file named 'intra_pred_equations.txt'.

R	A	B	C	D	E	F	G	H
I	a1	a2	a3	a4				
J	b1	b2	b3	b4				
K	c1	c2	c3	c4				
L	d1	d2	d3	d4				
M								
N								
O								
P								

Your hardware should start working after the input signal *start* is high for one clock cycle. I, J, K, L, M, N, O, P values (integers in the range [0-255]) will be given as inputs to your hardware. You should store these values into 8 bit registers. Your hardware should produce the output values a1 – d4 (integers in the range [0-255]) by implementing the intra prediction equations. Then, it should set the output signal *done* to high for one clock cycle.

In your hardware, you are not allowed to use multiplier or divider hardware for implementing multiplication with a constant and division by constant operations. These operations should be implemented using shifter and adder hardware. In your hardware, you are allowed to use only 16 adders/subtractors.

Write a behavioral Verilog model for your hardware design. In your Verilog model, the top-level Verilog module should have the following interface:

```
module intra_predictor (clk, reset, start, I, J, K, L, M, N, O, P,
                        done, a1, a2, a3, a4, b1, b2, b3, b4,
                        c1, c2, c3, c4, d1, d2, d3, d4)
  input clk, reset, start;
  input [7:0] I, J, K, L, M, N, O, P;
  output done;
  output [7:0] a1,a2,a3,a4,b1,b2,b3,b4,c1,c2,c3,c4,d1,d2,d3,d4;
  …..
endmodule
```

You should also write a Verilog testbench that verifies the correctness of your Verilog model. In this testbench, you should apply input values to your model and compare its outputs with the expected results.

Finally, put all of your Verilog files into one ".zip" file named Lab2_Partner1Lastname_Partner2Lastname.zip (e.g. *Lab2_Azgin_Hamzaoglu.zip*) and submit this zip file using EE310 SUCourse website.