EATCA-100

FPGA based ATCA Blade for RD 51 SRS System

User Manual

ver. 0, rev 1.1

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1. Functional description

EATCA-100 board is universal carrier for custom mezzanine modules implemented in ATCA standard. Available interfaces increase flexibility of the board as a building block for small and large scale data acquisition and/or processing systems.

The processing part of the board is divided into two equal channel: A and B. The structure of the single channel is presented in Table 1.

Name	Description
User FPGA	Virtex 6 family FPGA
SODIMM slot	SODIMM slot for DDR3 memory extension modules
Local Power Supplies	Local DC/DC converters and LDOs, which provide local voltages to components
Local Clock Cleaner	Dedicated LMK03200 based circuit for clock cleaning purposes
Mezzanine slot	Custom mezzanine slot for extension cards

Table 1. Elements of a single processing channel

In addition to processing part the board is also equipped with clock distribution units, global power supplies and additional communication interfaces (full mesh Z2 connections). The functionality of the board can be further extended by RTM boards plugged into Z3 connector. The further details of each subsystem are covered by the following chapters.

1.1. Board layout

The board layout is presented in Figure 1. Several key elements are highlighted. The full block diagram is presented in Figure 2.

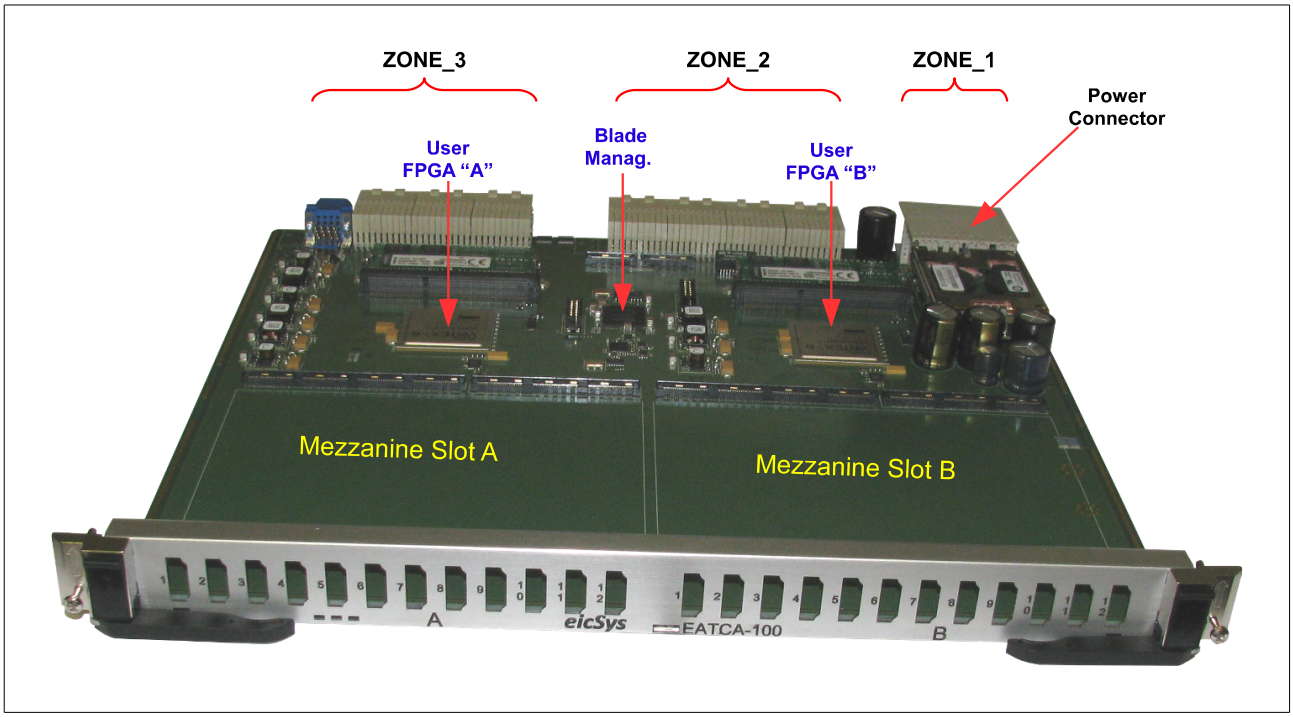

Figure 1. Board and its main components

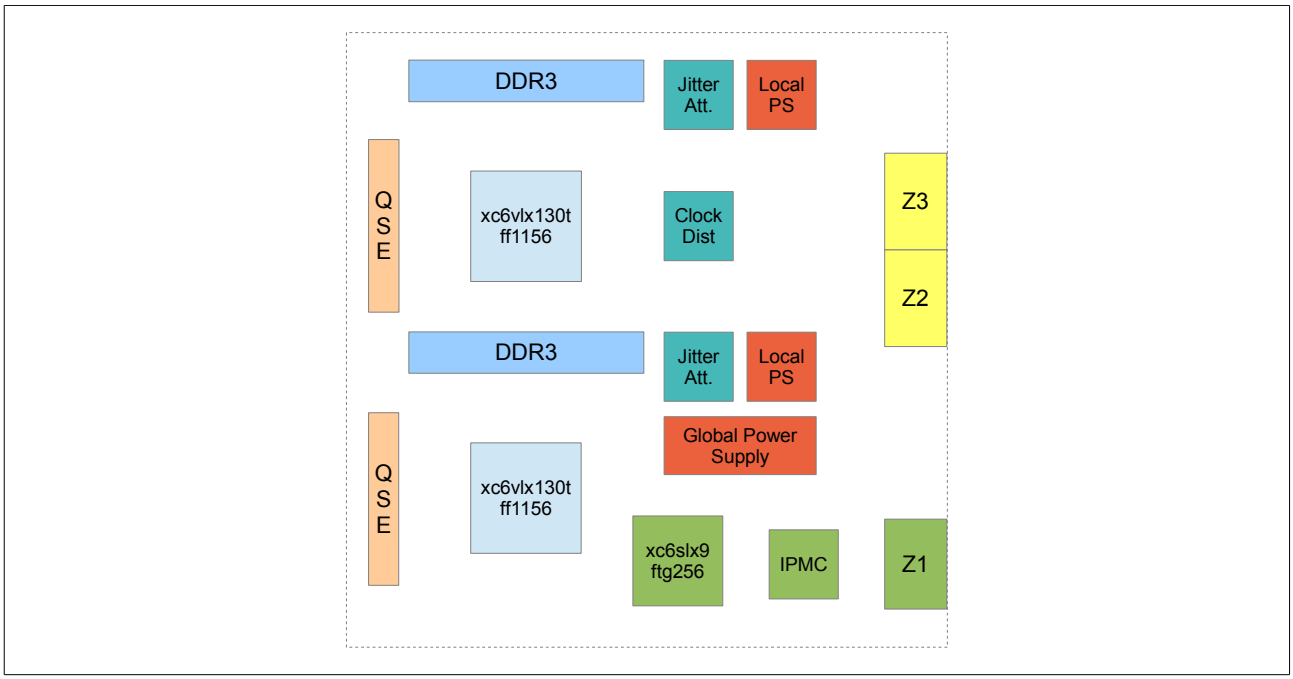

Figure 2. Main components of the board

1.2. Management

To fully accommodate management features available in ATCA standard and allow clear separation between User part and System part, dedicated management part has been isolated. It consists of small Spartan 6 family FPGA (for peripheral management, JTAG chain configuration, power management) and IPMC extension slot, which can be used for additional module, which implements communication with shelf manager. The layout of configuration components is presented in Figure 3. The functionality of this part can be accessed either via IPMC module or dedicated USB connector on the front panel.

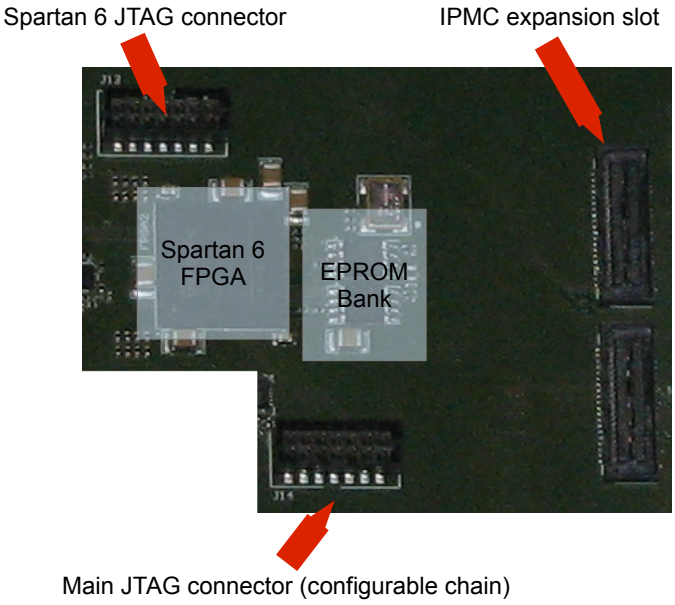

Figure 3. PCB layout of management components

The full block diagram with interfaces among different parts is presented in Figure 4.

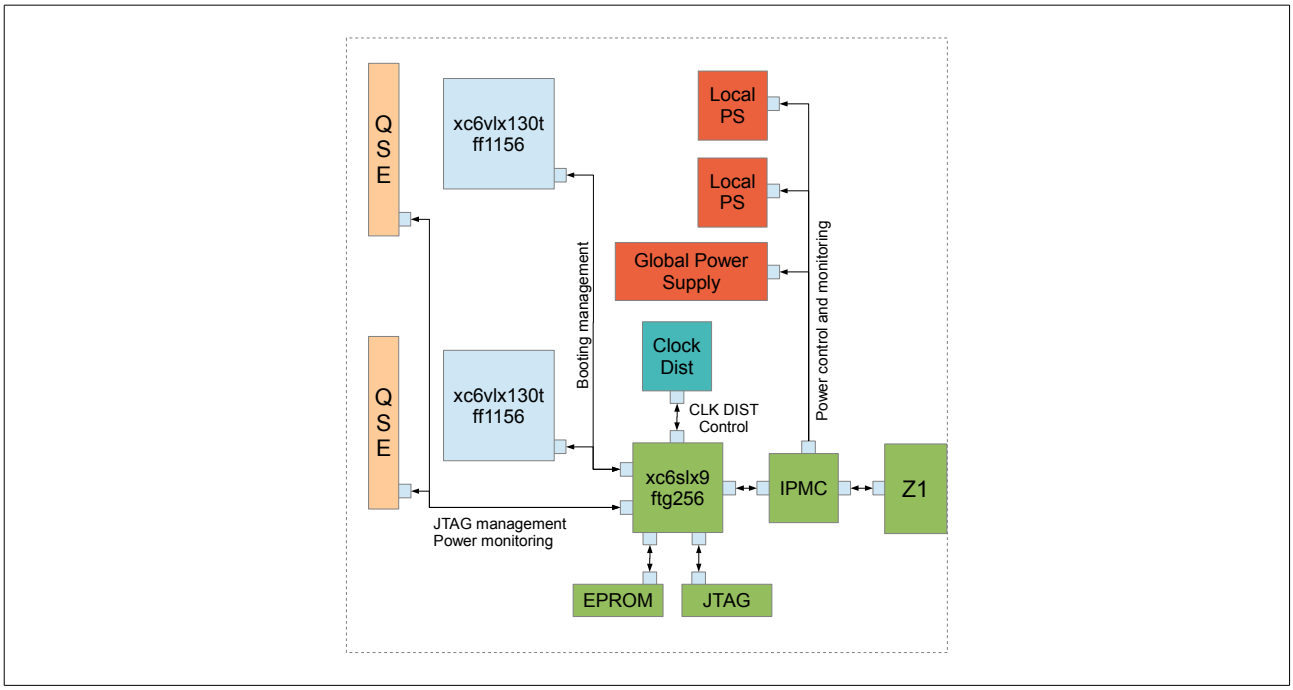

Figure 4. Block diagram of configuration part

1.2.1 JTAG chain configuration

Spartan 6 acts like JTAG switch. It allows to include JTAG capable components to be accessible in a single chain available via main JTAG connector. The possible endpoints for JTAG chain are presented in Table 2.. Each of them can be included independently.

Endpoint name	Description
Virtex 6 Channel A	JTAG interface of Virtex 6 Chip A and B
Virtex 6 Channel B	
Mezzanine Channel A	JTAG interface forwarded to Mezzanine Card A and B. Can be used for JTAG enabled devices placed on Mezzanine.
Mezzaniane Channel B	
ZONE 3	JTAG interface forwarded to Zone 3 connector. Can be used for JTAG enabled devices placed on RTMs.
Main JTAG connector	Min JTAG connector for external programmer conection

Table 2. JTAG enpoints

JTAG interfaces on the board consists of 4 lines – TDI,TDO,TCK,TMS. In addition to Main JTAG connector, the board is also equipped with Spartan 6 dedicated connector and W25Q64FV EPROM to store configuration part firmware. The size of the EPROM is sufficient for multiple firmware revisions.

1.2.2 EPROM management

The board is equipped with 4 W25Q64FV serial EPROMs, which are connected to Spartan 6 chip. Their control lines can be forwarded to any of Virtex 6 chips using booting management interface. This allows easy firmware version

management. The lines of booting management interface are presented in Table 3.

Name	Description
DONE PROG_B INIT_B	Configuration pins of Virtex 6 chips responsible for reset, configuration init and status monitoring.
CCLK DIN MOSI FCS_B	Serial EPROM interface of Virtex 6 chip. It can be used to multiplex eprom connections from EPROM bank. Configuration can be triggered using PROG_B pin.
CHANNEL_INDEX	Dedicated pin, which indicates channel index for Virtex 6 chip. It can be used if firmware for individual parts must be aware of its location. By default this pin is fixed to '0' for channel A and '1' for channel 'B'.

Table 3. Booting management interface

1.2.3 Power supply management

The IPMC part of configuration subsystem is responsible for power management. It is accomplished via dedicated PMBUS interfaces to each supply and set of I2C IO expanders for Enable and Status monitoring. This functionality can be monitored/accessed via Shelf Manager interface or 8-bit parallel bus to Spartan 6.

NOTE: If the IPMC module is missing, all the power supplies are on by default.

1.2.4 Other functions

The configuration parts performs some other functions such us Clock Distribution config, Gigabit links multiplexing etc. The description will be covered by the appropriate sections.

1.3. Clock distribution

Clock distribution sub-circuits provide clock signals to all on-board peripherals. The general block diagram is presented in Figure 5. The configuration of individual clock components is set via Spartan 6 chip. LMK03200 is using 3 wire serial interface for clock configuration. For detailed description of protocol and address space please refer to vendor's datasheet. Other components such as input clock multiplexer can be controlled using parallel pin to pin interface.

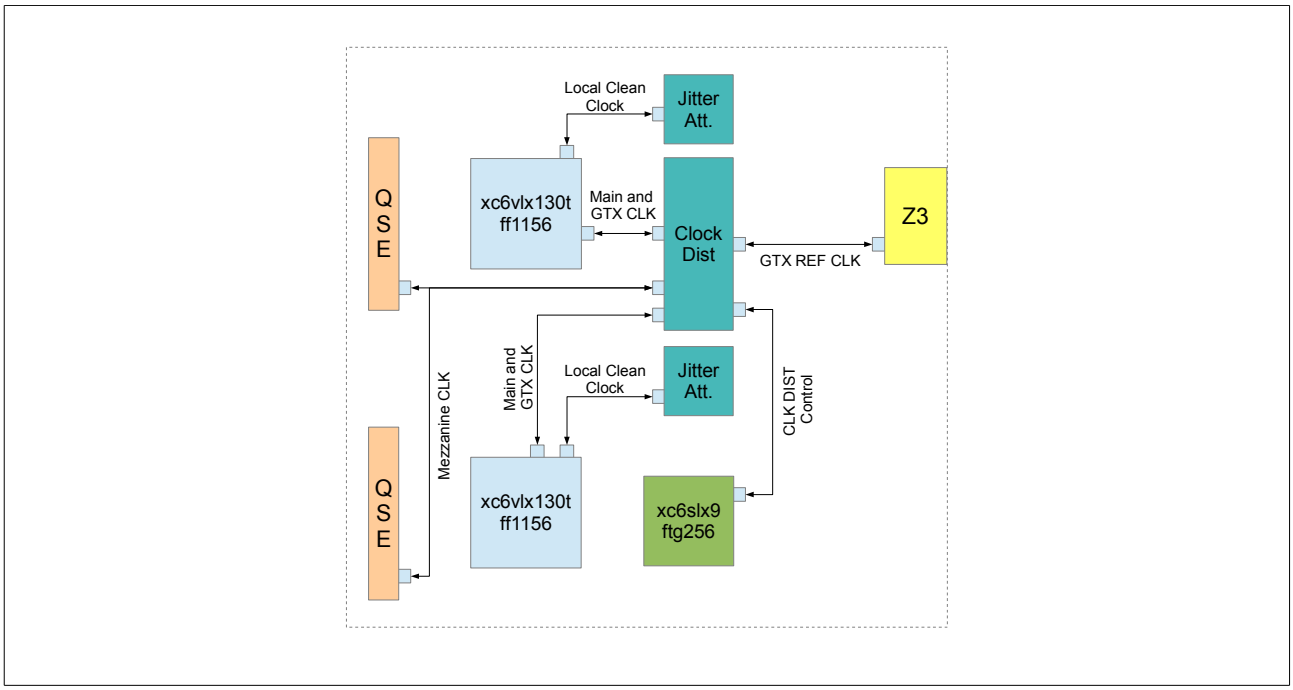

Figure 5. Block diagram of Clock Distribution subsystem

1.3.1 Mapping of LMK03200 outputs

The main component of clock distribution is LMK03200 chip. It is equipped with 8 outputs, which are distributed to different components. The description of each output is presented in Table 4. The chip can be sourced from local oscillator or 2 external RTM clocks. GTX clocks are connected to dedicated FPGA A and B pins.

N	Description
0	Mezzanine A clock
1	Mezzanine B clock
2	RESERVED
3	FPGA A clock
4	FPGA B clock
5	GTX clock for RTM – the clock is provided to FPGA A, FPGA B and Zone 3 connector
6	GTX clock A. The clock is provided to FPGA A and Mezzanine A
7	GTX clock B. The clock is provided to FPGA B and Mezzanine B

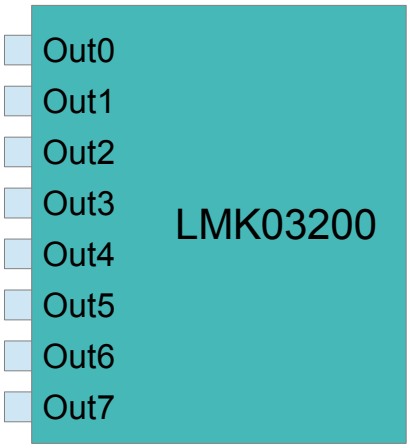

Table 4. Mapping of LMK03200 outputs

1.3.2 Local clock cleaner

In addition to global clock distribution, each channel is equipped with LMK03200 chip, which can be used to process FPGA generated clock. Full control set and clocks are connected directly to User FPGAs.

1.4. Power supplies

The main power supply voltage provided in ATCA standard is -48V. It must be converted to the levels which can be used by all ICs present on the board. The main power converter responsible for conversion from -48V to 12V is ATCR250. Further stages of power distribution convert 12V into voltages sufficient for various ICs. The power supplies are controlled by IPMC module if present. Otherwise they are enabled by default.

1.4.1 Global supply

Global supply voltage part provide commonly used voltages. It is based on switching converters. The structure and description is presented in Table 5.

Voltage [V]	Description
1.2	Supply for Config Part. Provided to mezzanine connectors
2.5	Supply for Config part, Virtex 6 IO banks and mezzanine connectors
3.3	Supply for Config Part, Clock Distribution and mezzanine connectors

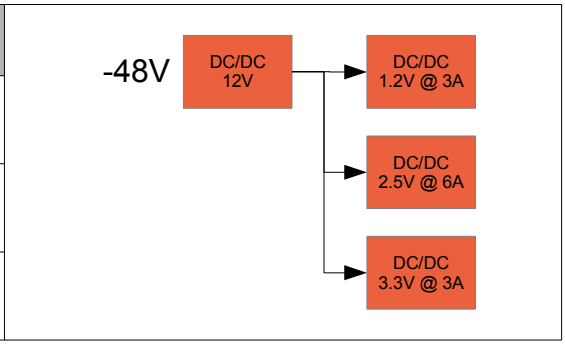

Table 5. Structure of Global Power Supplies

1.4.2 Local Supply

Local supply distribution provides dedicated voltages separately for devices in Channel A and B. it is based on switching converters and LDOs. The structure and description of individual voltages is presented in Table 6.

Voltage [V]	Description
1.0	VCCINT supply for Virtex 6
2.5	VCCAUX supply for Virtex 6
1.5	SODIMM supply and IO banks of Virtex 6
0.75	DDR3 termination voltage
1.0	GTX power supplies.
1.2	

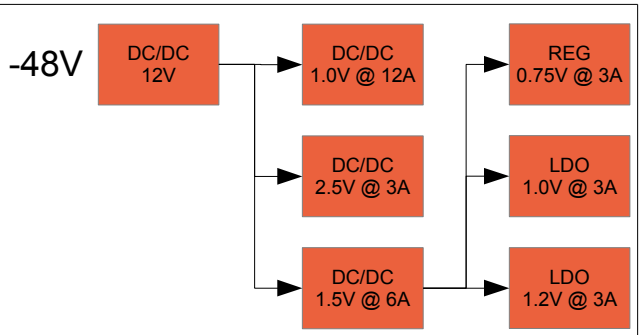

Table 6. Structure of Local Power Supplies

1.5. User FPGA

The main FPGA for each channel is Virtex 6 **xc6vlx130T** chip. The logic resources available for user firmware are presented in Table 7.

Type	Count
Logic Cells	128000
FlipFlops	160000
Look Up tables	80000
GTX	20
User IO	600
DSP slices	480

Table 7. Resource available in xc6vlx130T

The memory slot (SODIMM slot) can accommodate wide range of DDR3 SODIMM pluggable memories (single rank recommended). Such approach allows to match memory resources to the application needs. The board is delivered with 1 GB memory card from Kingston. The following chapters present user available interfaces for the FPGA necessary for custom firmware implementation.

1.5.1 General IO diagram

User FPGA is equipped with 600 user IO. Most of them has been used to interface with different subsystems. Due to component placement on PCB the following IO bank layout has been used.

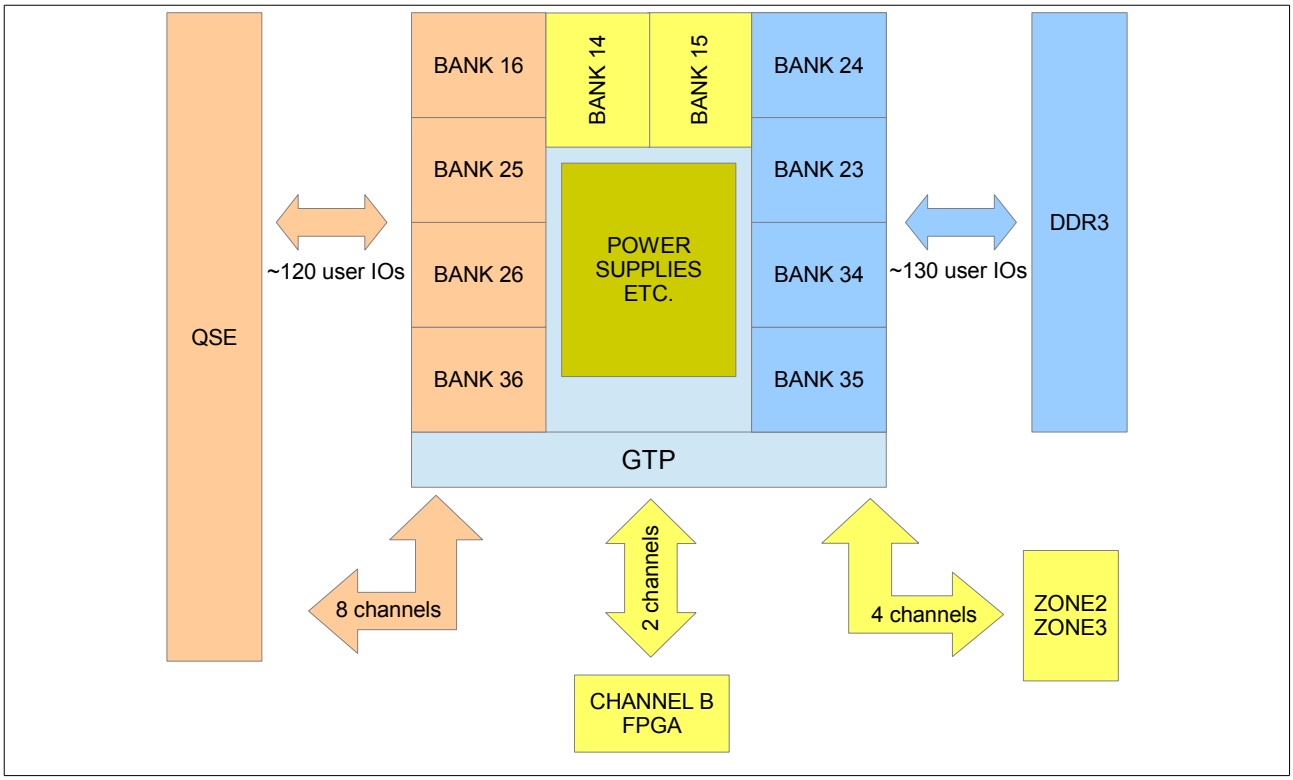

Figure 6. IO pin layout for user FPGA

The Figure 7. presents allocation of GTX links for each channel. All MUX/DEMUX are controlled from config part.

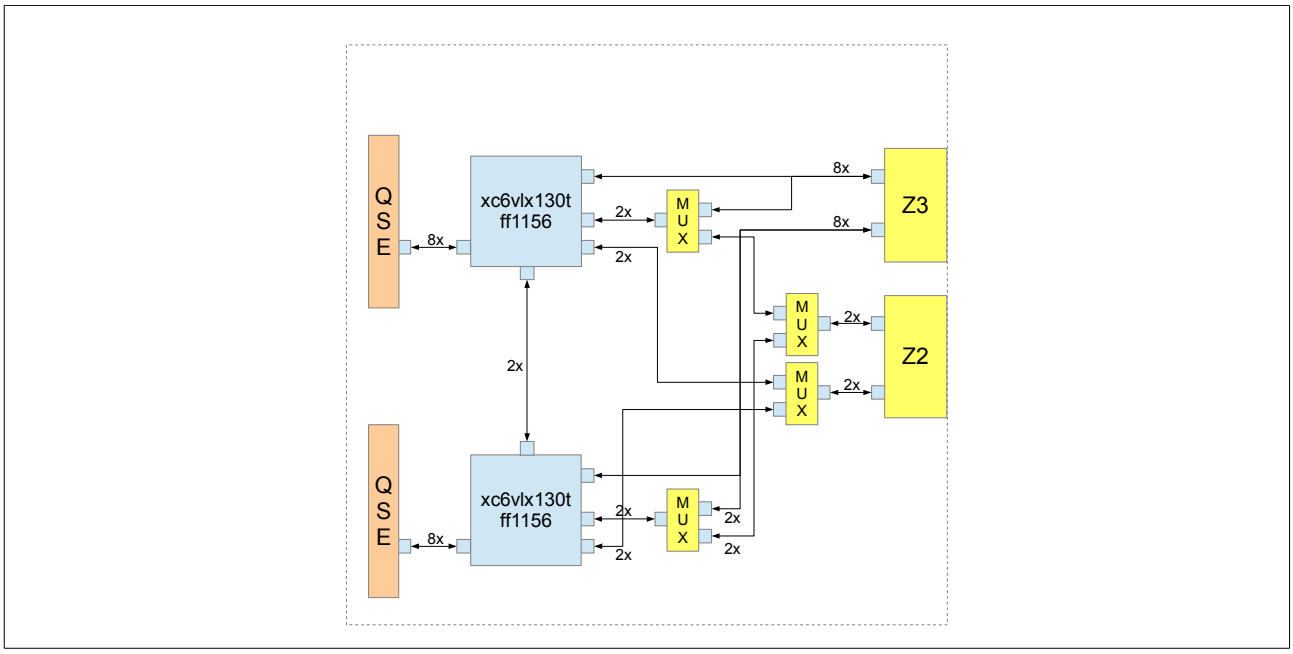

Figure 7. GTX allocation for A and B FPGAs

1.5.2 Mezzanine interface

The User FPGA is connected to custom mezzanine slot for extension modules. The main interface is dedicated for source synchronous transmission and is extended with additional GTX pairs, slow single ended lines and clock resources. It is presented in Table 8.

Name	Number of Pins	Description
BYTE interface	5x 10 diff pairs	Each byte consists of 8 data lines, data mask line and data strobe line. Data lines are connected to normal user IO and mask/strobe signals are connected to CC pins.
SLOW Interface	16 single ended	16 single ended lines dedicated for slow controls
GTX Interface	8 diff pairs	Connection to user FPGA GTX lines
CONFIG Interface		Interface to Configuration Subsystem for management
ADC CLK	1 diff pair	Main clock from clock distribution
GTX CLK	1 diff pair	GTX clock from clock distribution

Table 8. Mezzanine interface groups

The details on exact pin assignment are available in UCF section.

1.5.3 DDR3 interface

The main FPGA is connected to SODIMM slot, so the memory extension cards can be used. The slot is presented in Figure 8.

Figure 8. On-Board SODIMM Slot

The pin-out for the interface has been generated using Xilinx MIG tools. Dedicated work frequency is 400 MHz (maximum frequency for Speed Grade -1 FPGA). All tracks on the PCB has been equalized according to MIG requirements (+/- 5 ps for data groups, +/- 25 ps for control lines, +/- 100 ps between clock and data) and internal FPGA delays are not taken into account. The Table 9. presents SODIMM pin assignment.

FPGA Bank	Allocation
BANK 22	DDR3 control lines
BANK 23	BYTE0, BYTE1, BYTE2
BANK 32	BYTE3, BYTE4
BANK 33	BYTE5, BYTE6, BYTE7

Table 9. IO Bank allocation for DDR3 interface

The board is provide together with test firmware for the interface. Functionality can be verified using Chipscope Pro tool.

1.5.4 Zone 2 and Zone 3 interface

Zone 3 Interface is presented in Table 10.

Interface Name	Description
GTX	up to 16 lanes of GTX, 8 for Channel A and 8 for Channel B FPGA. General purpose interface to RTM devices. Please refer to GTX description Figure.
DTC	8 differential lines, 4 connected to A and 4 connected to B. Dedicated for DTC link implementation.

Table 10. Zone 3 Interface

Zone 2 interface can be used to implement back-plane communication between several carriers. It is presented in Table 11.

Interface Name	Description
GTX	up to 4 lanes of GTX connected to central slot. Depending on GTX MUX settings several configurations are possible: - 2 channels to A and 2 channels to B (Z3 interface has 16 GTX) - 4 channels to A or 4 channels to B (Z3 interface has 12 GTX)
FULL MESH	Additional interface implements full mesh connectivity on the back plane. Each back-plane channel consists of 8 diff pairs (4 connected to A and 4 connected to B). Total number of available slots is 13 so total width of interface is 104 diff pairs (52 to each channel)

Table 11. Zone 2 Interface

1.5.5 Inter-channel interface

The Channel A and Channel B user FPGAs are connected with inter-channel interface. Its layout is presented in Table 12. It allows to implement fast data interface for user defined purposes.

Name	Description
BYTE	10 diff lines dedicated for source synchronous transmission. Simillar to Mezzanine interface byte. It contains 8 dedicated data lines (connected to normal user IO), data mask and data strobe (connected to CC pins).
GTX	In addition to BYTE interface two lanes of GTX Quad 114 are connected P2P between FPGAs. They can be used to implement any GTX supported protocol.

Table 12. Inter-channel interface

1.5.6 Interface to Config subsystem

The user FPGA interfaces with config subsystem using 8 bit parallel bus. It consists of 8 differential pairs – one of them is connected to CC pin. It could be used as trigger distribution lines, general comm interface with config part, etc. In the current firmware revision it is not used.

2. Board Configuration

For proper operation of the board, the most recent system firmware should be loaded into configuration eprom. The board offers several interfaces to accomplish this task. The user manual will focus on JTAG configuration – this is only option if system eprom is not programmed. After initial programming also other interfaces can be used.

2.1. Firmware downloading

The board is provided with System FPGA firmware and basic firmware blocks for User FPGA, which allow to run basic tests for individual functional blocks. They allow to test clock distribution, memory, gigabit interfaces, data acquisition, etc. The firmware will be extended on demand and can be used as a base for user implementations.

2.1.1 JTAG interface for System FPGA

After connecting Xilinx JTAG cable Xilinx IMPACT tool can be used to detect devices in current JTAG chain. Figure 9. Presents layout of the chain – FPGA detected is Spartan 6 (xc6slx9) together with SPI eprom. All programming files can be assigned to devices and programmed using GUI interface functions.

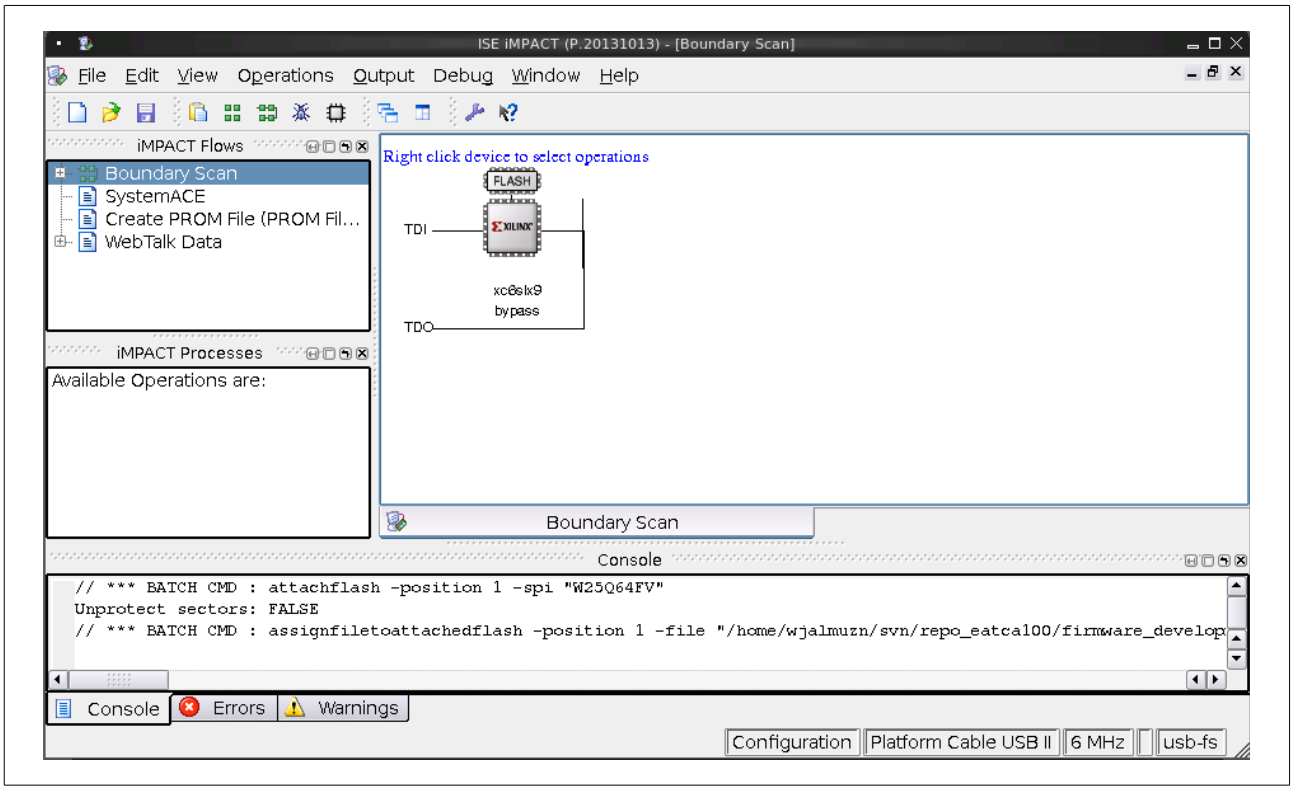

Figure 9. Xilinx IMPACT boundary scan configuration for System FPGAs

2.1.2 JTAG interface for User FPGAs

When System FPGA firmware is loaded into Spartan 6 FPGA, the second JTAG chain becomes active. Xilinx JTAG cable mus be reconnected to second JTAG socket and chain scan must be performed again. The process is presented in Figure 10. Both User FPGAs are visible and can be programmed with assigned firmware files.

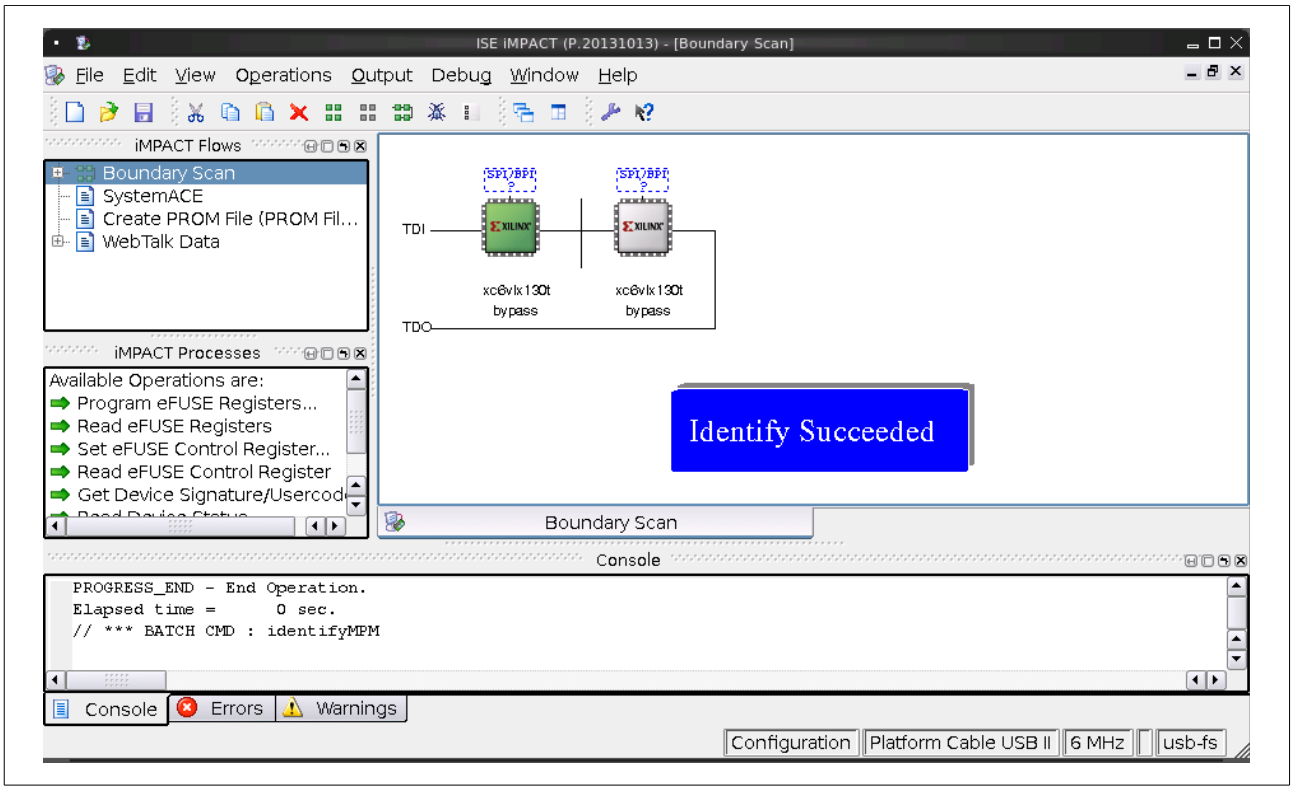

Figure 10. Xilinx IMPACT boundary scan configuration for user FPGAs

2.1.3 USB interface

The functionality will be updated in the next firmware revision. It will allow to program user FPGAs and make firmware update for system FPGA with single PC running application using USB interface.

3. Safety Instructions

1. Please read these safety instructions carefully.
2. Please keep this User's Manual for later reference.
3. One AC Inlets provided and service as Disconnect Devices, disconnect the equipment from both AC outlets use these AC Inlets before servicing or clearing. Use moisture sheet or cloth for cleaning.
4. For pluggable equipment, that the socket-outlet shall be installed near the equipment and shall be easily accessible.
5. Please keep this equipment from humidity.
6. Lay this equipment on a reliable surface when install. A drop or fall could cause injury.
7. Make sure the voltage of the power source when connect the equipment to the power outlet.
8. Place the power cord such a way that people can not step on it. Do not place anything over the power cord.
9. All cautions and warnings on the equipment should be noted.
10. If the equipment is not use for long time, disconnect the equipment from mains to avoid being damaged by transient overvoltage.
11. Never pour any liquid into openings; this could cause fire or electrical shock.
12. Never open the equipment. For safety reason, the equipment should only be opened by qualified service personnel.
13. If one of the following situations arises, get the equipment checked by a service personnel:
    a) The Power cord or plug is damaged.
    b) Liquid has penetrated into the equipment.
    c) The equipment has been exposed to moisture.
    d) The equipment has not work well or you can not get it work according to user's manual.
    e) The equipment has dropped and damaged.
    f) If the equipment has obvious sign of breakage.
14. The equipment can be operated at an ambient temperature of 55°C.

4. Getting Service

Contact us should you require any service or assistance.

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5. Change log

REV	DATE	COMMENT
1.0	25.03.2014	Initial revision of documentation

NOTES

APPENDIX LIST

1. Spartan 6 firmware
2. Virtex 6 firmware
3. Board schematics