Specifications and Implementation of an ART ASIC prototype for the MicroMegas Trigger system of the NSW Detector

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1. Overview of the ART ASIC Specifications [1]

The scheme for readout of trigger data for the MicroMegas detector in NSW is shown in the block diagram in Figure 1.

For the Micromegas detector, the trigger data is generated by considering only the first arriving hit in each 64-channel front-end IC for a given bunch crossing. The strip address of the hit (Address-in-Real-Time) is promptly produced by the VMM chip in serial form.

The Address-in-Real-Time words generated by the front-end ASIC (VMM) are sent to the trigger processor in USA15 via optical links in two steps. First, the ART from each of 32 front-end VMMs (four MMFE's) is serially transmitted, point-to-point, to a companion digital ASIC on the trigger data driver card; from there it is sent to USA15. The ASIC performs the following functions:

- Deserialize the ART stream and phase-align the hits to the BC clock.
- Identify the strip addresses of up to a fixed number of hits by means of cascaded priority encoders.
- Append the 5-bit geographical VMM ASIC address to the strip address of each hit.
- Send the ART addresses and the 12-bit BCID to a GBT configured to operate in parallel mode without Forward Error Correction (FEC).

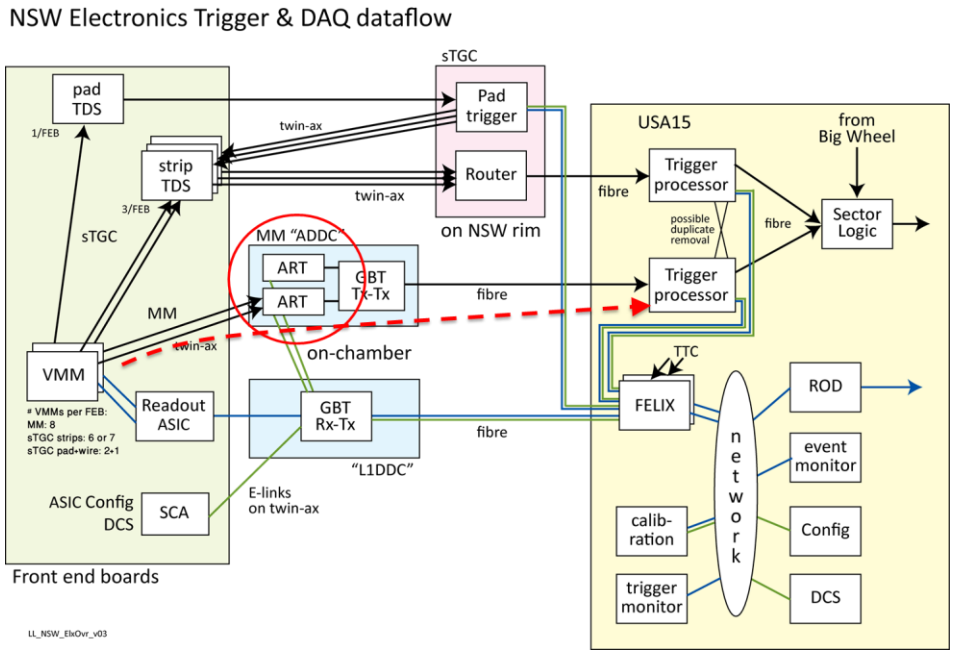

Figure 1. Block diagram of the Trigger and DAQ NSW electronics. The MicroMegas trigger path is designated with the red dotted arrow. The ART ASICs (red circle) are collecting trigger data (Address in Real Time) from the front-end VMM ASIC and formatting the output to the GBT chip. The information travels on fibers up to the Trigger Processors located in USA15.

There are a total of 512 ART data driver cards. Using the dual Versatile Transmitter (VTTx) significantly reduces the cost per link. The absence of the downlink, however, requires that the ART ASIC receive its TTC and clock signals from the Level-1 event readout downlink and that the ART GBT transmitter also be configured via that downlink.

2. Theory of Operation

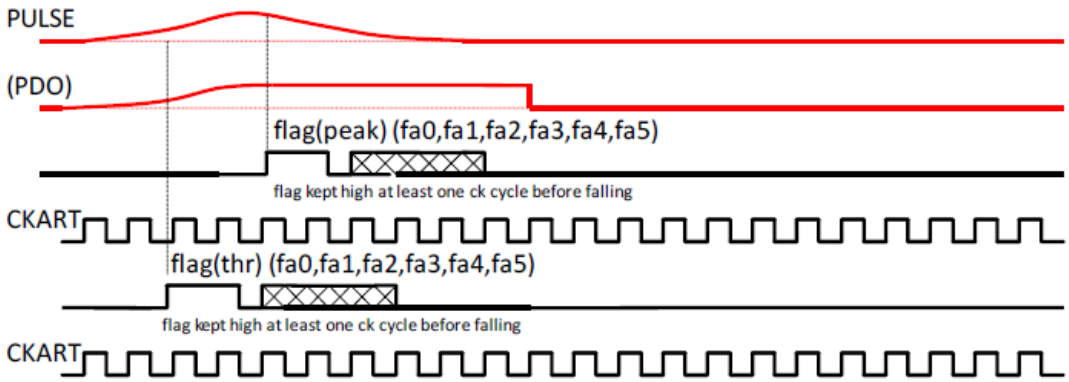

Figure 2. The ART signal [2]

The ART signal generated by the VMM front-end ASIC (figure 2) consists of a flag pulse, followed by 6 bits which indicate the address of the strip that received a hit. The internal circuitry of the VMM selects always the first channel that was hit, when more channels receive a signal nearly at the same time. The ART circuit is triggered either by the threshold crossing of the strip signal or by the peak detection circuit. For minimum latency, the threshold crossing will be used in the experiment. In DDR mode, the flag is high for two falling edges of the 160 MHz clock and kept low until the next rising edge of the clock. The 6 address bits are then serialized on each edge of the clock. Following the ART address, the ART circuit is internally reset for approximatively 10ns.

For the purpose of this discussion, a simplified version of the ART signal is shown in Figure 3, where the flag is reduced to a single bit of the 160 MHz DDR stream which is immediately followed by the 6 ART address bits. Since this signal is triggered asynchronously, the start of the ART signal may appear at any 160 MHz DDR tick, inside the 40 MHz BC clock window (see Figure 3).

The ART ASIC will register all ART signals coming anywhere inside one BC window. In Figure 3 the boundary between BC windows is represented by blue lines. The ART ASIC looks initially at the presence of flags. All ART flags which occurred in the 25 ns time window between time 0 and time 1 are therefore known at time (1). The ASIC can perform the selection of the hits immediately, even before some of the ART signals have completed (i.e. some of the 6 ART data bits are still flowing out of the VMM chips). Half BC is reserved for the hit selection operation. At time 1.5 (half BC time later) the hit selection is performed and the result is presented on the output bus. If there are more than 8 VMMs issuing ART signals in the same BC window, the ART ASIC will select only the 8 of them, based on a priority scheme which is detailed later.

At time (2) all the bits of the ART addresses are recorded and can be presented at the output. Therefore the ART ASIC generates the data to the GBT chip in two steps, at time (1.5) and time (2), corresponding to the 80Mbps transfer mode.

As it will be detailed in the following chapter, simulations performed for worst case of the technology showed that the hit selection operation can be performed in about 3-4 ns, which is considerably shorter than the 0.5 BC. Despite that, the latency cannot be shortened further because the deserialization step might not be completed in time for signals which burst at the very end of the BC window.

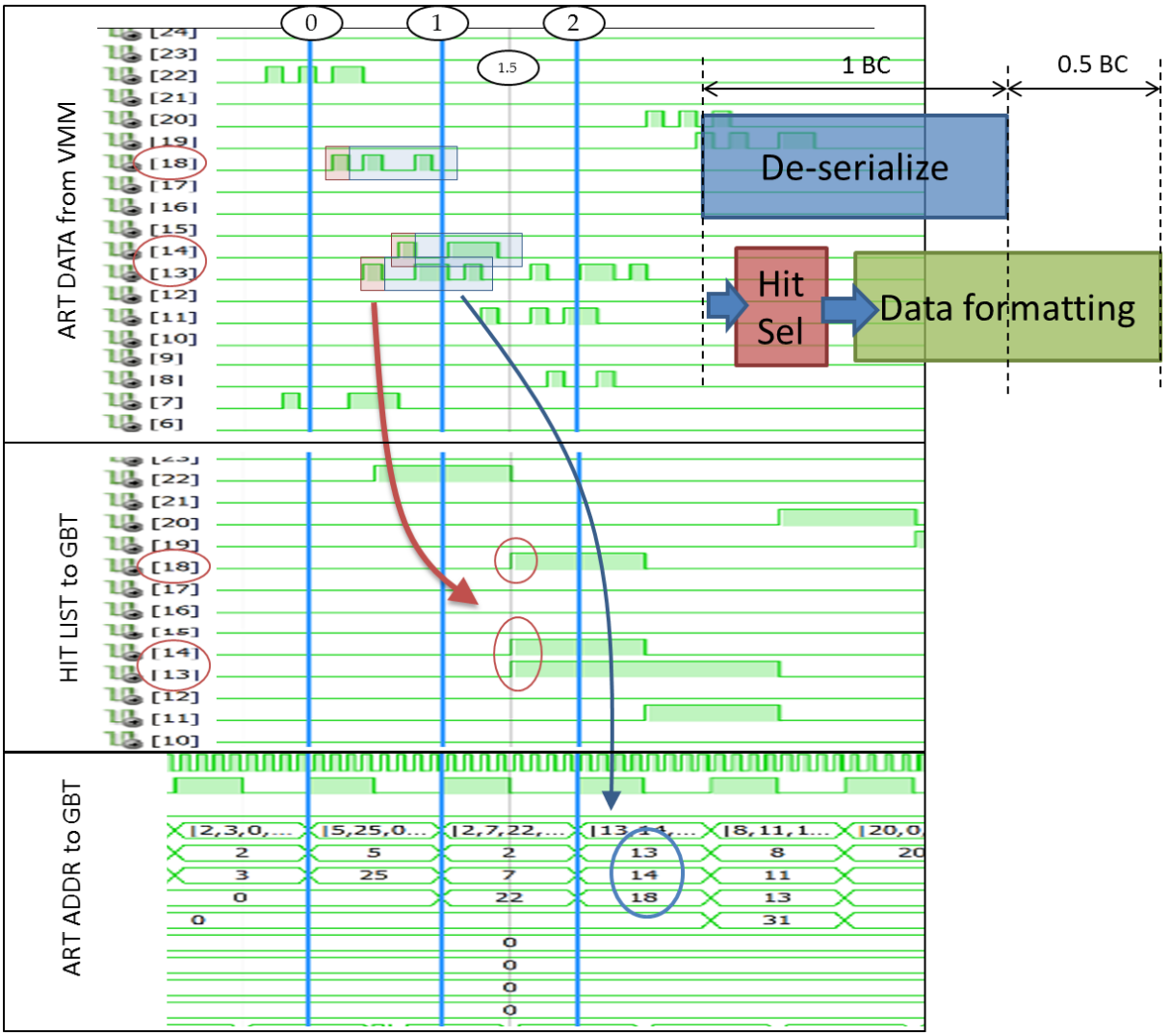

Figure 3. Theory of operation of the ART ASIC. Hit selection (red) is performed in parallel with ART data de-serialization (blue).

For transfer rates of 160 or 320 Mbps, the data flow to the GBT will be segmented in 4 or 8 steps (see Figure 4). This gives the possibility to lower further the latency by segmenting the data such that the information which is available earlier (i.e. first bits of the ART address) is serialized first. In this way, the data can be transferred to the GBTx while ART is still de-serializing the ART stream. For example, in 320Mbps mode, the Hit Selection operation presumably takes one 160 MHz DDR tick (3.125 ns) and it is immediately followed by the transfer of the hit information, which takes 4 ticks. By the time this transfer ends, the de-serialization of the ART data is half way completed, therefore first bits of each of the 8 ART addresses are already available for transfer.

Taking into account the time at which the GBTx registers the data from the ART ASIC, in 160Mbps and 320Mbps modes, the latency can be shortened by 0.5 BC and 0.75 BC, respectively, compared to the 80Mbps mode.

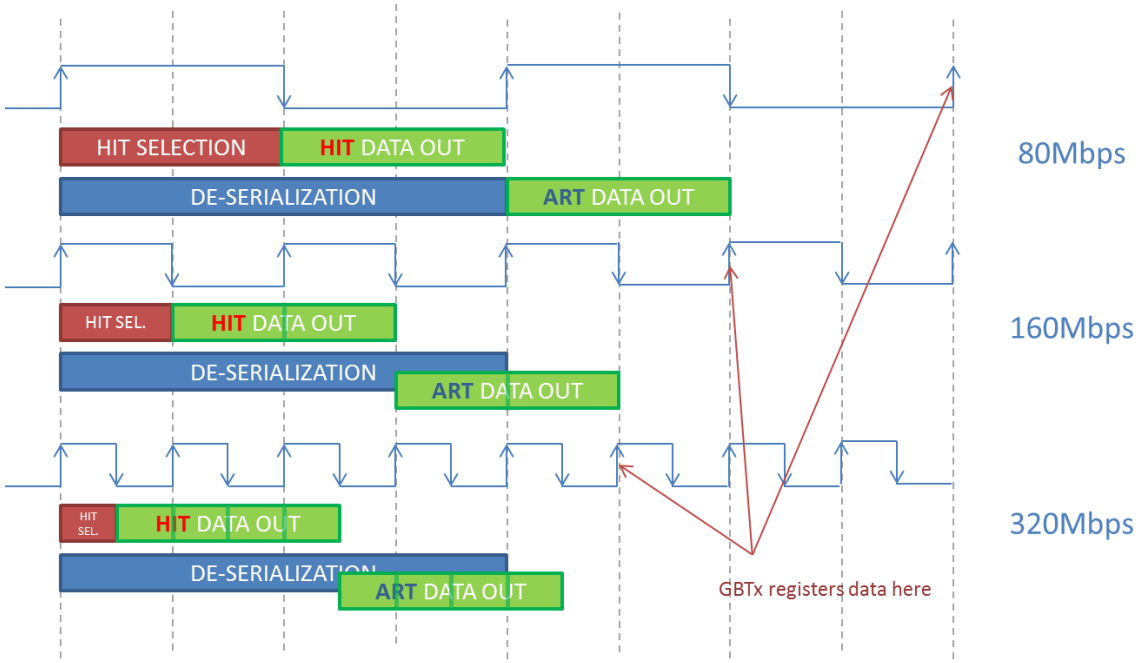

Figure 4. Optimal latency for the three possible output data rates

The implementation of the ART ASIC will target the use of 320 Mbps mode. This will give the best performance results while minimizing the number of pads. Considering all corners and worst conditions, the Hit Selection will probably not meet the optimal 3 ns propagation delay, therefore the latency of the ART ASIC will be limited to 1.25 BC.

3. ART ASIC Architecture and Detailed Specifications

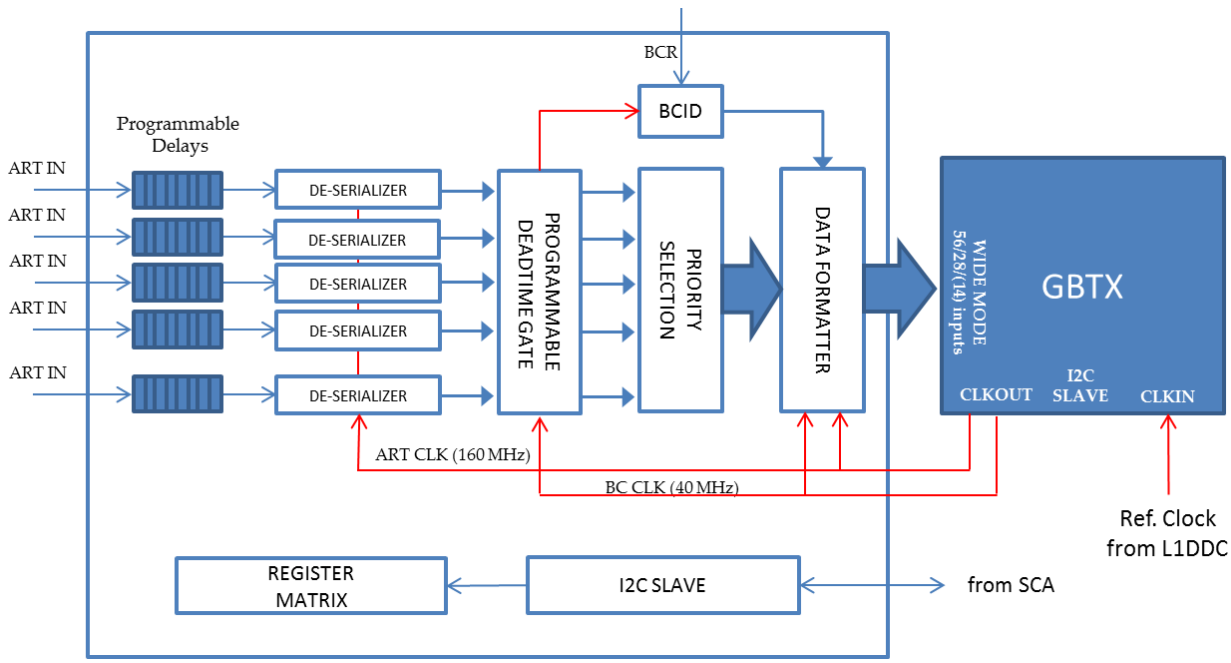

Figure 5. Architecture of the first ART ASIC

3.1. Programmable Delays

The purpose of the Programmable Delay block is to be able to skew the input signals to avoid setup or hold violations on the local clock phase, and adjust the ART stream to the correct clock phase. The preferred option is to use the CERN's DLL-based Phase Aligner IP core [3] which will eliminate the spread of the delay parameter with respect to process variations and operating conditions. The future VMM3 chip may integrate the option to register the entire ART signal to the 160 MHz ART clock. In this case, the automatic phase adjustment mode of the Phase Aligner core can be used, which does not require any user interaction.

The PhaseAligner IP has 8 data lines (Figure 6), therefore 4 cores are needed for the 32 ART inputs of the ASIC.

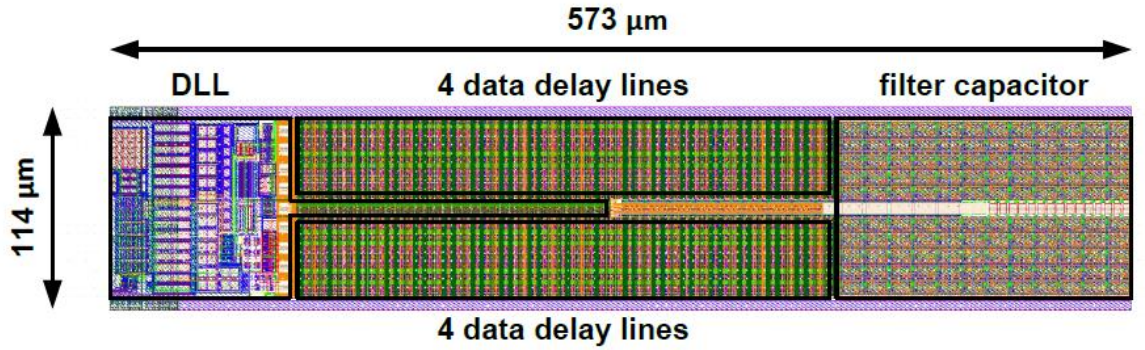

Figure 6. Layout of the CERN PhaseAligner IP [3].

3.2. ART De-serializer Circuit

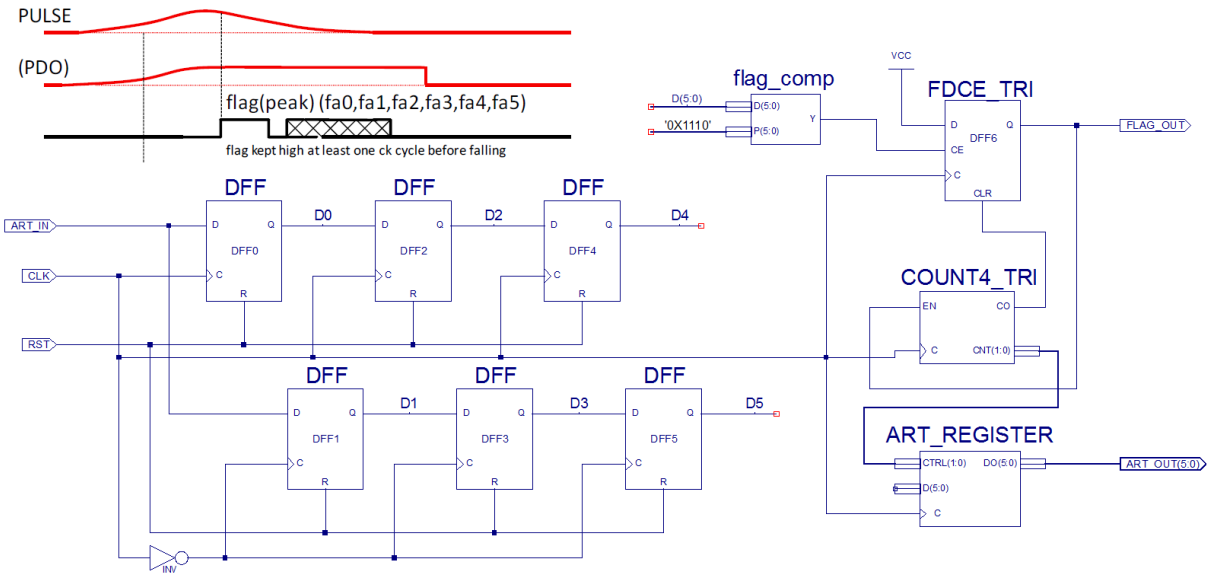

Figure 7. Schematic view of the ART de-serializer.

A schematic view of the ART de-serializer circuit is given in Figure 7. Flip-flops DFF0 to DFF5 form a DDR shift register which de-serialize the incoming data stream. In DDR mode, the flag pulse is kept high through the next two falling edges of the 160MHz CKART clock, being lowered by the

second falling edge. The first ART data bit is streamed at the following rising edge of CKART. The comparator *flag_comp* searches for the "0X1110" pattern[1] which indicate the presence of a flag pulse. A control flip-flop (DFF6) is triggered and kept high for 4 clock cycles (25ns) by a 2 bit counter (*COUNT4_TRI*). This signal is supplied to the hit selection circuitry which registers it on the 40 MHz BC clock domain.

The 2 bit counter also controls the output latches of the de-serializer circuit (*ART_REGISTERS)* to extract the 6 bit ART data from the DDR shift register at the appropriate moments. The circuit also calculates a parity bit which is transmitted to the GBTx chip together with the ART data (the parity circuit is not shown in Figure 7).

The search "0X1110" or "001110" pattern is not unique, i.e there are two(one) ART data symbols which may trigger a false flag, but this may happen only if the VMM sends ART signals while the ART ASIC is not alive (i.e in reset phase). In practice, the VMMs can be enabled only after the all ART ASICs were configured and running. In case of a spurious reset of the ART ASIC, the probability to signal the flag on the wrong pattern is less than 1/32[2]. The faulty locking is not permanent, the subsequent ART signal will be correctly detected.

Note. *If one more register is added to the DDR Shift Register circuit, a 7-bit search pattern can be used ("00X1110" or "0001110") which removes the ambiguity.*

The FDCE_TRI and COUNT4_TRI are forming the control logic of the circuit and are therefore triplicated. The other registers belong to the data path and do not need triplication. The parity error may be generated due to a SEU.

3.3. Programmable Deadtime

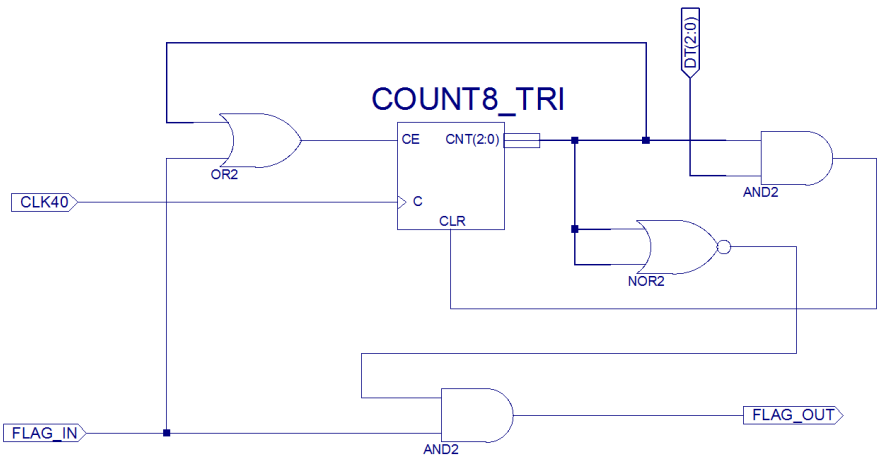

Figure 8. Schematic view of one channel of the Programmable Deadtime circuit.

This block creates an artificial deadtime for each VMM channel which is controllable via configuration. Subsequent data on a particular channel is ignored for a number between 0 and 7 BCs.

The block consists of a 3-bit counter which is triggered by the flag output of the deserializer circuit of the corresponding channel and operates on the 40 MHz BC clock (see Figure 8). The counter

[1] "X" indicates a don't care bit. The flag signal is raised asynchronously to the ART clock, therefore the rising edge of the signal may be registered on any clock edge. If the flag signal is registered at the falling clock edge internally by the VMM, this bit is replaced by a "0".

[2] In case the rise of the flag pulse is registered by the VMM chip and the "001110" pattern is used, the probability is less than 1/64.

counts up to the programmable value then is reset to 0. Counting is not resumed until the next flag signal. The channel is gated during the time the counter value is different than 0.

In the rare event of a radiation induced SEU, the circuit may introduce a spurious deadtime window extend a deadtime window which is in progress. Triplication may be needed to avoid spurious triggering of the deadtime counters.

3.4. Hit selection circuit

A few possible models for the hit selection circuitry where evaluated. The best results were obtained with the Hit selection circuit based on cascaded priority encoders as shown in figure 4. The first priority encoder will select the first ART flag (i.e. the most significant bit which is not zero from the 32-bit ART flag word). The result expressed in one-hot 32-bit format is subtracted from the initial ART flag word, and the result is presented to the following stage. The second priority encoder will therefore select the second non-zero bit from the ART flag word. The operation is cascaded 8 times to select a maximum of 8 non-zero flags. The one-hot result of each stage can be or-ed together to result a 32-bit hit list of the selected hit flags. This 32-bit word describes unambiguously the information that is required to be passed to the trigger processor (i.e. the addresses of the VMMs who issued an ART signal).

If absolute address numbers for each VMM hit are required instead, binary decoders have to be implemented for each of the 8 outputs, and the sum of non-zero bits has to be computed and attached to the output stream. These operations may have an impact on the propagation delay parameter.

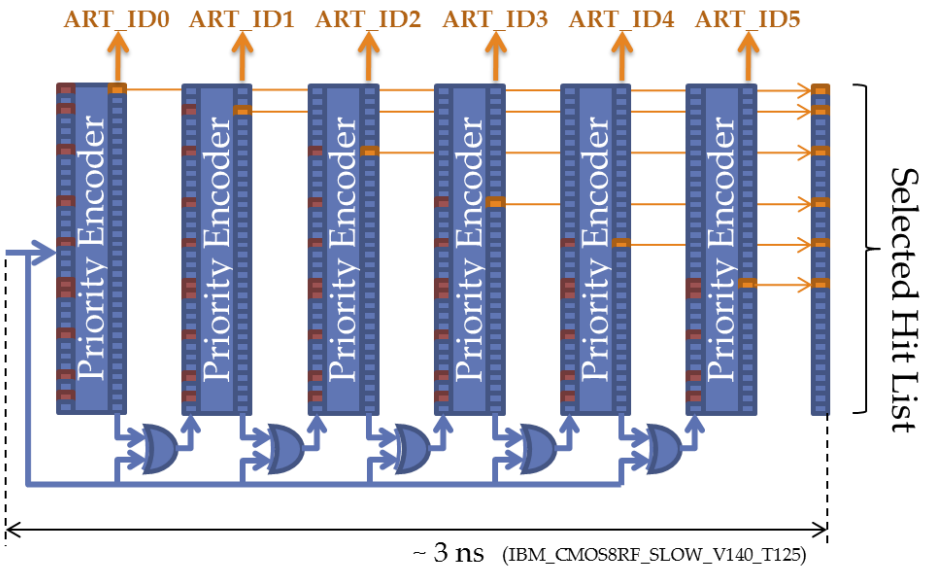

Figure 9. Hit selection circuitry based on priority encoders

3.5. Output Logic

The ART ASIC will transmit to the Trigger Processor the following information:

- Addresses of up to 8 VMM channels which had a hit in a particular BC
- The strip address of each of the 8 or less hits recovered from the ART stream (ART Data - Address-in Real-Time).
- 12 bit BCID for checking the synchronization.
- Other information (error flags, parity bits)

As it was described earlier, the information is transmitted to the GBtx chip in two steps. First, the selected VMM hit list is available (Hit Information), based on the flag bits issued by any of the 32 VMM chips at the input of the ASIC. Half BC later the corresponding ART Data is transmitted to the output, consisting of 8 x 6-bit strip addresses. The Wide Bus mode of the GBTx chip allows for 112 bits to be transmitted in a 25 ns (BC) window. 56 bits are allocated for each of the two transmission steps. For 160 and 320 Mbps modes, the 56 bits are segmented in 2 or 4 transfers, respectively, but the overall data segmentation into Hit Information and ART Data remains the same. The BCID

The Hit Information may be transmitted in two modes:

- Hit Map option consists of a 32-bits word where each bit corresponds to one of the 32 VMMs connected to the ART ASIC. All bits corresponding to the VMMs which were selected by the Hit Selection circuit in a given BC are set to “1”, while the others are kept low.
- Hit Address option identifies with a 5-bit number (VMM channel ID - 0..31) each VMMs which was selected by the priority. 8 x 5-bit addresses are transmitted at any given BC. Considering that the hit list is ordered, a value of 0 in other position than the first can indicate the end of list. An extra bit has to be used to signal the case where the list is empty.

In both cases, the 12-bit BCID is transmitted together with the Hit Information. The Hit Map option has 12 spare bits. These bits can be used to transmit a fixed word as frame delimiter (eg. “1010”). Other 8 bits may be used to transmit error flags from the core logic (i.e. error indicators from the 8 binary encoders attached to each priority encoder in the hit selection logic).

Optionally, the Hit Map may be unfiltered, carrying the hit or no hit information for all the 32 VMM connected to the ART ASIC. This mode may be useful for debugging spurious front-end activity. Only the first 8 hits will be have the ART address data transmitted.

The Hit Addresses option has 3 spare bits which can be used as frame indicator (i.e. “01”) and an error flag (ER).

Table 1. Output Data format

Hit Information Format:

Hit list	1	0	1	0	BCID[11:0]	ERR_FLAGS [7:0]	HIT_LIST[31:0]
Hit addresses	0	1	ER	EY	BCID[11:0]	8 x VMMID[4:0]	

ART DATA Format:

	8 x ARTDATA[5:0]	PARITY[7:0]

ER = Error flag
EY = Empty flag

For the second transfer step (i.e. corresponding to the falling edge of the BC clock), the 8 x 6-bit ART addresses use 48 bit, while the remaining 8 bits are used for parity bits computed by the deserialization logic. The implementation of the ASIC will target the 320 Mbps transfer mode. In order to take advantage of the optimum latency scheme possible in this transfer mode (see Section 2), the transfer of the ART Data fields is segmented such that the bits which arrive first at the ART ASIC are serialized first to the GBTx chip (Table 2).

Table 2. Segmentation of the ART Data transfer for optimum latency performance

Transfer #	1							2							3							4			
Ch #	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	PARITY
Bit Range	[0:1]	[0:1]	[0:1]	[0:1]	[0:1]	[0:1]	[0:1]	[0:1]	[2:3]	[2:3]	[2:3]	[2:3]	[2:3]	[2:3]	[2:3]	[2:3]	[4:5]	[4:5]	[4:5]	[4:5]	[4:5]	[4:5]	[4:5]	[4:5]	[0:7]

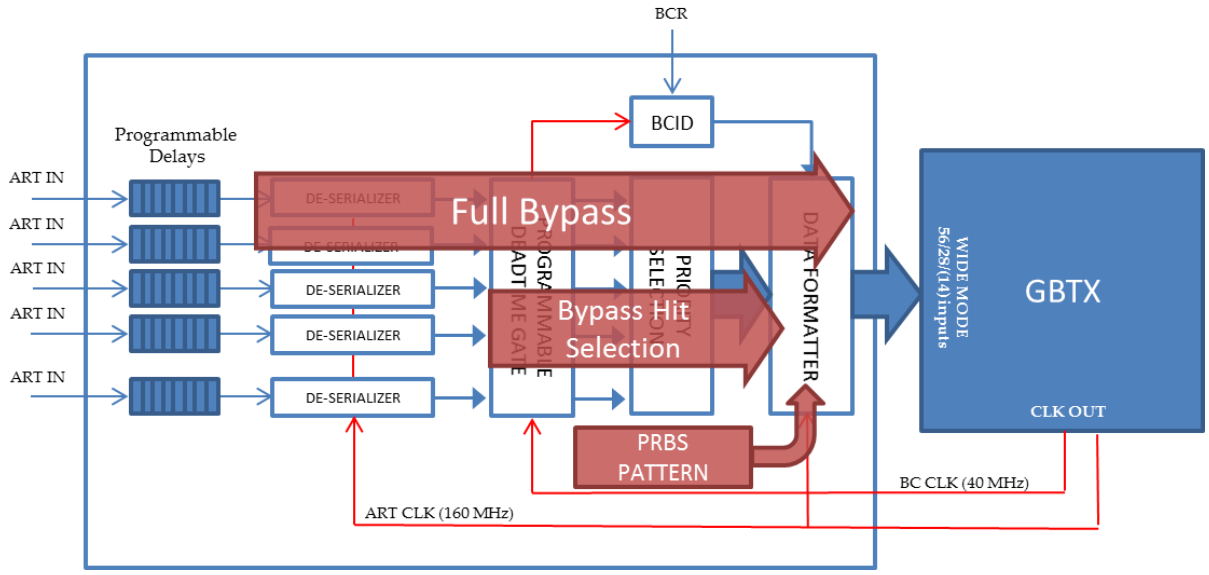

Figure 10. Bypass and test modes

Besides the normal operation modes, the ASIC will implement test modes where various parts of the system are bypassed or fixed or cyclic calibration data is transmitted to the GBTx chip. When possible, these test modes will be identified by different frame header patterns. The test modes are summarized below:

- Full bypass mode (direct connection of the output of programmable delays to the output pads of the ASIC).
    - This is used to verify and measure the propagation delay during ASIC initial verification and it is not accessible during normal operation of the ASIC.
- Bypass priority selection on ART data (debug mode)
    - Controlled by a configuration register, the input channels are connected directly to the output logic (8 channels at a time). Except for the frame header pattern, the output format is not altered. This mode can be used for in-system checking of the transmission between VMM chips and ART ASIC and setting the correct propagation delay of the Programmable Delays.
- Fixed output calibration pattern
    - A fixed pattern is sent continuously to the GBTx chip. The pattern is stored in local configuration registers and is accessible via the configuration path. Verification of the ART ASIC to GBT interface. This mode can be used for in-system geographical identification of individual ART ASICs.
- Cyclic output calibration pattern
    - Optional verification of the ART ASIC to GBT interface

3.6. I2C Slave and Register Matrix

All programmable parameters of the ART ASIC functionality are stored in a register bank. The register bank will be triple redundant and operate at slower speed (40MHz). The list of registers is given in Table 3.

The Register bank is accessed via an I2C Slave core. The slave is able write and read the values of individual registers. Also, the core gives read access to the delay setting of the Phase

Aligners when used in automatic mode or the SEU counters of the register bank. Special register access will perform Soft Reset of the ASIC or SEU counters.

Table 3. Programmable registers of the ART ASIC

Register Name	Functional Block	Description
INPUT_CTRL0..31	Inputs/Programmable delay	Individual VMM channel mask, polarity control, fixed delay value, automatic delay setting
SEARCH_PATT	DDR De-serializers	Global programmable search pattern for the flag pulse
DEADTIME	Programmable Deadtime	Global deadtime setting and enable
OUTPUT_CTRL	Output Logic	Controls the output modes and bypass modes
BYPASS_VMMSEL	Output Logic	In Hit Selection Bypass mode, the register controls which VMM channels are forced in the output format
OUTPUT_PATT	Output Logic	Fixed pattern for output calibration/identification
BCID_OFFSET	BCID Counter	Fixed offset loaded by BCID counter at BCR
BCID_RST_VAL	BCID Counter	Reset value for the BCID counter corresponding to the orbit time

Table 4. Read-only registers of the ART ASIC

Register Name	Functional Block	Description
DELAY_READ0..31	Programmable delay	Read back of the automatic programmable delay
SEU_COUNTER	Register Bank	Counter of SEU events in Register Bank
*VMM_COUNTER0..31**	-	Counts the number of flags registered for each VMM channel

*tbd

3.7. Clocking

The ART ASIC will have essentially use a single 160 MHz clock. A 40MHz clock input synchronous with the LHC clock will be used to gate faster clock for the blocks which operate at BC clock. The DDR de-serializers and output logic use directly the fast clock. The I2C core and register matrix will use directly the 40 MHz clock input.

Both clocks are supplied by the programmable clock manager of the GBTx chip which cleans and synthesizes via its internal PLL the reference clock supplied by the L1DDC card.

4. Configuration and Control

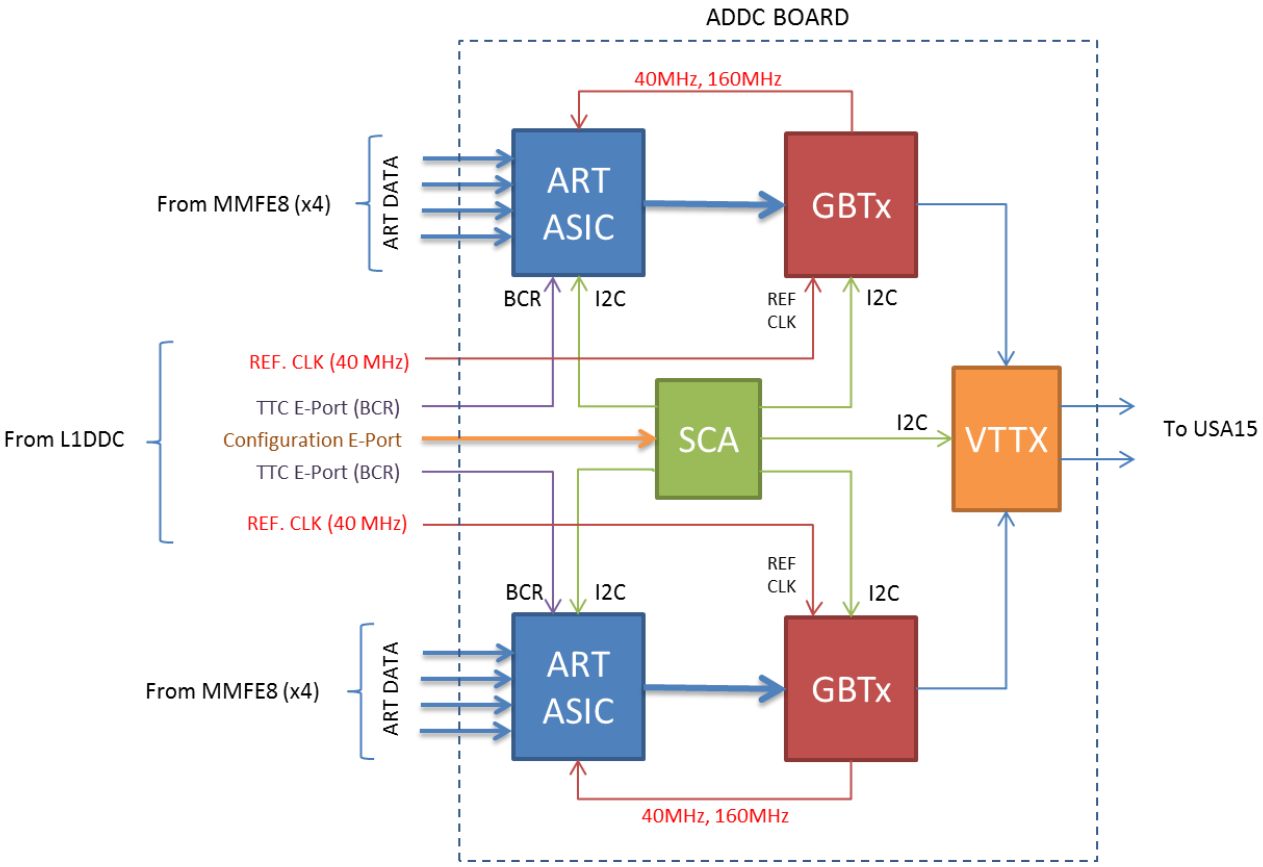

Figure 11. Block diagram of the ADDC board hosting the ART ASICs

The ART ASIC will be integrated on a front-end board called ADDC. This board will host two ART chips, two GBTx chips and one VTTx electro-optical module. In order to minimize the complexity of the ART chip, the SCA chip from the CERN GBT chipset will be used to configure the other chips on the board. The SCA chip has 16 independent I2C master interfaces [4], out of which 5 are used for configuring the two ART and GBTx chips and the VTTX module. The ART ASIC will integrate an I2C slave connected to its internal register matrix.

The Bunch Crossing Reset (BCR) signals will be forwarded along with the configuration E-Link from the L1DDC board. This board integrates a GBTx chip and acts as an aggregator for the data acquisition on the downlink and distributes TTC and configuration E-Links for all other components of the NSW Front-End system (see Figure 12).

The same board provides the 40 MHz reference clocks for the two ART-GBT subsystems, sourced by the programmable clock manager of the GBTx chip on the L1DDC board. The two clocks can be independently skewed for fine timing calibration of the trigger path. The reference clocks are supplied to the GBTx chips on the ADDC board, which, in turn, supply clean 40 MHz and 160 MHz clocks to the ART ASICs.

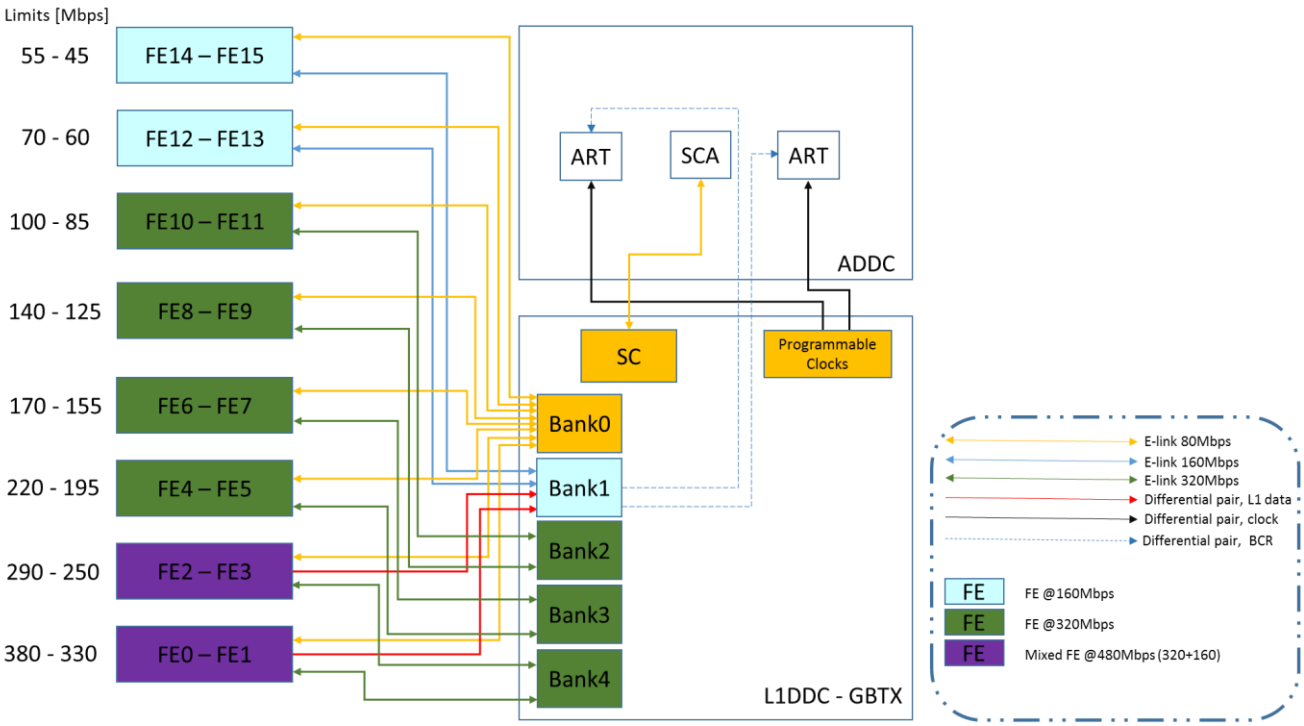

Figure 12. E-Link connectivity of the L1DDC board (courtesy of Panagiotis Gkountoumis and Theodoros Alexopoulos)

5. Radiation conditions and Triple Redundancy

The front-end electronics of the NSW detector will have to withstand total radiation dose below 100 krad [5]. The 130 nm CMOS technology was tested extensively and at much higher TID, being shown that it can withstand LHC conditions without the use of special layout techniques. Given the relatively low level of radiation, it is expected that the ASICs will be able to function properly for the entire duration of operation with minimum degradation. However, TID tests of the ASICs may be performed to assess the effects of the total radiation dose expected on the specific design, in particular the possible increase of power consumption due to leakage current.

Table 5. List of logic blocks which will be designed using triple redundancy or other SEU mitigation method.

Block	Data Protection	State Machine Protection
Programmable Delays	No	-
DDR De-serializers	Parity bit	Yes
Programmable Deadtime	-	Yes
Priority Selection	No	-
BCID Counter	Yes	
Output Logic	No	Yes
Register Matrix	Yes	yes
I2C Slave	Yes	yes

Single event effects due to instantaneous fluence of ionizing particles, however, must be mitigated with special design techniques like triple redundancy or Hamming encoding, especially for

the ASIC configuration registers and internal state machines. SEU effects on the DAQ data will most probably have little effect on the overall efficiency (see Table 6 for an estimation of SEU rates for the data and configuration logic). However, simple parity bits are calculated by the input de-serializers circuits and can be used downstream to tag possible data corruption. Table 5 shows the list of logic blocks of the ASIC which will require triple redundancy or another SEU mitigation method.

The ASICs will be tested in radiation taking into account the safety factors according to the ATLAS Policy on Radiation Tolerant Electronics [6] to ensure that possible locking situations are mitigated correctly by the triplication logic.

Table 6. Calculated SEU rates and average time between SEU events (MTBF) based on the radiation data available from simulations [5]

	Number of bits	SEU Rate (SEU/s)	SEU MTBF
Deserialization Flip-Flops	192	5,78E-07	20 days
Configuration Registers (non-protected)	400 (est.)	1,20E-06	9,6 days
Configuration Registers (TMR)	1200 (est.)	3,61E-06	3,2 days

6. Testability features

In addition to the functional test features integrated in the chip, which are summarized below, the ASIC may implement Scan Chain Testing option. An automated test pattern generator can be used with the Scan Chain, to identify various possible processing defaults. Given the small volume of chips needed (~1000), testing the chip on wafer may be an overkill. Instead, the packaged chips can be tested using bench-top dedicated test PCB with corresponding test fixture for the package used. The overhead of packaging faulty chips is likely smaller than the cost and complexity of a full wafer level testing procedure.

Functional Test modes implemented by the ART ASIC:

- Bypass of core logic.

The outputs of the 32 Programmable Delay Blocks are connected to 32 output pads, bypassing hit selection and GBT output formatter logic. This mode can be used prior to board assembly during ASIC verification for testing the delay blocks and for delay measurement.

- Bypass Priority Selection

The Priority Selection is locked to 8 of the VMM channels, by means of a configuration register. This way, the data from the de-serializers block of the corresponding VMM channel can be read continuously via the GBTx chip. This mode can be used in-system for determining if there are hold or setup time violations due to incorrect phase relationship between the incoming ART data and the local clock phase and adjust the programmable delays accordingly.

- Fixed (or cyclic) output pattern.

This mode may be used in system for determining proper communication between the ART ASIC and the GBTx chip.

- Mask and inversion bits for the 32 VMM channels.

The polarity of any of the input channels can be inverted or the channel can be masked using dedicated registers.

7. Fabrication and Packaging

The ART ASIC will be fabricated in IBM 130 nm CMOS technology sharing the same wafer with the VMM3 chip and the other companion ASICs. Using 320 Mbps communication mode to GBTx chip, the output bus of the chip is reduced to 14 SLVS ports (28 pads). The total number of functional pads is around 100. More options for the packaging of the chip will be investigated including QFN and BGA packages.

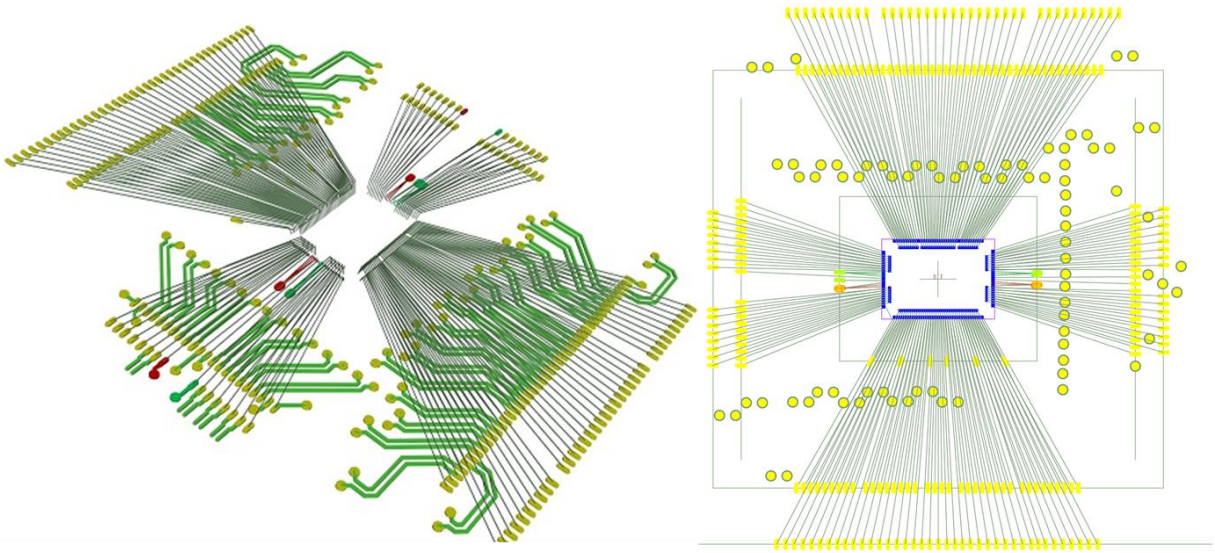

Figure 13. Wire-bonding diagram

The high number of pads and the limited space on the ADDC board might exclude the use of a non-BGA package (e.g. QFN, etc). Given the scarce offer in industry for low volume BGA packaging, this issue may be addressed together with the other chips in the collaboration.

8. Schedule

A first prototype of the ART ASIC containing the core priority logic, and HDLC e-link block and register matrix was fabricated in an earlier run. The prototype does not integrate all functionality described here, because it was laid out before these specifications were available. Due to the use of staggered pads which lead to several unsuccessful attempts for the PCB wirebonding solution, results from this prototype are still pending.

The next prototype of the ART ASIC is scheduled to be submitted together with the VMM3 ASIC and the other companion ASICs (TDS and ROC ASICs) in July 2015. Given the large die size of the VMM3 (about 1 cm^2) this is planned to be a dedicated submission, as opposed to part of a Multi-Project Wafer. Consequently there is some flexibility in the submission date.

9. Responsibilities

- S. Martoiu, IFIN-HH Bucharest, logic design, ASIC implementation & verification
- M. Renda, IFIN-HH Bucharest, prototype testing
- P. Vartolomei, IFIN-HH Bucharest, prototype testing
- T. Tulbure, Transilvania Univ. of Brasov - Romania, ASIC verification
- M. Gruia, Transilvania Univ. of Brasov - Romania, test PCB design

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