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2 ATLAS NSW Electronics Specification

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Component or Facility Name: VMM

4

5 VMM is the front end ASIC to be used in the front end electronics readout system of
both the Micromegas and sTGC detectors of the New Small Wheels Upgrade project.

6

Version: v1

7

Abstract

8 The VMM is a custom Application Specific Integrated Circuit (ASIC). It is intended to be used
9 in the front end readout electronics of both the Micromegas and sTGC detectors of the New
10 Small Wheels Phase I upgrade project. It is being developed at Brookhaven National Laboratory
11 by Gianluigi de Geronimo and his microelectronics design group. It is fabricated in the 130 nm
12 IBM 8RF-DM CMOS process. The 64 channels with highly configurable parameters will meet
13 the processing needs of signals from all sources of both detector types:

- 14 • Negative anode strip signals from the Micromegas detectors.
 - 15 • Negative wire-group signals from the sTGC detectors.
 - 16 • Positive cathode strip signals from the sTGC for precision spatial reconstruction.
 - 17 • Positive cathode pad signals used in the sTGC trigger.
- 18 To accomplish this the VMM has four independent data output paths:
- 19 • Precision (10-bit) amplitude and (effective) 20-bit time stamp read out at Level 1 accept.
 - 20 • A serial out Address in Real time (ART) synchronized to an 160 MHz clock and which is
21 used for the Micromegas Trigger.
 - 22 • Parallel prompt outputs from all 64 channels in a variety of selectable formats (including
23 a 6-bit ADC) for the sTGC trigger.
 - 24 • Multiplexed analog amplitude and timing outputs will not be used in the NSW but can
25 be valuable in development and debugging.
- 26 Version 3, to be submitted in December of 2015 in a dedicated run, will have all the design
27 features including Level-0 buffer and Level-1 handshake logic, and SEU mitigation circuitry for
28 both the configuration registers and the state machines. The devices will be packaged in a Ball
29 Grid Array with outline dimensions of $21 \times 21 \text{ mm}^2$ consistent with the Micromegas strip pitch.

30

Revision History

31

Rev. No.	Proposed Date Approved Date	Description of Changes (Include section numbers or page numbers if appropriate)	Proposed by: author Approved by: author
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	P: A:		P: A:
	P: A:		P: A:

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75 1 Conventions and Glossary

76	ADC Analog to Digital Converter.	94	MOSFET Metal Oxide Semiconductor Field Effect Transistor.
77	ART Address in Real Time.	95	
78	ASIC Application-Specific Integrated Circuit.	96	MSB Most Significant Bit.
79	BGA Ball Grid Array.	97	NSW New Small Wheel.
80	CA Charge Amplifier.	98	PDO Peak Detector Output.
81	CMOS Complementary Metal Oxide Semiconductor.	99	PtP Pulse to Peak.
82		100	PtT Peak to Threshold.
83	DAC Digital to Analog Converter.	101	ROC Read Out Controller.
84	DDF Delayed Dissipative Feedback.	102	SEU Single Event Upset.
85	DDR Double Data Rate.	103	SLVS Scalable Low Voltage Signaling.
86	DICE Dual Interlocked Cells.	104	SPI Serial Peripheral Interface.
87	EAR Export Administration Regulations.	105	sTGC small strip Thin Gap Chambers.
88	ENC Equivalent Noise Charge.	106	TAC Time to Amplitude Converter.
89	ESD Electrostatic Discharge.	107	TDO Time Detector Output.
90	FIFO First In First Out.	108	TDS Trigger Data Serializer.
91	LSB Least Significant Bit.	109	TID Total Ionizing Dose.
92	Micromegas Micro Mesh Gaseous Structure.	110	TMR Triple Modular Redundancy.
93	MO Monitoring Output.	111	ToT Time over Threshold.
94		112	TtP Threshold to Peak.

2 Related Documents

The VMM interfaces directly with 3 custom ASICs and indirectly with one. A brief description of the functionality of these ASICs and the relevant printed circuit boards, the specifications documents, as well as links to these document are provided below.

¹¹⁷ **1. The ReadOut Controller (ROC).** It reads data out of up to 8 VMM chips and provides
¹¹⁸ all interface readout control signals:

¹¹⁹ https://edms.cern.ch/file/1470540/1/NSW_VMM3_ROCReviewFeb2015_PDR_20150507.pdf

¹²⁰ 2. The Slow Control Adapter (SCA). Used for configuration and monitoring of the VMM:

121 <https://espace.cern.ch/GBT-Project/GBT-SCA/default.aspx>

122 **3. The Trigger Data Serializer (TDS).** It is used to handle the prompt signals (ToT and
123 strips) used in the sTGC trigger:

124 https://indico.cern.ch/event/327350/contribution/2/attachments/635918/875421/sTGC_Review_largerfigures.pdf

126 **4. The Front End Card with 8 vmm (MMFE-8),** is the front end card with 8 VMM chips:
127 (512 channels) used by the Micromegas Detectors

128 https://edms.cern.ch/file/1470529/1/NSW_MMFE-8-Specification-020515_PDR.pdf

129 **5 The Address in Real Time (ART) ASIC** receives synchronously with the BC clock the ART
130 signals from up to 32 VMM, encodes the strip address of those VMM with a hit, appends
131 the BCID and transmits the data to the MM trigger processor:

132 https://edms.cern.ch/file/1472976/1/NSW_ART_ASIC_specs_PDR_2015_2.docx

133 **6 The ART Data Driver Card (ADDC)** is the PCB housing the ART ASIC and GBT
134 chipset:

135 https://edms.cern.ch/file/1470535/1/NSW_ADDC_document_v1.0_PDR_2_2015.pdf

136 **7 sTGC Analog Requirements for the New Small Wheel VMM3 ASIC :**

137 https://edms.cern.ch/file/1536160/1/VMM3_Analog_Requirements_sTGC_EDMS_SpecsDocument_20150814.docx

139 **3 Description of Component or Facility**

140 The VMM is composed of 64 linear front-end channels. A block diagram of one of the identical
141 channels is shown in Figure 1. Each channel integrates a low-noise charge amplifier (CA) with
142 adaptive feedback, test capacitor, and adjustable polarity (to process either positive or negative
143 charge) optimized for a capacitance of 200 pF and a peaking time of 25 ns. The input MOSFET is
144 a p-channel with gate area of $L \times W = 180 \text{ nm} \times 10 \text{ mm}$ (200 fingers, 50 μm each) biased at a drain
145 current $ID = 2 \text{ mA}$; this corresponds to an inversion coefficient $IC \approx 0.22$, a transconductance
146 $g_m \approx 50 \text{ mS}$, and a gate capacitance $C_g \approx 11 \text{ pF}$. The filter (shaper) is a third-order designed in
147 delayed dissipative feedback (DDF) [1], has adjustable peaking time in four values (25, 50, 100,
148 and 200 ns) and stabilized, band-gap referenced, baseline. The DDF architecture offers higher
149 analog dynamic ranges, making possible a relatively high resolution at input capacitance much
150 smaller than 200 pF. The gain is adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).

151 Next to the shapers are the sub-hysteresis discriminators [2] with neighbor enabling logic,
152 and individual threshold trimming, the peak detector, and the time detector. The sub-hysteresis
153 function allows discrimination of pulses smaller than the hysteresis of the comparator circuit.
154 The threshold is adjusted by a global 10-bit DAC and an individual channel 4-bit trimming
155 DAC. The neighbor channel logic forces the measurements of channels neighboring a triggered
156 one, even if the channel does not have a signal over the set threshold. The neighbor logic extends
157 also the two neighboring chips through bidirectional IO. The peak detector measures the
158 peak amplitude and stores it in an analog memory. The time detector measures the peak timing
159 using a time-to-amplitude converter (TAC), i.e. a voltage ramp that starts at the time of the
160 peak and stops either when mode control signal ena is lowered or at a clock cycle of the BC

clock depending on the mode of operation as described below. The TAC value is stored in an analog memory and the ramp duration is adjustable in four values (125 ns, 250 ns, 500 ns, 1 μ s). The peak and time detectors are followed by a set of three low-power ADCs (a 6-bit, a 10-bit, and a 8-bit), characterized by a domino architecture [3] but of a new concept. These ADC are enabled depending on the selected mode of operation.

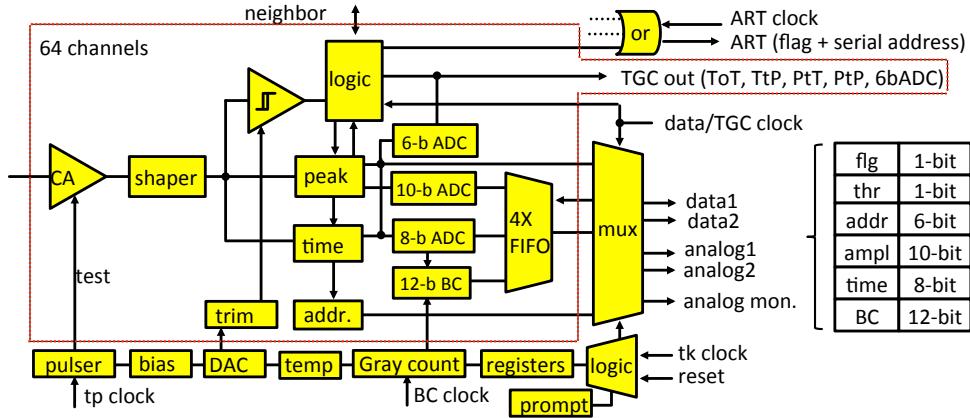


Figure 1: Architecture of VMM2.

The ASIC can operate in either a two phase analog mode (not used in NSW), or in a continuous , simultaneous read/write mode. In the two phase mode data are registered while the VMM is in acquisition mode and then read out after the system is switched to the read out mode. Acquisition is re-enabled after the readout phase is completed. In continuous mode the simultaneous read/write of data assures dead-timeless operation that can handle rates up to the maximum of 1 MHz per channel expected at the NSW. The ASIC has four independent output data paths:

1. Multiplexed analog amplitude and time stamp.
2. Digitized (10-bit amplitude, 8-bit vernier time stamp) in a 2-bit (DDR readout) digital multiplexed mode in either a short four-word buffer (existing already in VMM2) or with a deeper buffer sufficient for the expected Level-0 latency with the associated control logic to be implemented in VMM3.
3. Address in Real Time (ART) used in the Micromegas trigger schema.
4. Direct SLVS outputs of all 64 channels in parallel in one of five selectable formats, used in the sTGC trigger.

The overall connection scheme of these data paths with the rest of the NSW readout and trigger components is shown in Figure 2 and a detailed description of all modes of operation will be described in Section 11.

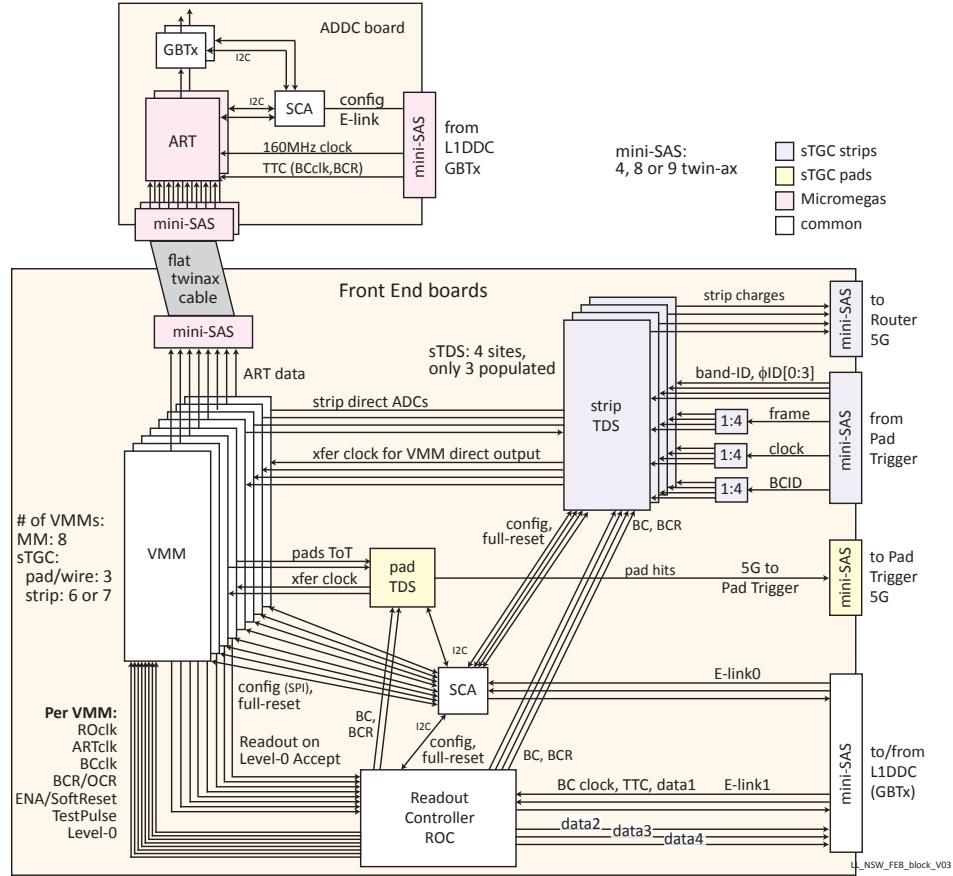


Figure 2: Overall connection diagram of the VMM.

Finally, the ASIC includes global and acquisition resets, an adjustable pulse generator connected to the injection capacitor of each channel, adjustable with a global 10-bit DAC, and triggered by an external clock synchronous to the BC clock. A global threshold generator is adjustable with a 10-bit DAC, a band-gap reference circuit, a temperature sensor complete the basic features of the VMM. It also integrates analog monitor capability to directly measure the global DACs, the band-gap reference, the temperature sensor, the analog baseline, the analog pulse, and the channel threshold (after trimming).

4 Signal Processing requirements

Both Micromegas and sTGC chambers of the NSW Upgrade will use the VMM as their front end processing ASIC. In this section the analog requirements for the VMM for both detectors are specified. There are several changes w.r.t. VMM2 as a result of beam, lab, and chamber measurements, and as result of extensive discussions and studies done jointly by the detector and electronics teams.

197 **4.1 MicroMegas Detectors**

198 The Micromegas signals from the anode strips (negative polarity signals) depending on the
 199 chosen gas gain and shaper integration time can be up to a maximum 250 fC, but typically half
 200 or even one fourth of the maximum. The input current waveform is shown in Figure 3.

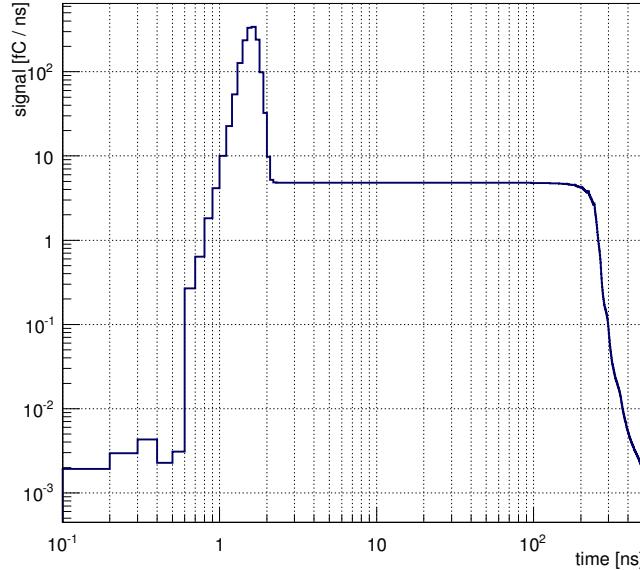


Figure 3: Simulated current induced by the motion of electrons and positive ions during the avalanche formation within the 128 μm amplification region of micromegas (the actual input to the VMM is of negative polarity).

201 The fast electron current is followed by the positive ion current. One can notice two features.
 202 Since the ions are moving in a constant electric field the current is uniform. Because of the short
 203 distance to the wire mesh (128 μm) the total signal duration is \sim 200 ns [4]. In addition to
 204 the current waveform and maximum input charge, the other relevant parameter is the electrode
 205 (anode strip) capacitance which varies from about 50 to 200-300 pF depending on the length of
 206 the strips.

207 **4.1.1 Dynamic Range and Noise Requirements**

208 The dynamic range for the Micromegas detectors is determined by the maximum collected pri-
 209 mary ionization charge, the fraction collected, and the maximum operating gas gain. Assuming
 210 a maximum gas gain of of 40,000, the dynamic range is 320 fC. The noise is determined by the
 211 requirement of single primary electron detection with a threshold 5 times the rms noise, a gas
 212 gain of 30,000, collecting half of the charge, and the maximum possible electrode capacitance of
 213 200 pF. These conditions determine the required noise level to be at 0.5 fC or 3,000 electrons
 214 rms.

215 **4.2 sTGC Detectors**

216 For the sTGC chambers, there are 3 different types of active elements on a detector: strips,
 217 wires, and pads. All 3 are read out via the VMM. Strips provide the precision coordinate
 218 measurement for track reconstruction, wires for the second coordinate, and pads are used for
 219 triggering purposes requiring a 3 out of 4 coincidence between the signals of pads in consecutive
 220 layers. The wire signals are negative while both the strip and pad sigmas are positive. Hence
 221 the need for the VMM to handle both polarities. A typical current waveform from an sTGC
 222 detector is shown in Figure 4. The total charge and the long ion tail impose specific requirements
 223 on the processing of the sTGC signals and are outlined below.

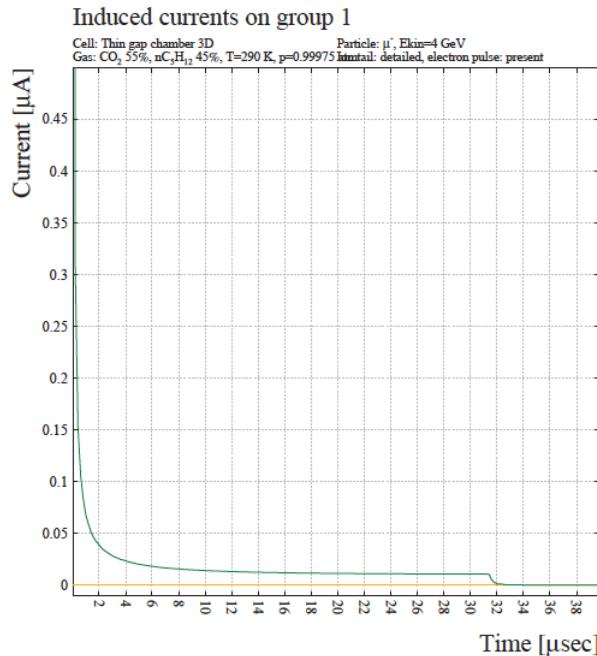


Figure 4: Simulated current induced by the motion of electrons and positive ions in an sTGC detector.

224 **4.3 Wire Signals**

- 225 1. The VMM should recover from wire signals of $\langle Q_w \rangle = 6 \text{ pC}$ within 200 ns .
 226 2. The linearity is not a critical factor here; however it is desirable for the linearity up to
 227 2 pC to be known in order to apply offline corrections.

228 **4.4 Pad Signals**

- 229 1. In ADC mode, the VMM should recover from pad signals of $\langle Q_p \rangle = \langle Q_w \rangle / 2 =$
 230 3 pC within 250 ns .
 231 2. The linearity is not a critical factor here; however it is desirable for the linearity up to
 232 2 pC to be known in order to apply offline corrections.

- 233 3. In direct-timing-only mode (Time-over-Threshold and 6-bit ADC):
- 234 (a) if the pulse charge is less than 6 pC , the dead time shall be 60 ns after the trailing
235 edge of the ToT pulse or 60 ns after the readout of the last bit.
- 236 (b) if the pulse charge is more than 6 pC , the dead time increases with the charge and
237 at 50 pC is expected to reach $\approx 1 \mu\text{s}$ from the peak.

238 **4.5 Strip Signals**

- 239 1. The VMM should recover from strip signals of $< Q_s > = < Q_w > / 6 = 1 \text{ pC}$ within 200 ns .
240 The factor of 6 comes from the assumption that the signal will be distributed over three
241 strips on average.
- 242 2. Linearity within $\pm 2\%$ up to 2 pC is required.

243 **4.6 Input Capacitance and Rate per VMM**

- 244 1. The capacitance of the largest pad on sTGC detectors will be 2 nF or less, defining the
245 maximum capacitance the VMM must work within the requirements set out in the pre-
246 ceding sections, in particular in terms of dead time and recovery time.
- 247 2. The expected/estimated maximum rate at luminosity of 7×10^{34} is 0.8 MHz per VMM
248 channel for pads and 0.9 MHz per VMM channel for strips. An average strip multiplicity
249 of 4.7 is assumed in this, including from neighbor-on mode.

250 **4.7 Dynamic Range and Noise Requirements**

251 As mentioned in the previous sections the sTGC signals span a very large range from 1 pC on a
252 given strip to about 50 pC on a pad. The dynamic range for the revision strip measurement is 2
253 pC. Assuming that one wants to measure 2.5% of this charge with a 2% resolution and a 200 pF
254 electrode capacitance, the required noise level for a 25 ns integration time should be about 1 fC,
255 or 6350 electrons. The noise for the digital signals from the pads with much larger capacitance
256 (up to 2 nF) will be substantially higher and will be determined when the front end optimization
257 design is completed.

258 **5 Physical Description of the VMM**

259 The VMM is a fully custom ASIC fabricated in the 130 nm IBM 8RF-DM. process. In this section
260 the current version, VMM2, is described since the final design is not yet available. It should be
261 noted that the vast majority of the features, pin assignment and layout will be identical in the
262 final version with only a very small number of pins (less than 10 out of 400) will be different. In
263 Table 3 the Input/ Output signal will be described with the new features included when known.
264 The document will be updated as the new information becomes available.

265 The VMM2 is packaged in a 400 ball, 1 mm pitch BGA. The device size is $21 \times 21 \text{ mm}^2$.
266 consistent with the pitch of the Micromegas detectors. The layout size is $13.518 \times 8.384 \text{ mm}^2$
267 and the die size is $13.599 \times 8.464 \text{ mm}^2$. The die layout is shown in Fig. 5. With the addition of
268 the Level-0 buffer the die size is expected to increase by about 1 mm in its long side. Although

269 it is possible to accommodate the few new pins required in the same 400 ball BGA, we are
 270 examining the possibility of using a higher ball count package in order to strengthen the power
 271 distribution, especially in the mixed signal supply. Again the overall layout will follow the one
 272 of the current device. The ball assignment is shown in Fig. 6, and the detailed pin list and their
 273 function in Table 1.

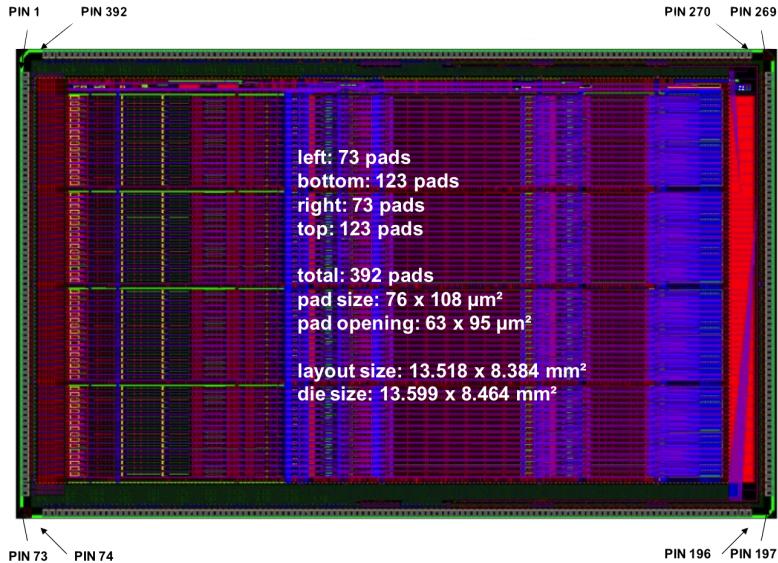


Figure 5: VMM2 die layout

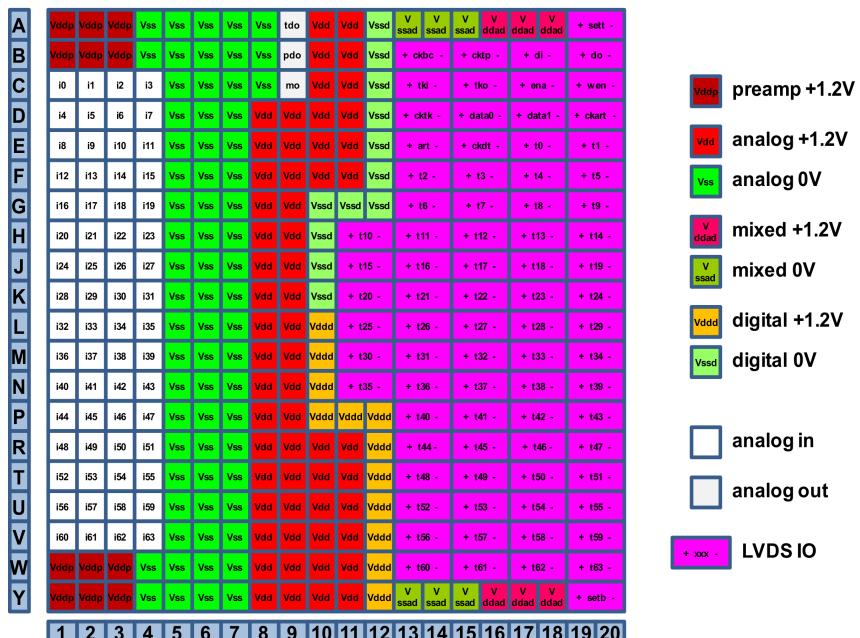


Figure 6: VMM2 pinout (top view)

Specification for VMM

274 **6 Manufacturer**

275 **6.1 Wafer Processing**

276 The VMM will be fabricated in the IBM 130 nm 8RF-DM CMOS process through MOSIS.
277 Because of its size it is more economical to be submitted in a custom dedicated run even for
278 prototypes. The wafers will be thinned to 0.010" (250 μm), diced, inspected, and sorted to waffle
279 packs.

280 **6.2 Packaging**

281 As mentioned in Section 5 the VMM2 is packaged in a 400 ball BGA with 1 mm pitch. The
282 design of the new substrate will start immediately after the layout is completed in consultation
283 with the groups designing the front end cards, and the packaging house. The new BGA may have
284 a higher ball count and, necessarily, smaller pitch in order to strengthen the power distribution.
285 The implications of this change are being studied and a decision will be made before the final
286 design review. We are in contact with two new packaging vendors, IMEC and Signetics. They
287 both agreed to accept the project in spite of the low (by industry standards) volume of 50,000
288 chips at production.

289 **6.3 Export License Issues**

290 The design does include the PROMPT circuit. The appropriate office at BNL has determined
291 that the VMM does not need Export Administration Regulations (EAR) license and, therefore,
292 it can be freely distributed to all of our NSW collaborators.

293 **7 Power**

294 The VMM is designed to operate at a nominal voltage of 1.2 V . It requires four different supplies
295 in order to minimize the contribution to the Equivalent Noise Charge (ENC) of the digital and
296 mixed analog-digital circuits. These four power supplies are:

- 297 • **Vddp:** Charge amplifier supply connected to the sources of the p-channel input MOSFETs
- 298 • **Vdd:** Powers all other analog circuits
- 299 • **Vddad:** Mixed Analog–Digital (ADC)
- 300 • **Vddd:** Supplies the digital circuits and SLVS drivers

301 Table 2 summarizes the requirements and tolerances for the four supplies. The power dissipation
302 depends on the selected functionality and mode of operation. It ranges from 500 mW to 800 mW.
303 For example the SLVS outputs can be disabled when not needed, e.g., in Micromegas operation
304 or the wire readout in the sTGC detectors.

Table 1: Pad/Pin or Connector Assignments

BGA Ball Assignment	
Ball/Pin name	Description-Comments
Vdd,Vss	Analog supplies 1.2 V and grounds 0 V – 123 pins total, max current 400 mA
Vddd, Vssd	Mixed-signal (ADC) supplies 1.2 V and grounds 0 V – 12 pins, max current ~200 mA
Vddd, Vssd	Digital supplies 1.2 V and grounds 0 V 21 pins
Vddp	Charge amplifier supplies 1.2 V 9 pins, max current ~150 mA
i0-i63	Analog inputs ESD protected
mo	monitor multiplexed analog output
pdo	Peak Detector multiplexed output Not used by NSW
tdo	Time detector multiplexed analog output Not used by NSW
sett	Ch 0 neighbor trigger SLVS
ckbc	Bunch Crossing clock SLVS, Advances 12-bit Gray-code BC counter
cktp	Test Pulse Clock SLVS
di	Configuration data input CMOS in VMM3
do	Configuration data output CMOS in VMM3
tki	Level Zero (L0) Token input in analog mode
tko	Token output Used in analog mode only
ena	Acquisition start/stop: <ul style="list-style-type: none"> • ena high, wen low: acquisition is enabled <ul style="list-style-type: none"> • internally enabled after 40 ns from ena high • in two-phase (analog) mode is acquisition • in continuous (digital) mode is acquisition and readout • ena low, wen low: in two phase (analog) is readout • ena pulse, wen high: configuration mode
wen	Configuration enable <ul style="list-style-type: none"> • wen high: configuration mode • wen pulse: acquisition reset (also resets BC counter)
cktk	Token and configuration clock
data0	Flag and first data line in digital DDR mode (flag and address in analog mode)
data1	Second data line in digital DDR mode
ckart	Address in Real Time (ART) clock
art	ART output
ckdt	Data out and 6-bit ADC clock
ttp0-ttp63	Direct digital outputs
setb	ch63 neighbor trigger

Table 2: VMM Power Supply Requirements

Supply	Voltage[V]	Ripple	Max Current [mA]
Vddp	$1.2 \pm 5\%$	$< 10 \mu\text{V rms}, 1\text{--}10 \text{ MHz}$	150
Vdd	$1.2 \pm 5\%$	$< 100 \mu\text{V rms}, 1\text{--}10 \text{ MHz}$	400
Vddad	$1.2 \pm 5\%$	$< 100 \mu\text{V rms}, 1\text{--}10 \text{ MHz}$	200
Vddd	$1.2 \pm 5\%$	$< 1 \text{ mV rms}, 1\text{--}10 \text{ MHz}$	

305 8 Cooling

306 As mentioned already the VMM power dissipation depends on the features used with a maximum
 307 of $\sim 1 \text{ W}$. Although not excessive, enclosed in a Faraday cage in the high density environment
 308 of the NSW (especially in the case of Micromegas detectors), cooling of the VMM chips is
 309 mandatory. A system with water as coolant is being designed by the teams working on the
 310 detectors.

The IBM CMOS8RF Design Manual specifies the operating temperature range to be from -55°C to 125°C . However device life time degrades rapidly at high temperatures. The case temperature should be kept below 50°C and preferably in the range 30–40 and should be verified and compared to the junction temperature provided by the VMM ASIC. The VMM includes a temperature sensor which can be read out by programming the monitor output and digitized by the SCA setting (in configuration mode) $\text{scmx} = 0$, $\text{sm5-sm0} = 000100$ (see Table 5). The die temperature is approximately given by:

$$^\circ\text{C} = 725 - \frac{V_{\text{sensor}}}{1.85}$$

where V_{sensor} is the temperature sensor reading in mV. The case temperature of a single-chip

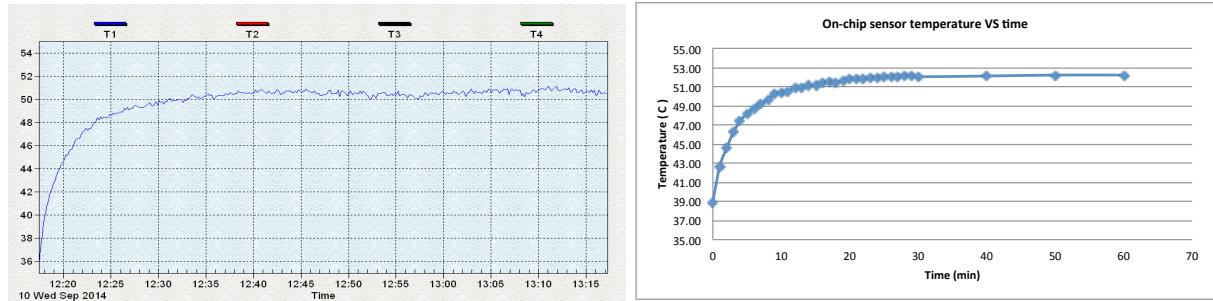


Figure 7: Left plot, the VMM case temperature. Right plot, the junction temperature as a function of time after turn-ON

311 board was measured from turn ON until thermal equilibrium and was compared with the die
 312 temperature. The results are shown in Figure 7. The difference of about 2°C is consistent with
 313 the typical junction to case thermal resistance for BGA devices of similar size, $\sim 1^\circ\text{C}/\text{W}$.
 314

315 9 Input and Output

316 The input and output connections of the VMM are shown in Table 3.

317 10 Detailed Functional Description and Specifications

318 As mentioned already the VMM has four independent data paths and can operate in one of two
 319 modes, two-phase (analog) and continuous (digital). Configuration of the ASIC is yet another
 320 mode. In the following sections these modes and the relevant specifications will be described in
 321 detail.

322 10.1 Configuration Process

323 The ASIC can be put in configuration mode by having the *ena* signal high and the *chipSelect*
 324 low. When in the configuration mode, the ASIC registers are accessible through the SPI clock
 325 *ckspi* and the data inputs *di*. The data transmitted are shifted at the falling edge of *ckspi* in
 326 groups of 96-bits and latched when the *chipSelect* is high. The written configuration is available
 327 at the *do* output for daisy-chain configuration. The timing diagram of the configuration of up
 328 to 8×VMMs is shown in Figure 8.

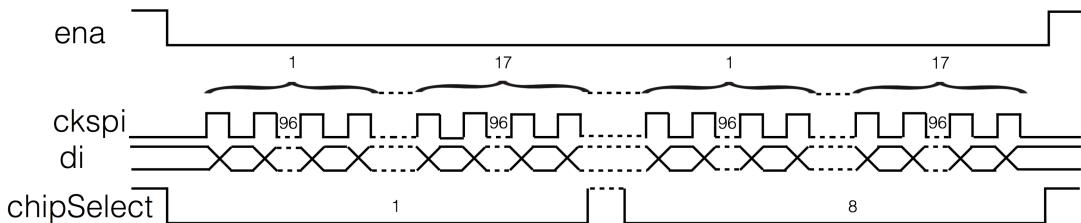


Figure 8: Configuration timing diagram of 8×VMMs.

329 The configuration is 17×96 -bits of which 80-bits are the global registers and 1536 are channel
 330 registers. Each of the 64 channels has a 24-bit configuration. The list of registers is shown in
 331 Tables 5,6. The first bit to write is the channel 63 last bit and the last to write is the global *spg*
 332 register. The sequence is shown in Table 4

Table 4: Sequence of Configuration Registers of the VMM.

Register Type	Sequence
global registers	[spg sdp sbmx sbft sbfp sbfm slg sm5:sm0 scmx sfa sfam st1:0 sfm sg2:0 sng stot sttt ssh stc1:0 sdt9:0 sdp9:0 sc010b:sc110b sc08b:sc18b sc06b:sc26b s8b s6b spdc sdcks sdcka sdck6b sdrv stpp res00 res01 res02 res03 nu nu]
channel register (64×)	[sp sc sl st sm sd0:sd3 smx sz010b:sz410b sz08b:sz38b sz06b:sz26b nu nulast]

Table 3: Input and Output Signals of the VMM. The already known changes in VMM3 are shown in red bold.

Name, Position	Con- nection	In, Out or I/O	Type of Signal or Max/Min	Description
sett A19-20	VMM	I/O	SLVS	Channel 0 force-neighbor signal
setb Y19-20	VMM	I/O	SLVS	Channel 63 force-neighbor signal
ckbc (BCclk) B13-14	ROC	In	SLVS	Bunch crossing clock of 40 MHz
cktp (Test Pulse) B15-16	ROC	In	SLVS	Test pulse clock
cktk (Level-0) D13-14	ROC	In	SLVS	Token clock / L0 (digital NSW mode)
ckdt (ROclk) E15-16	ROC	In	SLVS	Data clock
ckart (ARTclk) D19-20	ROC	In	SLVS	ART clock
di B17	SCA	In	CMOS	Configuration data input
chipSelect B18	SCA	In	CMOS	Chip Select
do B19		Out	CMOS	Configuration data output (not used in NSW)
ckspi B20	SCA	In	CMOS	Input SPI clock
t0-t63 E17-W20	TDS	Out	SLVS	Direct digital outputs
mo C9	SCA	Out	0-1 V	Analog output for calibration
tki (BCR/OCR) C13-14	ROC	In	SLVS	Token input (analog mode) / (BCR-OCR)
tko C15-16		Out	SLVS	Token output (analog mode)
ena (ENA/Soft Reset) C17-18	ROC	In	SLVS	Acquisition start/stop
ck6b C19-20	TDS	In	SLVS	6-bit ADC Clock
art E13-14	ART2GBT	Out	SLVS	Address in Real Time
data0 D15-16	ROC	Out	SLVS	Flag and first data line
data1 D17-18	ROC	Out	SLVS	Second data line

Table 5: Global Configuration Registers of the VMM.

Global bits (defaults are 0)	Description
spg	input charge polarity ([0] negative, [1] positive)
sdp	disable-at-peak
sbmx	routes analog monitor to PDO output
sbft [0 1], sbfp [0 1], sbfm [0 1]	analog output buffers, [1] enable (TDO, PDO, MO)
slg	leakage current disable ([0] enabled)
sm5-sm0, scmx	monitor multiplexing. <ul style="list-style-type: none"> • Common monitor: scmx, sm5-sm0 [0 000001 to 000100], pulser DAC (after pulser switch), threshold DAC, band-gap reference, temperature sensor) • channel monitor: scmx, sm5-sm0 [1 000000 to 111111], channels 0 to 63
sfa [0 1], sfam [0 1]	ART enable (sfa [1]) and mode (sfam [0] timing at threshold, [1] timing at peak)
st1,st0 [00 01 10 11]	peaktime (200, 100, 50, 25 ns)
sfm [0 1]	leakage current disable ([0] enabled)
sg2,sg1,sg0 [000:111]	gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)
sng	neighbor (channel and chip) triggering enable
stot [0 1]	timing outputs control 1 <ul style="list-style-type: none"> • stpp,stot[00,01,10,11]: TtP,ToT,PtP,PtT • TtP: threshold-to-peak • ToT: time-over-threshold • PtP: pulse-at-peak (10ns) • PtT: peak-to-threshold
sttt [0 1]	timing outputs enable
ssh [0 1]	sub-hysteresis discrimination ([1] enable)
stc1,stc0 [00 01 10 11]	TAC slope adjustment (125, 250, 500, 1000 ns)
sdt9-sdt0 [0:0 through 1:1]	coarse threshold DAC
sdp9-sdp0 [0:0 through 1:1]	test pulse DAC
sc010b,sc110b	10-bit ADC conversion time
sc08b,sc18b	8-bit ADC conversion time
sc06b, sc16b, sc26b	6-bit ADC conversion time
s8b	8-bit ADC conversion mode
s6b	6-bit ADC enable (10-bit and 8-bit disable)
spdc	ADCs enable
sdcks	dual clock edge serialized data enable
sdcka	dual clock edge serialized ART enable
sdck6b	dual clock edge serialized 6-bit enable
sdrv	tristates analog outputs with token, used in analog mode
stpp [0 1]	timing outputs control 2

Table 6: Channel Configuration Registers of the VMM.

Channel bits (defaults are 0)	Description
sp [0 1]	input charge polarity ([0] negative, [1] positive)
sc [0 1]	large sensor capacitance mode ([0] $<\sim 30\text{ pF}$, [1] $\sim 30\text{ pF}$)
sl [0 1]	leakage current disable [0=enabled]
st [0 1]	1.2 pF test capacitor [1=enabled]
sm [0 1]	mask enable [1=enabled]
sd0-sd3 [0:0 through 1:1]	trim threshold DAC, 1 mV step ([0:0] trim 0 V, [1:1] trim -15 mV)
smx [0 1]	channel monitor mode ([0] analog output, [1] trimmed threshold))
sz010b, sz110b, sz210b, sz310b, sz410b	10-bit ADC zero
sz08b, sz18b, sz28b, sz38b	8-bit ADC zero
sz06b, sz16b, sz26b	6-bit ADC zero

333 10.2 Two-Phase Analog Mode

334 In two-phase (analog) mode, which is the mode originally implemented in VMM1, the ASIC
 335 operates in two separate phases: acquisition with *ena* high and readout with *ena* low. During
 336 the acquisition phase the events are processed and stored in the analog memories of the peak
 337 and time detectors. As soon as a first event is processed, a flag is raised at the digital output
 338 *data0*. Once the acquisition is complete the ASIC can be switched to the readout phase and the
 339 readout proceeds injecting a token at the token input *tki*. The first set of amplitude and time
 340 voltages is made available at the analog outputs *pdo* and *tdo*. Analog buffers can be enabled
 341 using the bits *sbfp* and *sbft*. The address of the channel is serialized and made available at the
 342 output *data0* using six data clocks. The next channel is read out by advancing the token with
 343 the token clock. The token is sparse, passed only among those channels with valid events. If,
 344 after the token clock occurs, the *data0* goes low, the readout is complete and the token is routed
 345 to the output *tko* for the readout of the next chip. This allows a daisy-chained readout with a
 346 single token input. Figure 9 shows the complete timing diagram of the analog mode operation.

347 This mode will not be used in the NSW, but is being left in subsequent versions as an
 348 option. It should be noted that the two trigger paths, the 64-channel parallel outputs as well as
 349 the ART stream are active in this mode as well. The flag of the ART can be used, for example,
 350 as a fast OR of all 64-channels whereas the prompt parallel outputs can be used to implement
 351 more sophisticated trigger algorithms. If not needed the parallel SLVS outputs can be disabled
 352 with significant savings in power consumption and noise immunity from digital activity.

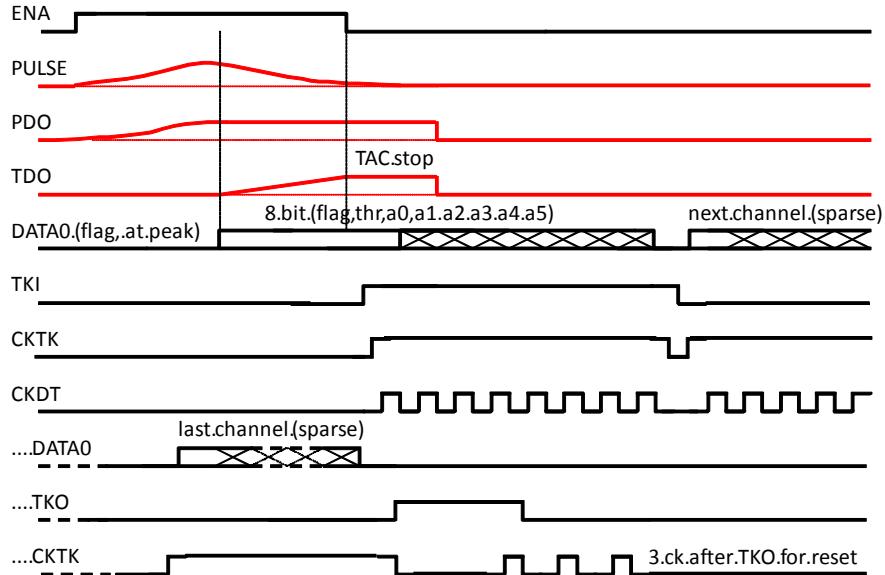


Figure 9: Data Readout with PDO,TDO and external ADC (2-phase mode)

353 10.3 Continuous (digital) Mode

354 In the continuous mode the 64 channel digital outputs ttp are activated and provide one of four
 355 different timing pulses: time-over-threshold (ToT), threshold-to-peak (TtP), peak-to-threshold
 356 (PtT), or a 10 ns pulse occurring at peak (PtP), and can be set using the global bits stot and
 357 stpp. The channel self resets at the end of the timing pulse, thus providing continuous and
 358 independent operation of all 64-channels. Alternatively, if the bits spdc and s6b are both set
 359 high, the peak detector converts the voltage into a current that is routed to the 6-bit ADC.
 360 The 6-bit ADC provides a low-resolution A/D conversion of the peak amplitude in a conversion
 361 time of about 25 ns from the peak time. The conversion time and the baseline (zeroing) are
 362 adjustable using the global bit set sc6b (the conversion time is the number of data clocks set
 363 by the sc6b bits) and the channel bit set sz6b respectively. The serialized 6-bit data is made
 364 available at the channel output immediately after an event flag which occurs at the peak time.
 365 The flag is lowered at the next clock cycle of the data clock, and the 6-bit ADC data is shifted
 366 out after that, either at each clock cycle or at each clock edge of the data clock depending on
 367 the global bit sdck6b. The channel reset occurs after the last bit has been shifted out.

368 In this mode the peak and time detectors convert the voltages into currents that are routed
 369 to the 10-bit ADC and 8-bit ADC respectively. The 10-bit ADC provides a high resolution A/D
 370 conversion of the peak amplitude in a conversion time of about 200 ns from the occurrence of the
 371 peak. The conversion time and baseline (zeroing) are adjustable using the global bit set sc10b
 372 (the conversion time is a 200 ns base plus a 60 ns increment for the MSB and LSB phases, set
 373 by the sc10b bits) and the channel bit set sz10b respectively. The 8-bit ADC provides the A/D
 374 conversion of the peak timing (measured using the TAC) from the time of the peak to a stop
 375 signal. The TAC stop signal occurs at a next clock cycle of a shared 12-bit Gray-code counter
 376 which is incremented using the external clock signal BC. The counter value at the TAC stop
 377 time is latched into a local 12-bit memory, thus providing a total of 20-bit deep timestamp with

378 a nanosecond resolution. The conversion time and baseline (zeroing) are adjustable using the
 379 global bit set *sc8b* (the conversion time is a 100 ns base plus a 60 ns increment for the MSB
 380 and LSB phases, set by the *sc8b* bits) and the channel bit set *sz8b* respectively. The channel is
 381 reset once both the 8-bit and 10-bit conversions are complete and the digital values are latched
 382 in digital memories. Thus, in continuous (digital) mode a total of 38-bits are generated for each
 383 event. The first bit is used as a readout flag, the second is the threshold crossing indicator
 384 (allows discrimination between above-threshold and neighbor events). Next is a 6-bits word
 385 for the channel address, followed by 10-bits associated with the peak amplitude, and 20-bits
 386 associated with the timing. The digital output bit assignment is summarized also on the table
 387 of Figure 1. At this point two modes should be distinguished. The non-ATLAS mode described
 388 in the following subsection, and the ATLAS-specific to be used in NSW which will be described
 389 in Section 11.

390 10.3.1 Non-ATLAS Continuous Mode

391 In this mode, already existing in VMM2, the 38-bit word is stored in a 4-event deep deran-
 392 domizing FIFO (there is one such FIFO per channel) and it is read out using a token-passing
 393 scheme where the token is passed first-come first-serve only among those FIFOs that contain
 394 valid events. The first token is internally generated as needed (i.e. the *tki* and *tko* IOs are not
 395 used) and advanced with the token clock. The data in the FIFOs is thus sequentially multi-
 396 plexed to the two digital outputs *data0* and *data1*. The first output *data0* is also used as a flag,
 397 indicating that events need to be read out from the chip. The external electronics releases a sync
 398 signal using the token clock as well (i.e. the token clock provides both advancement and data
 399 output synchronization), after which the 38-bit data is shifted out in parallel to the *data0* and
 400 *data1* outputs using either 19 clock cycles or 19 clock edges of the external data clock, depending
 401 on the global bit *sdcks*. The timing diagram relevant to this mode is shown in Figure 10

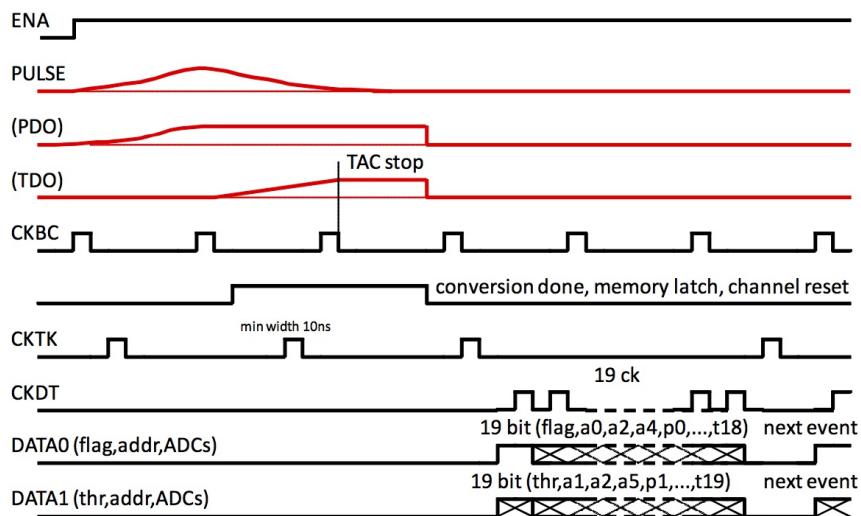


Figure 10: Data Readout with ADCs (continuous mode, 1 bit/ck).

402 11 NSW-specific Readout

403 For the NSW the readout requirements are significantly more complex requiring Level-0 in-VMM
 404 buffering (or the single-level now being considered by the ATLAS TDAQ group) since the VMM
 405 output bandwidth is not sufficient for the rates expected in some regions of the sTGC detectors.
 406 The requirements for such a readout have been established by the Readout Working group and
 407 are included in the "Requirements for the NSW VMM3 readout ASIC and the Readout Controller
 408 ASIC Design Review Report"

409 https://edms.cern.ch/file/1470540/1/NSW_VMM3_ROCReviewFeb2015_PDR_20150507.pdf

410 For completeness these specifications are reproduced here with notes where modifications
 411 are necessary and/or proposed.

412 11.1 Summary of requirements and external constraints

413 General requirements

- 414 1. Level-0 rate: up to 1 MHz (Phase 2)
- 415 2. Level-0 latency: up to 10 μ s fixed latency (Phase 2)
- 416 3. There is no simple dead time for Level-0; the complex dead time parameters are unknown.
- 417 4. Since several BCs may be read out per Level-0 trigger, a BC may belong to more than one
 trigger.
- 419 5. Level-1 rate: Phase 1: up to 100 kHz Phase 2: up to 400 kHz
- 420 6. Level-1 latency: Phase 1: 2.5 μ s fixed latency Phase 2: up to 60 μ s, variable latency
- 421 7. Configurable E-link speeds: 80, 160 or 320 Mb/s
- 422 8. Configuration registers and state machines must use TMR for SEU protection
- 423 9. The number of bunch crossings read out for a trigger must be configurable from 1 to 8.
- 424 10. A mechanism to completely identify the detector source of the data, independent of cable
 connections, must be provided.
- 426 11. The VMM and ROC will be configured via an SCA ASIC.
- 427 12. The ROC should generate test pulse trigger for the VMM in response to a TTC test pulse
 bit.
- 429 13. In response to the test pulse input, the VMM should generate the test pulse on the next
 BC clock.
- 431 14. Radiation tolerance. See: "New Small Wheel Radiation and Magnetic Field Environ-
 ment" [5].
- 433 15. The VMM and ROC must provide an SEU flag or counter to be read, reset, by the SCA.
- 434 16. Resets: full reset (via pin and on power up); reset all but configuration registers.
- 435 17. The ITAR fuse from CERN must be placed in both the VMM and the ROC in order to
 be free of export restrictions.

437 VMM specific requirements

- 438 1. Max VMM output BW: 800 Mb/s (640 Mb/s, net with 8b/10b encoding)
- 439 2. The VMM configuration/monitor path must be operable independently of the acquisition
 state.
- 441 3. The VMM3 must provide a buffer overflow counter (per channel or per VMM?) to be read
 by the SCA.
- 442 4. Each VMM must have a dedicated (i.e. not shared) configuration connection to the SCA.

- 444 5. Each VMM must have a dedicated test pulse trigger pin and a test pulse enable configura-
 445 tion bit.
- 446 6. The hit output to the Read out Controller must be 8b/10b encoded. There must be at
 447 least one comma character sent between Level-0 events and they must be sent continuously
 448 when events are not sent.

449 **Notes:**

- 450 1. The VMM configuration/monitoring path, though independent of the acquisition path can
 451 not be operable while data taking. A configuration operation when VMM is sensitive (i.e.
 452 is acquiring data) would be extremely disruptive, and measurements would be certainly
 453 corrupted, with settling times typical of the stabilizers in the analog circuits. Considerable
 454 changes would be needed to attempt protection of the sensitive circuits and alleviate these
 455 effects.
- 456 2. The buffer overflow is handled by the digital interface (see section on exception messages).
- 457 3. The VMM3 does include a dedicated test pulse pin. It should be clarified that the test
 458 pulse should be aligned with the Bunch Crossing clock.

459 **ROC specific requirements**

- 460 1. TTC information is provided to the ROC via GBT from FELIX
- 461 2. The ROC must provide BCR and BC clock to other on-board ASICs, and, in addition,
 462 Level-0 Accept, ART clock (160 MHz), and RO (160 MHz) clock to each VMM.
- 463 3. The ROC will receive a 40 MHz BC clock, but needs a PLL to generate clocks for the 80,
 464 160, 320 Mb/s E-links.
- 465 4. The data sent on the E-links must be 8b/10b encoded with Start-of-Packet and End-of-
 466 Packet symbols framing the data for one trigger.
- 467 5. Depending on a configuration bit, the ROC will send either the Level-0 Accept or the
 468 Level-1 Accept signal out as the “Level-0” signal.
- 469 6. The ROC E-links must adhere to SLVS or LVDS standards
- 470 7. When its buffers are nearing full, the ROC must be able to generate the BUSY-ON symbol
 471 in the Level-1 data flow to FELIX so that FELIX can generate RODBUSY to the Central
 472 Trigger. BUSY-OFF, with hysteresis, must be generated when the buffers return to a safe
 473 occupancy.

474 **11.2 VMM**

475 The overall block diagram for the part of the readout in the VMM is shown in Figure 11. It
 476 consists of FIFOs and logic blocks described below.

477 The existing VMM2 has a 4-deep FIFO per channel, implemented in custom layout. This will
 478 remain for non-ATLAS users wishing to operate in the existing VMM2 mode. The data (format
 479 shown in Figure 12) in these FIFOs is a sequence of hits that are transferred to a corresponding
 480 deep FIFO, implemented with the digital library, for the ATLAS-mode. Note that the 4-deep
 481 FIFO is filled asynchronously whenever the VMM peak detector finds a peak in its input signal.
 482 The channel has a minimum 200 ns dead time after a peak is found. Each channel will transfer
 483 between its FIFOs autonomously.

484 The maximum hit rate per channel is 5 MHz. With a 64-deep “latency” FIFO all hits for a
 485 period of 12.8 μ s can be buffered, provided that the hits are read out at a rate of least 5 MHz.

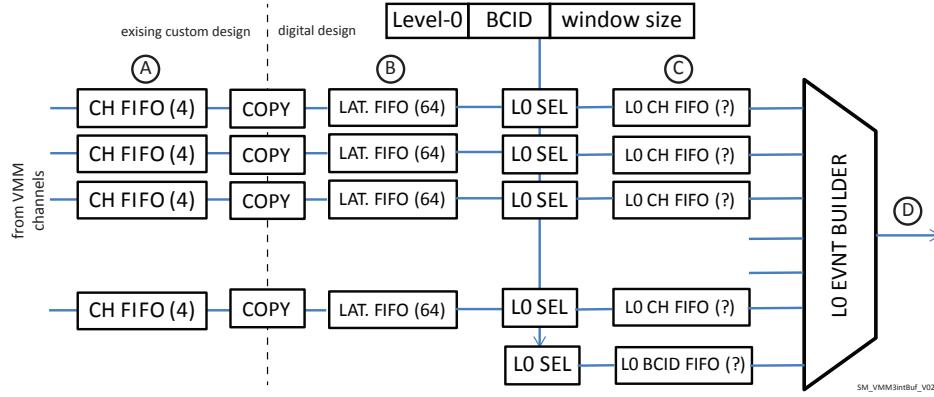


Figure 11: VMM3 internal buffers for Level-0 event output. The formats of the data at points A, B, C and D are shown in the figures following.

hit data	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
	F	N	Chan# (6)		ADC (10)																																	

LL_format_fromVMM2_V01

Figure 12: Data format from the VMM custom logic (Point A in Figure 11) “N” indicates that the hit is because the neighboring channel was above threshold. “F”, flag, is always 1.

486 Since Level-0 Accepts can occur for consecutive bunch crossings, the read rate must be 40 MHz.
 487 Therefore overflow of the latency FIFOs cannot occur for Level-0 latencies smaller than 12.8 μ s,
 488 unless the readout of the FIFOs stops (see below). The data format (“B”) in the latency FIFO
 489 is shown in Figure 13. Since there is one FIFO for every channel, the channel number need not
 490 be stored.

chan FIFO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
	P	N	ADC (10)																														

LL_format_LatFIFO_V01

Figure 13: Format of the data in the Level-0 latency FIFO (Point B in Figure 11) “P” is a parity bit.

491 11.2.1 Level-0 data selector

492 Each channel has a Level-0 Selector circuit which is connected to the output of the channel’s
 493 latency FIFO. The selector finds events within the BCID window (maximum size of 8 BCs) of a
 494 Level-0 Accept and copies them to the L0 Ch FIFO. The latency FIFO operates as a first-word-
 495 fall-through FIFO so that the FIFO output can be examined before it is discarded or copied.
 496 Since the maximum window size, 8 BCs, i.e. 200 ns, is less than the minimum dead time of a
 497 VMM channel, 200 ns, there can be at most one hit per channel in a trigger time window.
 498 The selector compares the BCID field of the hit data in the FIFO (when the FIFO is not
 499 empty) with the content of a global BCID counter. This counter is offset by the Level-0 latency
 500 (less the number of BCs in the readout window before the triggering BCID) from the BCID

501 counter used to tag hits when their peak is detected. In this way it indicates the BCID at the
 502 time of tagging, even though it is being examined after the Level-0 latency.

- 503 • On every BC clock, if the hit data becomes older than the Level-0 window, the data is
 504 flushed from the latency FIFO.
- 505 • If a Level-0 Accept is received for the given BCID and the BCID field of the hit data is
 506 inside the Level-0 window the hit data is copied to the following Level-0 FIFO.
- 507 • If a channel's L0 Sel circuit does not find a hit with a BCId falling within the window, a
 508 'no data' item (first bit equal 0) is passed to the L0 Ch FIFO for that BCID.
- 509 • Therefore all L0 Ch FIFOs receive for each Level-0 Accept either a single 'hit data' or a
 510 'no data' item and therefore all will simultaneously overflow when they are full (provided
 511 that the FIFOs are also read simultaneously). The L0 Ch FIFOs are effectively a single
 512 wide FIFO.
- 513 • Note that a hit may be copied more than once if more than one Level-0 Accept occurs
 514 within a BCID window.

515 The 24-bit item for a valid hit and for "no data" (format "C") is shown in Figure 14. For
 516 valid hit data the L0 Sel circuit also calculates a 3-bit relative BCId with respect to the BCId.
 517 The value of this relative BCId is 3 if the BCId in the data found in the latency FIFO and
 518 the BCId associated with the Level-0 Accept are equal. The parity bit is the parity bit read
 519 from the latency FIFO, checked and recalculated for Format "C". If the parity check failed, the
 520 recalculated parity bit is inverted to force detection of a parity error by the downstream logic.
 521 A parity error counter is also incremented.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
hit data	1	P																						N rel BCID
no data	0	P	0																					undefined
msg	0	P	1	R																				msg TBD (20)
BCID FIFO	V	P	V'	orb																				BCID (12)

LL_format_L0FIFO_V02

Figure 14: Format of the data in the Level-0 select output derandomizer FIFO (Point C in Figure 11)

522 For each Level-0 Accept, the BCID and a 2-bit orbit count associated with the Level-0
 523 Accept are entered into a 16-bits wide FIFO, the L0 BCID FIFO (see Figure 11) together with
 524 a parity bit, P, and two overflow condition bits, V, V' (see Figure 14). If writing the items for
 525 the current Level-0 Accept caused the L0 Ch FIFOs to become full, the Overflow bit, V, in the
 526 BCID item is set and further writing to the L0 Ch FIFOs is suspended until their level falls
 527 below a lower level. Note that the BCID FIFO is deeper than the L0 Ch FIFOs so writing to
 528 the BCID FIFO on every Level-0 Accept continues, but with the overflow bit set to indicate
 529 that there are no corresponding items in the L0 Ch FIFOs. If writing the BCID FIFO would
 530 cause an overflow, the second Overflow status bit (V') is set and subsequent writing to the BCID
 531 FIFO is suspended for the next 'Nskip' Level-0 Accepts. This is at least 'Nskip' μ s and allows
 532 time for several events to be transferred out of the BCID and L0 Chan FIFOs.

533 **Automatic suspension of noisy channels** can be based on the result of counting hits
 534 during a certain time interval or for a number of consecutive Level-0 Accepts. This requires the
 535 implementation of counters that are incremented for hits and are decremented in absence of hits

536 during a certain time interval or for a number of Level-0 Accepts. A more straightforward option
 537 would be to monitor the filling degree of the latency FIFOs and to shut off a channel once its
 538 latency buffer is filled to a configurable level. A natural place for monitoring the filling degree
 539 would be the copy stage. Once the latency FIFO is filled to the maximum level, data should
 540 still be copied to the FIFO, but seen as invalid data by the L0 Sel and be discarded once the
 541 BCId is earlier than the earliest BCId of the search window. To make this possible an additional
 542 bit is needed for each item entered in the L0 Ch FIFO indicating that the channel is inactive
 543 or active (so the FIFO would need to be 33-bits wide). The channel could become active again
 544 once the filling degree of the latency FIFO falls below a second level. By an appropriate choice
 545 of the levels the probability of an overflow condition of the L0 Ch FIFOs can be made small.

546 A data format is also defined for message data. It could be used to pass a message to the
 547 L0 Ch FIFO indicating the shutting off of a channel instead of transferring the “invalid data
 548 format”.

549 11.2.2 Level-0 event building

550 For each Level-0 Accept, the outputs of the BCId FIFO and of the L0 Ch FIFOs are read in
 551 round-robin manner, starting with the BCId FIFO. Only valid data is forwarded to the event
 552 builder stage. To achieve synchronous overflow of all L0 Ch FIFOs the data of these FIFOs is
 553 transferred synchronously into registers which are then read in sequence by the Event Builder.

554 The format of the Level-0 Event Builder output, the data sent to the Read out Controller,
 555 is shown in Figure 15. The header is always sent, even when there are no following hits. The
 556 truncation bit, “T”, indicates that the number of hits exceeded the (configurable) maximum for
 557 a VMM and that further hits for this Level-0 trigger have been discarded. It is set in the last
 558 hit that is transferred.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
header	O	P	orb	BCID (12)																															
hit data	1	P	O	T	Chan# (6)						ADC (10)						TDC (8)				N	rel BCID													
msg	1	P	1	R	R	msg ID						msg TBD (23)																							

LL_format_VMM3out_V03

Figure 15: Format of the data sent to the ROC ASIC (Point D in Figure 11) Zero or more hits may follow the header.

559 Once the overflow bit, “V”, in the BCID word is active, only the header is output; the
 560 BCId read from the BCId FIFO is the first BCId for which the overflow occurred. To make
 561 this possible the depth of the BCId FIFO has to be at least one word larger than that of the
 562 L0 Ch FIFOs. For outputting 64 32-bit words output via a link with an effective bandwidth
 563 of 512 Mb/s, 4 μ s is needed, i.e. 160 bunch crossings. In this time, for Phase 2, on average
 564 four Level-0 Accepts would occur, but in theory up to 160 could occur. Complex dead time
 565 would reduce this, but the complex dead time parameters for Phase 2 are not known. However,
 566 since the complex dead time parameters are not known, possible BCID FIFO overflows must be
 567 handled. If a BCID word written into the FIFO would cause the BCID FIFO to be full, it is
 568 written with the overflow bit, V’, set (Figure 14). The Level-0 Event Builder sends a message
 569 word indicating this overflow. The ROC then knows not to expect data from this VMM for the
 570 next ‘Nskip’ Level-0 Accepts.

571 Event building in one stage at an average Level-0 Accept rate of 1 MHz requires that a
572 complete round-robin cycle on average should be completed in $1\ \mu\text{s}$, i.e. in 15 ns per step. Event
573 building in two stages would allow reducing this to 30 ns, i.e. a 40 MHz clock can be used.

574 In order to optimize the depths of all FIFOs a simulation is required. For this, a model
575 for the input rates of the VMM is needed. Small clusters of strips or wires are typically hit,
576 but larger clusters may be hit in case of e.g. δ -ray or neutron production. Initially a Poisson
577 distribution for the time distribution of Level-0 Accepts can be used, but for a more detailed
578 simulation the complex dead time and the LHC bunch structure needs to be taken into account.
579 A simulation of the logic is being developed by the Brasov group.

580 **11.2.3 Transfer from VMM to Readout Controller**

581 The data transfer from VMM to Readout Controller is via two serial lines (even bits on one, odd
582 bits on the other) running at 160 MHz with Double Data Rate (DDR) giving a total bandwidth
583 of 640 Mb/s. Two lines are used to reduce the clock rate. The Readout Controller supplies the
584 clock for this transfer. 8b/10b encoding is used with one or more comma characters transmitted
585 continuously between Level-0 events. The 8b/10b encoding reduces the effective bandwidth to
586 512 Mb/s. The 512 Mb/s VMM output capacity is clearly sufficient. (The readout clock input of
587 the VMM can be up to 200 MHz, but this would require modifying the CERN ePLL to produce
588 200 MHz output.)

589 **11.2.4 VMM clock domains**

590 40 MHz (BC clock): Front-end, Latency FIFOs, Level-0 Selection, Level-0 FIFOs (in port)
591 160 MHz (VMM Readout clock): Level-0 FIFOs (out port), Event Builder

592 **11.3 Trigger Paths**

593 The VMM, in addition to the information recorded at Level-1 (or Level-0), provides trigger
594 primitives for both Micromegas and stGC detectors. In each case an independent trigger data
595 path provides information to the trigger processor at the bunch crossing frequency. In the next
596 two subsections a short description, the requirements, and implementation of the two data paths
597 will be discussed.

598 **11.3.1 Micromegas Trigger Primitive**

599 The Micromegas Detector in the NSW has a total of ~ 2 million channels that would make it
600 impossible to have a trigger system using information from these channels in parallel and in
601 real time. The Micromegas trigger concept takes advantage of the fine pitch ($\approx 0.5\ \text{mm}$) of the
602 detectors in the following way. Each VMM provides, at a single dedicated digital output, art,
603 the address of the first on-chip above-threshold event, called address in real time (ART). The
604 system, thus, is equivalent to a trigger system with segmentation of $3.2\ \text{cm}(64 \times 0.5\ \text{mm})$ with
605 spatial resolution of order $300\ \mu\text{m}$ sufficient for the angular resolution required in order to reject
606 candidates that are not consistent with those originating at the interaction point. This way the
607 trigger channel count is reduced to $\sim 32,000$ channels.

608 The ART mode is enabled with the bit *sfa*. Either at the pulse threshold crossing (bit *sfam*
609 low) or at the pulse peak (bit *sfam* high) a flag is released at the art output. The flag is followed

610 by the serialized address of the event. Also in this case the address is released either at each
611 clock cycle or at each clock edge of the external ART clock, depending on the global bit *sdcka*.

612 **ART Requirements/Properties**

- 613 • Arbitration logic blocks subsequent to the first hit those occurring 2 or more ns later.
- 614 • The ART stream clock frequency is 160 MHz and is provided in each VMM of a front end
615 board by a dedicated SLVS line from the ROC serving the front end board.
- 616 • It can be optionally clocked at both edges of the clock for an effective rate of 320 MHz .
- 617 • The ART must be aligned to the ART clock.
- 618 • It can optionally be provided at threshold crossing or at peak found. In the NSW imple-
619 mentation we choose the former. It reduces the latency by about the peaking time and at
620 the same time allows the use of longer integration time which results in lower electronic
621 noise and higher charge collection. Furthermore, for the trigger path, amplitude slue is
622 not an issue.
- 623 • While the direct outputs are active simultaneously with all modes of operation they are
624 not needed in Micromegas. It must be possible to turn off the SLVS drivers in order to
625 reduce power consumption and the possibility of digital interference with the front end
626 operation.

627 The ART latency is the sum of several delays

- 628 1. Time from instantaneous charge event to 1% of the peak is ~ 10 ns
- 629 2. Time from pulse peak to peak found ~ 5 ns
- 630 3. Digital latency from comparator firing to leading edge of ART is ~ 5 ns
- 631 4. Digital latency from peak found to leading edge of ART is ~ 5 ns

632 Or ~ 15 ns for the threshold crossing option or ~ 20 ns + peaking time if the peak detect is
633 chosen. The above assumes a typical case of input capacitance of 200 pF and a load of 20 pF at
634 the digital output.

635 **11.3.2 sTGC Trigger Primitives**

636 The sTGC detector trigger concept uses projective, overlapping cathode pads to define a candi-
637 date track segment by a 3 out of four coincidence in both quadruplets in a sector. The projective
638 tower defines then bands of strips to be read out and sent to the sTGC trigger logic. The pad sig-
639 nals operate in the direct-output mode in which the 64 channel digital outputs ttp are activated
640 and provide one of four different timing pulses:

- 641 • Time-over-threshold (ToT)
- 642 • Threshold-to-peak (TtP)

- 643 • Peak-to-threshold (PtT)
 644 • A 10ns pulse occurring at peak (PtP)

645 The mode can be set using the global bits *sot* and *stpp*. The channel self resets at the end
 646 of the timing pulse, thus providing continuous and independent operation of all 64 channels.
 647 Alternatively, if the bits *spdc* and *s6b* are both set high, the peak detector converts the voltage
 648 into a current that is routed to the 6-bit ADC. The 6-bit ADC provides a low-resolution A/D
 649 conversion of the peak amplitude in a conversion time of about 25 ns from the peak time. The
 650 conversion time and the baseline (zeroing) are adjustable using the global bit set *sc6b* (the
 651 conversion time is the number of data clocks set by the *sc6b* bits) and the channel bit set *sz6b*
 652 respectively. The serialized 6-bit data is made available at the channel output immediately after
 653 an event flag which occurs at the peak time. The flag is lowered at the next clock cycle of the
 654 data clock, and the 6-bit ADC data is shifted out after that, either at each clock cycle or at
 655 each clock edge of the data clock depending on the global bit *sdck6b*. The channel reset occurs
 656 after the last bit has been shifted out.

657 Because of the large area of some pads and the high rate, dead time per channel with an
 658 effect in efficiency is of concern for the sTGC trigger system and therefore choice of the direct
 659 output format is important. We summarize here the requirements of the digital part (see section
 660 4 for the analog requirements):

661 sTGC digital trigger requirements/properties

- 662 • While the direct outputs are active simultaneously with all modes of operation they are not
 663 needed in readout of the sTGC strips and wires. It must be possible to turn off the SLVS
 664 drivers in order to reduce power consumption and the possibility of digital interference
 665 with the front end operation.
- 666 • The 6-bit stream clock frequency is 160 MHz and is provided in each VMM of a front end
 667 board by a dedicated SLVS line from the TDS serving the front end board.
- 668 • It can be optionally clocked at both edges of the clock for an effective rate of 320 MHz .

669 The direct mode latency can be calculated from the following:

- 670 1. Time from instantaneous charge event to 1% of the peak is ~ 10 ns
- 671 2. Time from pulse peak to peak found ~ 5 ns
- 672 3. Digital latency from comparator–threshold to the leading edge of ToT is ~ 4 ns
- 673 4. Digital latency from peak found to leading edge of 6-bit ADC is ~ 4 ns

674 Therefore the total latency is 14 ns for ToT or 18 ns + peaking time for the 6-bit ADC option. The
 675 dead time because of the 10-bit ADC latency is ~ 200 ns after the peak. However it is possible
 676 to interrupt the 6-bit ADC conversion when the signal drops below threshold (the earliest the
 677 channel can be reset) thus providing a lower resolution peak value with the minimum dead time.

678 12 Radiation Tolerance and SEU

679 The VMM ASIC is expected to be exposed to a total ionization dose of 100 krad according to
 680 the simulations done [6]. Deep sub-micron technologies are known to be immune to much higher
 681 TID doses because of increasingly thinner oxide layers which can trap smaller amounts of charge.
 682 Although not expected to be a problem, the VMM3 will be tested for TID tolerance in the ^{60}Co
 683 source irradiation facility at BNL. However single event upsets (SEU) become increasingly more
 684 serious as the technology feature size decreases because of the smaller capacitance in the storage
 685 elements that need smaller energy depositions in order to flip their state. In the VMM there
 686 are two types of storage elements that require SEU protection, the configuration register, and
 687 the state machine control logic. In the data domain perhaps the 12-bit BCID register (under
 688 discussion) whereas the FIFOs need not be protected as an occasional data corruption is not an
 689 issue. To mitigate the SEU effects in the VMM storage elements two different techniques are
 690 used:

- 691 1. Dual Interlocked Cells (DICE) for the protection of the configuration register, and
- 692 2. The more common Triple Modular Redundancy (TMR) for the state machines and possibly
 693 the BCID register

694 The DICE uses redundancy to significantly reduce susceptibility to an upset. D flip flops based on
 695 the dual interlocked cell latches have redundant storage nodes and restore the cell's original state
 696 when an SEU error is introduced in a single node [7]. The scheme fails if multiple nodes are upset
 697 but this is far less likely, especially at the rather modest neutron levels of $\sim 10^{12} n/\text{cm}^2/\text{year}$
 698 at luminosity $7 \times 10^{34} \text{s}^{-1}\text{cm}^{-2}$. The TMR technique is used to protect the small number (less
 699 than 20) storage elements of the state machines. At the measured upset cross sections of order
 700 $10^{-14} \text{cm}^2/\text{bit}$ the upset probability is of order one tenth of an upset per VMM per year.

701 The first version of the VMM was tested in the NSCR Demokritos Tandem accelerator. The
 702 VMM1 was irradiated in the area of the configuration registers for $\sim 44 \text{ h}$ n of energy range
 703 $\sim 18\text{-}22 \text{ MeV}$ achieving an integrated n flux of $3.1 \times 10^{11} \text{ncm}^{-2}$. The measured cross-section
 704 found to be $(4.1 \pm 0.7) \times 10^{-14} \text{cm}^2/\text{bit}$. This shows a probability of $\sim 60 \text{ SEU/y/VMM2}$ for the
 705 NSW expected n flux.

706 13 Testing, Validation and Commissioning

707 The production testing of the VMM will be done along with the functional testing of the ASIC.
 708 The testing will be based in the noise, alive channels and functionality that will be defined
 709 as crucial for the ASIC validation before mounted to the boards. An automated test pattern
 710 generator can be used to test the packaged chips on the bench-top with a dedicated test PCB.
 711 The chips will be categorized based on the criteria to "Good", "Good as Spare" and "Rejected".

712 14 Reliability Matters

713 14.1 Consequences of Failures

714 The consequences of VMM failures are easily deduced from the system architecture and overall
 715 NSW design. In increasing severity they are:

- 716 • Occasional inoperative individual channels due to a variety of reasons have little impact
717 on the quality of data. An isolated channel will result in reduced (local) spatial resolution
718 in both the Micromegas and sTGC detectors, while two or more adjacent channel failures
719 will have a (local) effect in efficiency as well
- 720 • Failure of a VMM will result in the loss of information from all 64 channels. In the case of
721 the Micromegas detectors this would result in a dead segment 3.5 cm in radius of a single
722 plane of a given sector. In the case of sTGC, because of the larger pitch, it would result
723 in a significantly larger loss depending on the type of readout affected (strips, pads, wires,
724 as well as the location in a sector).

725 **14.2 Prior Knowledge of Expected Reliability**

726 No such knowledge exists at this point. .

727 **14.3 Measures Proposed to Insure Reliability of Component and/or System**

728 The assembled front end cards will undergo burn-in following guidelines described in the IBM
729 8RF Design Manual, with perhaps modifications to be determined.

730 **14.4 Quality Control to Validate Reliability Specifications during Production**

731 The production devices will be tested in an automated station to be designed and fabricated by
732 the Tomsk group in collaboration with BNL. The goal will be to identify fully operational units,
733 failed ones to be discarded and functional ones with issues that might be useable if necessary.
734 The exact test protocol and parameters that will determine usability will be determined as we
735 gain more experience with the VMM2 and VMM3 prototypes.

736 **References**

- 737 [1] G. De Geronimo and S. Li. “Shaper Design in CMOS for High Dynamic Range”. *Nuclear*
738 *Science, IEEE Transactions on* **58** (Oct. 2011), p. 2382. DOI: [10.1109/TNS.2011.2162963](https://doi.org/10.1109/TNS.2011.2162963).
- 739 [2] G. De Geronimo *et al.* “VMM1 - An ASIC for Micropattern Detectors”. *Nuclear Science,*
740 *IEEE Transactions on* **60** (June 2013), p. 2314. DOI: [10.1109/TNS.2013.2258683](https://doi.org/10.1109/TNS.2013.2258683).
- 741 [3] G. De Geronimo *et al.* “ASIC for Small Angle Neutron Scattering Experiments at the
742 SNS”. *Nuclear Science, IEEE Transactions on* **54** (June 2007), p. 541. DOI: [10.1109/TNS.2007.893718](https://doi.org/10.1109/TNS.2007.893718).
- 744 [4] G. Iakovidis. “Research and Development in Micromegas Detector for the ATLAS Up-
745 grade”. [CERN-THESIS-2014-148](#). PhD thesis. Natl. Tech. U., Athens, Oct. 2014.
- 746 [5] R. Edgar *et al.* *New Small Wheel Radiation and Magnetic Field Environment*. Jan. 2015.
- 747 [6] ATLAS Collaboration. *New Small Wheel Technical Design Report*. [CERN-LHCC-2013-006](#).
748 [ATLAS-TDR-020](#). Geneva, June 2013.
- 749 [7] F. Faccio *et al.* “Total dose and single event effects (SEE) in a 0.25 μm CMOS technology”.
750 *Electronics for LHC experiments. Proceedings, 4th Workshop, Rome, Italy, September 21-
25, 1998*. 1998.