Trigger Processor Overview and Status

Nathan Felt

Harvard University

On behalf of the Trigger Processor effort

BNL, Bucharest, Harvard, IHEP Beijing, Illinois, Weizmann

ATLAS Muon Week

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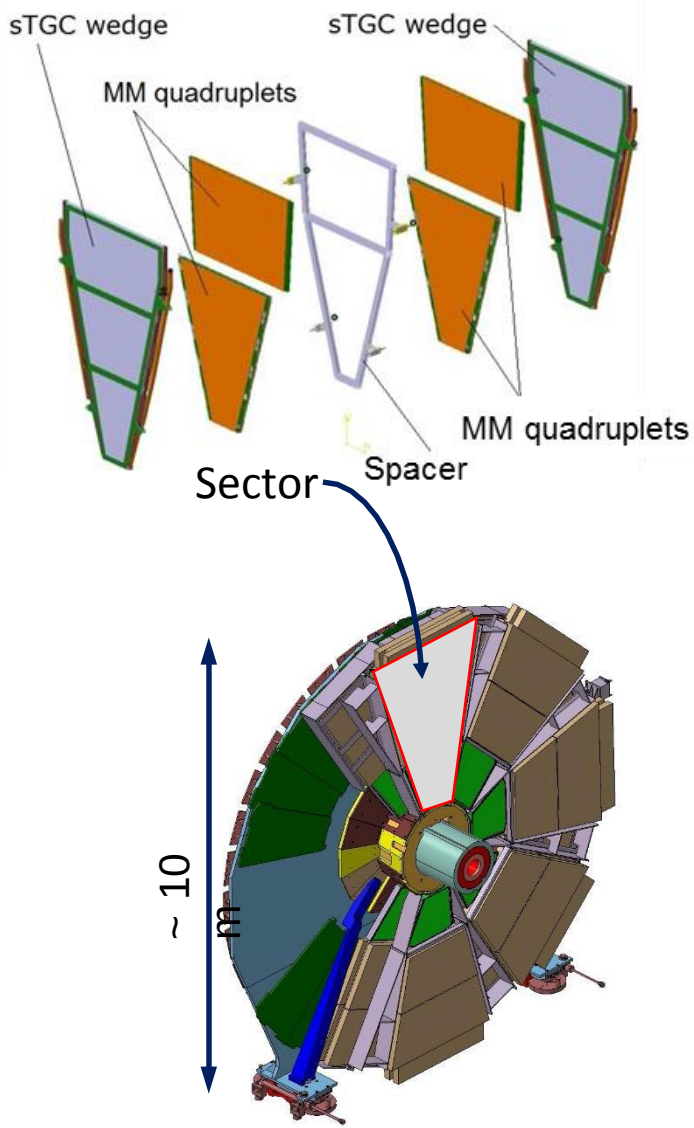
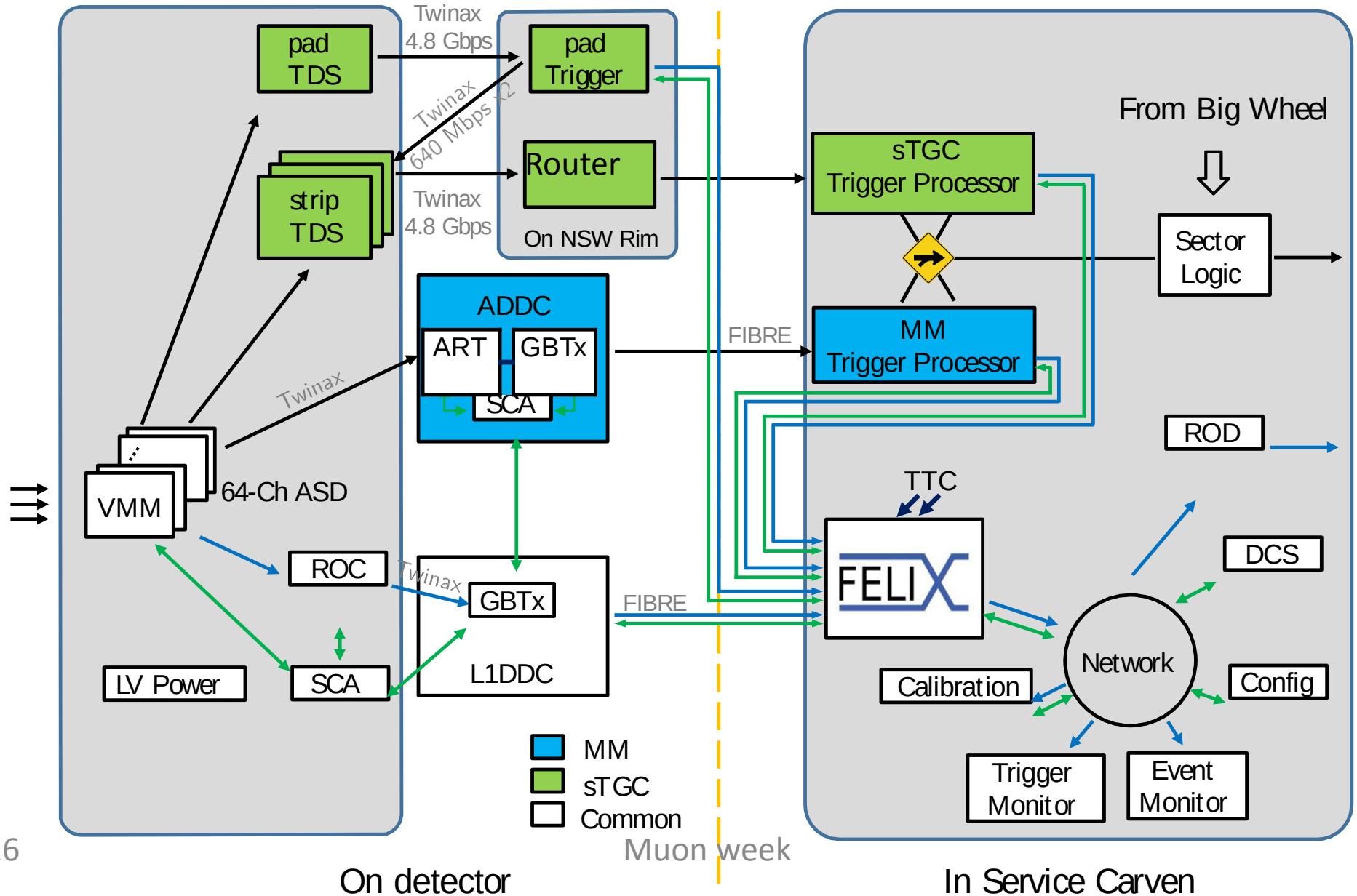
NSW Trigger Summary

- Micromegas: 2M strips, 0.4mm
- sTGC: 280K strips (3.2mm), 45K pads, 28K wires
- sTGC and MM find track candidates independently,
  - sTGC up to 4 Candidates/BC
  - MM up to 8 Candidates/BC
- Candidates merged for Sector Logic (max 8 / BC)

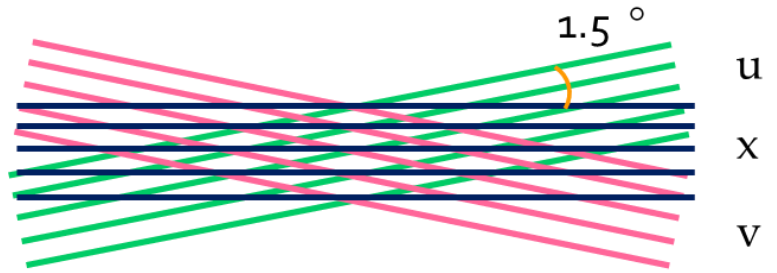


NSW Trigger Processor Data Flow

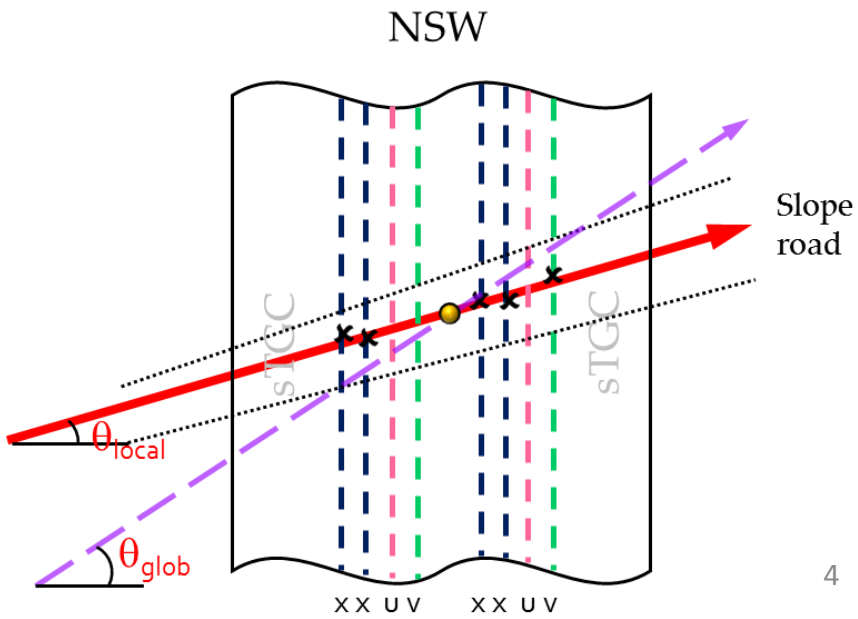


MM Trigger Algorithm

- Find the slope of each hit strip with respect to the IP
- Collect hits that are in the same slope roads and produce a multi-plane coincidence trigger “Finder”
- $\Delta\theta$ calculated from X slopes (mx Local and mx global)
- ϕ is calculated using the U and V slopes

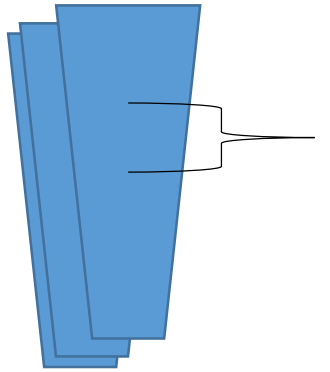


x: horizontal strip (2 plans per quad.)
u,v: stereo strip (1 each per quad.)



MM Trigger Processor Implementation

- Current algorithm being tested can process tracks from a 1/16 slice of a sector.
- This corresponds to 8 x MMFE 8, one per plane, or 2 GBT fibers
- This is currently being expanded to process a wider area



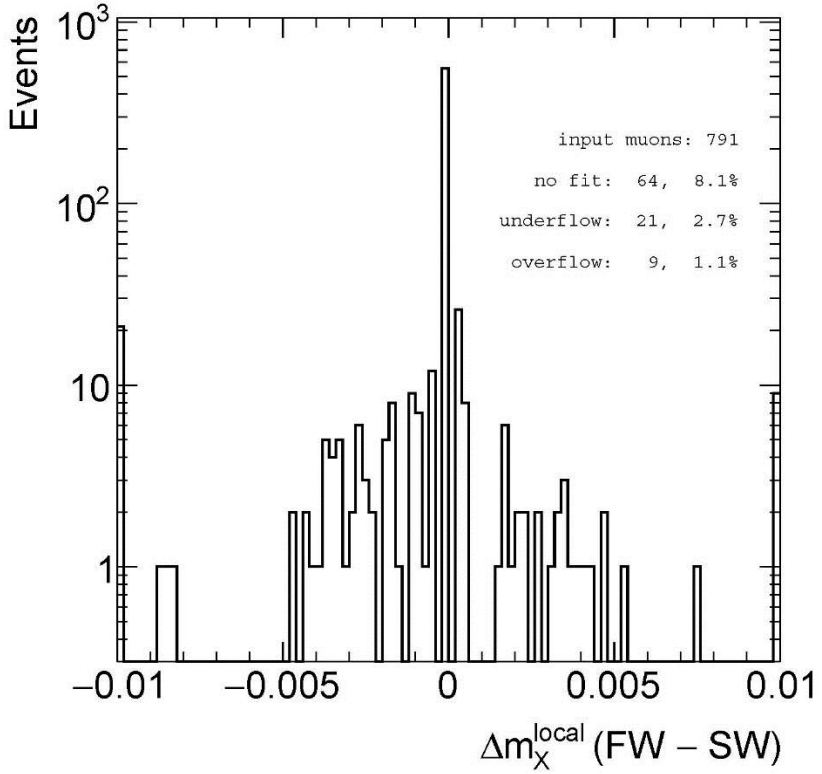
Hit Data from representing 1/16 of a sector

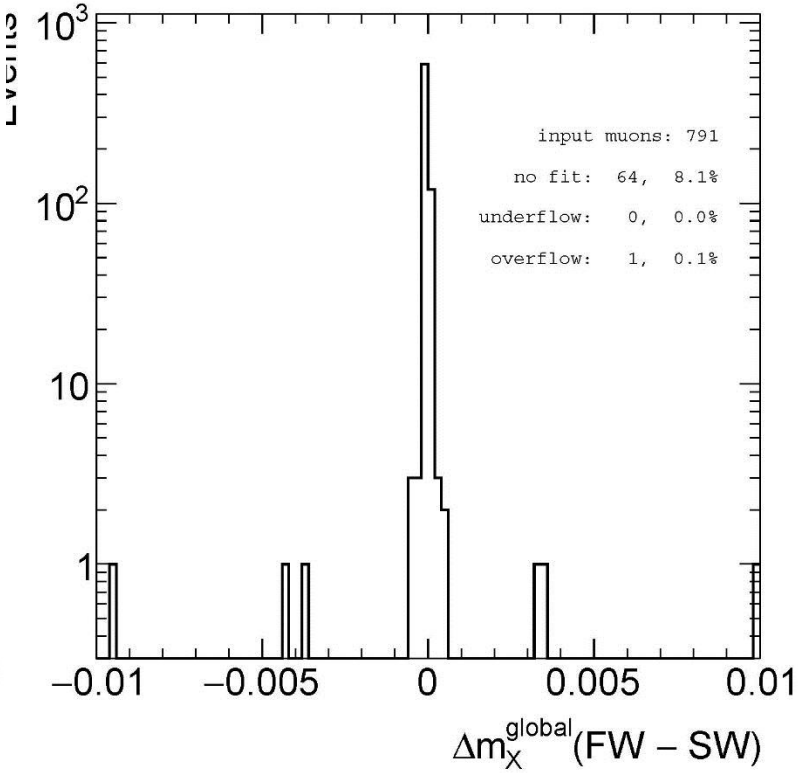
8 planes

MM Trigger Processor Firmware Simulations

- Firmware simulations are done using ModelSim
- Matlab is used for simulation data formatting and acquisition

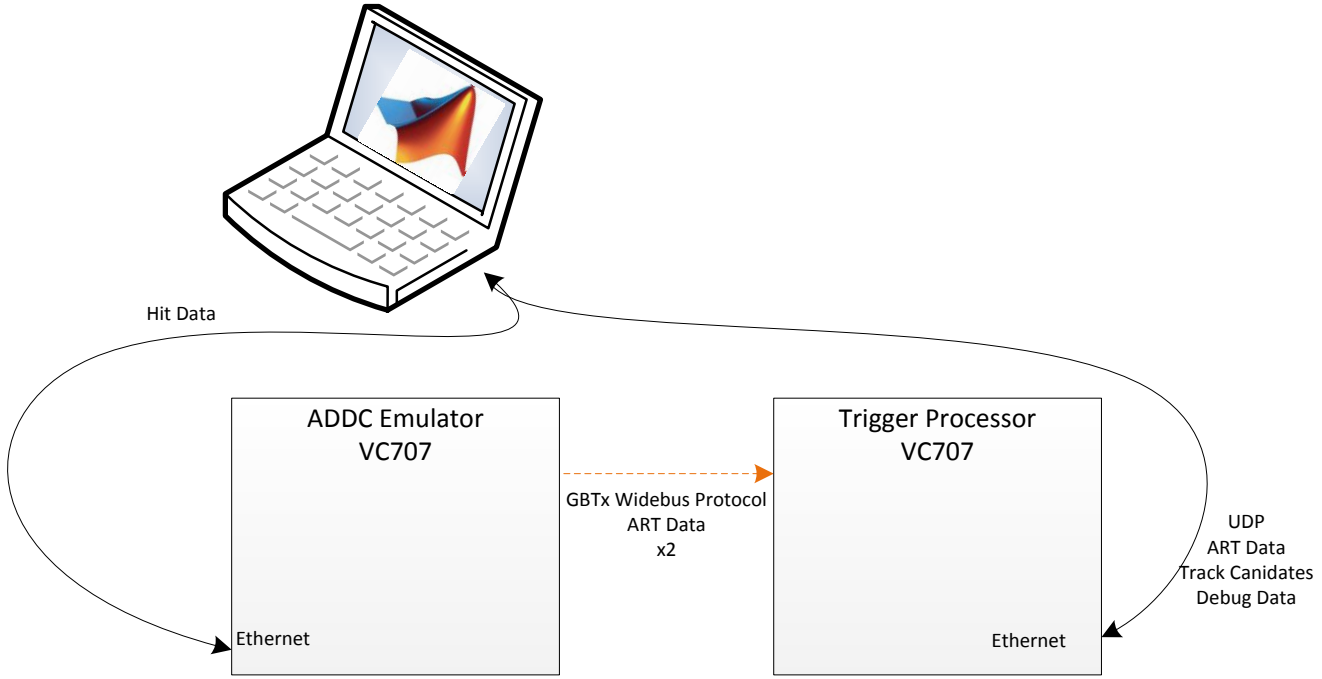
- Simulation hit data are Athena generated 100 GeV muon events
  - 791 Total
  - ~5% bad fit
  - ~10% failed fit





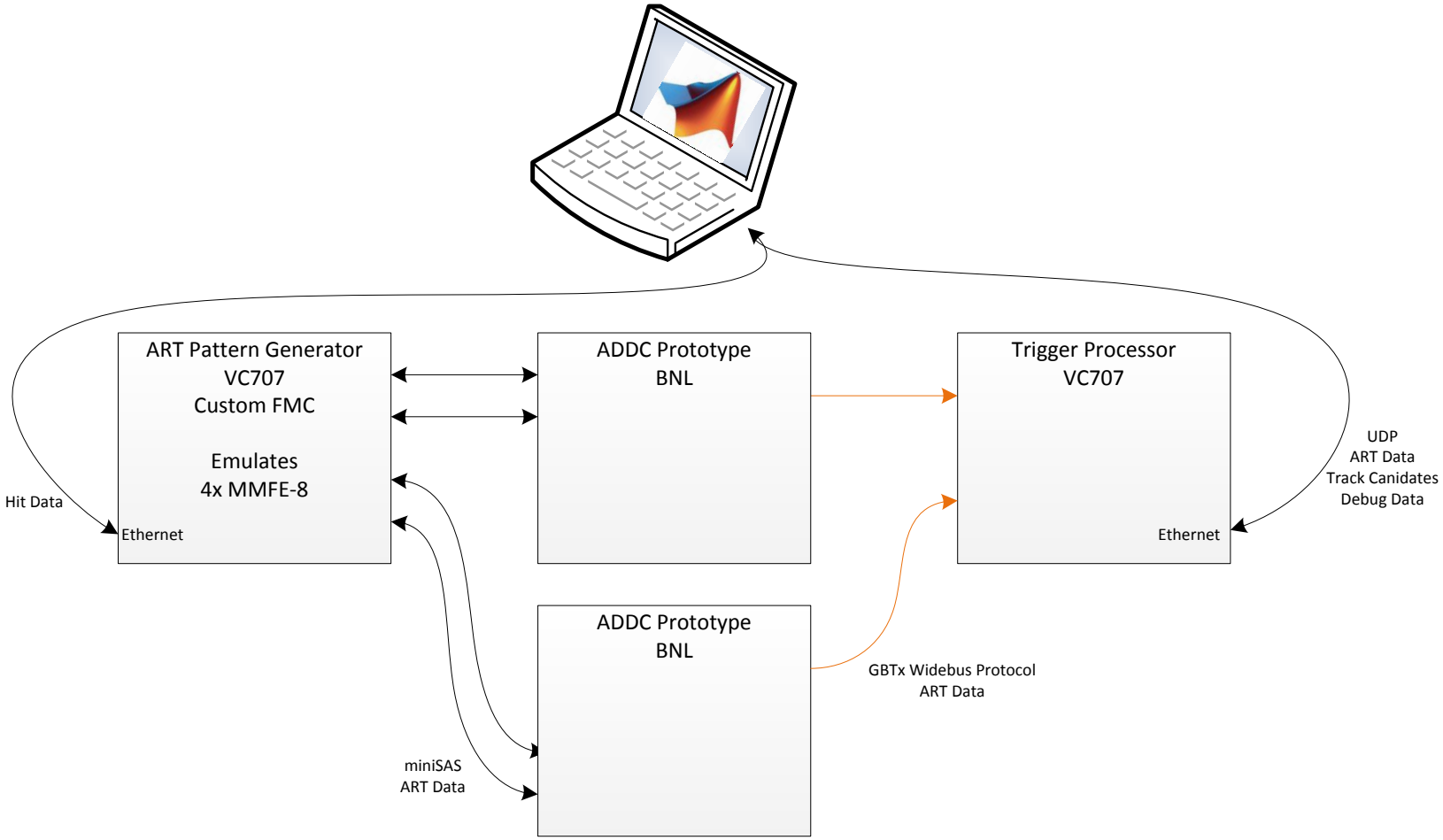
MM Trigger Processor Hardware Testing

- Xilinx Virtex 7 based development boards (VC707) is used for testing the firmware on hardware



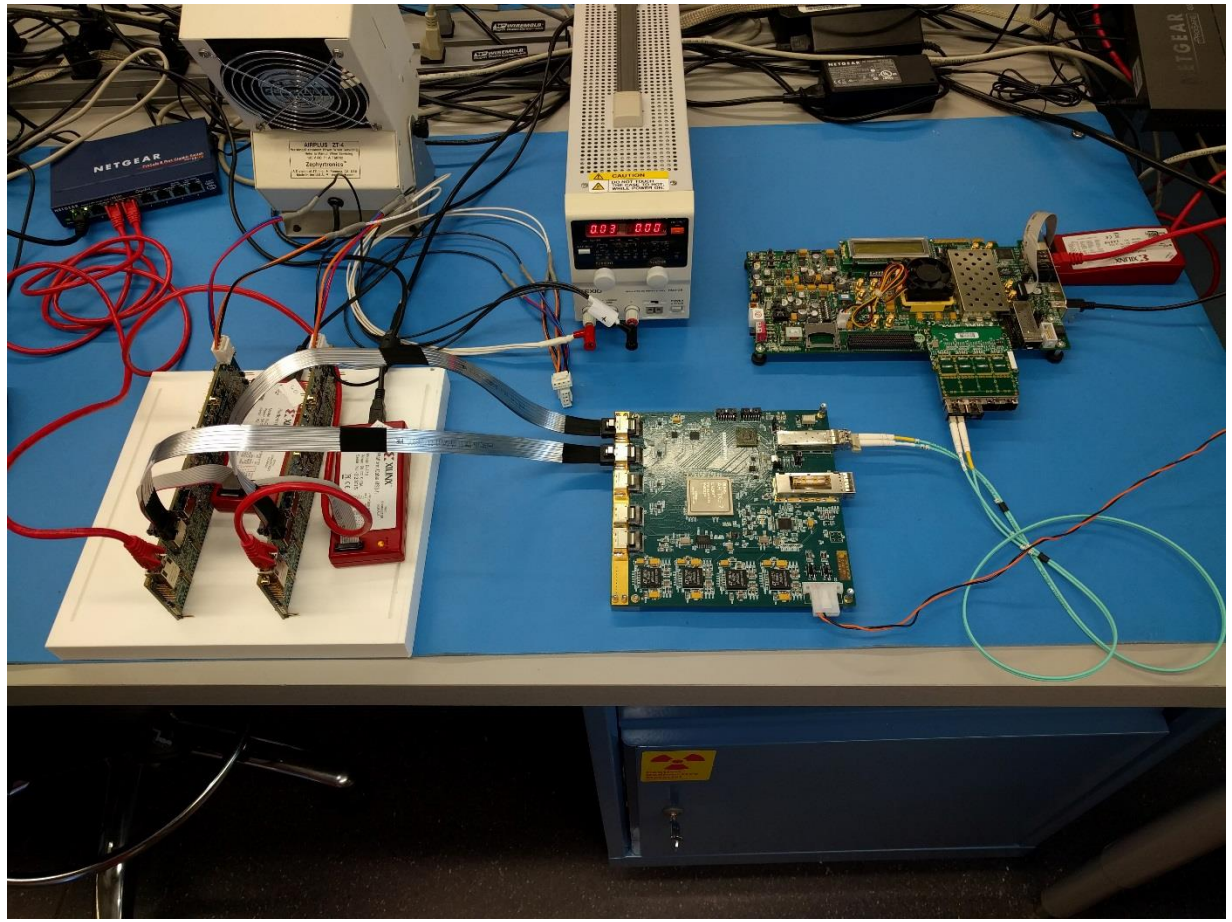
MM Trigger Processor
Pattern Generator - ADDC Porotype Integration

- ART Pattern Generator was used to produce ART data as from a VMM
- Emulates 4 x MMFE 8
- Tested at BNL last summer



MM Trigger Processor
MMFE 8 - ADDC Prototype Integration

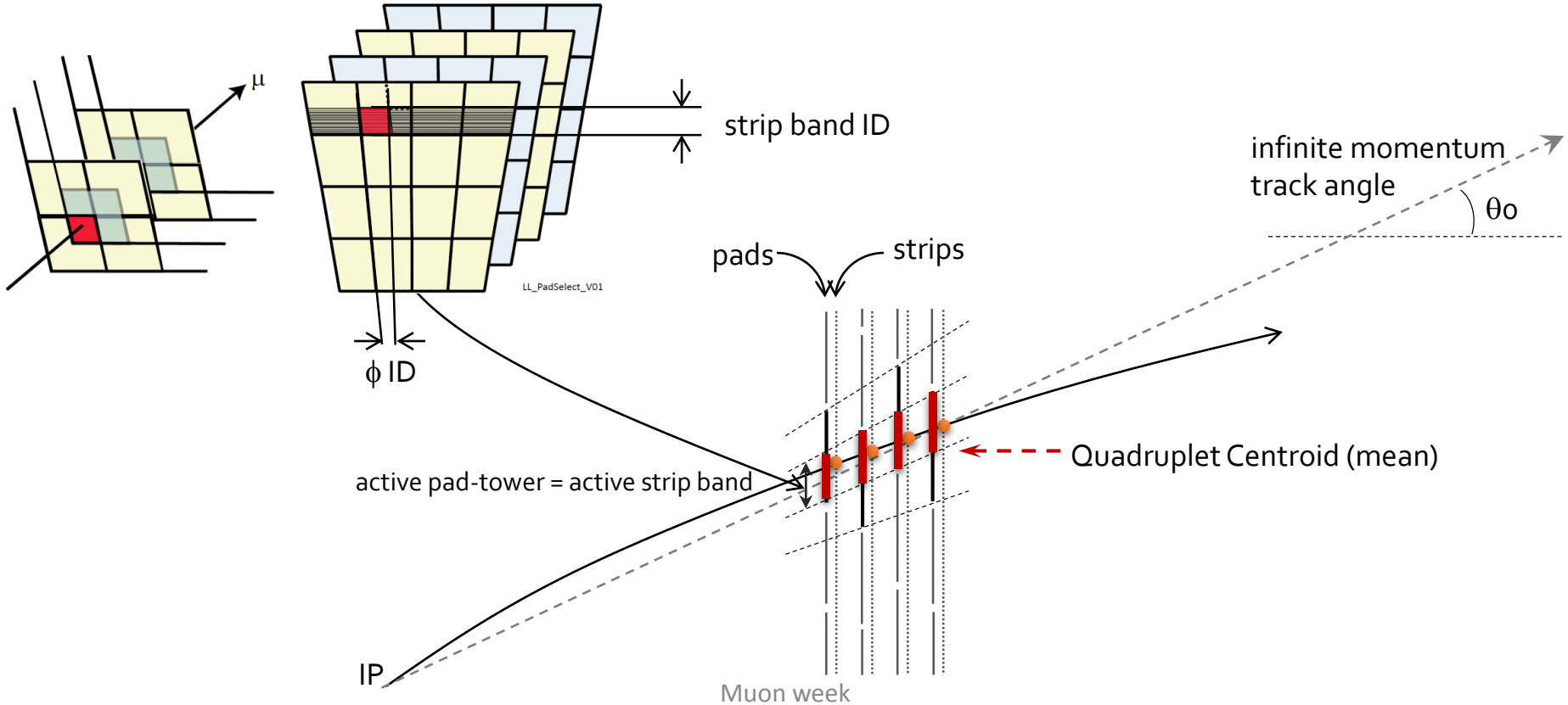
- Observed the clock and ART data from MMFE8 using VMM internal pulser.
- Ready to connect MMFE8 to existing test stand (Previously tested using ART Pattern Generator)



sTGC: Pre-trigger From the Pad Towers

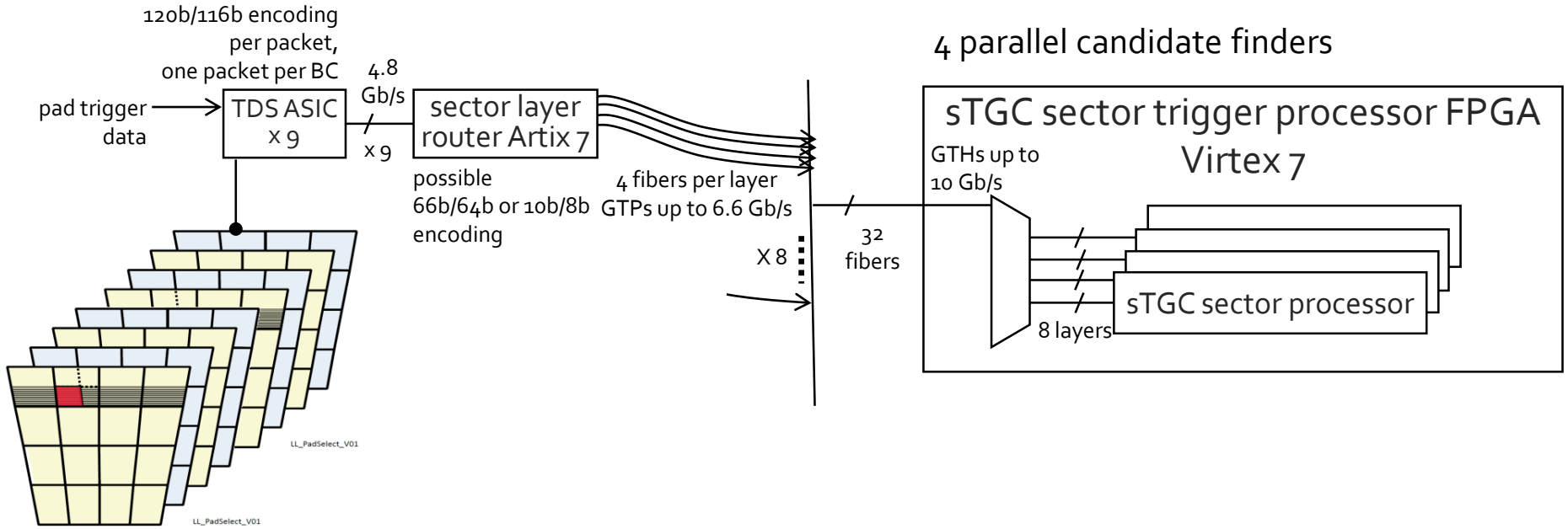
There are about 280,000 strips in sTGC.
To minimize the amount of a transmitted charge information to off-detector Trigger Processors, pad coincidence information is used.

The Pad Trigger selects the strips passing through a pad tower made from a coincidence of overlapping pads.



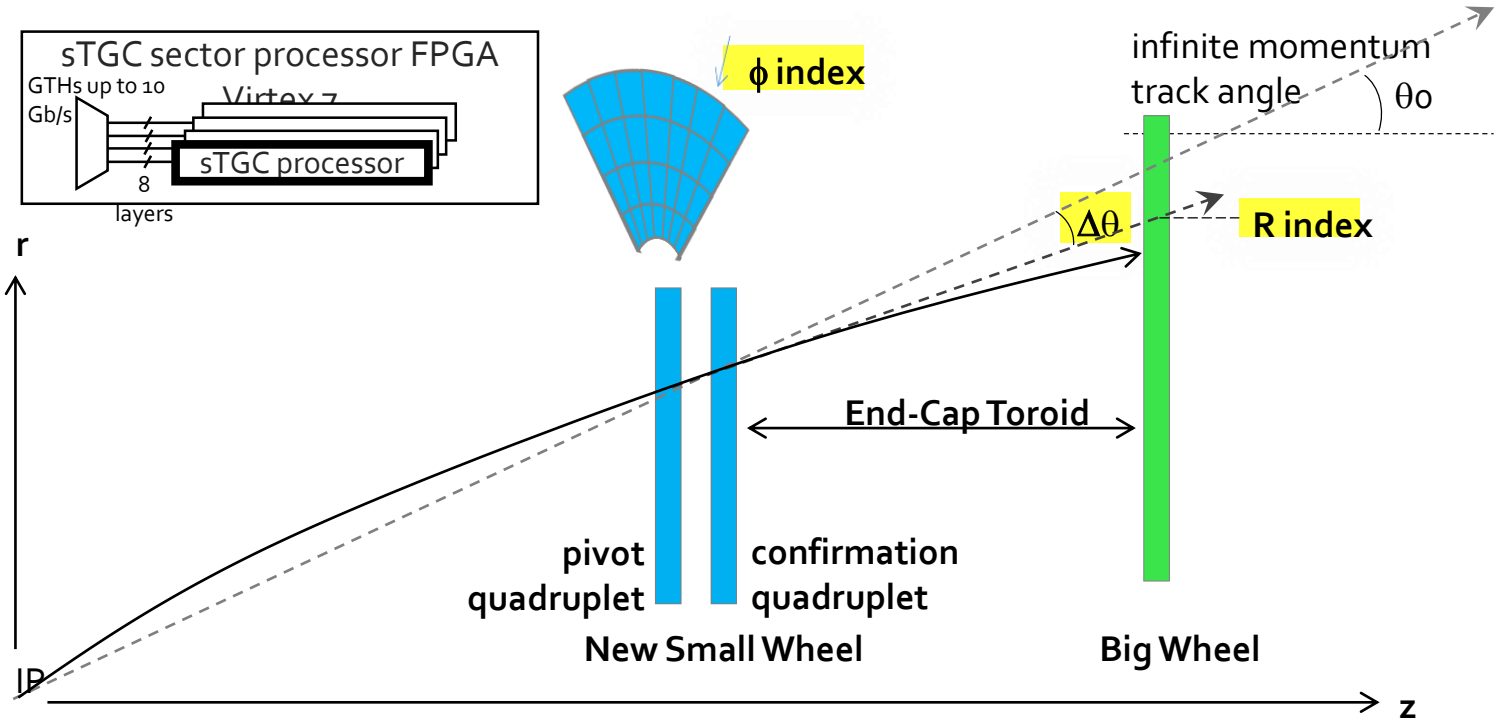
sTGC Interface: NSW side

- One sTGC sector trigger processor serves one sector.
- Pad trigger data is sent with corresponding strip data to the Trigger Processor



sTGC Trigger Processor Algorithm

- Compute centroid of each layer using a 5 strip window of active strips
- Compute the Centroid from each quadruplet using the layer centroid - $\Delta\theta$ data
- ϕ information is from pad data



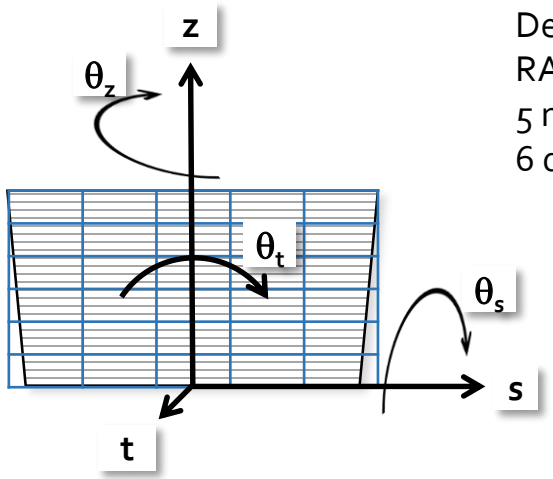
Algorithm input: ϕ ID, strip band ID, Misalignment Correction offset

Algorithm Output:

Field:	sTGC hit	MM hit	$\Delta\theta$ (mrad)	ϕ index	R index	spare
Num of bits:	2	2	5	6	8	1

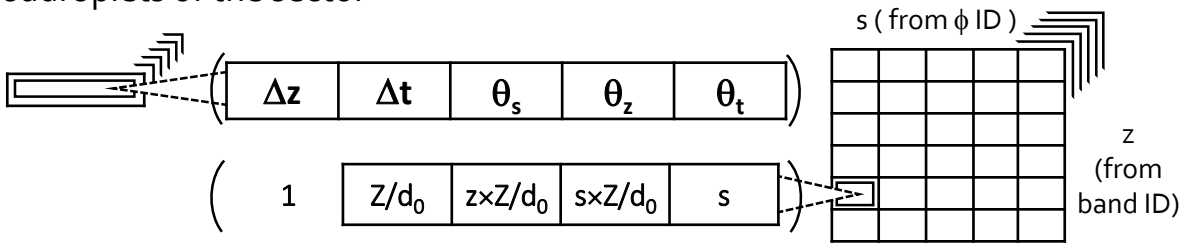
sTGC: Quadruplet Misalignment Correction

AMDB (ATLAS muon detector database), describes the geometry of the ATLAS muon spectrometer.



Detector alignment parameters RAM (from AMDB) are 5 measured values per each of 6 quadruplets of the sector

Detector geometrical parameters ROM LUT per each of 6 quadruplets of the sector

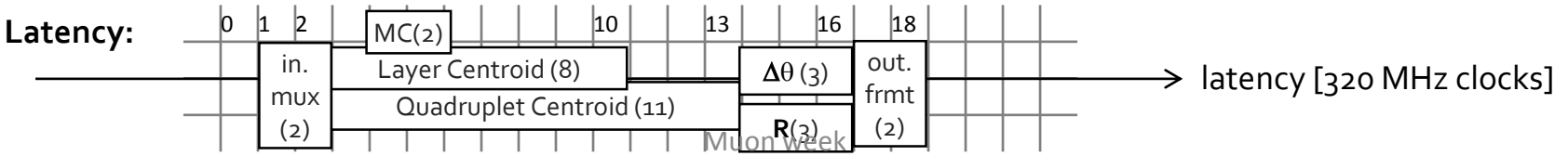


- Misalignment correction offset per quadruplet is a vector dot product of the Detector alignment parameters and the geometrical parameters
- (Δz , Δt , θs , θz , θt) • (1, Z/do , z×Z/do , s×Z/do , s)

Note: AMDB Z is NSW R, d_o is a distance to IP.

- This calculation is done in parallel with the centroid finding and does not impact latency

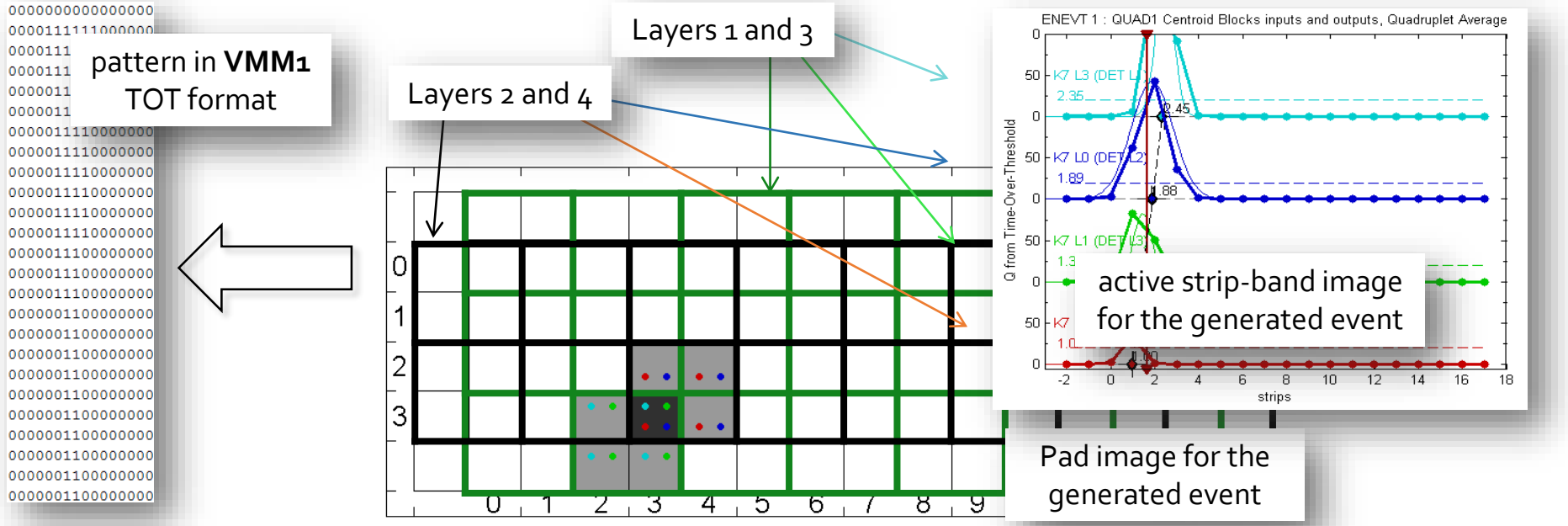
Total algorithm latency: 18 clocks = 56.25 ns = 2.25 BC



sTGC: Algorithm testing: patterns

Test pattern generation:

- Values for track angle, hit radius, hit intensity and hit position are taken from a uniform distribution within predefined limits.
- The event parameters are then parsed into trigger processor algorithm input patterns for each of the eight layers.
- Expected algorithm results are calculated to be compared with an actual algorithm outputs.



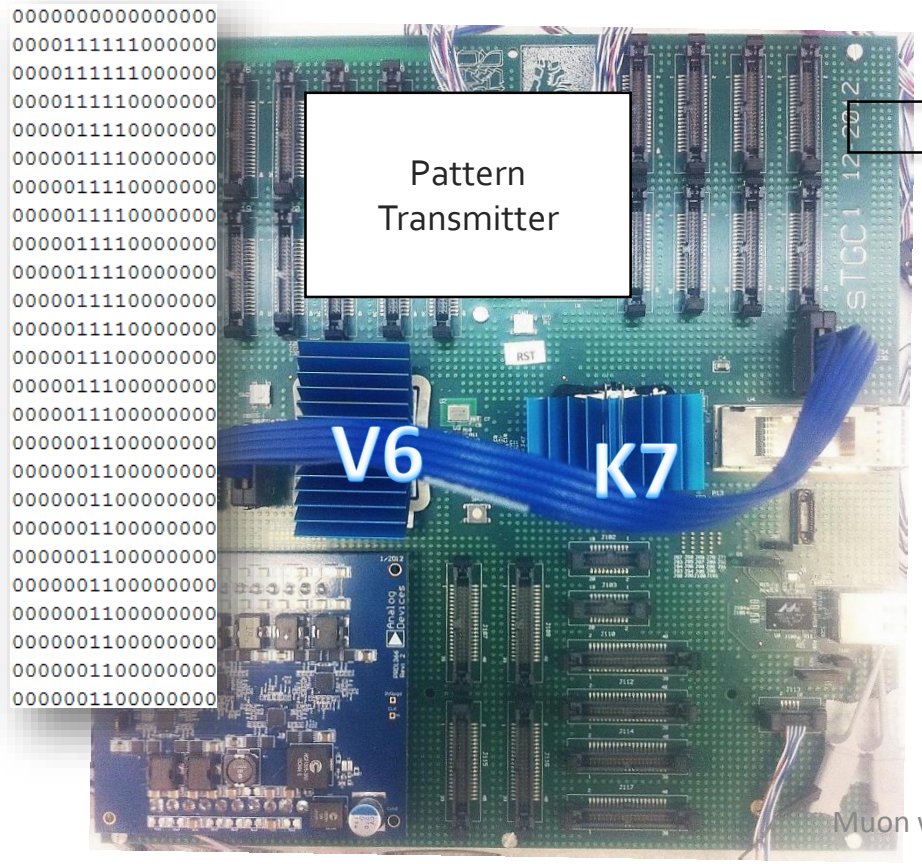
- **Simulated muon events will be formatted into patterns in a similar way and allow algorithm performance test.**
- **Events recorded on the beam test will be formatted into patterns in a similar way and allow advanced algorithm performance test.**

sTGC: Algorithm testing : patterns – cont.

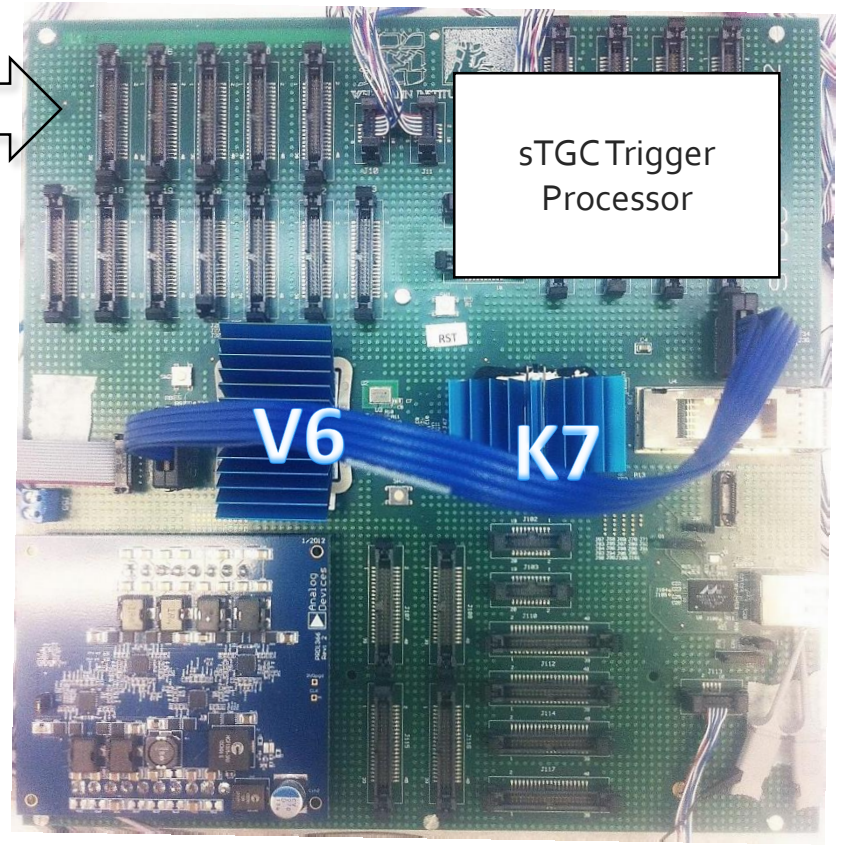
Test pattern is loaded into sTGC demo board (7K325TFFG900 / XC6VLX130TFF1156).

Two identical boards are connected, when one is configured as test pattern transmitter and emulates VMM1 TOT outputs and other is configured as an sTGC trigger processor.
Algorithm results are sent from sTGC Trigger Processor board via LAN to PC for verification.

sTGC demo board with preloaded pattern

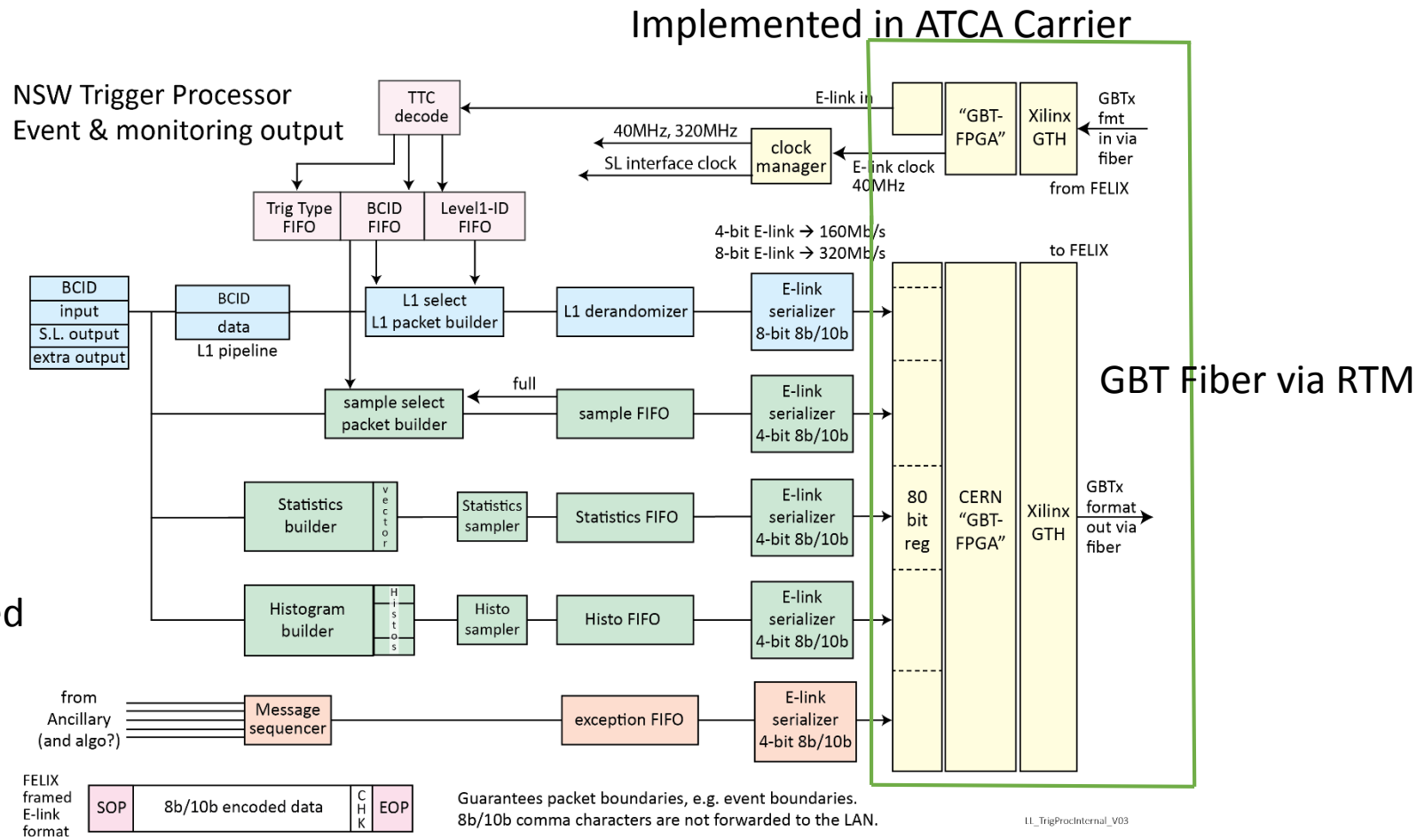


sTGC demo board with trigger processor

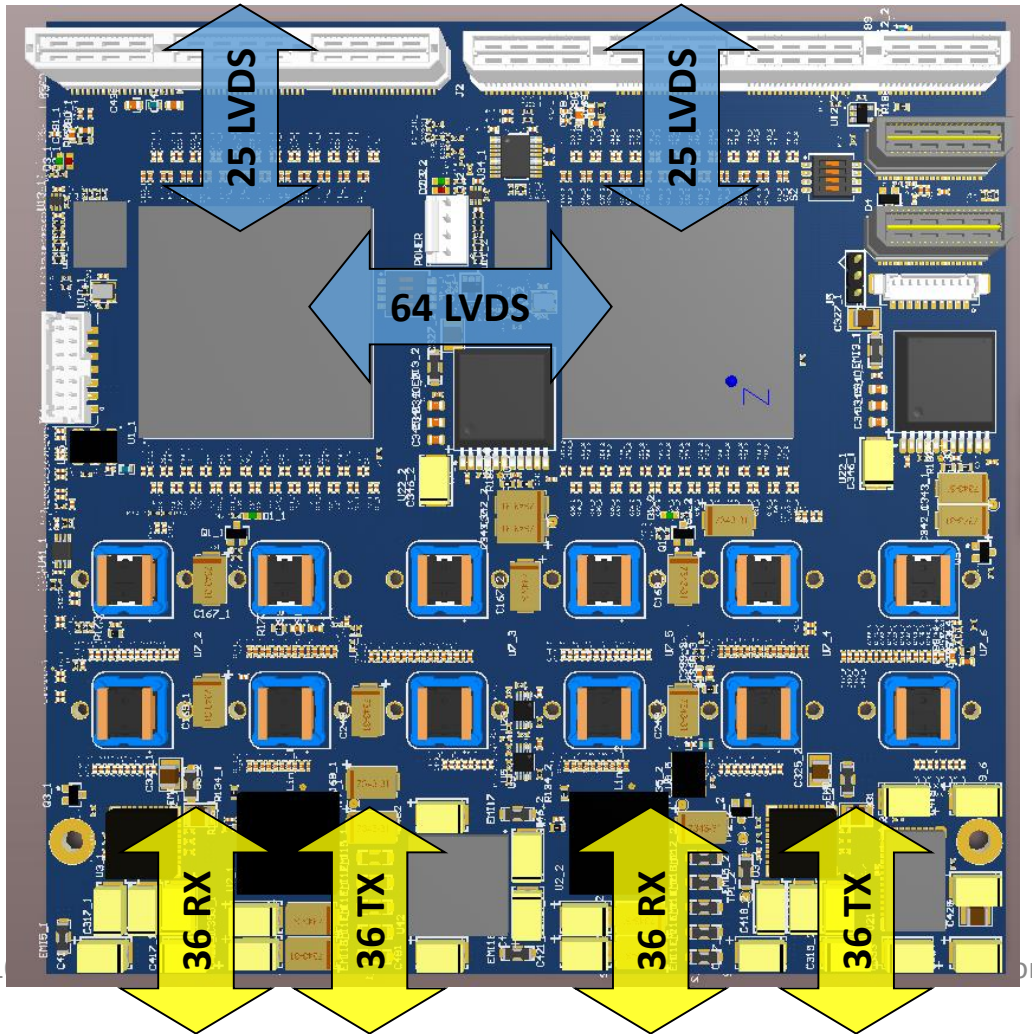


NSW Trigger Processor Ancillary functions

- Ancillary Functions
  - Readout on Level-1 trigger
  - Monitoring
  - Configuration
  - Statistics
  - Histograms
  - Playback for debug
  - Output to Sector Logic
- Work shared by
  Harvard, Illinois, Weizmann
- E-Link connection to mezzanine
- GBT FELIX interface implemented in carrier FPGA using RTM fiber connection
- Looking into including an Ethernet Debug connection via RTM



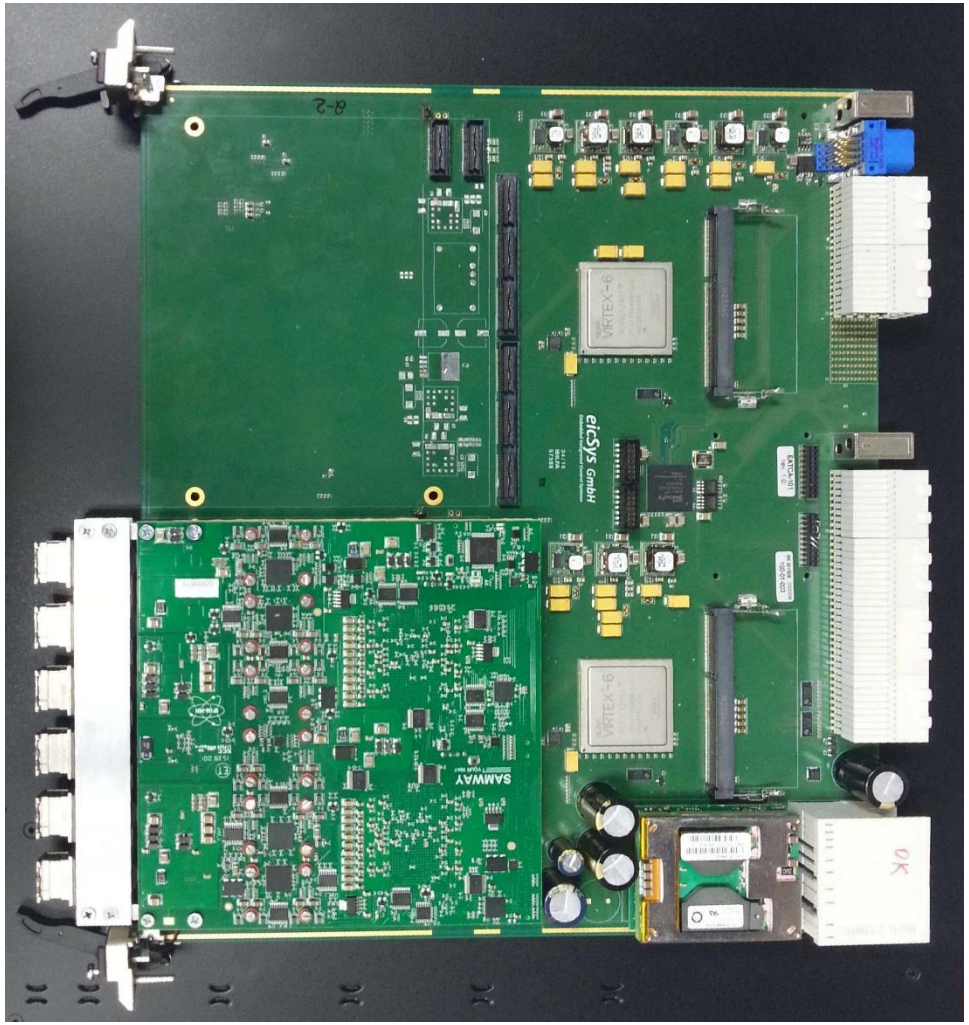
Trigger Processor Hardware Platform
High Density Optical Mezzanine (HORX)



- Designed at IFIN-HH Bucharest
- ATCA mezzanine build under specification for ATLAS NSW Trigger Processor
- 2 x Virtex-7 690 FPGA s
  - sTGC and MM share a single mezzanine
  - 2 mezzanine / ATCA Carrier
- 36 Optical transceivers /FPGA
  - Avago Micropods (12 duplex fibers)

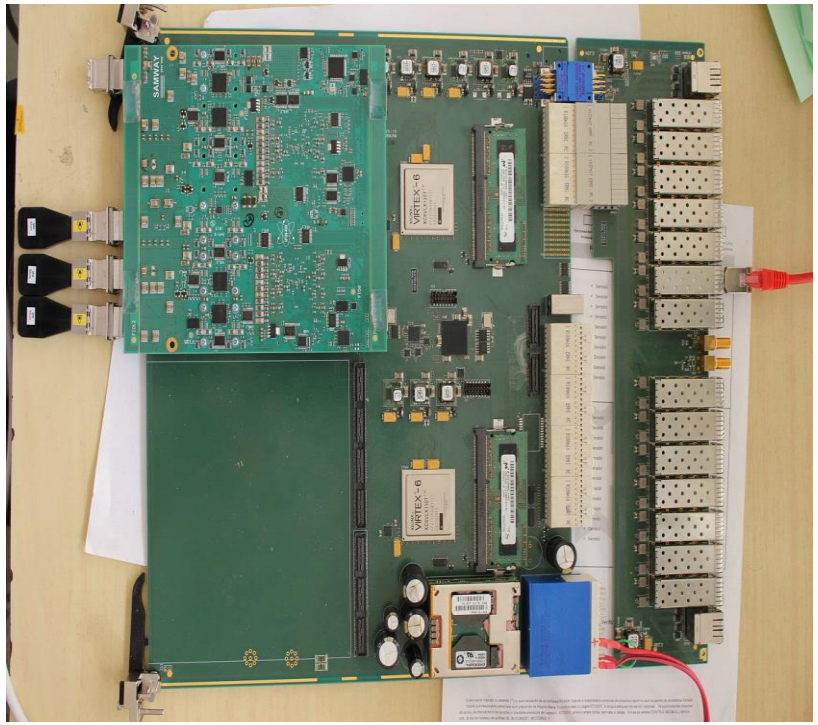
Trigger Processor hardware

- Critical interfaces have been tested and verified at Bucharest
  - 36 optical transceivers
  - Lateral communication between MM and sTGC FPGA for track candidate merging
  - Connections to carrier
    - Clocks
    - Ancillary function data
- HORX currently being used with ATCA carrier at Harvard to test MM Trigger processor algorithm using an internal ADDC emulator



Summary of Illinois Activities and Plans

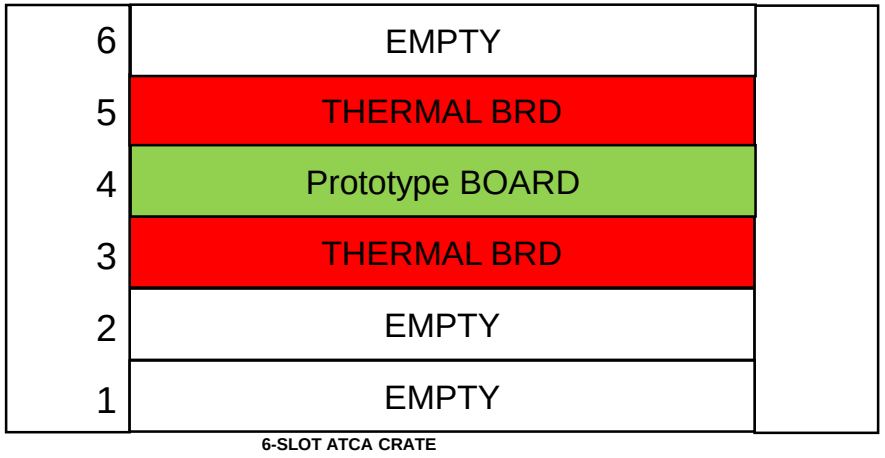
- Received a complete set of hardware
  - Mezzanine, ATCA Carrier, RTM,IPMC
- Hardware testing
  - Thermal tests
  - Remote FPGA programming
  - Data path
    - Mezzanine → Carrier → RTM
      - RTM provides GBT Link for FELIX (TTC, event monitoring and algorithm configuration)
      - RTM can also provide a Ethernet debug connection
- Monitoring Ancillary function Firmware & Software development



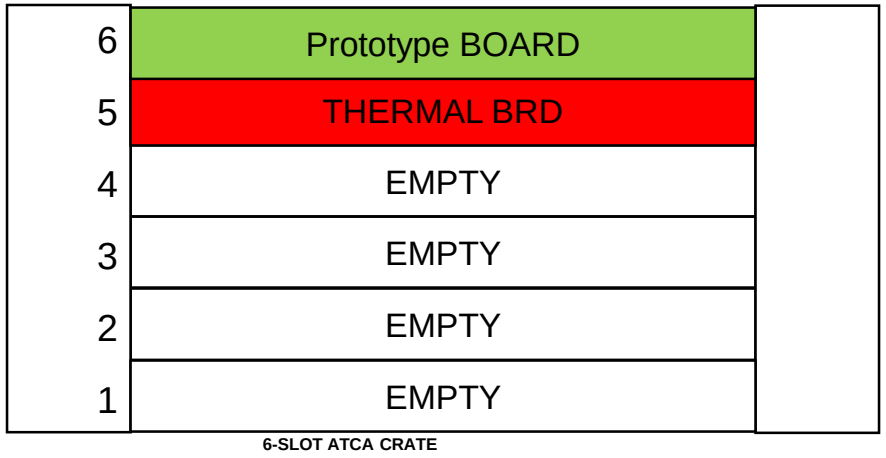
Thermal Testing

- Hardware configuration for thermal tests of prototype system
  - Trigger Processor hardware: Mezzanine card, Carrier blade, RTM, IPMC
  - Use thermal heat load boards to test board functionality with heat load of nearby boards
    - Two heat load boards produced in house
      - Deliver 200W or 400 W
    - Have an additional heat load board from COMTEL
      - Delivers a range 0-350W

heat load boards produced in-house



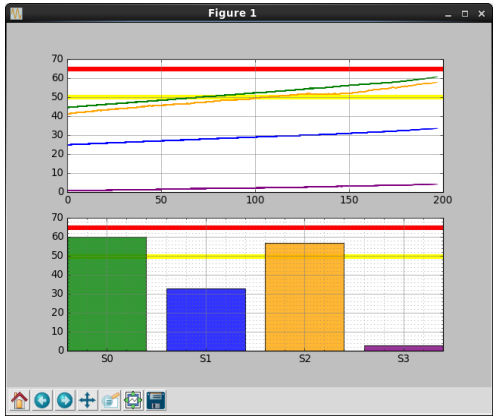
Middle-slot Test



Edge-slot Test

Thermal Test – Stand Status

- Temperature data recorded for analysis from sensors on thermal load boards and between them (air)
- Plan to add the temperatures from COMTEL prototype board (via IPMC)
- System mostly ready
  - waiting for delivery of new 6-slot crate
  - IPMC documentation needed

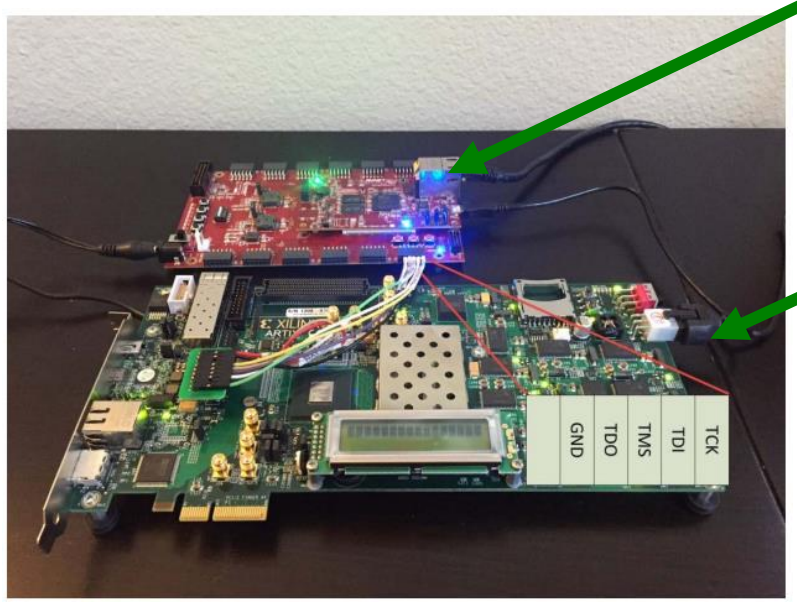


Temperature Readout software

Thermal test stand

Preliminary tests for FPGA programming

- Explored the possibility of replacing ATCA Carrier Spartan6 with a Zync processor running XVC for remote FPGA programming via RTM Ethernet connection
- Testing done using a Zync development board to program an FPGA on a Xilinx V7 development board
- Next steps:
  - Verify procedure with multiple FPGAs in a chain
    - Implement in ATCA carrier prototype hardware
  - Explore other options such as programming via IPMC
    - Awaiting IPMC documentation

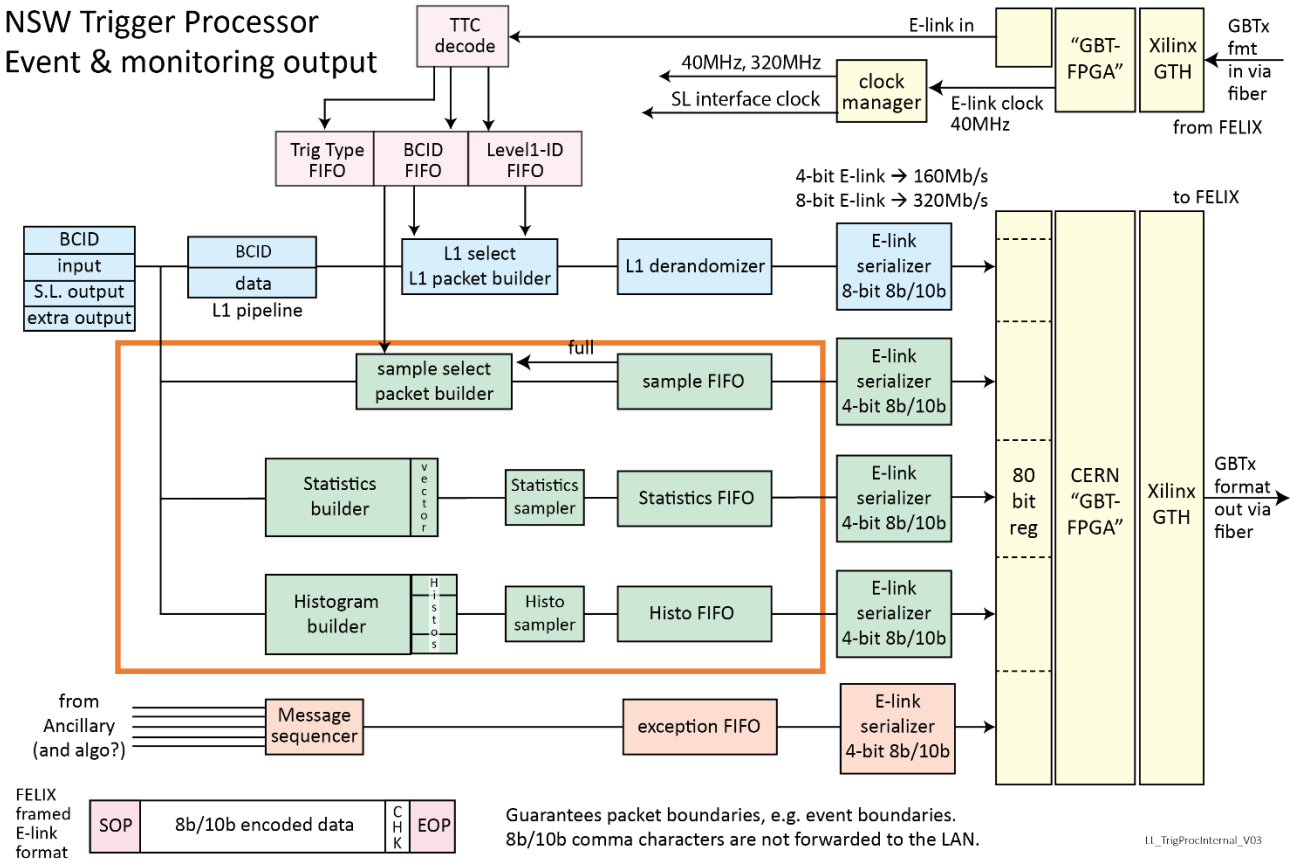


Zync processor used as XVC master

VC707 FPGA used as XVC slave

Monitoring Ancillary Functions

- The preliminary monitoring functions are defined in Ancillary Functions Specifications document
  - See document here
- Input needed for a complete specification
- Work ongoing on firmware implementation
  - focusing on MM first, will work on sTGC as well
  - Interface between MM Trigger algorithm and monitoring is being defined and implemented
  - Monitoring firmware developed using emulated Trigger Processor interface
- Monitoring software work ramping up
  - Working on ROOT based monitoring
  - Getting GNAM setup



Illinois Activity Plan – Summary

- Main goal is to test the prototype hardware and ensure that the prototype hardware satisfies the project's needs

1. Define the method to program and debug the FPGAs
    - Investigating remote access options
        - Regular network resources
        - Limited physical access (ATCA + USA-15 room)
        - Only Xilinx devices: XVC protocol is a possibility
2. Perform basic electric tests – power on crate + boards, etc
3. Perform thermal tests
4. Deploy the programming and debug methods
5. Verify data transfer to Carrier and RTM for Monitoring
    - In parallel work on the monitoring specifications and on the software
6. Contribute to remaining tests

sTGC: current trigger processor activities

- Deserializer input and serializer output
- Data distributer stage to prepare input to the algorithm
  - Sometimes input for a single candidate is split over two fibers
- The core algorithm
- Current prototype is PC-based commercial FPGA card.
  - Deploy ATCA-based system with the prototype NSW Trigger Processor

Next

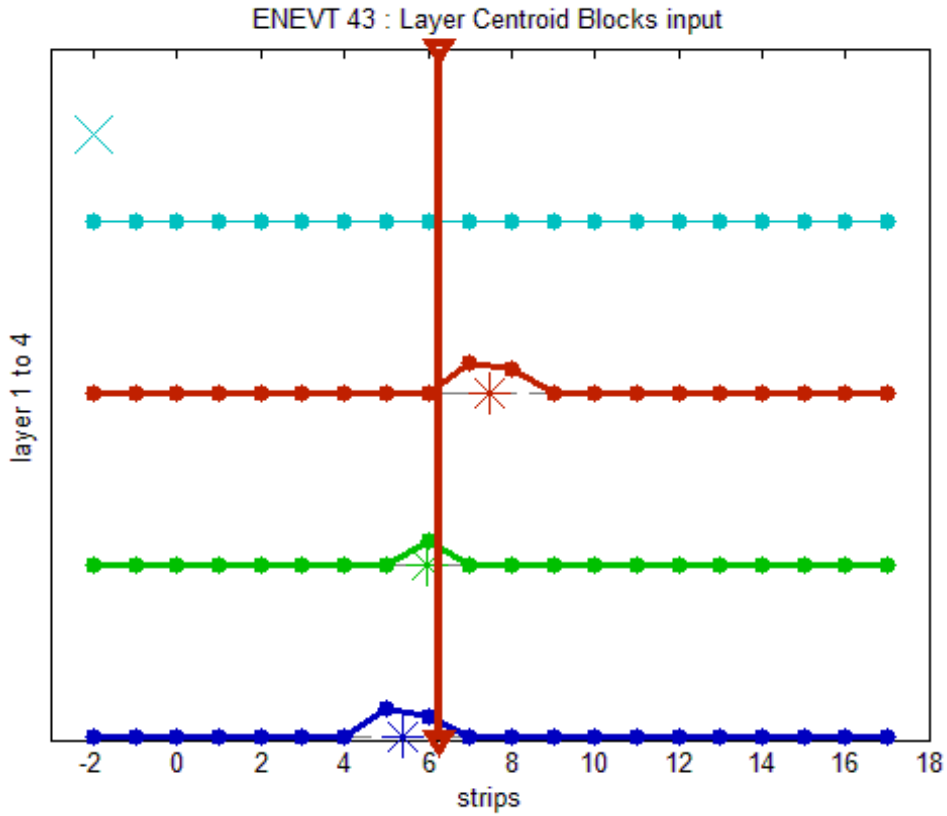
- Ancillary functions:
  - Level-1 logic
  - Ethernet debug path via carrier/ RTM
- Alignment corrections
- Simulation to understand performance

MM Trigger Processor current activities

- Timing closure and hardware implementation for current algorithm
- Understand failed simulation muon events and validate dtheta and ROI algorithm results.
- Expand algorithm from 1/16 sector(2 GBT links) to full sector. (32 GBT links)
- Alignment corrections
- Implement optimized GBT interface on MM Trigger Processor hardware (HORX)
- Hardware integration
- Monitoring data ancillary function interface

Backup

sTGC: Centroid algorithm concept (one event example)



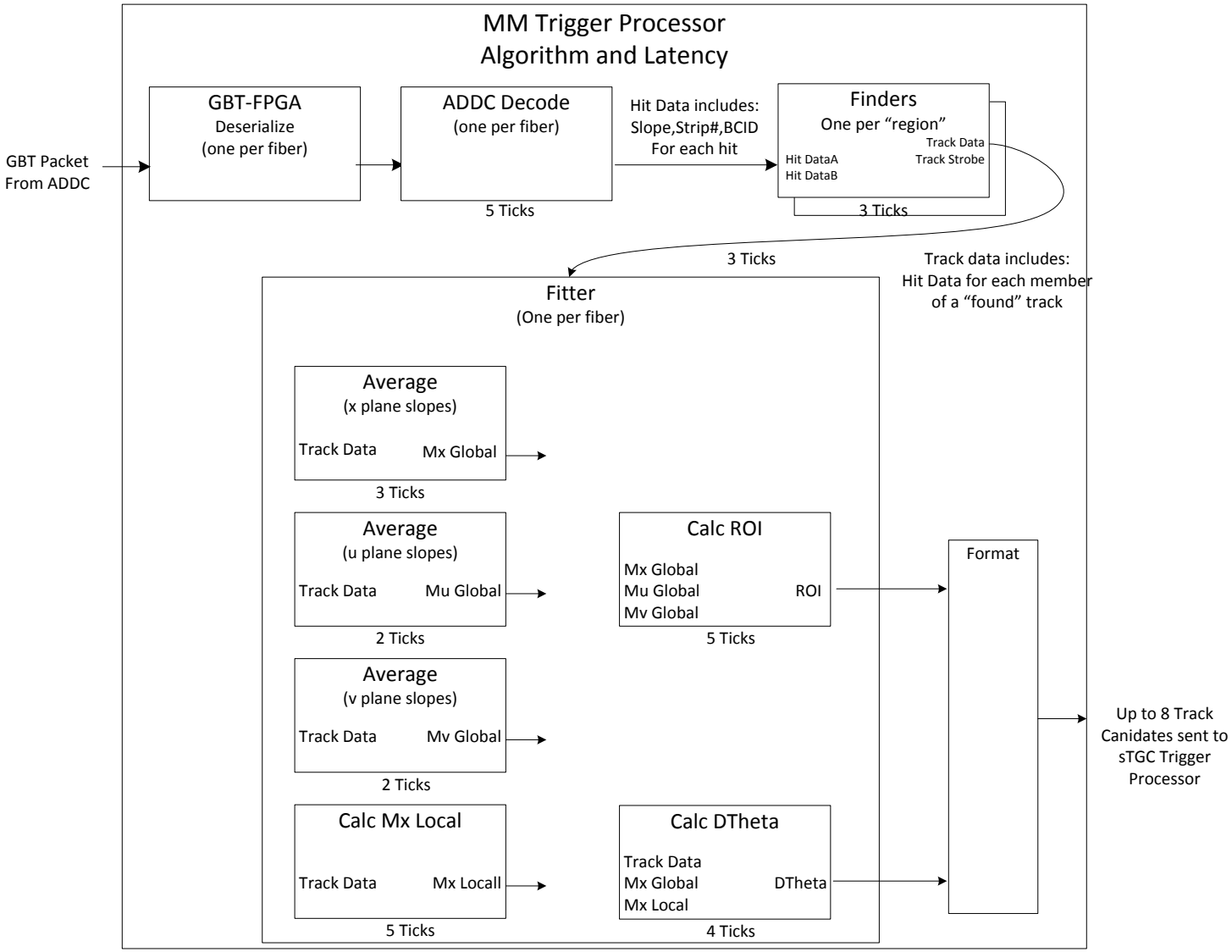
Layer centroid algorithm (per event):

1. We find a 5 strip window of active strips (if there are more then 5 active strips in event, layer centroid is considered invalid for now)

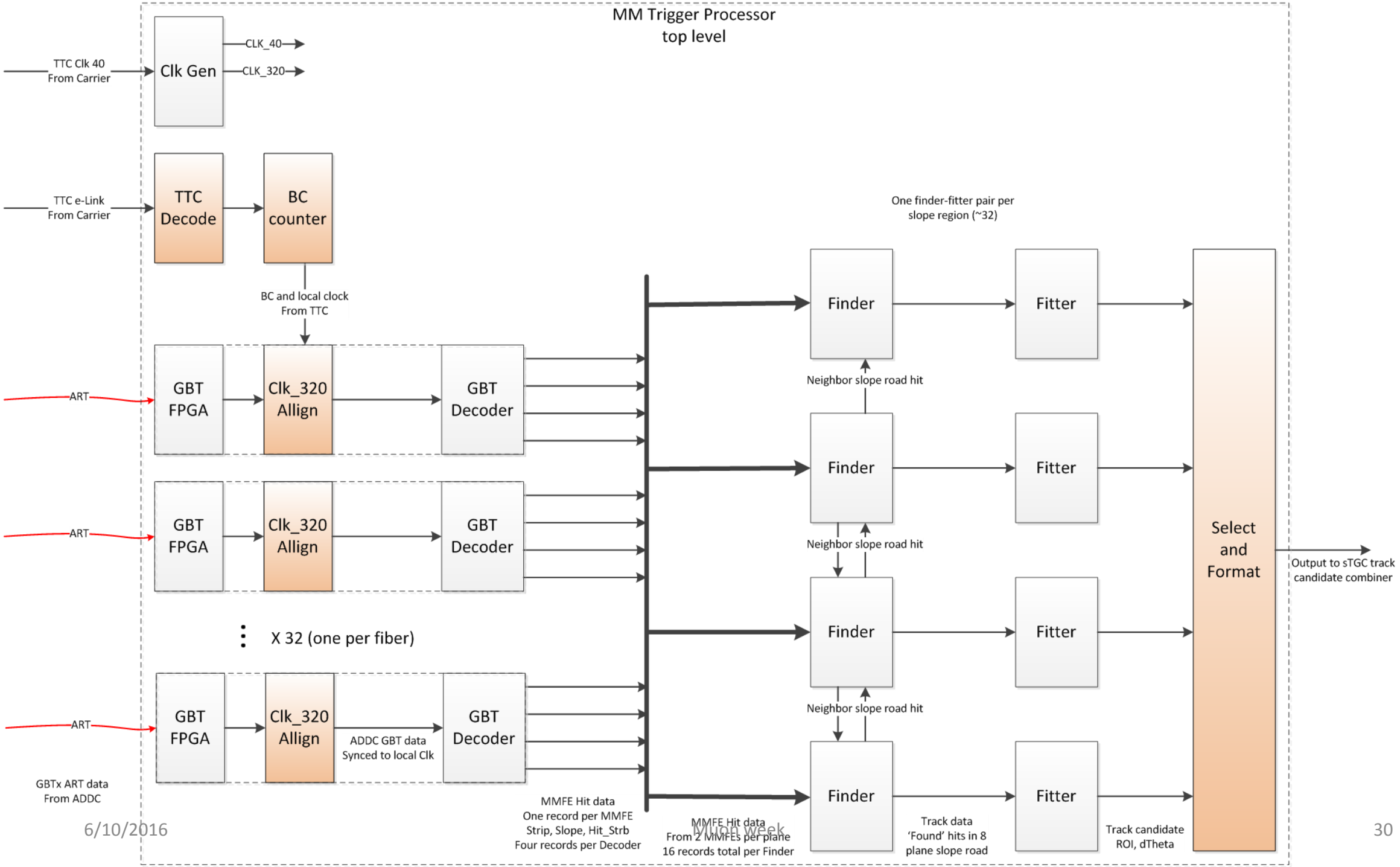
2. Layer Centroid $= \Delta + \frac{\sum_{n=1}^{5} n \times s_n}{\sum_{n=1}^{5} s_n}$, when Δ is a 5-strip window offset within 20 strips, s_n is a value if strip #n in nsec, n is a strip number within the 5-strip window

Quadruplet centroid

$QC = \frac{\sum_{n=1}^{N} C_n}{N}$, when N is the number of valid centroids, C_n is a value of Centroid n.

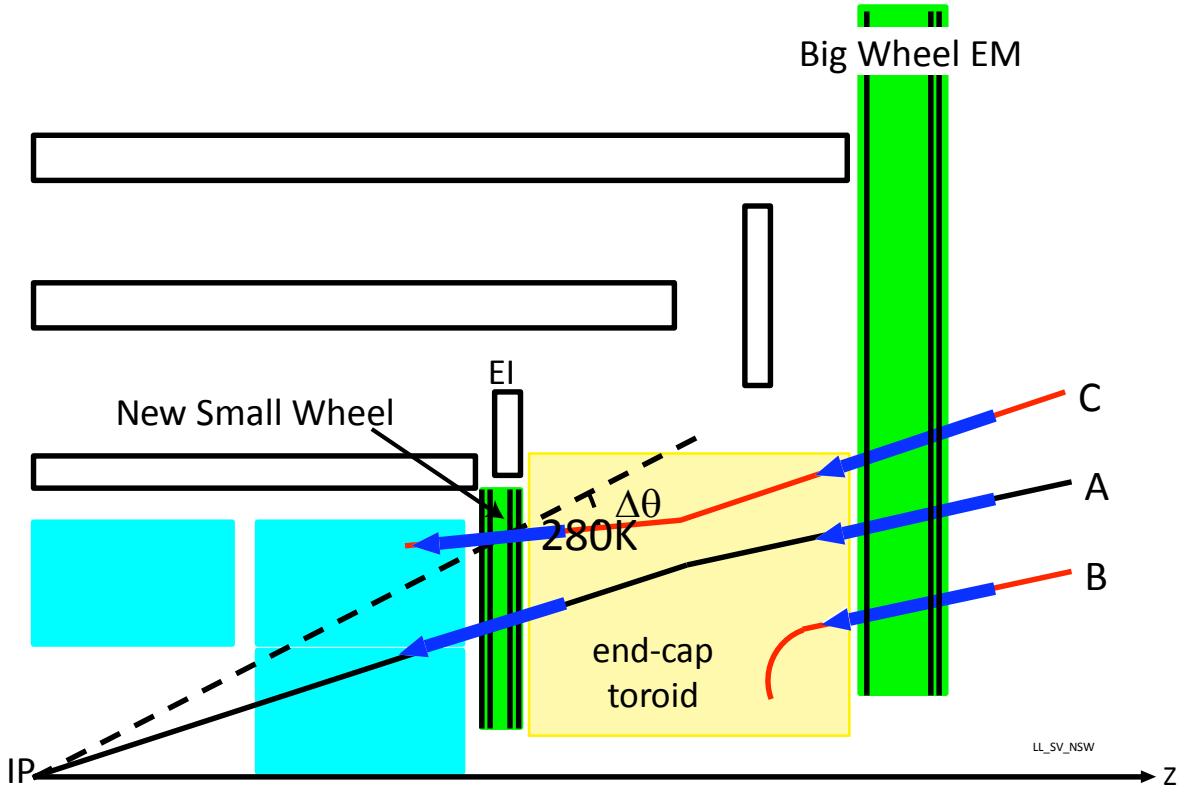


Algorithm Critical path total 20 clock ticks


MM Trigger Processor
top level
TTC Clk 40
From Carrier
Clk Gen
CLK_40
CLK_320
TTC e-Link
From Carrier
TTC
Decode
BC
counter
BC and local clock
From TTC
One finder-fitter pair per
slope region (~32)
ART
GBT
FPGA
Clk_320
Allign
GBT
Decoder
Finder
Fitter
Neighbor slope road hit
X 32 (one per fiber)
Select
and
Format
Output to sTGC track
candidate combiner
ADDC GBT data
Synced to local Clk
GBTx ART data
From ADDC
MMFE Hit data
One record per MMFE
Strip, Slope, Hit_Strb
Four records per Decoder
MMFE Hit data
From 2 MMFEs per plane
16 records total per Finder
Track data
'Found' hits in 8
plane slope road
Track candidate
ROI, dTheta

NSW Trigger Processor Overview

- Phase I upgrade: Increased backgrounds, but must maintain existing trigger rate
- Find muon candidates that originate from the IP
- **Challenge is latency**

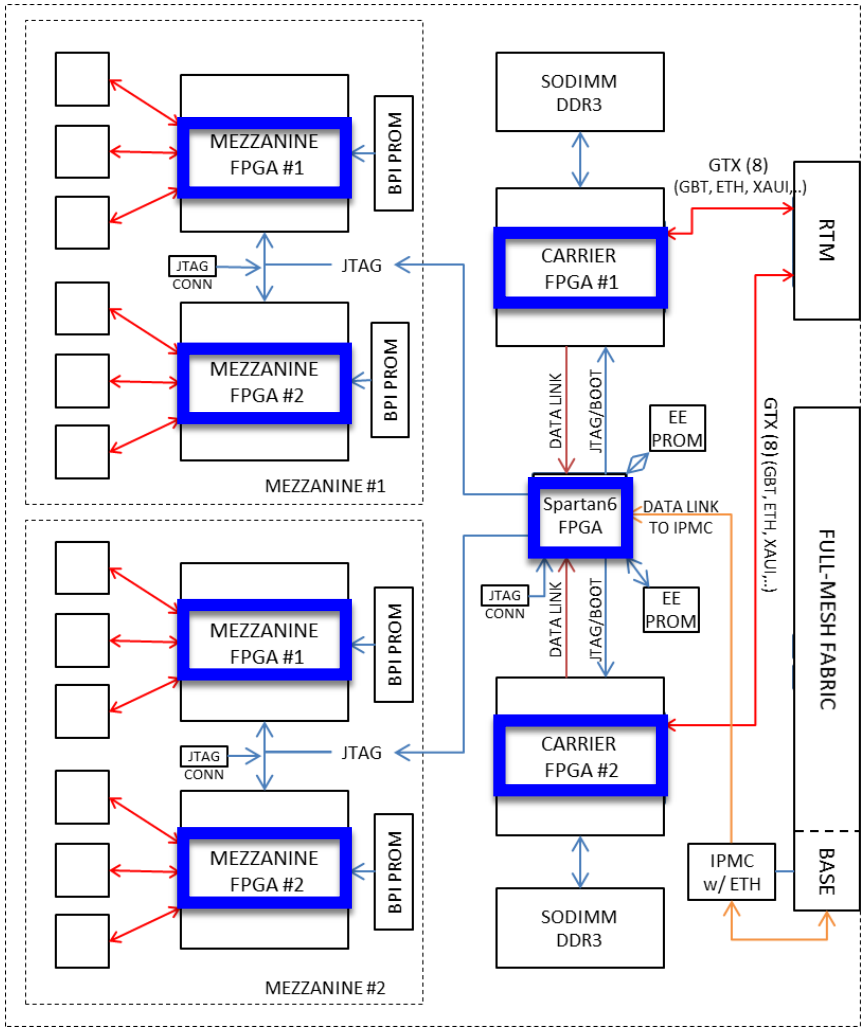


Δθ: Angle relative to 'infinite momentum track' — resolution goal < 1 mrad

NSW
Micromegas and sTGC
Track segments
1.3 < |η| < 2.7

BW
TGC
Track segments
1.0 < |η| < 2.4

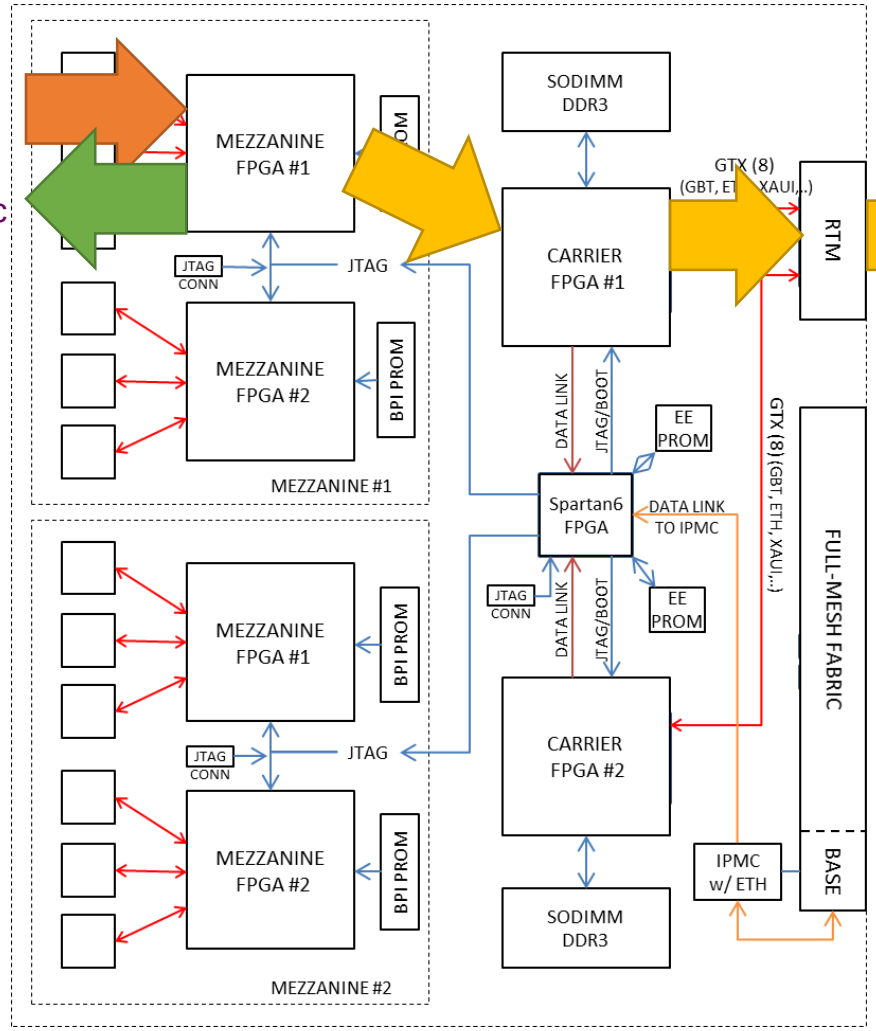
FPGA Programming



HORX prototype diagram

- Several FPGAs on Mezzanines and carrier
  - Investigating how to access the FPGAs from outside of the ATCA crate
  - Investigating options to program all the FPGAs remotely
- ATCA carrier boards will be different, mainly because FPGAs on carrier to be replaced
  - Spartan6 FPGA not supported in Xilinx Vivado IDE
  - Xilinx 6 series FPGAs on carrier to be moved to 7 series to match Mezzanine card FPGAs

Data Path through Carrier and RTM



To FELIX: Readout
Monitoring TTC Config

- Most I/O is to Mezzanine card FPGA
  - Input from MM/sTGC
  - Output to sector logic
- Working on testing the data path through carrier and RTM
  - Implementing for monitoring

HORX prototype schematic