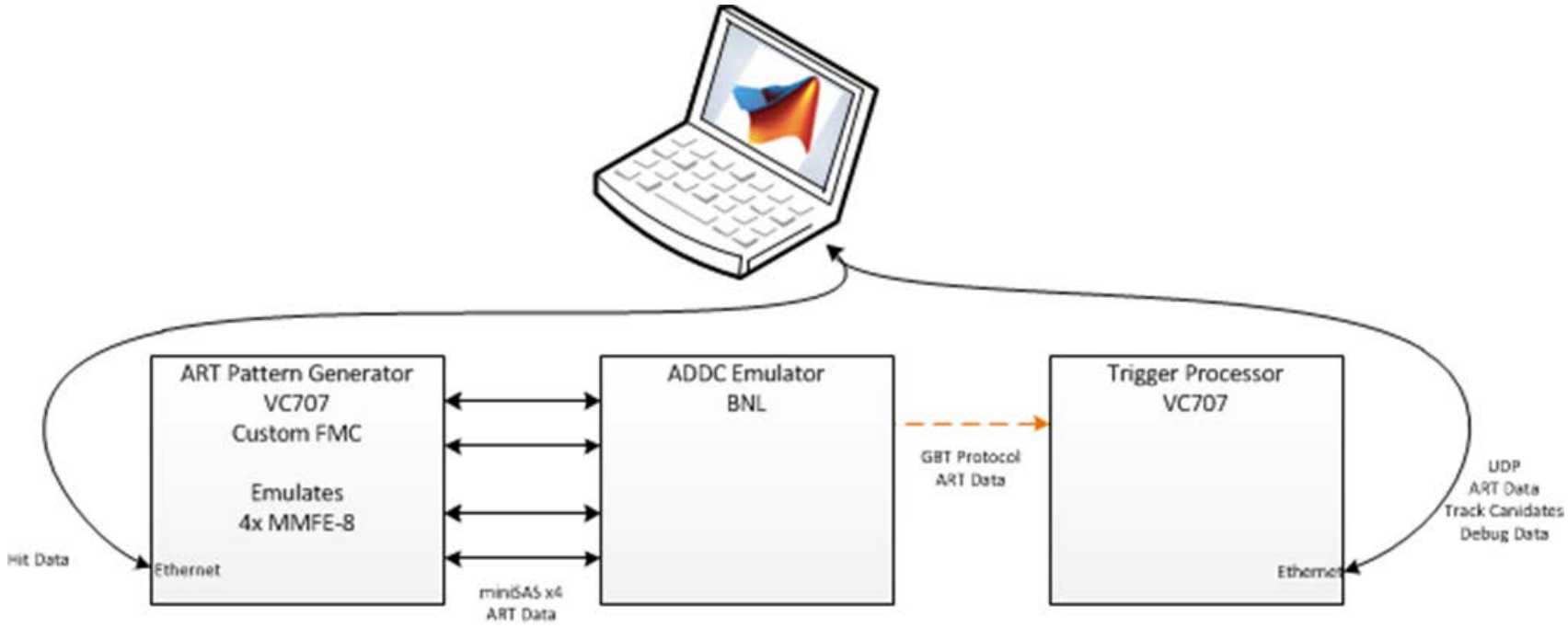
MM Trigger Processor Update

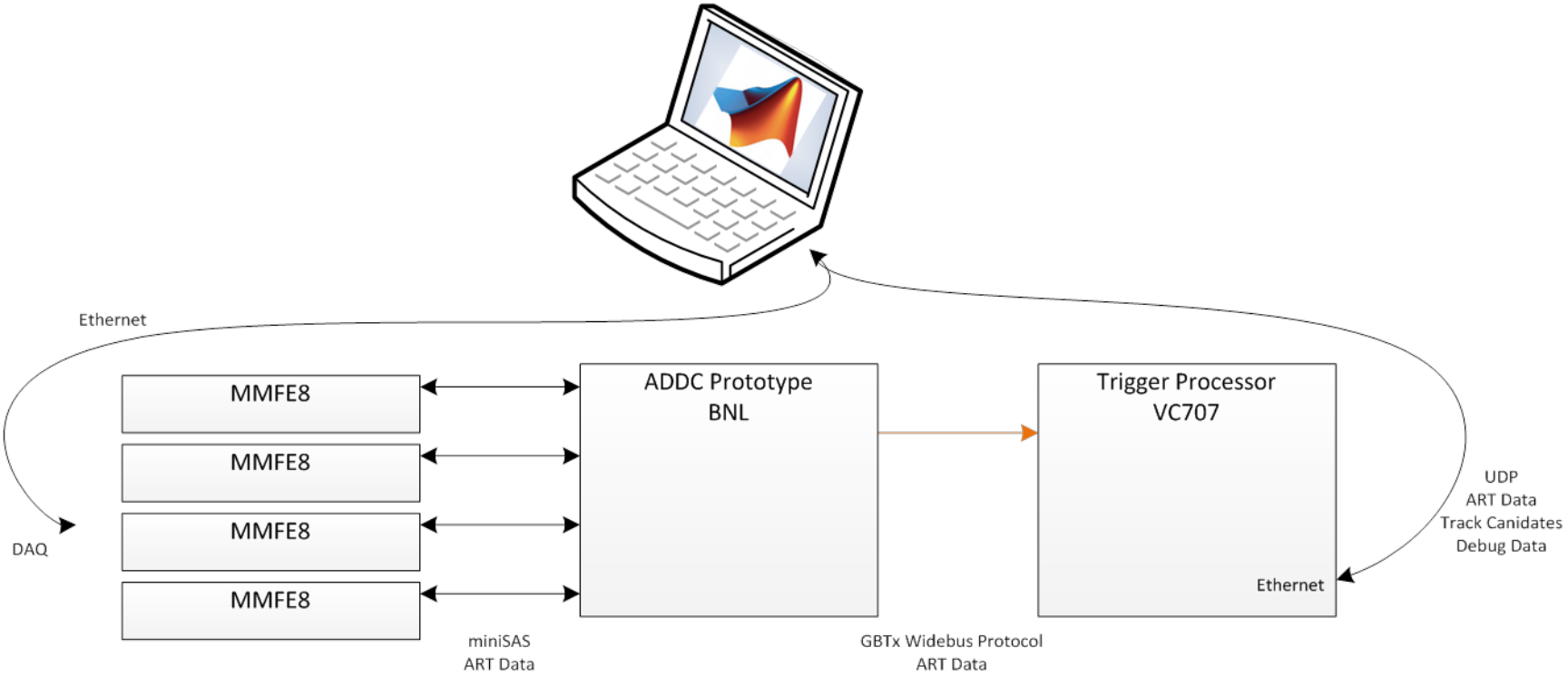
MMFE8 ART Data

- Observed ART data from MMFE8 VMM using charge injection to various VMM / channels.
- Sourced 160 Mhz clock signal from MMFE8
- Ready to connect MMFE8 to existing test stand (Previously tested using ART Pattern Generator)

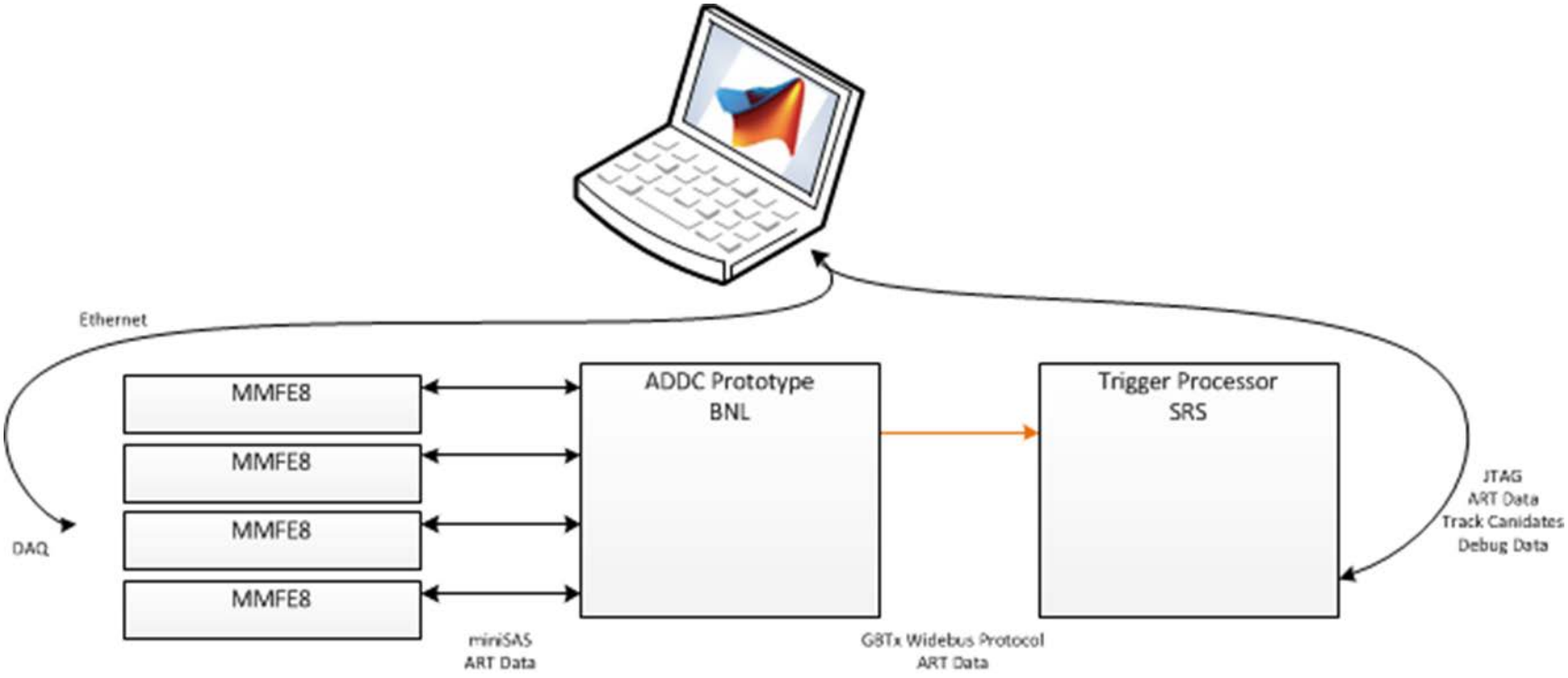
Existing Test Stand



MMFE8 ART source



SRS Trigger Processor



Trigger Processor Firmware

- Implementing GBT with SRS as a target
- Reused Sorin's AMC PLL configuration for clocks
- David is working on Algorithm HDL simulation and bug fixes as well as Matlab DAQ code for software and hardware simulation.