ATLAS NOTE

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Specification of the Ancillary Functions of the ATLAS New Small Wheel Trigger Processor

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Abstract

Specification of Ancillary Functions of the New Small Wheel Trigger Processor

Contents

1 Introduction

In addition to implementing the trigger algorithms for the MM and sTGC systems, the NSW Trigger Processor has to perform several ancillary functions. These include time synchronization, configuration, monitoring and debugging mode, among others. Several functions are common to both MM and sTGC and their firmware can be shared as well-defined packages. These functions introduced below:

Interface for algorithm and other configuration parameters Parameters for the algorithms must be stored at runtime. Examples are the ?? and other cuts, the BCID offset, alignment parameters, the parts of the detector to be considered as disabled, road size, etc. Configuration can be done via Ethernet and the carrier board or via an E-link from FELIX that is available on the link that brings the TTC information. Read back of the parameters must also be provided.

Note: if there are a large number of configuration parameters it may be advisable to use serial bus to set them locally to where they are used.

TTC interface FELIX provides the following TTC information on an E-link from the 8-bit TTC broadcast packet and the raw B-channel (for the Trigger Type):

L1A	BCR	ECR	Brcst[2]	Brcst[3]	Brcst[4]	Brcst[5]	B-chan

The E-link provides the 40 MHz BC clock which is used to synchronize the output to the Sector Logic. This also includes the logic to synchronize a local bunch-crossing ID to the Sector Logic by means of a configurable BC offset loaded on BCR into a local BCID register. Note that the various input links will not have the same phase and may not even be matched to the same BC clock. Input processors must ensure that all sources are aligned to the same BC clock. Both technologies include a BCID or its low bits in the packet sent on every bunch-crossing. Should the offset of this BCID from the local BCID differ from what is expected, an exception message (see below) must be sent. The firmware to do this alignment is not shared.

Clocks for the serial links and the 320 MHz algorithm clock must be generated from the 40 MHz BC E-link clock.

Level-1 output buffer For bunch-crossings in which at least one segment is found, the input data and the output segment data that is sent to the Sector Logic is stored, along with its BCID for later matching to the BCID of a Level-1 Accept. Those bunch-crossings that have Level-1 Accepts (and possibly those preceding and following) are transferred to the Level-1 output buffer (aka derandomizer). The data must be stored for the duration of the Level-1 latency. The output bandwidth should be sufficient for the rather small fixed input and output data lengths at the full Level-1 rate of 400 kHz. If not, this logic could provide a BUSY output to the RODBUSY system when its output buffer becomes close to full.

Monitored event buffer A random sample of complete events is collected for sending to a monitoring process. Example criteria are: any event, event with at least one segment found, events with segments outside the ?? cut, ...) The data buffered as one event includes all the input data and the output segment data that is sent to the Sector Logic for a given BC.

Statistics buffer Statistics are continuously collected and periodically transferred to the Statistics buffer. Statistics includes the number of bunch-crossings that have candidates that are not accepted by Level-1, their distribution in R-ϕ?, the multiplicity of segments per bunch-crossing, etc.

Exception buffer In the course of processing, exceptional conditions may be found, usually due to corrupted data. A convenient way to handle these is to store an exception code and some context data into a buffer which will be passed to the monitoring PC via FELIX.

Playback mode to fake input links For development and testing we require that simulated data can be injected in place of the data received by the links to the Front End. One way to do this is via an E-link from FELIX that is available on the link that brings the TTC information. Play back can be at full speed, i.e. 40 MHz.

Segment output to Sector Logic and to the 'other' detector Segments are sent out either to the Sector Logic via the FPGA serializer or to the 'other' detector via a parallel LVDS bus. The candidate packet to be sent to the Sector Logic must be pre-pared from the segments found. Clones must be made and the output links to the Sector logic must be driven. If the segments found are to be sent to the 'other' detector's Trigger Processor, the segment data must be sequenced out onto the parallel LVDS bus.

Merge buffers into the output GBT link to FELIX The Level-1, Monitoring, Statistics and Exception buffers are merged, using different E-links onto a fiber link to FELIX. FELIX then routes them to the ROD and Monitoring PCs.

Front End input links Since the MM uses the GBTx to transmit the data from the Front End and the sTGC uses native FPGA serializers, the link interface firmware cannot be shared.

Note that the monitoring of board temperatures and voltages is done by the ATCA Shelf Manager using IPMI.

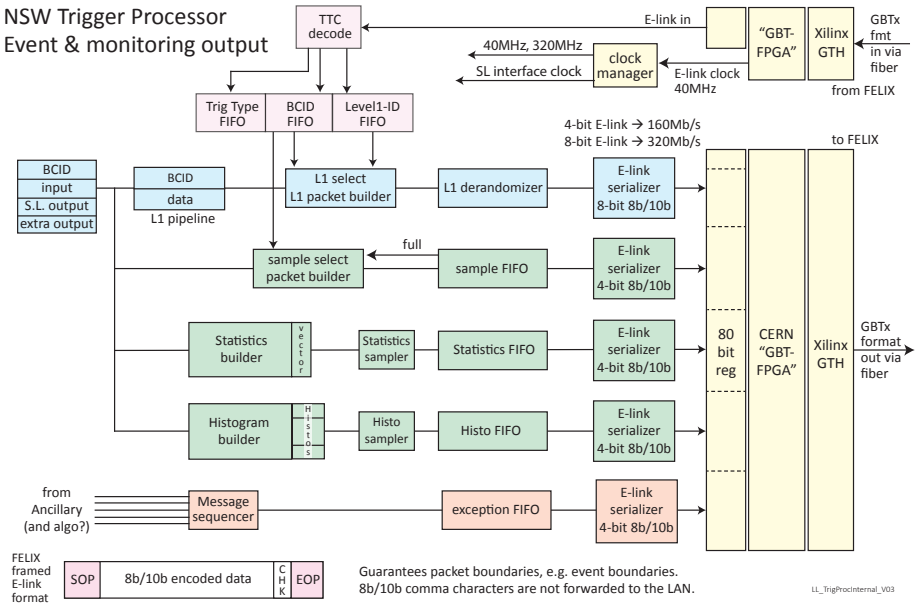

Figure 1

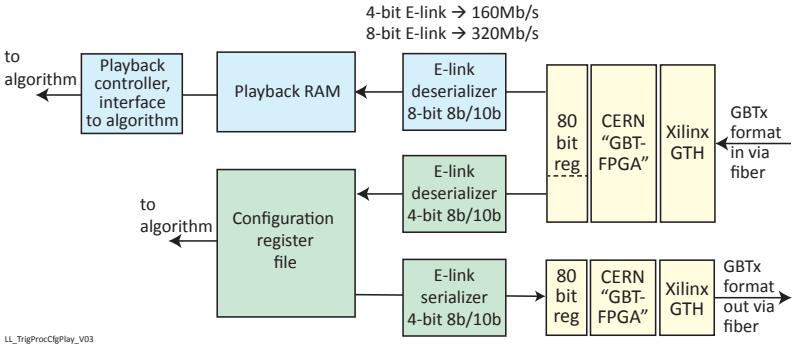

Figure 2

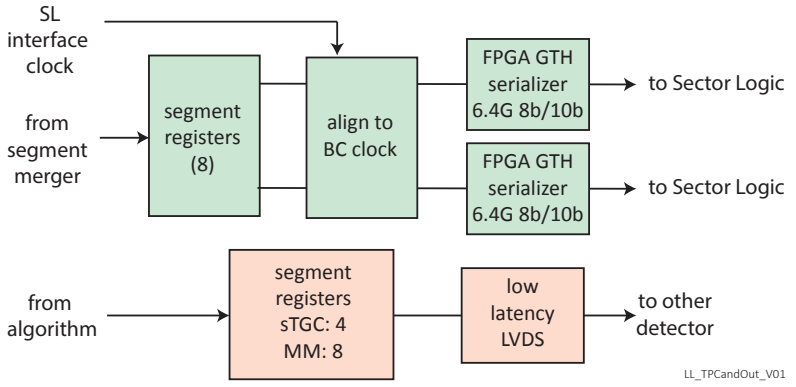

Figure 3

2 Interface for algorithm and other configuration parameters

3 TTC interface

4 Level-1 output buffer

5 Monitored event buffer

As part of the debugging features of the trigger processor, a sample select packet builder will be included for the purpose of collecting random samples of events passing through the trigger processor.

Event Criteria The first main question in collecting a sample events is to define what will be considerd as an 'event' to be potentially collected. Possible criteria for an 'event' include:

1. any set of coincidences
2. any set of coincidences passing the coincidence threshold
3. any set of coincidences passing the trigger algorithm
4. any set of coincidences passing the trigger algorithm plus addition constraints

The choice regarding which set of criteria will provide the most useful set of sample events should be made with the help of simulations, which should provide information regarding the relative amounts expected to fit each of the definitions previously listed.

Randomization Modes Once the event criteria have been chosen, another question is determining how to choose which events will be written into the buffer out of the full set of possible events that pass the event criteria. It must be made sure that this randomization mode does not introduce any manufactured bias in the collected events. Possible randomization modes include:

1. collecting the first event every T amount of time
2. collecting every Nth event
3. collecting X number of events in a row every T amount of time
4. collection X number of events in a row and skipping the next Y events

The third and fourth options have the potential to provide information regarding any unwanted correlation between successive events possibly due to timing errors.

Data and Buffer Format The data format of the collected event has not yet been decided. Depending on the event criteria, the data could include the BCID, number of coincidences, $\Delta\theta$, ROI, VMM signal origin, or any other input/output/signal of the trigger processor.

Functionality The sample select packet builder should have the ability to switch between randomization modes and event criteria. Additionally, the sampled events should be able to be read out or reset/cleared at any point in time.

6 Statistics buffer

Statistics regarding the trigger processor will also be gathered for debugging and monitoring purposes. These statistics are split into a set of simple counters and histograms.

Counters Some possible values to be counted are listed below:

- Coincidences
- Number of instances coincidence threshold is met
- Candidates passing trigger algorithm
- Negative local slopes calculated
- Number of instances of data overflow

If possible, the coincidence counter will count X, U, and V coincidences separately. The ratio between the total coincidences, number of instances the coincidence threshold is met, and candidates passing trigger algorithm is expected to remain relatively consistent and thus provide useful debugging information in the case of significant deviations from the expected ratios. Additionally, the number of negative local slopes calculated by the trigger algorithm will provide information on background effects. For example, an abnormally large number of negative local slopes calculated could be an indication of detector misalignments or an unexpected/new source of background hits. Also, the data overflow counter will provide information about how much potential data has been lost due to the cap set at 8 VMM hits per BC.

Histograms Some possible values for which histograms could be made are listed below:

- slope road coincidence distribution
- $\Delta\theta$ distribution
- ϕ distribution
- multiplicity of VMM ART signals per BC
- types of track candidates passing trigger algorithm
- signal origin

Based on symmetry, it should be expected that the ϕ distribution be a flat distribution showing no preference towards any value or range. Similar symmetry arguments can shed light on the expected distributions for other values such as the signal origin. Additionally, simulations can be used to find the expected distributions for the other histograms.

Data and Buffer Format Each counter can be made using a simple bus of a width appropriate for the expected range to be counted. The first four bits of the bus can be used as a 'counter ID' specifying which value is being counted in that bus.

Functionality The statistics buffers should be able to be read and rest at any point in time. Additionally, the different counters and histograms should be able to be activated/deactivated at any point.

7 Exception buffer

8 Playback mode to fake input links

9 Segment output to Sector Logic and to the 'other' detector

10 E-link processors

11 Front End input links

12 Work Breakdown

The first step is to define the data formats for both detector types:

- Input from FE format for MM and sTGC
- Output to Sector Logic
- Extra per BC output format for MM and sTGC
- Level-1 event output format for MM and sTGC

The Work Breakdown tasks are shown in Tables 1 and 2.

Table 1: Functions that are the same for the two technologies

	Task	**length**	**assigned**
1.1	TTC FIFOs & clock managers		Harvard
1.2	E-link serializers & interface to the GBT-FPGA package		Weizmann
1.3	Level-1 selector		Weizmann
1.4	Message sequencer and exception FIFO		
1.5	Candidate output to the Sector Logic & to the 'other' trigger processor		
1.6	FPGA configuration via the ATCA and Ethernet		Illinois
1.7	GBT-over-ethernetfor development		

Table 2: Functions that are slightly different for the two technologies

	Task	**length**	**assigned**
2.1	Level-1 packet builder and derandomizer		Weizmann
2.2	Sample select packet builder and sample FIFO		Illinois
2.3	Statistics builder and statistics FIFO		Illinois
2.4	Histogram builder and histogram FIFO		Illinois
2.5	Playback controller and RAM		
2.6	Configuration register file		

For the configuration register file, the paramaters for the algorithms are different; the paramaters for the ancillary functions are the same. There are issues regarding the number of copies of algorithm parameters and if some could be in RAM LUTs as opposed to registers.

The input from the Front Ends and their timing alignment are significantly different for the two technologies and so may be developed by different people.

Table 3: Input data deserializing and preparation of input data for the algorithm and monitoring

	Task	**length**	**assigned**
3.1	sTGC TDS/Router data		Weizmann
3.2	MM ART data		BNL

Appendix

In a paper, an appendix is used for technical details that would otherwise disturb the flow of the paper. Such an appendix should be printed before the Bibliography.

Auxiliary material