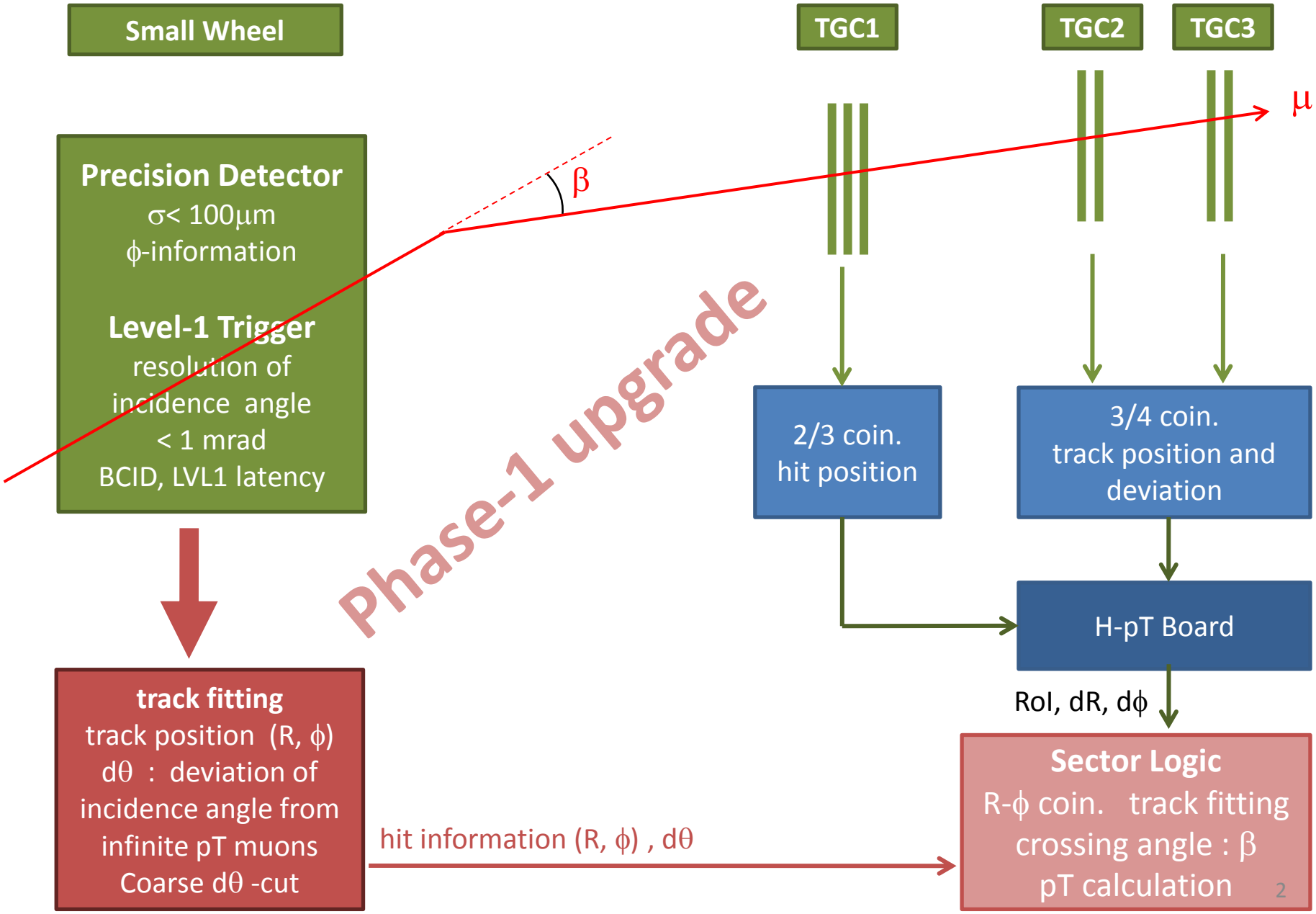
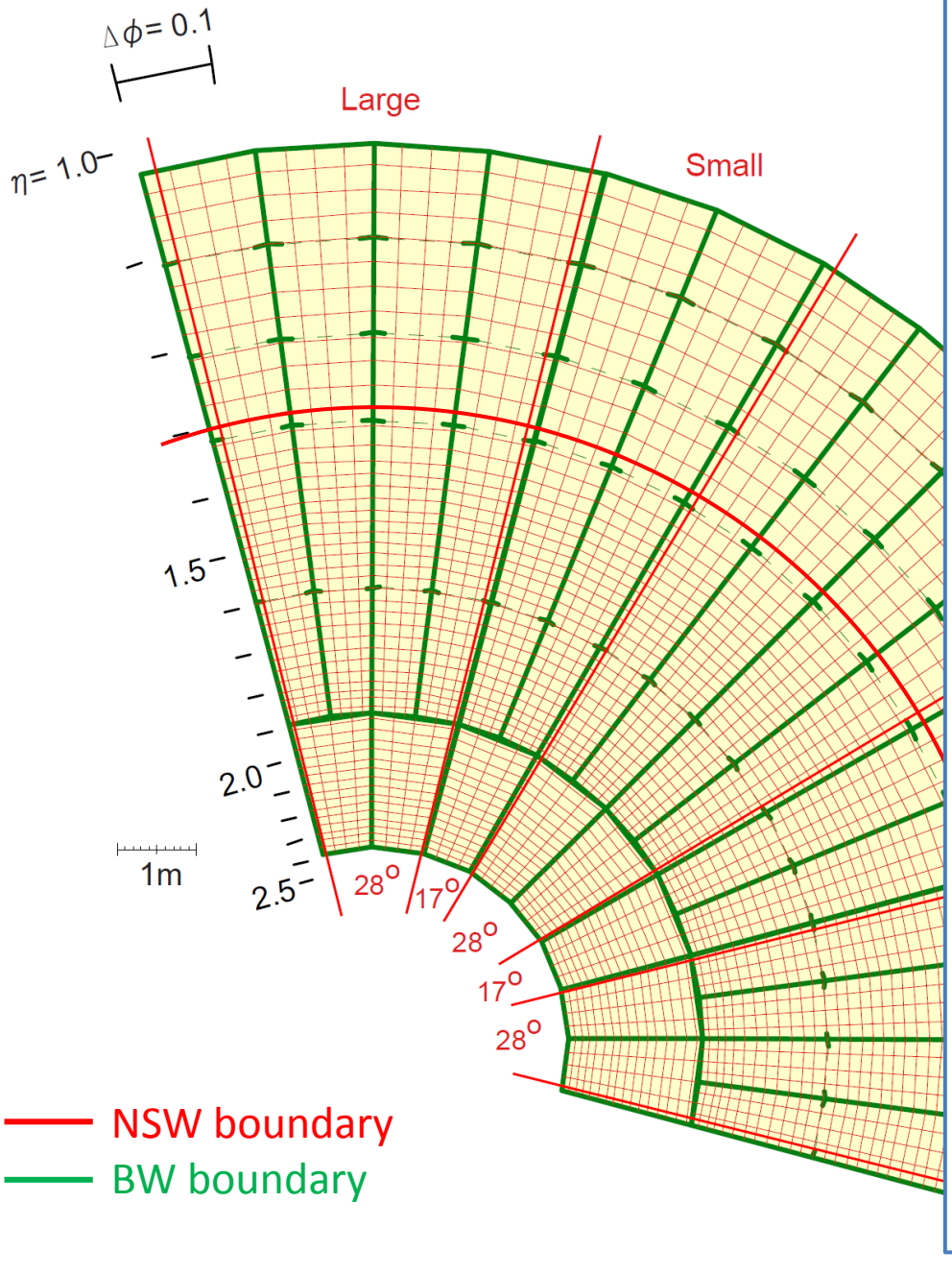
Trigger processor

John Huth
Harvard

NSW + TGC of BW's



Matching between BW sector and NSW, bit format



NSW coverage : η = 1.3 – 2.4
# of RoI's in Large SW Sector : 560
# of RoI's in Small SW Sector : 366

Position info.
ϕ/η : 0.02-0.03 precision (RoI size)
β calculation : need η ~ 0.01

# of granularities per SW Sector < 1024

# of bits per track is 16-bit
- Position : 10-bit
- dθ : 5-bit, 1mrad resolution
- hit flag : 1-bit
- Total: 16-bit

# of tracks per fibre @ 40MHz
- 4 tracks @ 40 MHz
- (16+4)-bit x 4 x 40MHz = 3.2 Gbps

Max. # of tracks per Large SW Sector
- up to 8 or 12 tracks, 2 or 3 fibres

Max. # of tracks per Small SW Sector
- up to 4 or 8 tracks, 1 or 2 fibres

Present TGC Level-1 Trigger	nsec	CLK	Total CLK
TOF from interaction point to TGC	65	2.5	2.5
Propagation delay on wire/strip	15	1	3.5
TGC response	25	1	4.5
ASD	10	0.5	5
Cable to PS-Board (12.5m max.)		2.5	7.5
Variable Delay, Bunch ID, OR		2	9.5
Variable Delay		1	10.5
3/4 Coincidence Matrix or 2/3 Coin.		2	12.5
LVDS			
Cable			
LVDS			
Variabl			
H-pT			
G-Link			
Optical Fibre to USA15 (90m max.)		18	41
Optical Rx + G-Link Rx (HDMP-1034A)		2.5	43.5
Sector Logic		8	51.5
Cable to MUCTPI (10m)		2	53.5
MUCTPI (4 + variable)		11	64.5
Cable to CTP (2.4m)		0.5	65
CTP (5 + varable[0-11])		6	71
Cable to LTPi (10m)		2	73
LTPi + LTP + TTCvi + TTCex		2	75
Variable Delay		2	77
Optical Cable to TGC frontend (110m)		22	99
TTCrq + fanout		3	102
Cable to PS-Board (5m max.)		1	103
			2.575μsec

Small Wheel Detector + TGC (BW)	nsec	CLK	Total CLK
TOF from interaction point to SW (10m)	34	1.5	1.5
Propagation delay along wire	25	1	2.5
Detector Response		X	X+2.5
ASD	10	0.5	X+3
Signal Processing		Y	X+Y+3
Serializer (64-bit/clk,3.2Gbps) + Optical Tx		2	X+Y+5
Optical Fibre Cable (90m)		18	X+Y+23
Optical Rx + De-ser. (64-bit/clk,3.2Gbps)		2	X+Y+25
Signal Processing		Z	X+Y+Z+25
Serializer (64-bit/clk,3.2Gbps) + Optical Tx		2	X+Y+Z+27
Optical Fibre Cable (5m)		1	X+Y+Z+28
Optical Rx + De-ser. (64-bit/clk,3.2Gbps)		2	X+Y+Z+30
			44
SW - TGC(BW) combined HERE			
New Sector Logic			
TGC R-phi coin.(LUT) MDT-TGC coin.		3	47
crossing angle calculation		3	50
pT calculation (LUT)		3	53
pT encoding		1	54
Serializer (64-bit/clk,3.2Gbps) + Optical Tx		2	56
Optical Fibre Cable to MUCTPI (10m)		2	58
MUCTPI (4 + variable)		10	68
Cable to CTP (2.4m)		0.5	68.5
CTP		6	74.5
Cable to LTPi (10m)		2	76.5
LTPi + LTP + TTCvi + TTCex		2	78.5
Variable Delay		2	80.5
Optical Cable		22	102.5
TTCrq + fanout		3	105.5
Cable to Frontend Electronics		1.5	108
			2.675μsec

Rendezvous at 44 ticks in the front of SL

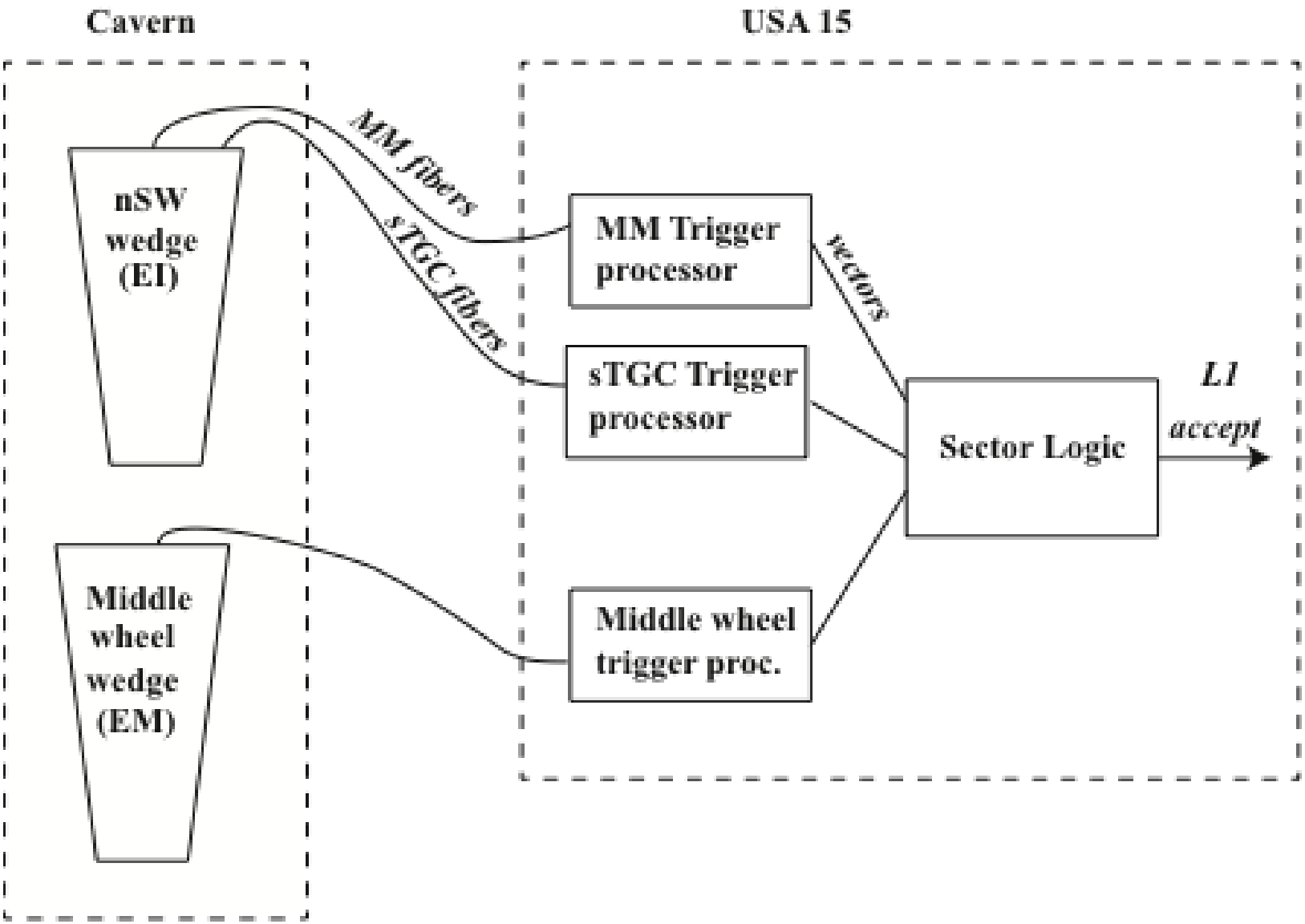
New SL : 10 ticks

Requirements to Trigger Processor of NSW detector

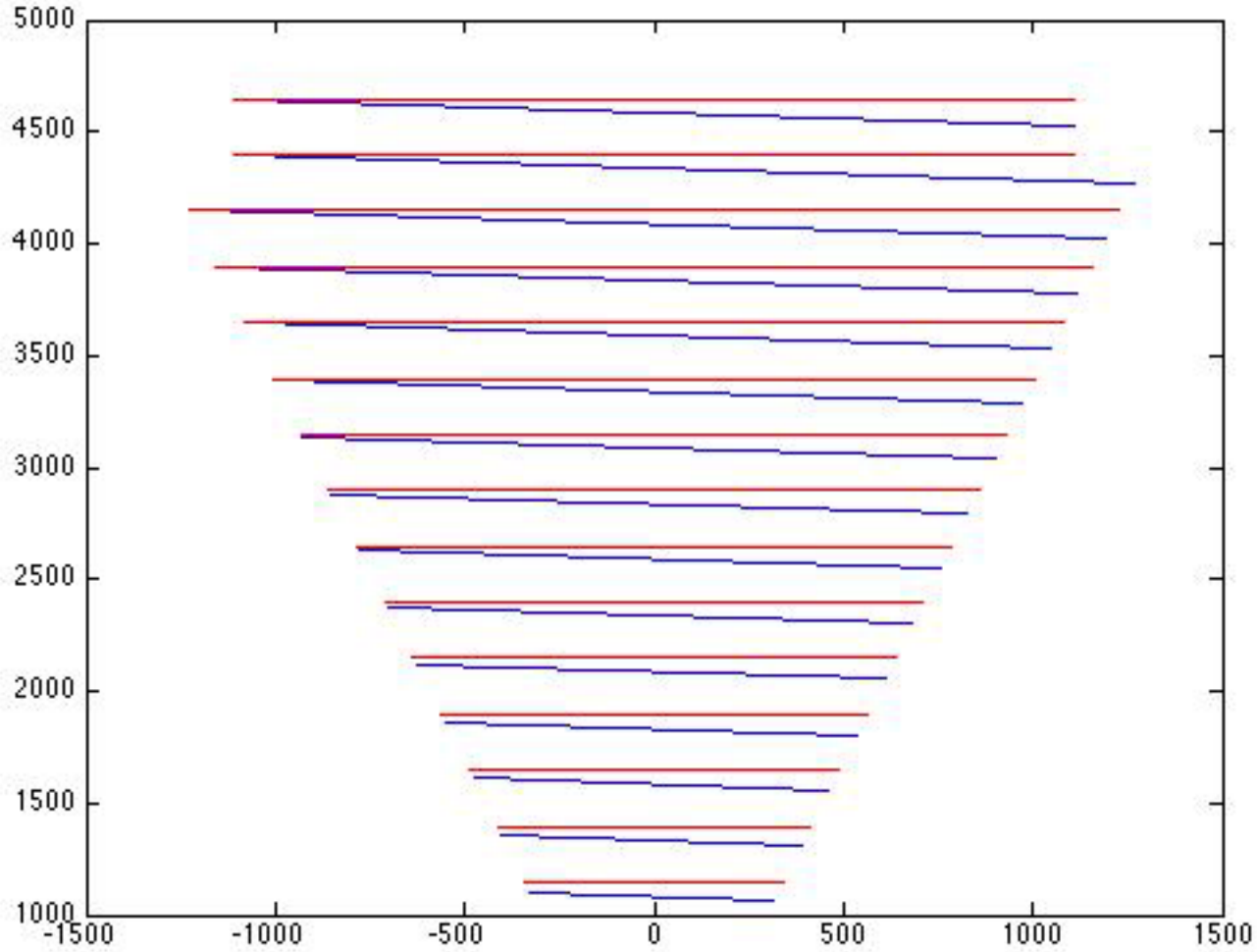
- Outputs to Sector Logic should be fully synchronous to 40 MHz clock.
  - Packets in every clock contain a complete set of track info. of each bunch, independent of each other.
  - Fixed latency
    - No queuing structure at Sector Logic
  - 3 fibres for Large SW Sector
  - 2 fibres for Small SW Sector
- NSW detectors should combine track info's from sTGC and MicroMegas. Do not deliver them separately.
- Latency to Sector Logic is shorter than 44 clk's.

- New Sector Logic incorporate segments info. from BIS7,8, EES and EEL into the level-1 trigger decision.

Additional box for Osamu?



Matlab first pass simulation



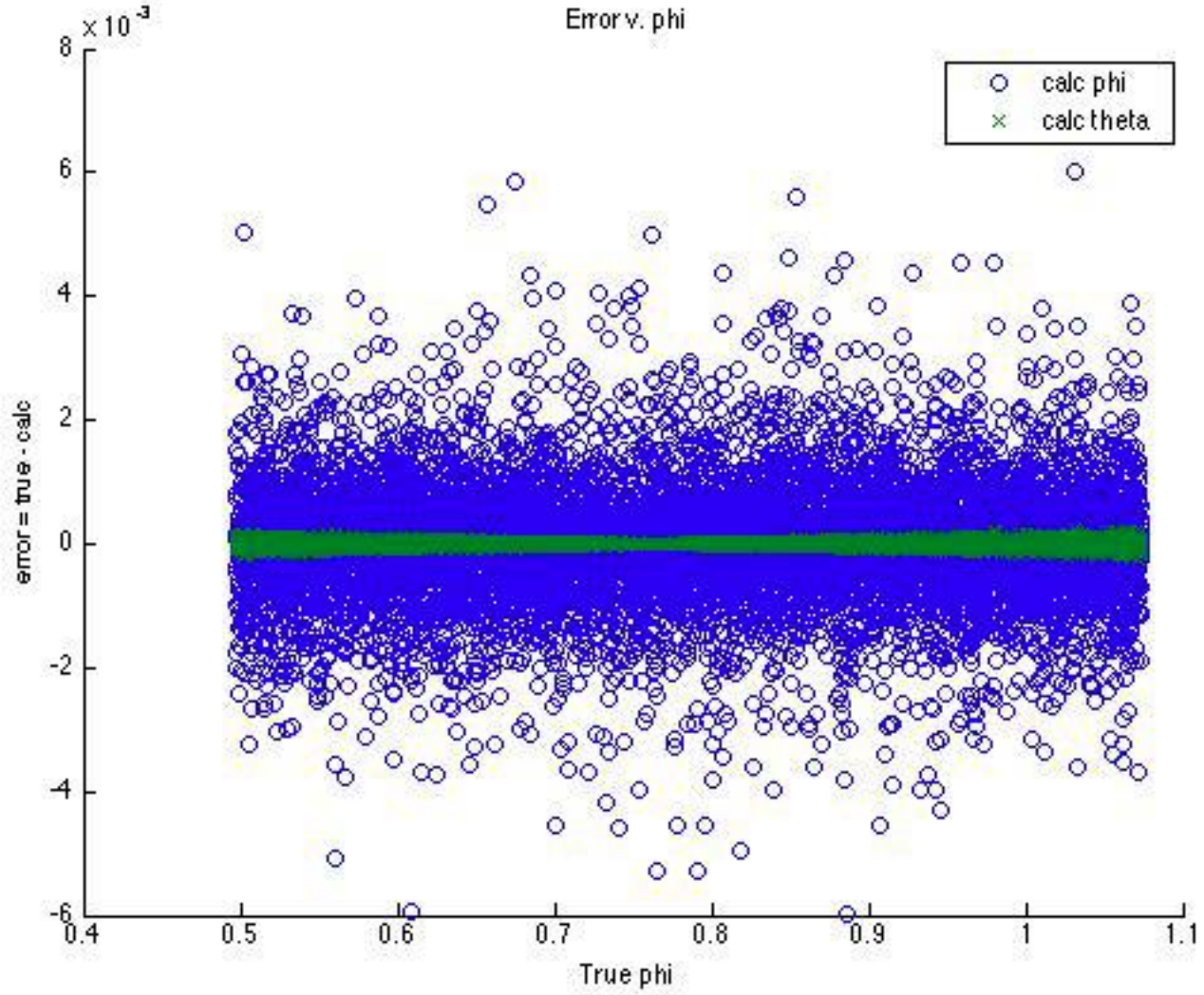
Assumptions about number of bits required for spatial information

[F/B] [L/S] [Wedge] [Plane] [Strip]

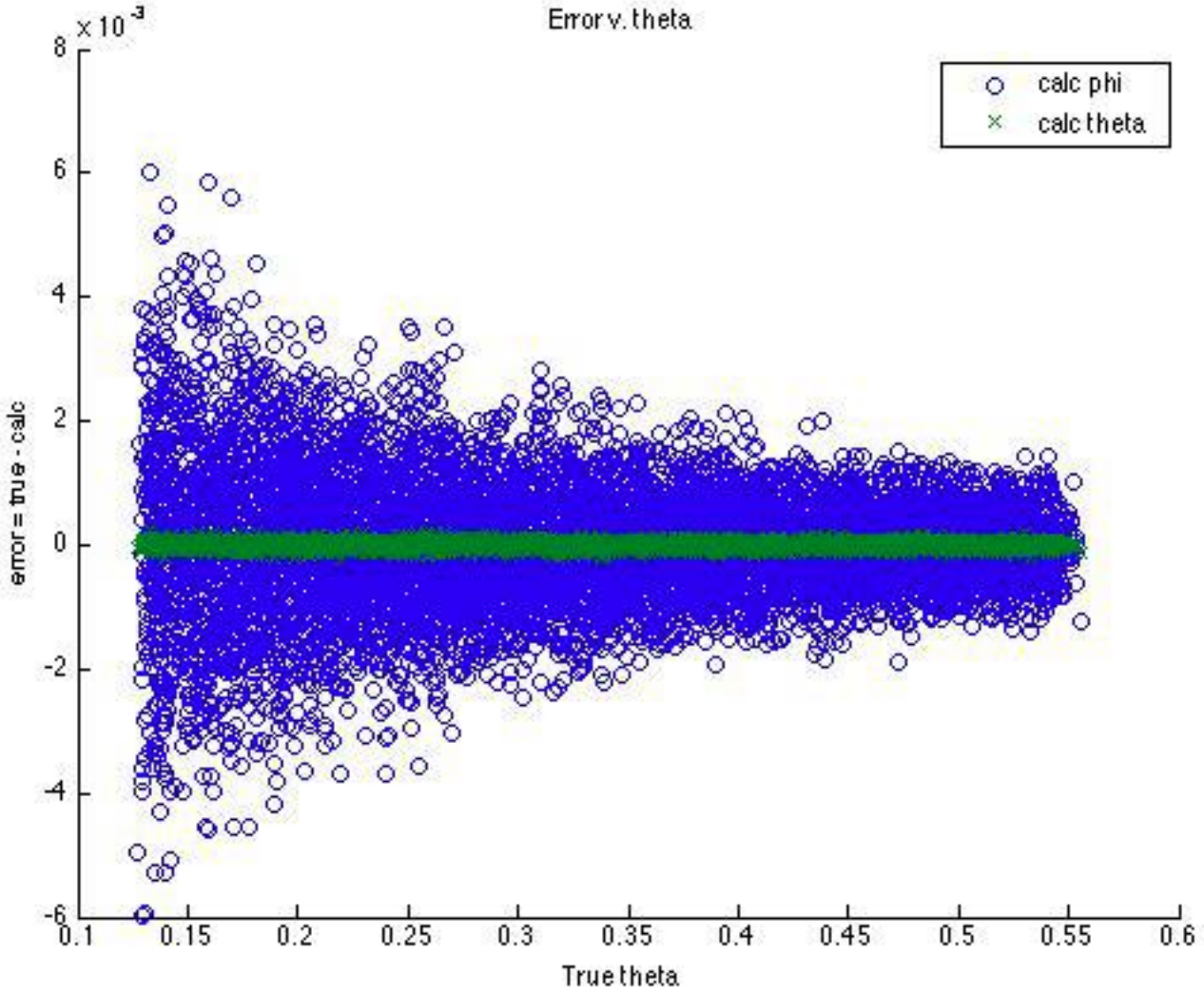
1 + 1 + 4 + 4 + 14 = 24 bits

Need BCID – integrate over four crossings

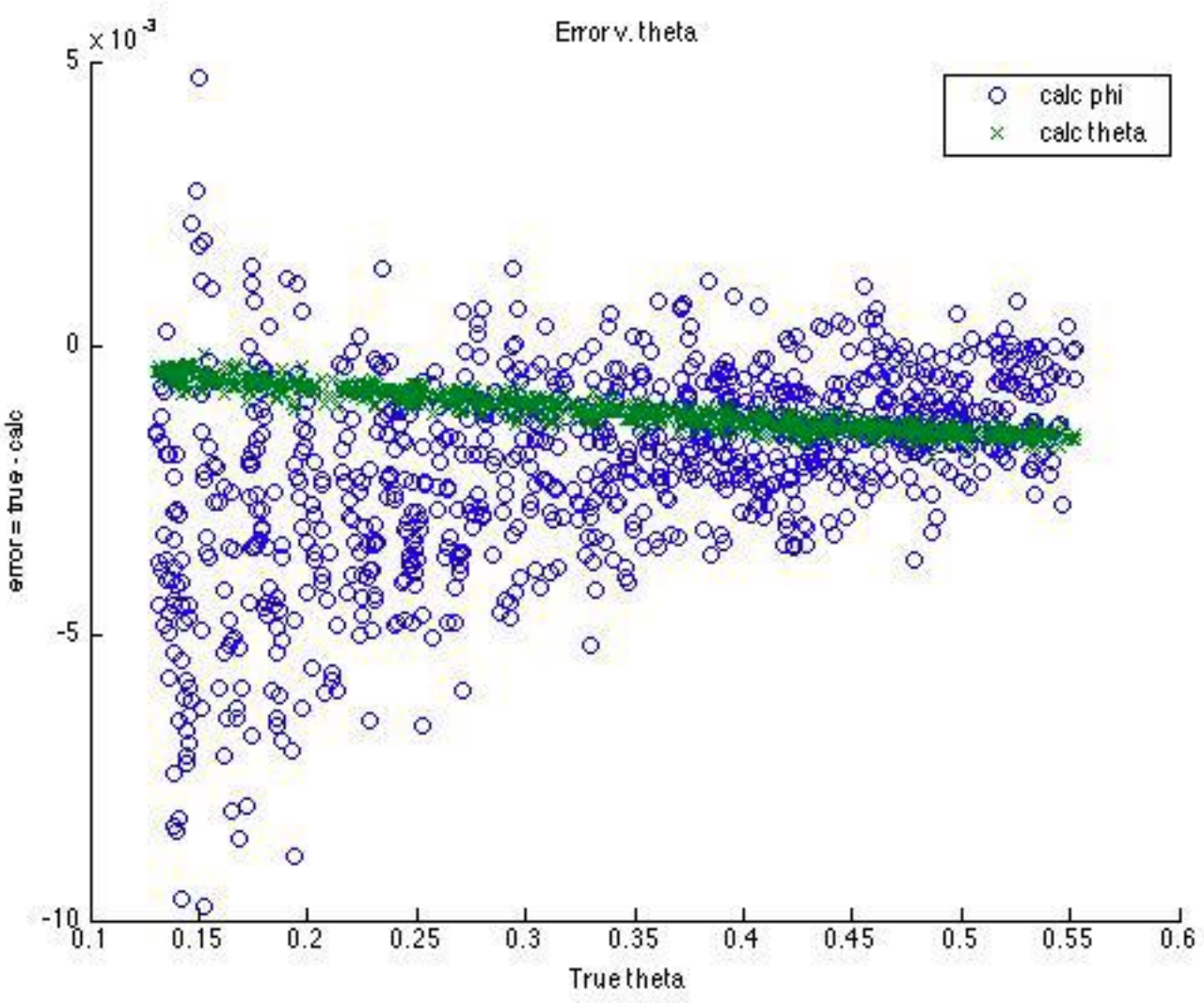
Full use of trigonometric functions
Early results with old geometry
(will show updated geometry)



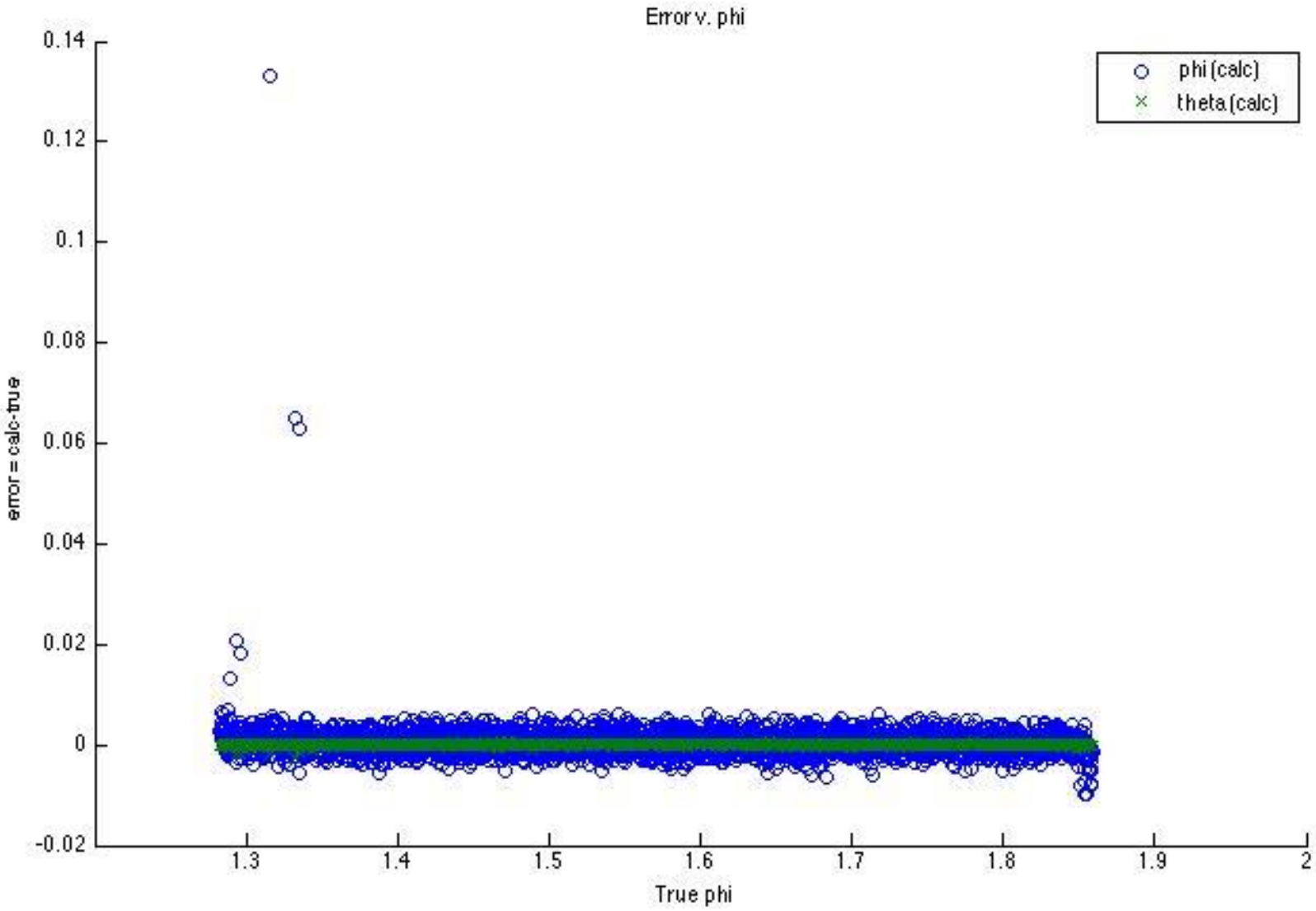
Full use of trigonometric functions



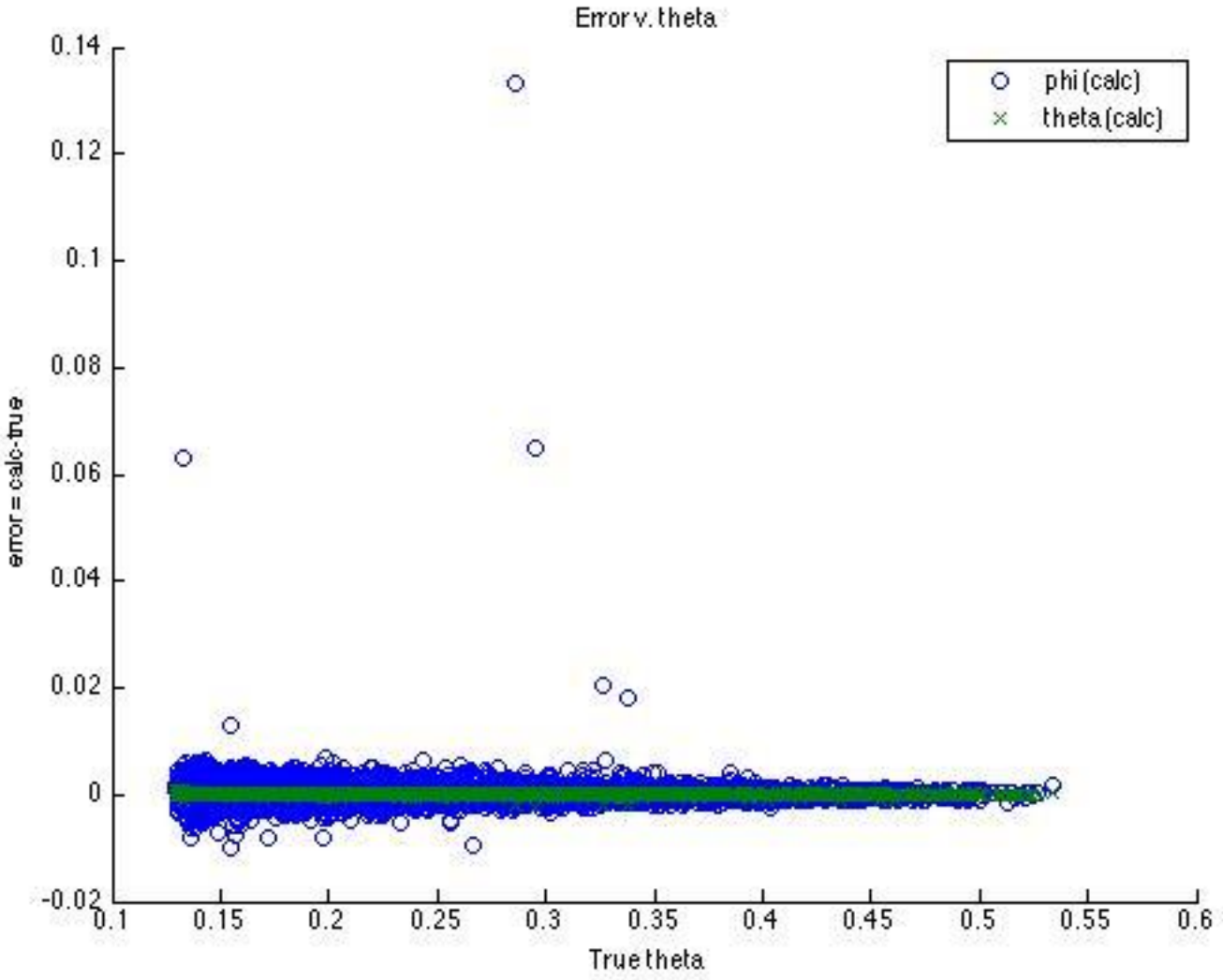
First pass at strip address search algorithm



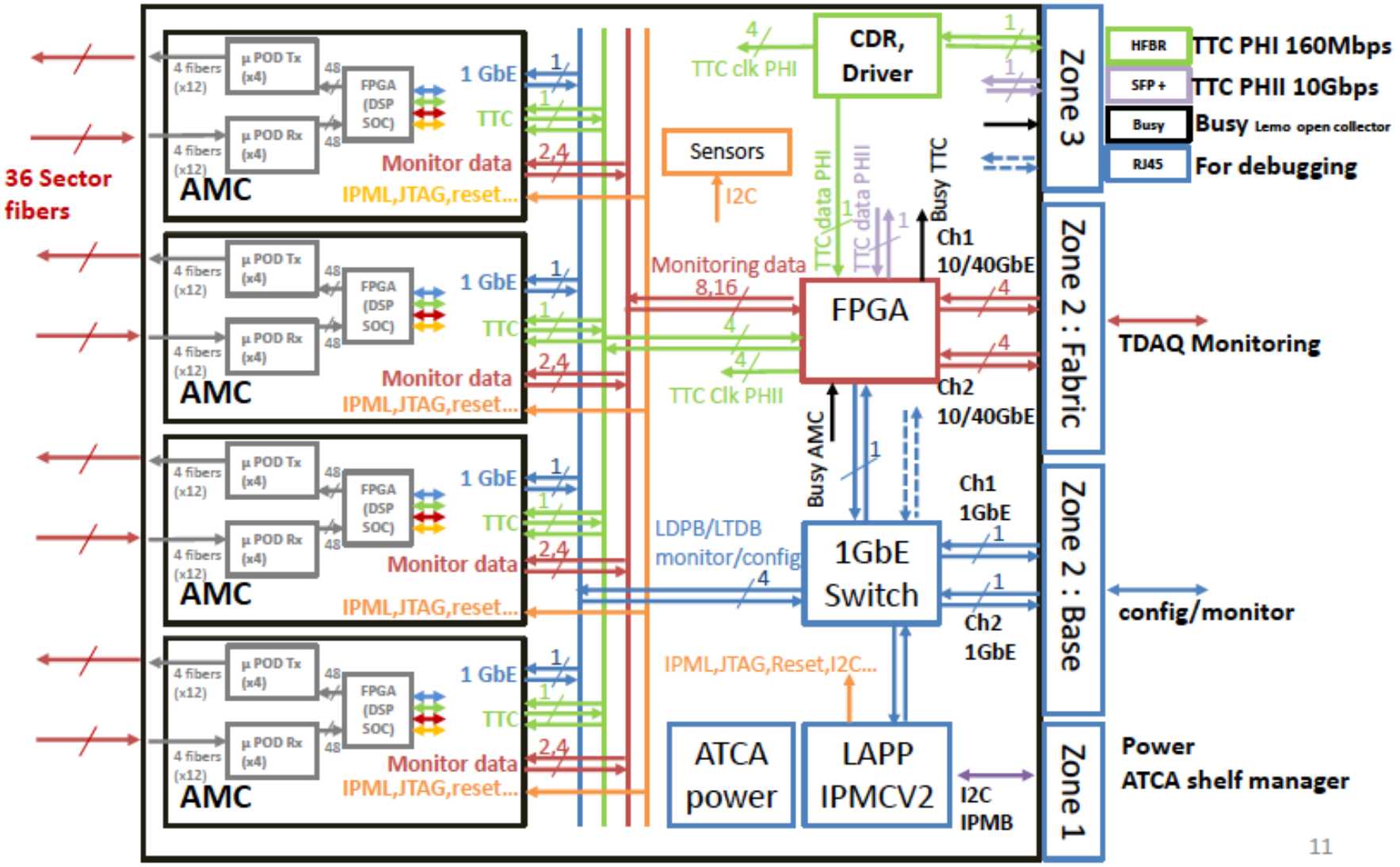
Current XUV Geometry
Random background, radial fall-off



0.1% fakes, probably can be improved



Ken's version of processor (based on LAr card)



Personnel at Harvard

- J. Huth
- D. Lopez Mateos
- B. Clark
- N. Felt (EE)
- J. Oliver (EE)

To do list (short term):

- Implementing new geometry (XUV)
- Background
- BCID integration
- Algorithm exploration
- FPGA function exploration+timing
- Examine stereo orientations in Z
- Begin use of Athena when digitization is fully implemented