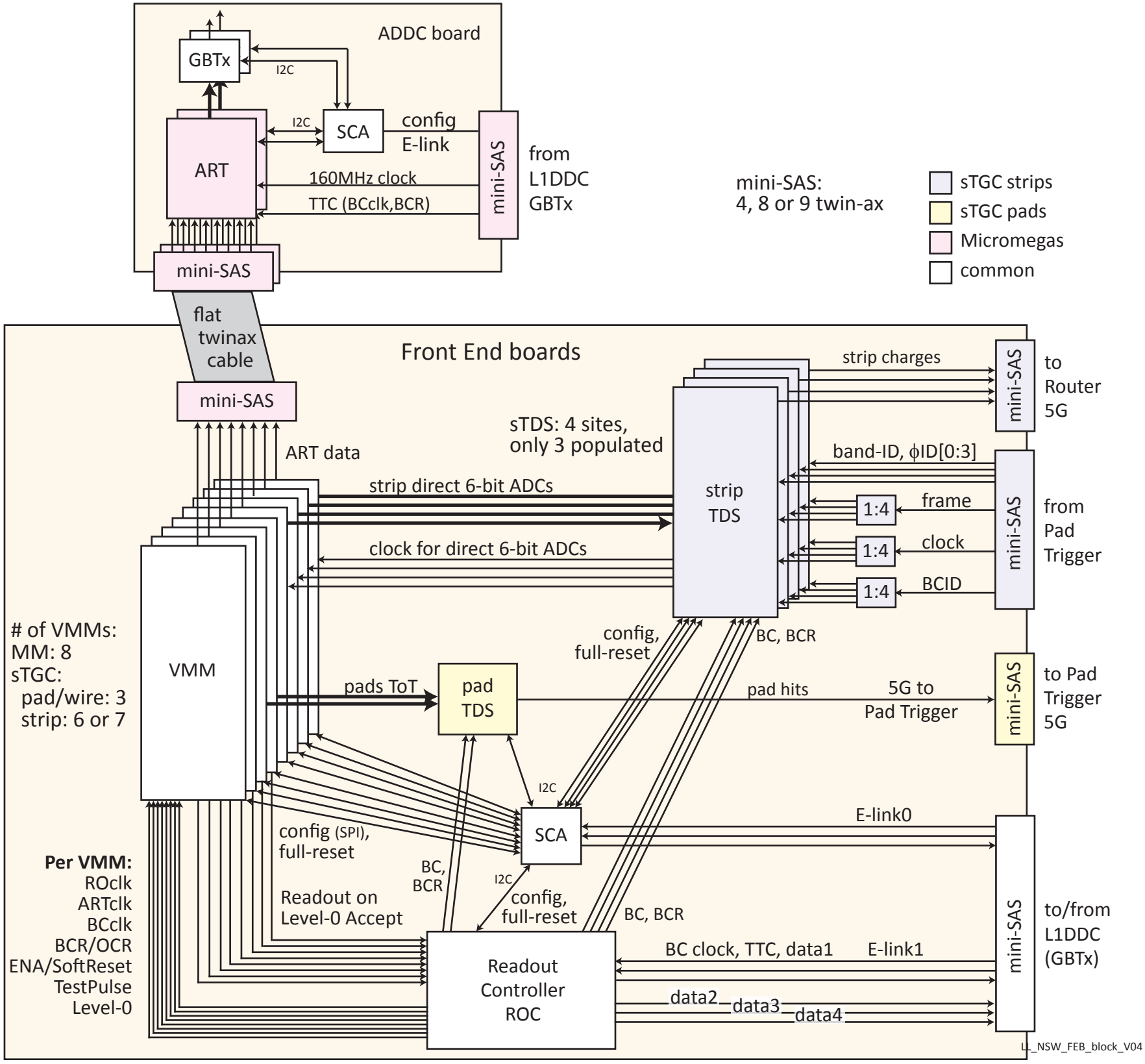
ADDC board
GBTx
I2C
I2C
SCA
config
E-link
ART
160MHz clock
TTC (BCclk,BCR)
mini-SAS
from
L1DDC
GBTx
mini-SAS
mini-SAS:
4, 8 or 9 twin-ax
sTGC strips
sTGC pads
Micromegas
common
flat
twinax
cable
mini-SAS
Front End boards
strip charges
mini-SAS
to
Router
5G
sTDS: 4 sites,
only 3 populated
ART data
band-ID, ϕID[0:3]
strip direct 6-bit ADCs
strip
TDS
1:4
frame
mini-SAS
from
Pad
Trigger
clock for direct 6-bit ADCs
1:4
clock
1:4
BCID
# of VMMs:
MM: 8
sTGC:
pad/wire: 3
strip: 6 or 7
VMM
config,
full-reset
BC, BCR
pads ToT
pad
TDS
pad hits
5G to
Pad Trigger
mini-SAS
to Pad
Trigger
5G
I2C
SCA
E-link0
config (SPI),
full-reset
Per VMM:
ROclk
ARTclk
BCclk
BCR/OCR
ENA/SoftReset
TestPulse
Level-0
BC,
BCR
I2C
Readout on
Level-0 Accept
config,
full-reset
BC, BCR
BC clock, TTC, data1
E-link1
mini-SAS
to/from
L1DDC
(GBTx)
Readout
Controller
ROC
data2
data3
data4
LL_NSW_FEB_block_V04