FELIX and TTC

3 April 2015

TTC data sent to Front End

For Phase 1, the standard encoded TTC signal will arrive to FELIX via a standard TTC fiber and will be decoded by the TTC FMC card and FPGA firmware. TTC data will be stuffed, on each BC clock, with fixed latency, directly into *all* output E-links to the Front End with the "TTC" attribute. Each E-link can be configured to choose one of the possible options shown in the table below:

E-link option		bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
0	2 bits	L1A	B-chan						
1	4 bits	L1A	BCR	ECR	B-chan				
2	4 bits	L1A	BCR	ECR	Brcst[2]				
3	8 bits	L1A	BCR	ECR	Brcst[2]	Brcst[3]	Brcst[4]	Brcst[5]	B-chan
4	8 bits	L1A	BCR	ECR	Brcst[2]	Brcst[3]	Brcst[4]	Brcst[5]	Brcst[6]

For Options 0, 1 & 3, the destination must decode the B-channel, one bit per 40MHz clock. The wider fields may be defined as multiple 2-bit or 4-bit E-links at lower bit rates.

- Note that the E-link clock can be 40MHz, but, for example, the 4-bit field can be transferred at 160Mb/s if the receiver generates a ×4 multiple of the 40MHz E-link clock.
- Typically, the reverse direction of the event data E-link can be used for TTC.
- Transparent upgrade to the Phase-II TTC using a mezzanine board in FELIX
- The case of a FELIX with only TTC input and only TTC output, i.e. a TTC distributor, is an extreme, but potentially useful, case.

For Phase2 we could add a C-channel that could be filled via a network, i.e. non-TTC, source.

option		bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
5	4 bits	L1A	B-chan	C-chan					
6	8 bits	L1A	BCR	ECR	Brcst[2]	Brcst[3]	B-chan	C-chan	
7	8 bits	L1A	BCR	ECR	Brcst[2]	Brcst[3]	Brcst[4]	C-chan	

TTC data sent to network endpoints

Proposed format for a 20-byte TTC network message (Phase 2 compatible) sent, for example, to the ROD, etc., via TCPIP.

0	1	2		3	4	5	6	7	8	9	10	11
FMT(8)	Len(8)	reserved		BCID(12)	XL1ID(8)	L1ID(24)			orbit(32)			
12	13	14		15	16	17	18	19				
trigger type		reserved			L0ID(32)							

Note that the latency of the message is NOT fixed.