Athena simulation data

Formatted input file (strip #, time, FIFO address)

DAQ Interface for communication

1 FIFO per VMM

8 FIFOs per FEB

PC

FPGA

Ethernet

Generic interface

Address decoder

20 bit counter @ 320 MHz

Small FIFO

Strip

Time

Time Check

Serializer

Mini SAS to ADDCs

FEB 0

FEB 7