

NSW sTGC Router Design Report

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**University of Michigan
February 10th , 2015**





Outline

- sTGC Router Introduction
- sTGC Router Design R&D
- sTGC Router Implementation
- Prototype V0 Preliminary Testing
- Next Step

sTGC Router Introduction

- Location:** On the rim of the New Small Wheel (TID ~5kRad)
- Functionality:** route active strip signals to trigger processor at USA15 and drop NULL packets
- Two main signal flow paths**
 - Data link:
 - TDS-Router: 4.8Gbps electrical link
 - Router-USA15: 4.8Gbps optical link
 - TTC link: Two E-Links from GBTx

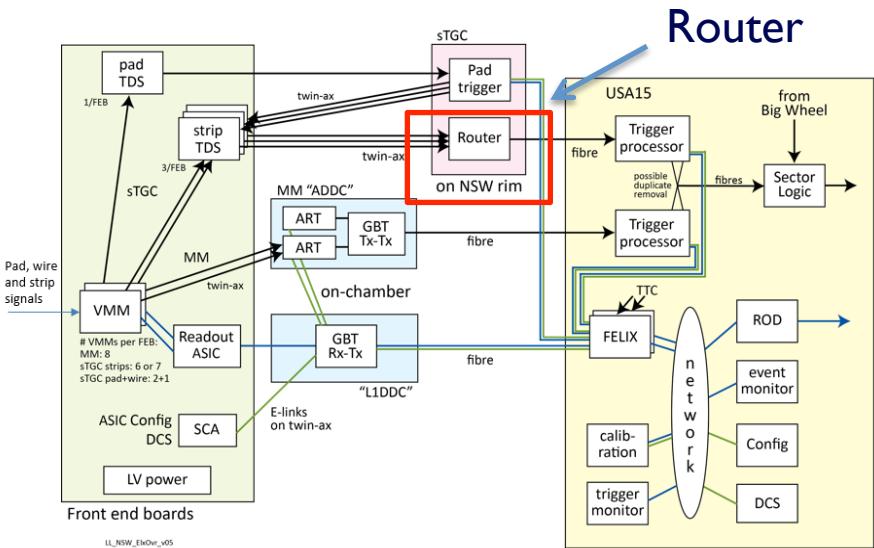


Figure 1: Diagram of the frontend and readout system for the NSW sTGC detectors

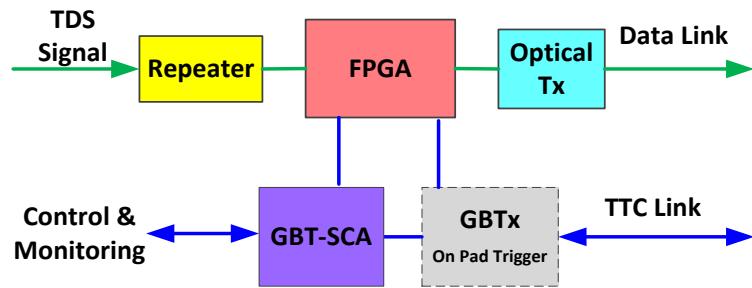


Figure 2: sTGC Router Signal flow

Layers	8
Sectors/Wheel	16
Wheels	2
Total # Router Boards	256

Table 1: Total NO. of Router Boards

sTGC Router Design R&D

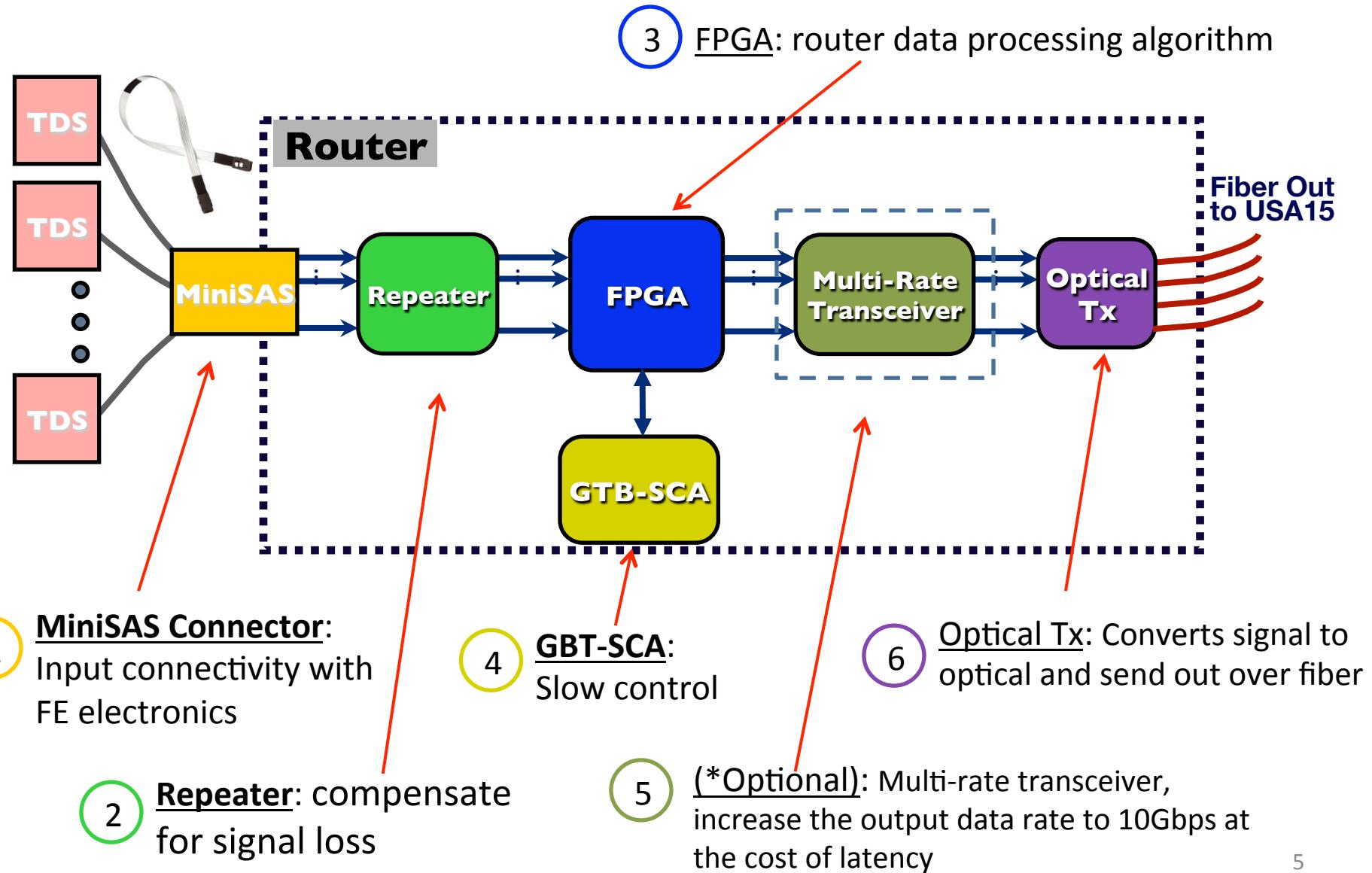


• Design Requirements

- ❖ One router board per sector-layer: any failure is isolated into a single layer
- ❖ Router can recover the degraded TDS electronic signal after 3m~4m cable
- ❖ Input channels up to 16, output channels 3 ~4
- ❖ Router need to process all data packets and drop the NULL packets
- ❖ Stable data link @4.8Gbps (or higher)
- ❖ Minimal latency: 80~90ns
- ❖ Radiation tolerant (~TID 5kRad & SEU mitigable)
- ❖ Low power
- ❖ Low cost

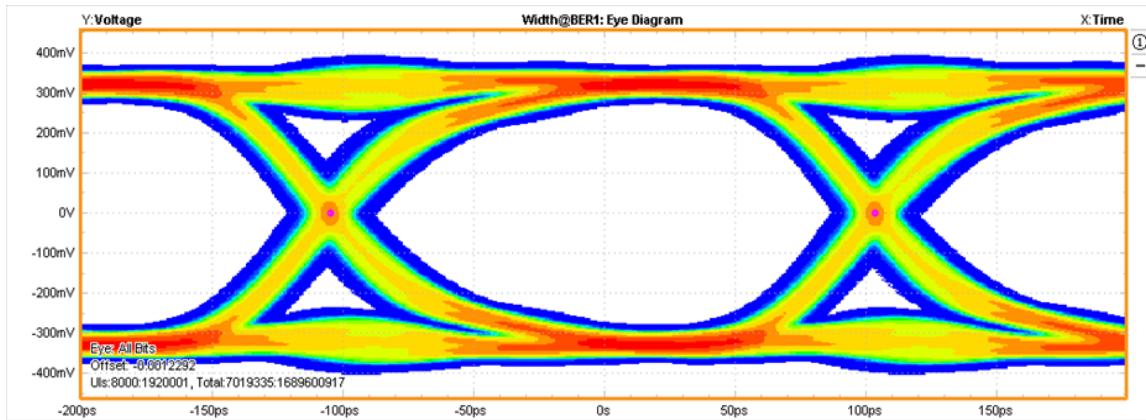


Router Block Diagram

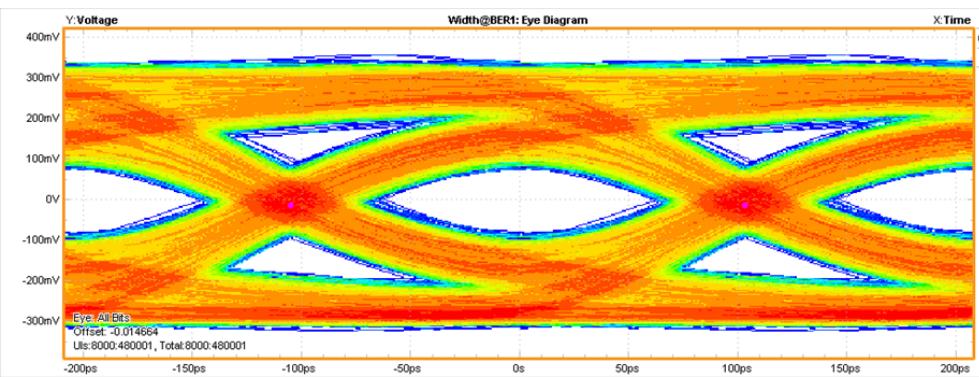


TDS Signal Treatment

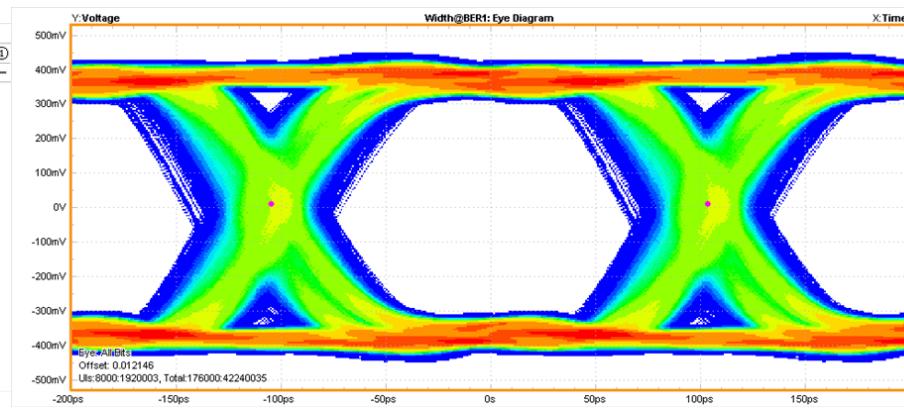
- ❖ TDS electrical signal: degraded due to loss of power in 3m ~4m transmission
- ❖ Repeater (DS100BR410): low power (220mW), quad-channel, ~10Gbps



Eye of TDS-SER output
@4.8Gbps



Eye of TDS-SER output after 0.5m cable w/o repeater

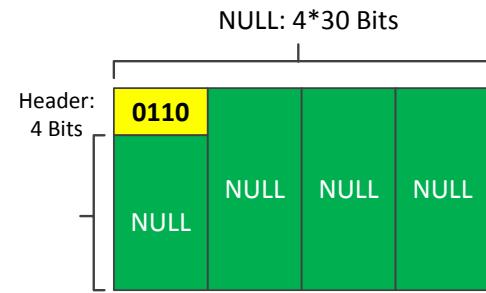
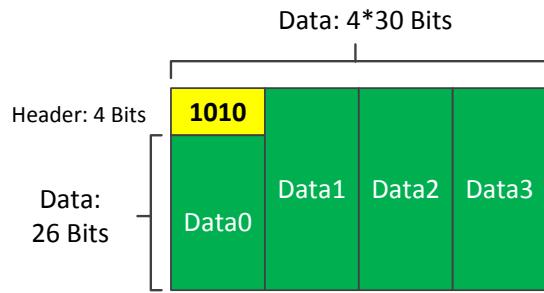


Eye of TDS-SER output after 4m cable w/ repeater

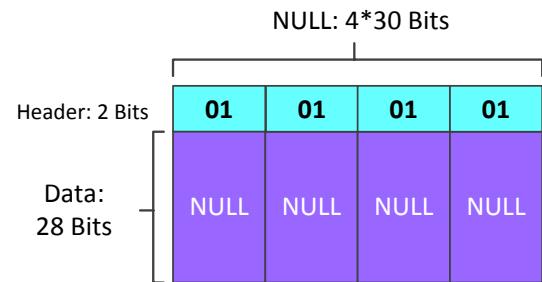
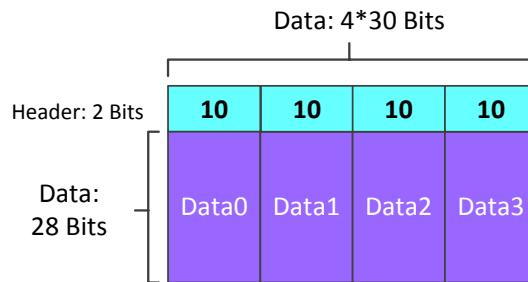
Router Data Processing

❖ Router data formats: defined by strip-TDS

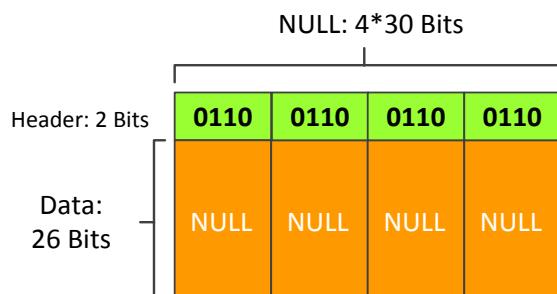
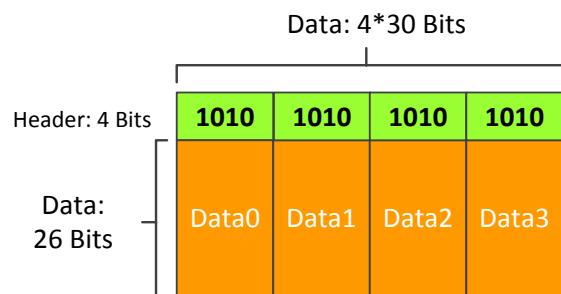
- Current TDS version: overall 150bits, cannot send all out in 1BC
- Next TDS version: overall 120 bits, three possible formats



(I) One 4-bits header for 120bits



(II) Four 2-bits header for 30bits



(III) Four 4-bits header for 30bits

Router Data Processing

❖ Artix-7 FPGA

- Selected based on performance, cost, I/O number
- XC7A200T-2FFG1156 : 16 GTPs, 6.6Gbps, ~\$300
- GTP link evaluation in AC701 using Xilinx IBERT

Test Hardware	Test Pattern	Line Rate	Bit Error Ratio & Count	Eye scan (Chip Scope)
One AC701 & 1M SMA Cable Loop	PRBS 7-bit & PRBS 31-bit	6.25Gpbs	E-015 & 0	OPEN
One AC701 & SFP Adapter	PRBS 7-bit & PRBS 31-bit	6.25Gpbs	E-015 & 0	OPEN
Two AC701s & 1M SMA Cable	PRBS 7-bit & PRBS 31-bit	6.25Gpbs	E-015 & 0	OPEN
Two AC701s & 1M SFP male-to-male Adapter	PRBS 7-bit & PRBS 31-bit	6.25Gpbs	E-014 & 0	OPEN
Two AC701s & 3M 4Gbps SFP optical module	PRBS 7-bit & PRBS 31-bit	3.125Gpbs	E-014 & 0	OPEN
Two AC701s & 3M 8Gbps SFP optical module	PRBS 7-bit & PRBS 31-bit	6.25Gpbs	E-015 & 0	OPEN

Figure 1: Summary of IBERT test result of Xilinx GTP links

❖ Two basic requirements:
stable functionality & low-fixed latency

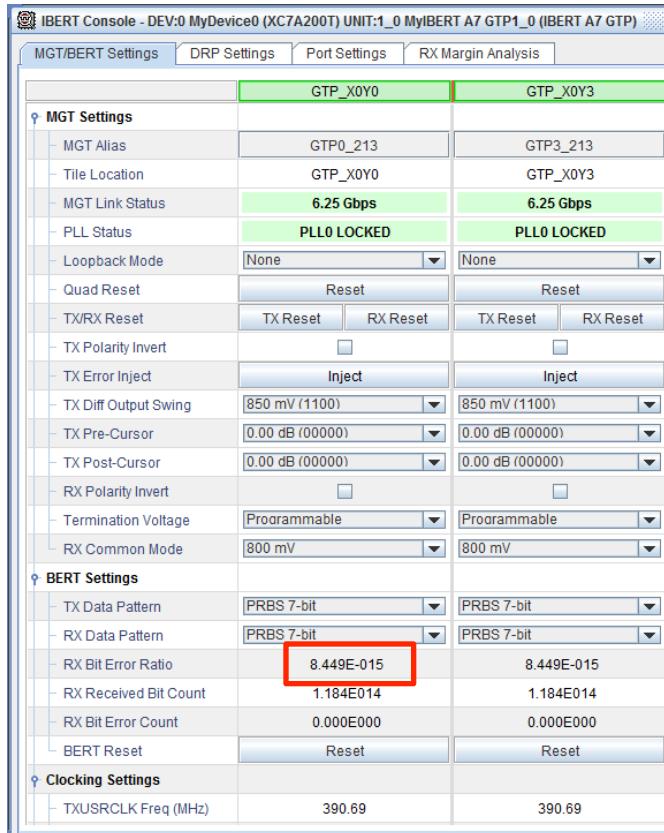
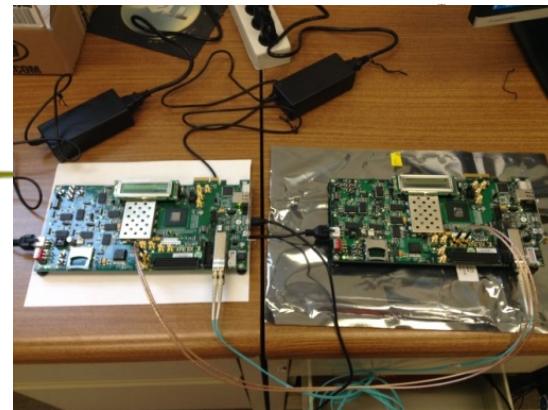


Figure 2: AC701 e.g. IBERT test result

Router Optical Transmitter

- **CERN Versatile link** (radiation hard)
 - Two transmitters in a latch
 - 5 Gbps GBLD driver
 - SFP+ to LVDS differential

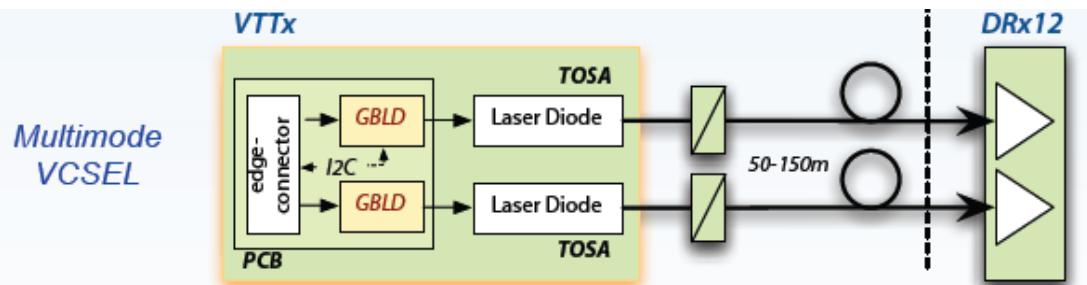


Figure 1: Multimode VCSEL



Latch holding
VTTx or VTRx

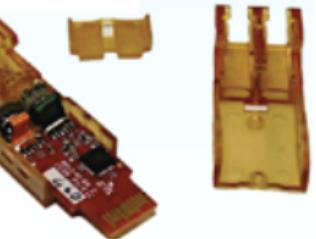


Figure 2: Latch holding VTTx or
VTRx

- **ATLAS LAr MTX by SMU** (radiation hard)
 - Two transmitters in a latch
 - 8 Gbps LOClD driver
 - Custom electrical connector

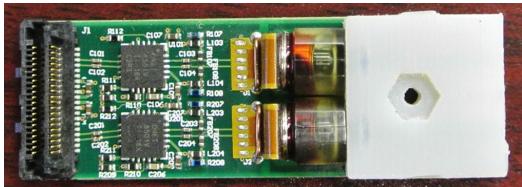


Figure 3: MTx Module by SMU

❖ R&D is conducted by Taiwan group



Router Power & Slow control

➤ Power

- Power connector: Micro-Fit 3.0 43650 series, each position~ 5A
- Input voltage: +12V ?
- Two separate voltage lines are expected: isolate power plane for GTP (ripple voltage < 10mV) & other parts
- Voltage level: +3.3V, +2.5V, +1.8V, +1.2V, +1.0V
- Power sequencing requirement [*Ref: Xilinx DS181*]
- Radiation hard power device (LV power group)
- Initial power estimation of Artix-7 FPGA (~5.4W)
- Router (final version) power estimation: ~10W → Cooling ?



➤ Slow control

43650-0401

- Two E-links from GBTx on Pad Trigger logic board
 - One is for GBT-SCA
 - One is for FPGA (under consideration)
- Router BC clock: E-link clock or GBTx programmable clock output
- Jitter cleaner: LMK03200 (TID ~14.9kRad) → under consideration

sTGC Router Implementation

- Prototype V0 objectives

- Demonstrate full integration at Board level (MiniSAS, Repeater, Artix-7 FPGA, MTx...)
- Reliably transmit data
 - ✓ Speed & latency tests
 - ✓ Radiation test (SEU)
- Demonstrate the system data flow
 - ✓ →TDS→Router→USA15
 - ✓ Router data processing algorithm
- Test power options & study cooling issues
- Fabrication & assembly evaluation

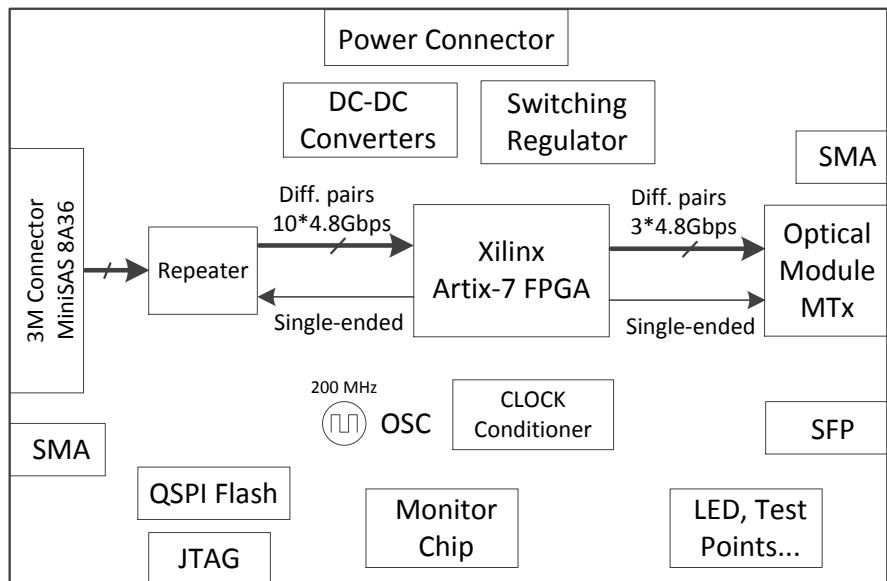


Figure 1: Block diagram of router prototype v0

Prototype V0 Sch. Design

❖ Signal flow path:

- Input (MiniSAS/SMA) → Repeater → Artix-7 FPGA → Output (MTx/SMA/SFP)

❖ Service blocks

- Local configuration: JTAG & QSPI
- Clock distribution: GTP reference clock (LMK03200), extra clock for system ctrl & monitoring (Osc.)
- Power supply: Two power scheme (LTM4619 & LT8612). Total ~16W power consumption
- Control & monitoring: One SFP used for remote control and monitoring (with LTC2991/LTC2945) demonstration.

❖ Backup I/O interface: Both input & output (SMA, SFP)

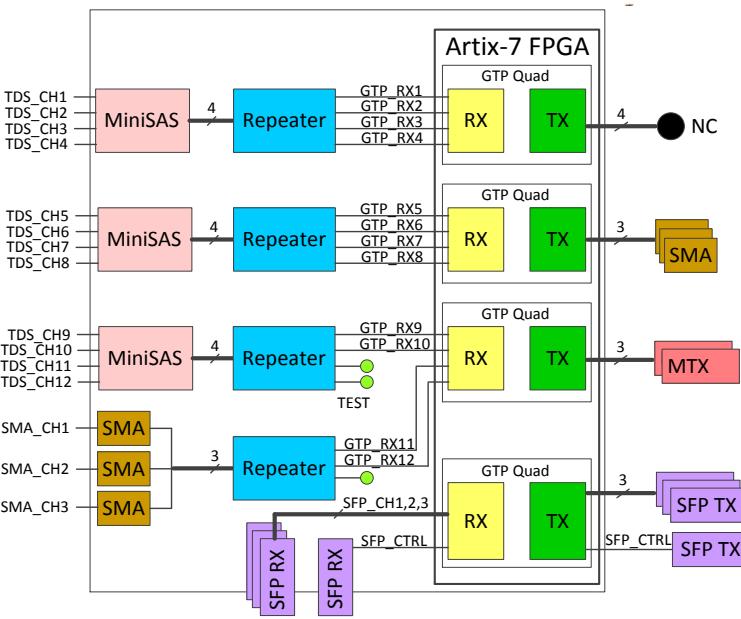


Figure 1: Signal flow paths on prototype v0

A	B	C	D	E	F	G
Source	Voltage (V)	Current (A)	Margin	Power /One Chip	Power /board	Power-on seq
1	1.0V	3.1A	(*1.25)= 3.875 A	3.875W	3.875W	SEQ 1
2	FPGA Vccint	1.0V	0.009A	(*1.25)= 0.011 A	0.011W	0.011W
3	FPGA Vccbram	1.0V	0.043A	(*1.25)= 0.054A	0.097W	0.097W
4	FPGA Vccaux	1.8V	40mA/Bank *G	(*1.25)=0.3A	0.99W	0.99W
5	FPGA Vcco3V3	3.3V	50mA/Bank *4	(*1.25)=0.25A	0.625W	0.625W
6	FPGA Vcco2V5	2.5V	50mA/Bank *4	(*1.25)=0.25A	0.625W	0.625W
7	FPGA MGTVcc	1.0V	1.231A	(*1.25)= 1.54A	1.54W	1.54W
8	FPGA MGTVtt	1.2V	0.78A	(*1.25)= 0.98A	1.17W	1.17W
9	Osc					
10	200MHz/125MHz	2.5V	0.07A	(*1.25)= 0.09A	0.23W	0.23W*4=0.92W
11	LMK03200	3.3V	0.16A	(*1.25)= 0.2A	0.66W	0.66W
12	QSPI Flash (config)	3.3V	0.1A	(*1.25)= 0.125A	0.42W	0.42W
13	Monitor LT2991	3.3V	1.1mA	(*1.25)= 0.0013A	0.04W	0.04W*2=0.08W
14	DS100BR410	2.5V	0.11A	(*1.25)= 0.14A	0.35W	0.35W *4=1.4W
15	MTx	3.3V/2.5V	/		(150mW/ch)	0.3W*2=0.6W
16	GRT-SCA?					1.24W*4=4.96W (prototype v0)
17	SFP	3.3V	0.3A	(*1.25)= 0.38A	1.24W	
18	Quick Summary: Total No. of FPGA's (and corresponding parts) will be 256 & 256 Router boards in the whole detector					
20	Voltage(V)	Current(A)	Power(W)			
21	1.0V	5.43A	5.43W			
22	1.2V	0.98A	1.17W			
23	1.8V	0.054A	0.097W			
24	2.5V	1.18A	2.95W			
25		2.15A	7W (prototype v0)			
26	3.3V	1.2A	3.96W (prototype v1)			

Table 1: Power estimation for prototype v0

Prototype V0 PCB Design

- ❖ PCB design of router prototype V0 was finalized in mid Oct. 2014.
- ❖ V0 size is 190mm * 180mm * 2.28mm, 14 layers.
- ❖ Estimation of final envelope of router will be 150mm * 180mm * 2.2mm.

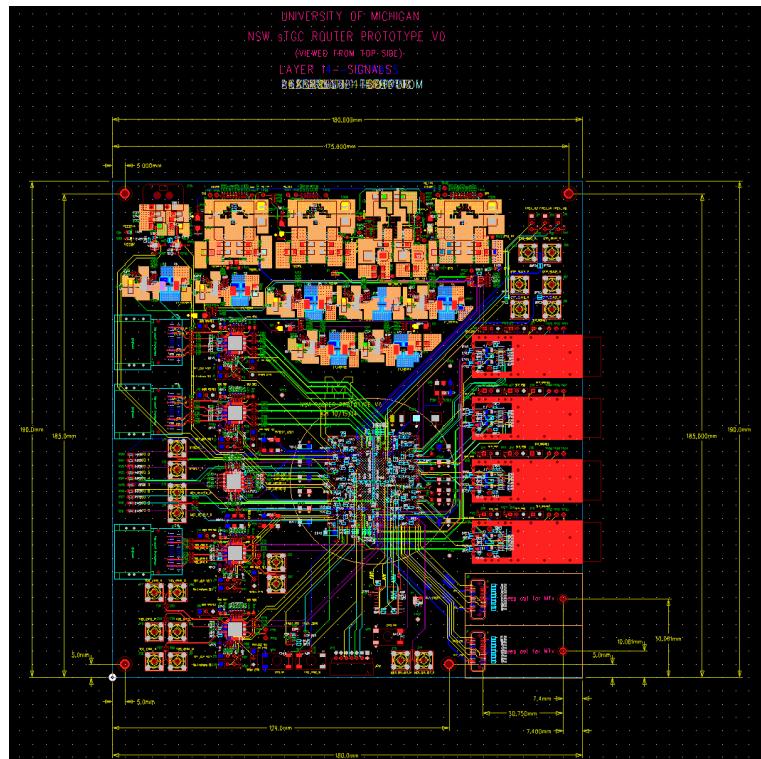


Figure 2: Stack up details of router prototype v0

Prototype V0 Construction

- ❖ Construction of prototype v0 was done by Liverage (Taiwan) in mid Dec. 2014
- ❖ Prototype V0 (2 assembled PCBs) arrived on Jan. 5th, 2015
 - Two weeks delay due to holiday season

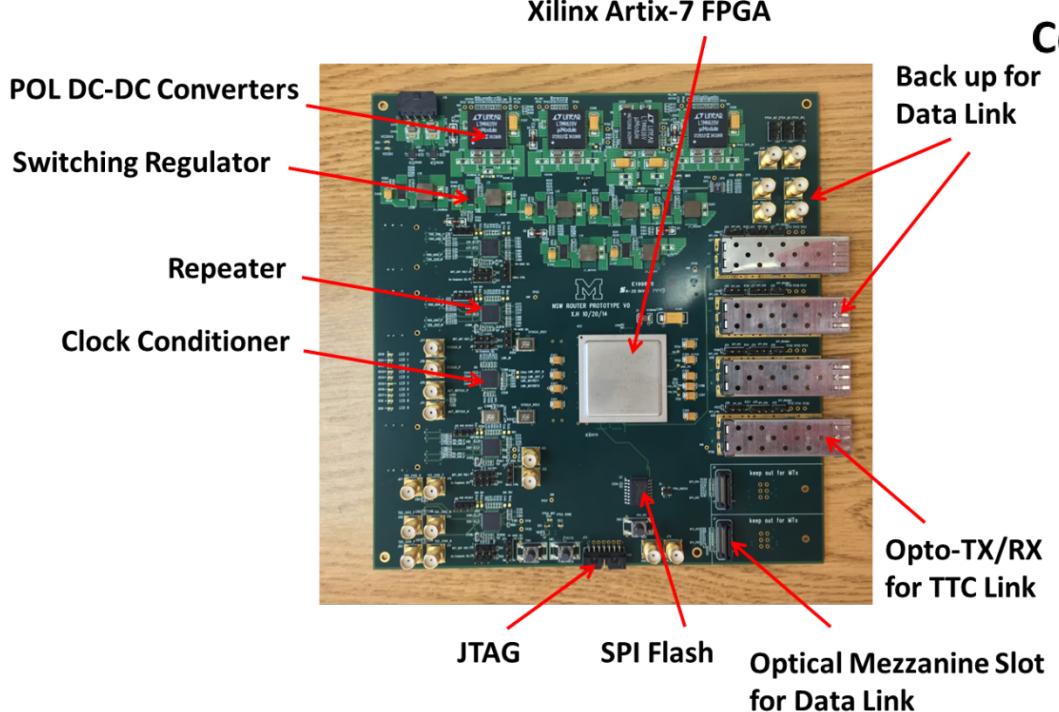


Figure 1: Photograph of the router prototype v0 (Top)

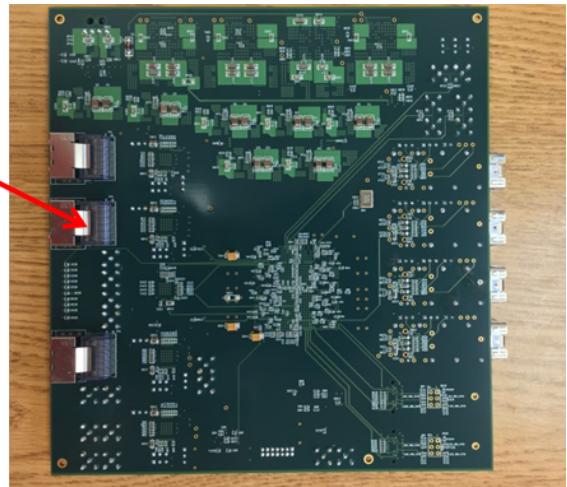


Figure 2: Photograph of the router prototype v0 (Bot)

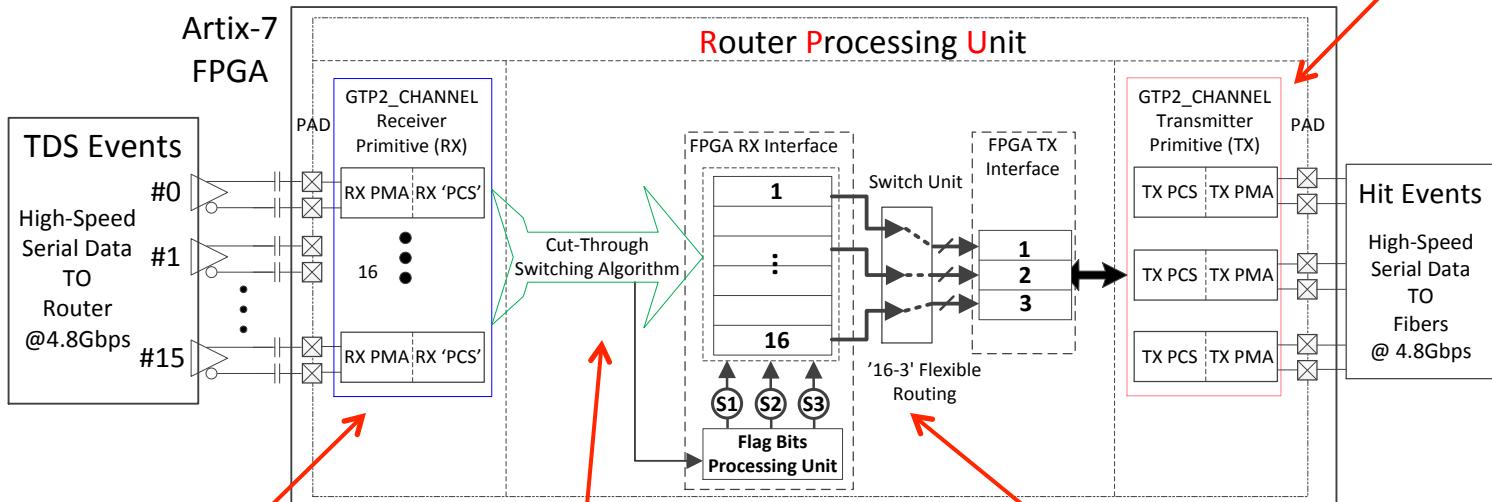
Prototype V0 Firmware Design

❖ Three parts

- Router processing unit
- Control & monitoring logic
- Soft error mitigation logic

❖ Router processing unit

- Based on current TDS data format



1 Optimal GTP RX logic + Sync. Buffer

2 Cut-Through switching algorithm

3 '16-3/4 Flexible routing'

Prototype V0 Firmware Design

❖ Router processing unit

- Latency estimation: ~92ns
- “Breakdown”
 - Artix-7 GTP RX with 20-bit data width & optimized PCS: 183UI (123UI PMA + 3 RXUSRCLK cycle)
 - User logic: syn. buffer, descrambler, flexible routing: ~30ns
 - Artix-7 GTP TX with 20-bit data width, TX user interface and encoding: 114UI (34UI PMA+4 TXUSRCLK cycle)

[Ref: <http://www.xilinx.com/support/answers/58981.html>]

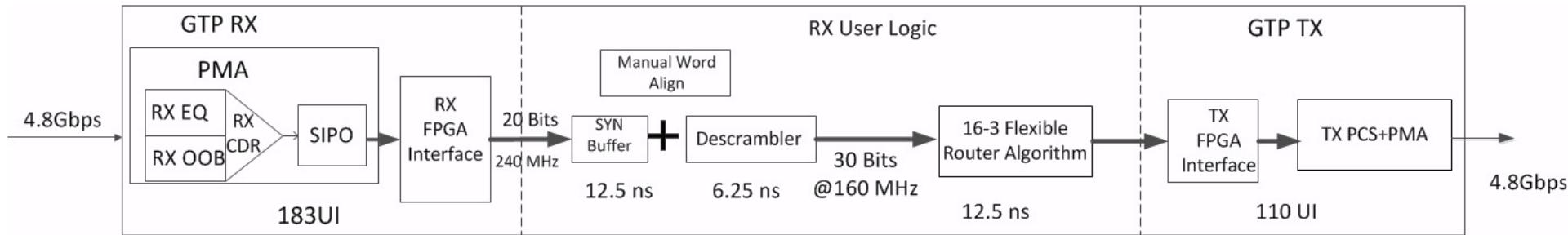


Figure 1: “Breakdown” of estimated router latency

Prototype V0 Firmware Design

❖ Control & monitoring logic

- Communicate with repeater, clock conditioner chip, monitor chip, SFP, MTx

❖ Router soft error mitigation logic

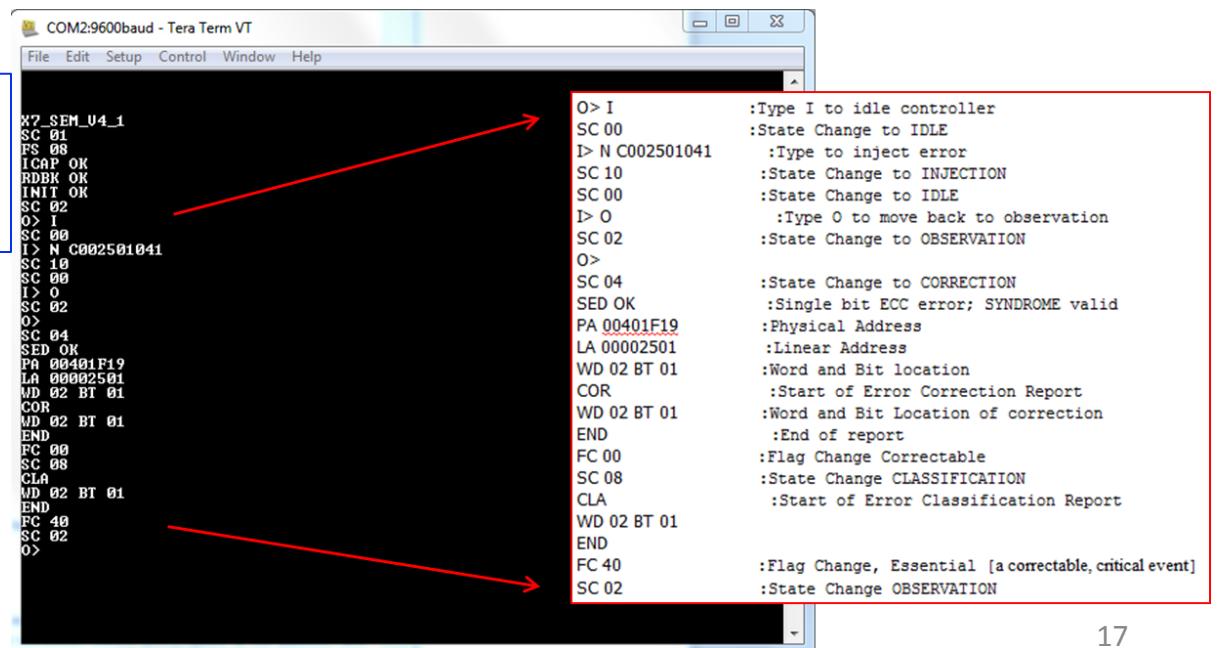
- SEU correction through configuration scrubbing
 - MultiBoot: fully reconfigure itself with an alternate bitstream
 - Soft error mitigation (**SEM**) controller
- **TMR** (Triple modular redundancy): user logic

MultiBoot & SEM Controller

Logic: Evaluated in AC701 [OK]

Next step: will migrate

into router prototype v0



```

COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help

X7_SEM_U4_1
SC 01
FS 08
LCOP OK
RDBK OK
INIT OK
SC 02
O> I
SC 00
I> N C002501041
SC 10
SC 00
I> O
SC 02
O>
SC 04
SED OK
PA 00401F19
LA 00002501
WD 02 BT 01
COR
WD 02 BT 01
END
FC 00
SC 08
CLA
WD 02 BT 01
END
FC 40
SC 02
O>

O> I :Type I to idle controller
SC 00 :State Change to IDLE
I> N C002501041 :Type to inject error
SC 10 :State Change to INJECTION
SC 00 :State Change to IDLE
I> O :Type O to move back to observation
SC 02 :State Change to OBSERVATION
O>
SC 04 :State Change to CORRECTION
SED OK :Single bit ECC error; SYNDROME valid
PA 00401F19 :Physical Address
LA 00002501 :Linear Address
WD 02 BT 01 :Word and Bit location
COR :Start of Error Correction Report
WD 02 BT 01 :Word and Bit Location of correction
END :End of report
FC 00 :Flag Change Correctable
SC 08 :State Change CLASSIFICATION
CLA :Start of Error Classification Report
WD 02 BT 01 :Flag Change, Essential [a correctable, critical event]
END :State Change OBSERVATION
FC 40
SC 02

```

Prototype V0 Preliminary Testing

❖ Test plan for router prototype V0

- Front end data link: TDS-Router joint test
- Back end data link: Router-KC705
- TTC link: plan to use AC701 to handle remote control and monitoring

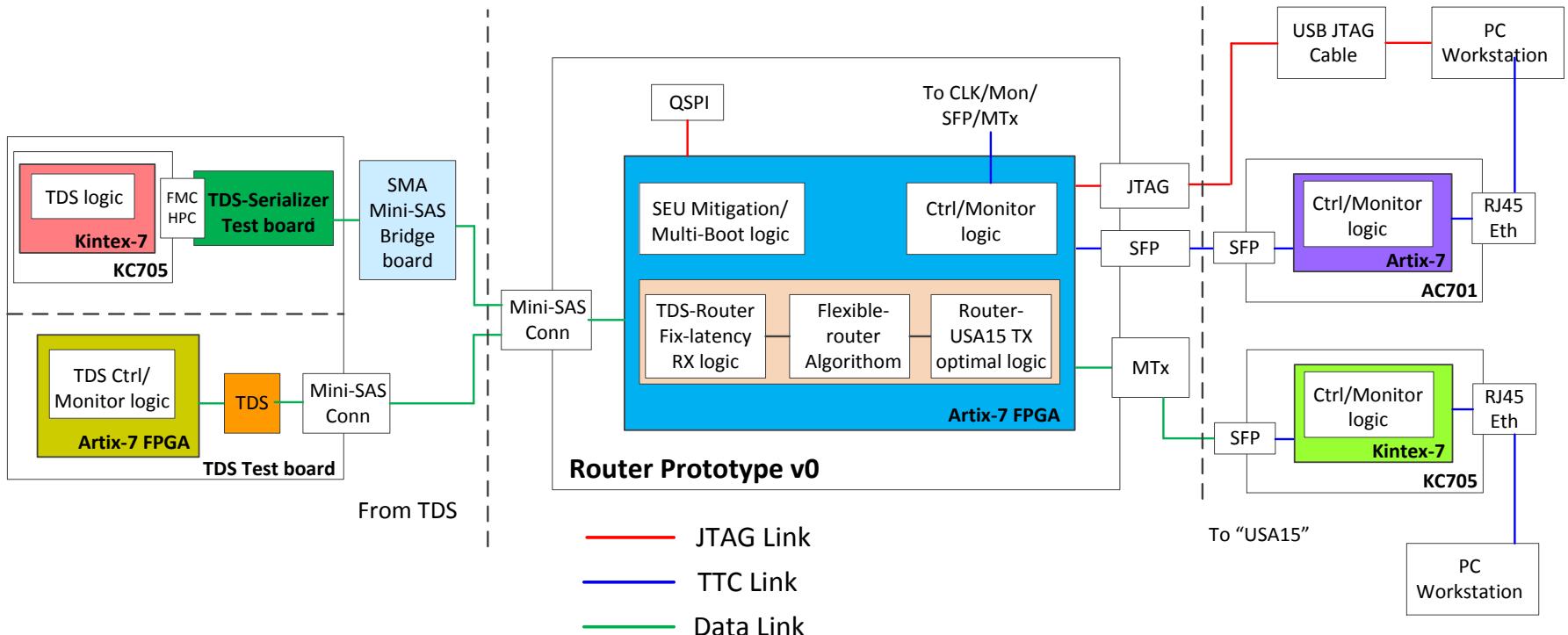
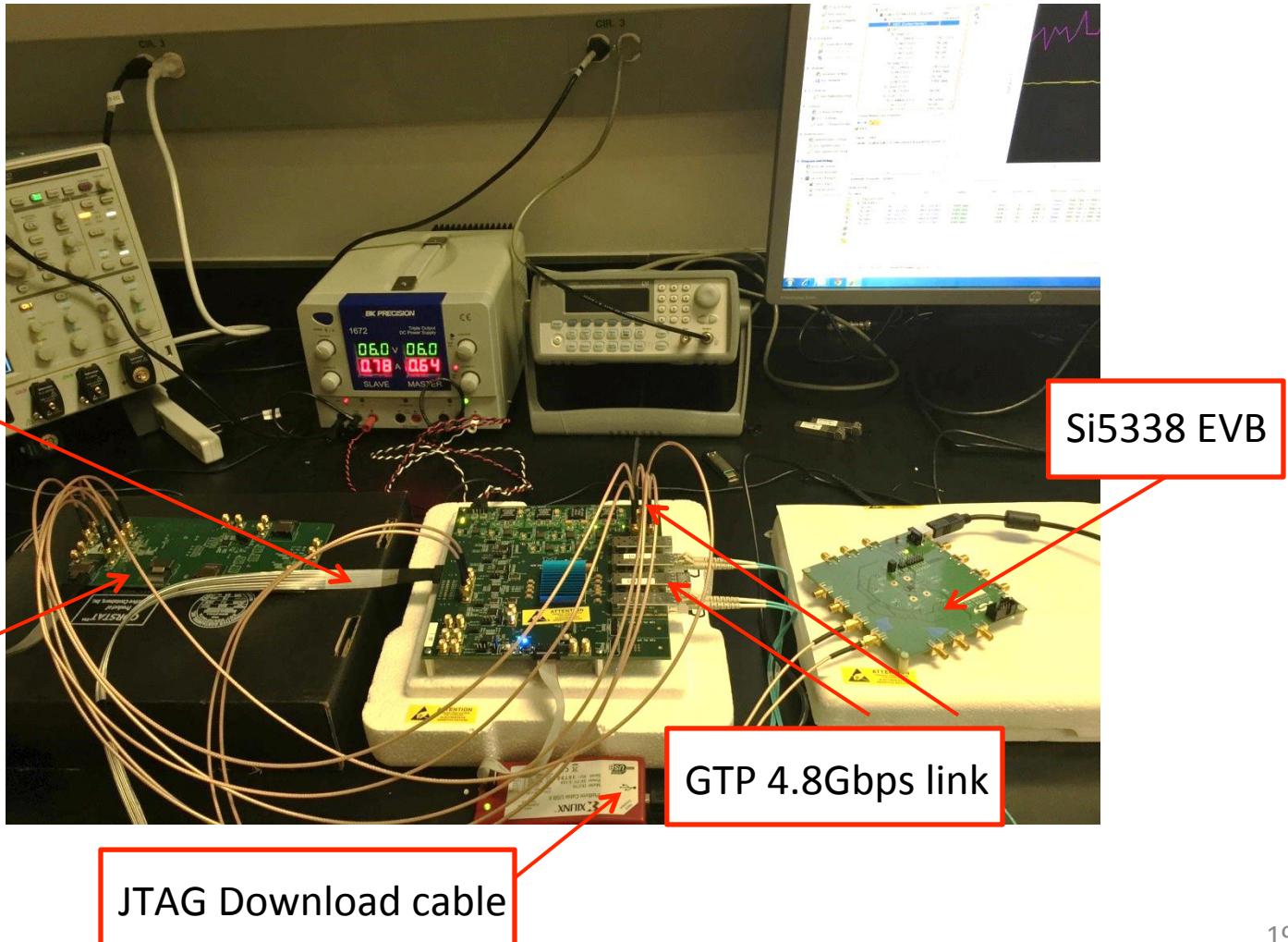


Figure 1: Router prototype v0 test plan

Prototype V0 Preliminary Testing

✧ Current test setup at University of Michigan





Prototype V0 Preliminary Testing

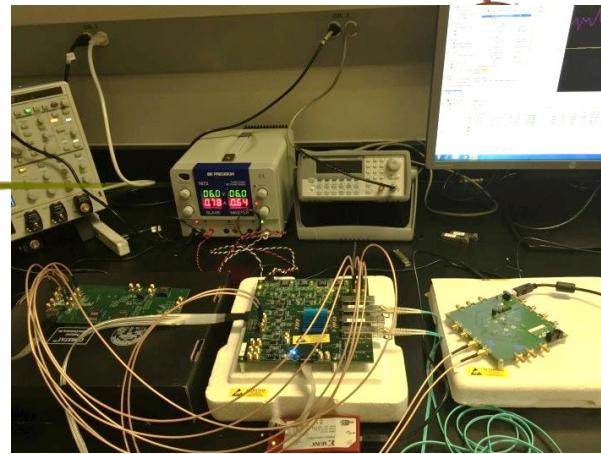
✧ Step by step evaluation test result

- Power supply test
 - Scheme 1: LTM4616 & LTM4619 [OK]
 - Scheme 2: LT8612 [OK]
- Repeaters (DS100BR410) [OK]
- Clock Distribution test
 - On board Oscillators [OK]
 - Clock Conditioner: LMK03200 [OK]
- Initial test of Artix-7 FPGA (XC7A200T-2FFG1156I)
 - Two sets of power-on sequence circuits [OK]
 - JTAG Download link [OK]
 - Simple logic test (blinking LED) [OK]
 - QSPI flash [OK]

Prototype V0 Preliminary Testing

❖ Step by step evaluation test result

- Artix-7 FPGA GTP link test
 - IBERT Test
 - GTP & SFP → Two SFP Links [OK] (4.8 Gbps, BER 3.23E-15)
→ The other two still under debugging
 - GTP TX → SMA → MiniSAS SMA Bridge board → MiniSAS → Repeater → GTP RX [OK] (4.8 Gbps, BER 3.23E-15)



Serial I/O Links																
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
Ungrouped Links (0)																
Link Group 1 (5)							Reset	PRBS 7-bit	PRBS 7-bit			Inject	Reset	Reset		None
Link 1	MGT_X1Y1/TX	MGT_X1Y1/RX	4.800 Gbps	3.092E14	0E0	3.234E-15	Reset	PRBS 7-bit	PRBS 7-bit			Inject	Reset	Reset	Locked	Locked
Link 3	MGT_X1Y3/TX	MGT_X1Y3/RX	4.800 Gbps	3.092E14	0E0	3.234E-15	Reset	PRBS 7-bit	PRBS 7-bit			Inject	Reset	Reset	Locked	None
Link 5	MGT_X1Y5/TX	MGT_X1Y5/RX	4.800 Gbps	3.092E14	0E0	3.234E-15	Reset	PRBS 7-bit	PRBS 7-bit			Inject	Reset	Reset	Locked	None
Link 6	MGT_X1Y6/TX	MGT_X1Y6/RX	4.800 Gbps	3.092E14	0E0	3.234E-15	Reset	PRBS 7-bit	PRBS 7-bit			Inject	Reset	Reset	Locked	None
Link 7	MGT_X1Y7/TX	MGT_X1Y7/RX	4.800 Gbps	3.092E14	0E0	3.234E-15	Reset	PRBS 7-bit	PRBS 7-bit			Inject	Reset	Reset	Locked	Locked

MGTX1Y1 & MGTX1Y3: SFP Link

17 hours test

MGTX1Y5 & MGTX1Y6 & MGTX1Y67: SMA Twinax Link

Prototype V0 Preliminary Testing

❖ TDS-Router full link & latency test

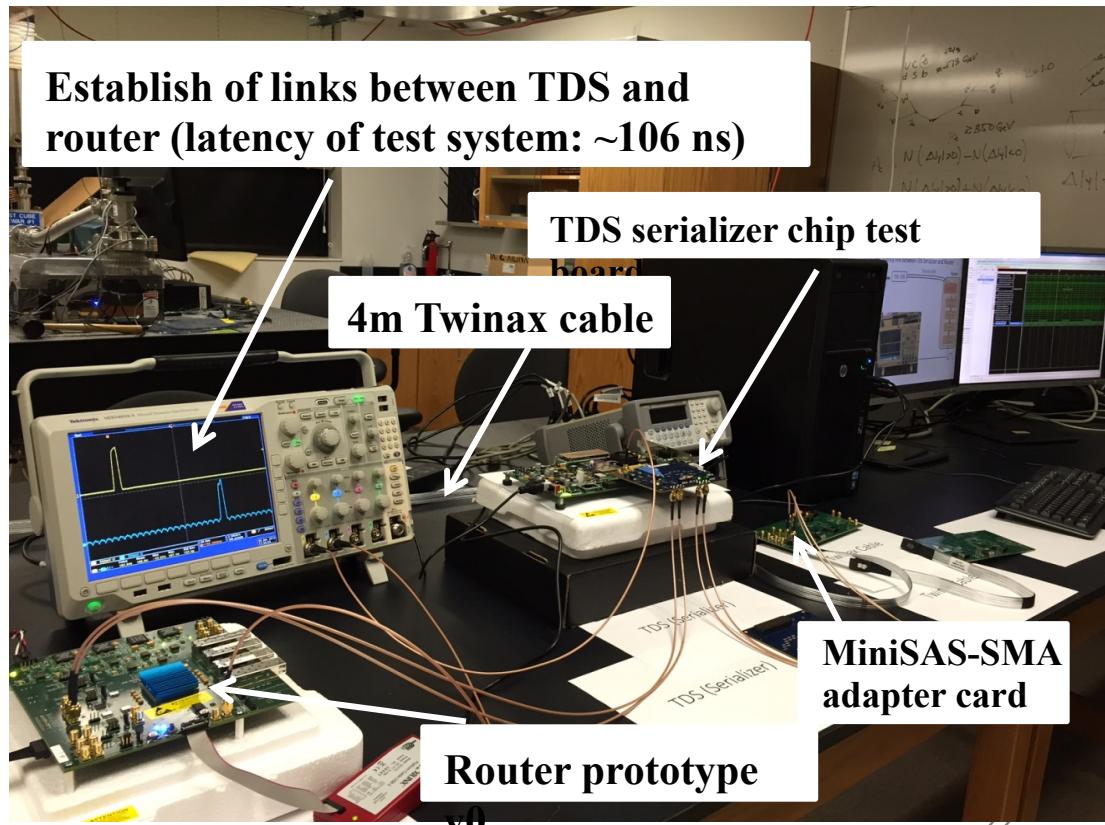
- Functionality: Router Optimal GTP RX logic + Sync. Buffer + Cutting-through switching algorithm (**tested with TDS current data format**)
- Latency of TDS-Router link is tested (Total ~106ns)

TDS end ~22ns

Cable latency (4m Twinax + 1m SMA)
~25ns

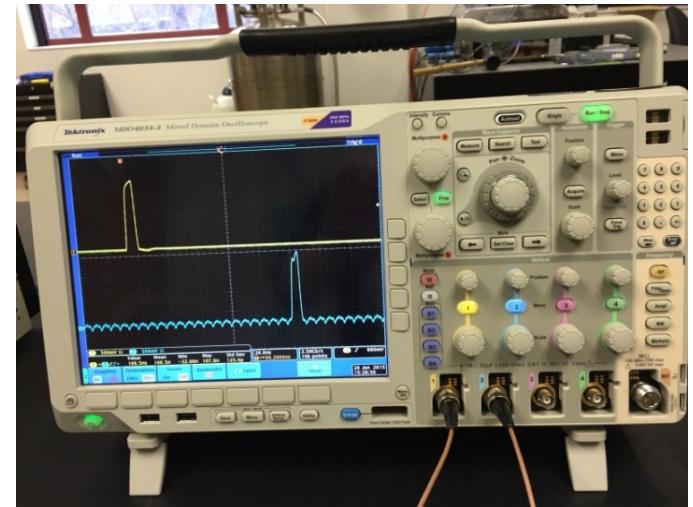
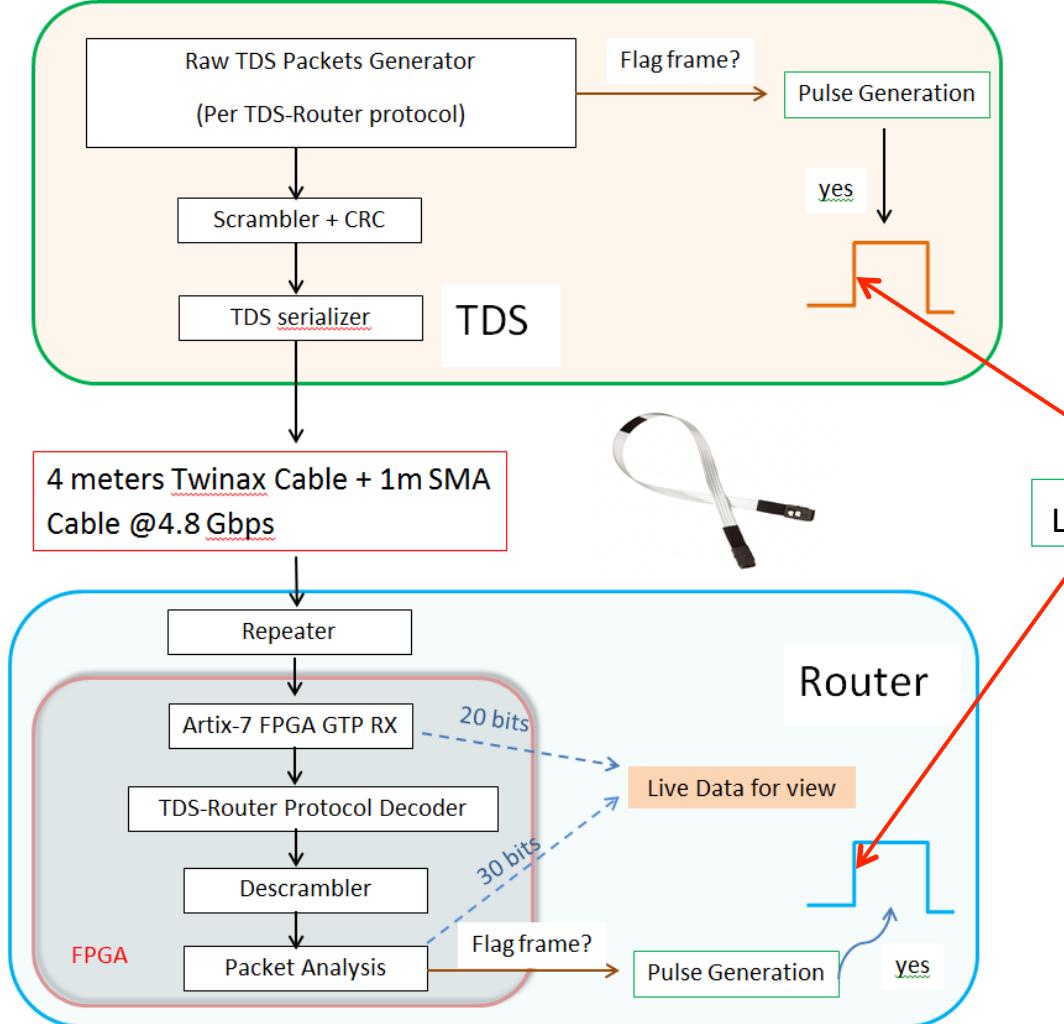
Reading time ~6.25ns

Router optimal RX + Sync. Buffer +
Cutting-through ~ 53ns (matched
with latency estimation)



Prototype V0 Preliminary Testing

❖ Serial link rate: 4.8 Gbps



Latency showed on scope: rising edge to rising edge

- Latency showed on scope
 - TDS end ~22ns
 - Cable total length 5m ~25ns
 - Reading time ~ 6.25ns
 - Router RX end ~53ns



Next Step

✧ More tests of prototype v0 in next

- Monitoring chip (LTC2991 & LT2945) test: I2C
- MTx test: I2C
- Evaluate TDS-Router link based on three possible TDS data formats
- SEU firmware development
- Five more v0 are under assembly: will be used in Artix-7 FPGA radiation test
- Integrate test of full router firmware
- Repeater, LMK03200 radiation test?

✧ Will start design prototype v1 soon

- GBT-SCA will be implemented on this version if it is ready
- Evaluate power scheme with FEAST device
- More options on optical transmitter



General Project Schedule

First prototype design, construction, and testing	1-Oct-2015
Second prototype design, construction, and testing	29-Apr-2016
Final Production Readiness Review	29-Nov-2016
Final prototype production and shipping	7-Apr-2017

Open issues

1. Router envelope limitations
2. Power device choices (FEAST ?)
3. Cooling issues for router
4. Optical transmitter options
5. Router output link speed
6. Router BC clock choice
7. The number of E-Links connected to router
8. Router configuration options
9. Radiation Tolerance Criteria for router components

Backup

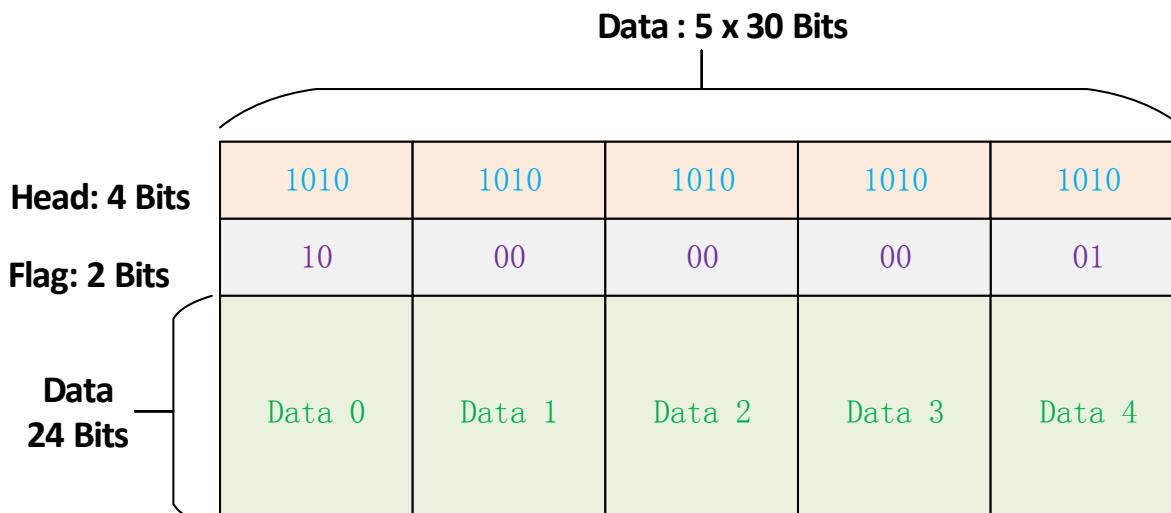
Current TDS Data format

# bits	Data field
12	BCID
8	Band-ID
5	Phi-id
4	Checksum or CRC
29	Total

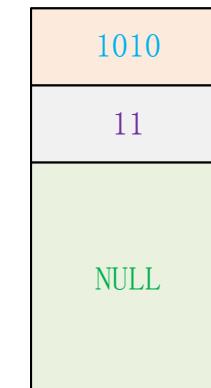
Field	15 strips with Hi/Low
Hi/Low	1
Hit map	
# strips	15
Strip data	90
Total length	$120=29+1+90$

- Data: 120 bits / trigger
- Need additional bits for building a stable serial link with router

120 bits of data occupied 4 frames of 30 bits, plus additional serial overhead,
At least we need 5 frames to send out all the info.



Example of a data frame



Example of two NULL frames

Summary of possible TDS/Router data formats

Router FPGA Selection

- Larger number of I/O's to minimize the number of FPGA's we need
- > 5Gbps Tx/Rx
- Low cost (\$50K-\$100K for all FPGA's needed)

FPGA	Spartan-6/ XC6SLX75T-3	Artix-7/ XC7A200T-2	Kintex-7/ XC7K325T-2
# of Transceivers	8	16	16
Speed	3.2Gb/s	6.6Gb/s	10.3125Gb/s
Logic cell	74,637	215,360	326,080
Price	~\$170	~\$280	~\$1550
TX Latency	4.5~11 Cycles	66~234UI	94~421 UI
RX Latency	12~20+ Cycles	141~916UI	136.5~967.5UI

Table 1: Comparison of Xilinx Low cost FPGA

LMK03200

Clock jitter		Random (RMS, ps)	periodic (pk-pk, ps)
Before cleaner		5.9	81.2
After cleaner	CDCE62005	5.1	6.5
	LMK03200	1.4	12.9

Device	Part number	Radiation	TID (Gy)	Degradation	Max power current change
QSFP optical transceiver	AFBR-79EIDZ	X-ray	81	No	Not measured
Jitter cleaner	LMK03200	X-ray	149	No	1%
LVDS-LVTTL clock buffer	CDCLVC1310	X-ray	12300	No	15%
LVDS block buffer	CDCLVD1212	$^{60}\text{Co } \gamma$	11300	No	50%

[Ref]: “The Clock Distribution System for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade Demonstrator”

- Los Alamos Neutron Science Center (LANSCE)
- Maximum energy: 800MeV

Device	Radiation type	Non-SEFI SEU		SEFI	
		σ (cm ²)	Est. err rate (1/week)	σ (cm ²)	Est. err rate (1/week)
AFBR-79EIDZ RX	Proton	$<1.3 \times 10^{-11}$	<0.02	$<1.3 \times 10^{-11}$	<0.02
AFBR-79EIDZ TX+RX	Neutron	$<2.3 \times 10^{-11}$	<0.03	$<2.3 \times 10^{-11}$	<0.03
LMK03200	Neutron	$<2.5 \times 10^{-11}$	<0.04	6.1×10^{-10}	0.88
CDCLVD1212	Neutron	$<2.3 \times 10^{-11}$	<0.03	$<2.3 \times 10^{-11}$	<0.03
CDCLVC1310	Neutron	$<8.0 \times 10^{-12}$	<0.01	$<8.0 \times 10^{-12}$	<0.01
XC7K325T RX	Neutron	$<2.2 \times 10^{-10}$	<0.31	$<2.0 \times 10^{-10}$	<0.31

Router FPGA Power Estimation

Xilinx Power Estimator (XPE) - 2014.2
Artix®-7, Kintex®-7, Virtex®-7, Zynq®-7000
Release: 4-Jun-2014

Project

Settings

Family	Artix-7
Device	XC7A200T
Package	FFG1156
Speed Grade	-2
Temp Grade	Industrial
Process	Typical
Voltage ID Used	
Characterization	Production, v1.0, 2012-07-11

Environment

Junction Temperature	<input type="checkbox"/> User Override
Ambient Temp	25.0 °C
Effective OJA	<input type="checkbox"/> User Override
Airflow	250 LFM
Heat Sink	None
OSA	
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
OJB	
Board Temperature	

Implementation

Optimization	Power Optimization
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Summary

Total On-Chip Power	5.385 W
Junction Temperature	40.7 °C
Thermal Margin	59.3°C / 19.7W
Effective OJA	2.9 °C/W
Power supplied to off-chip devices 0.000W	

46%	Transceiver.....	2.467W
0%	I/O.....	0.021W
51%	Core Dynamic..	2.720W
3%	Device Static....	0.177W

On-Chip Power

Resource	Power (W)	(%)
CLOCK	0.854	16
LOGIC	1.755	33
BRAM	0.112	2
DSP	0.000	0
PLL	0.000	0
MMCM	0.000	0
Other	0.000	0
PCIE	0.000	0
I/O	0.021	0
GTP	2.467	46
Transceiver		
Device Static	0.177	3

Power Supply

Source	Voltage	Total (A)
V _{CCINT}	1.000	3.100
V _{CCBRAM}	1.000	0.009
V _{CCAUX}	1.800	0.043
V _{CCAUX_I_O}		
V _{CCO 3.3V}	3.300	
V _{CCO 2.5V}	2.500	
V _{CCO 1.8V}	1.800	
V _{CCO 1.5V}	1.500	
V _{CCO 1.35V}	1.350	
V _{CCO 1.2V}	1.200	
-	1.800	
MGTAV _{CC}	1.000	1.231
MGTAV _{TT}	1.200	0.777
-		
-		
-		
-		
V _{CCADC}	1.800	0.020

Messages

[XILINX Power Advantage \(check for updates\)](#)
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[File Support Request \(WebCase\)](#)
[Introduction to XPE \(video\)](#)

[Whitepaper - 7 Steps for Worst Case Power Estimation](#)

Summary Snapshot Graphs IP_Manager Clock Logic IO BRAM DSP CLKMGR GTP Other User Release

Xilinx Latency Table for 7-Series FPGA

FPGA RX interface	Data width =16	Data Width=20	Data Width=32	Data width = 40	Data width = 32 (4x2 mode)	Data width=40 (4x2 mode)
	2 RXUSRCLK	2 RXUSRCLK	2 RXUSRCLK	2 RXUSRCLK	1 RXUSRCLK + 1 RXUSRCLK2	1 RXUSRCLK + 1 RXUSRCLK2
Comma Detect	With Bypass Comma alignment block			Without bypassing Comma alignment block		
	1 XCLK cycle			The latency through the block is 2 XCLK cycles plus NN UI, where NN is the comma alignment selection (internal variable sel[6:0]). Please see Comma Detect table alongside.		
8B10B decoder	Use 8B10 Decoder			Without 8B10B Decoder		
	1 XCLK			0		
Rx Elastic Buffer	Bypassed			Used		
	Internal data width =16	Internal data width =20	Internal data width =16	Internal data width =20	3-30 USRCLK	3-30 USRCLK
RX PMA Latency in UI	bypassing RX buffer			When using RX buffer		
	Internal data width =16	Internal data width =20	Internal data width =16	Internal data width =20	93	107
Total Rx latency in UI	Minimum			Maximum		
	141			916		

- Minimum latency based on bypassing PCS blocks (See <http://www.xilinx.com/support/answers/58981.html>)
- Essential blocks will be implemented and optimized in user logic
- Red circled blocks represent minimal chosen options
- Note absolute lowest achievable latency for RX is RX PMA + 3 RXUSRCLK = 141 UI (data with 16)
- Fixed PMA dominates latency (105 UI)

