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## 2 ATLAS NSW Electronics Specification

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### Component or Facility Name: VMM

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5 VMM is the front end ASIC to be used in the front end electronics readout system of  
both the Micromegas and sTGC detectors of the New Small Wheels Upgrade project

6

Version: v0.1

7

### *Abstract*

8 The VMM is a custom Application Specific Integrated Circuit (ASIC). It is intended to be used  
9 in the front end readout electronics of both the Micromegas and sTGC detectors of the New  
10 Small Wheels Phase I upgrade project. It is being developed at Brookhaven National Laboratory  
11 by Gianluigi de Geronimo and his microelectronics design group. It is fabricated in the 130 nm  
12 IBM 8RF-DM CMOS process. The 64 channels with highly configurable parameters will meet  
13 the processing needs of signals from all sources of both detector types:

- 14 • Negative anode strip signals from the Micromegas detectors.
  - 15 • Negative wire group signals from the sTGC detectors
  - 16 • Positive cathode strip signals from the sTGC for precision spatial reconstruction.
  - 17 • Positive cathode pad signals used in the sTGC trigger.
- 18 To accomplish this the VMM has four independent data output paths:
- 19 • Precision (10-bit) amplitude and (effective) 20-bit time stamp read out at Level 1 accept.
  - 20 • A serial out Address in Real time (ART) at every bunch crossing for the Micromegas  
Trigger.
  - 22 • Parallel prompt outputs from all 64 channels in a variety of selectable formats (including  
a 6-bit ADC) for the sTGC trigger.
  - 24 • Multiplexed analog amplitude and timing outputs will not be used in the NSW but can  
be valuable in development and debugging.
- 26 Version 3 to be submitted in December of 2015 in a dedicated run will have all the design  
27 features including Level-0 buffer and Level-1 handshake logic, and SEU mitigation circuitry for  
28 both the configuration registers and the state machines. The devices will be packaged in a Ball  
29 Grid Array with outline dimensions of 21x21 mm consistent with the Micromegas strip pitch.

30

### Revision History

31

Rev. No.	Proposed Date Approved Date	Description of Changes (Include section numbers or page numbers if appropriate)	Proposed by: author Approved by: author
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	P: A:		P: A:

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## 72 1 Conventions and Glossary

73 <b>ADC</b>	Analog to Digital Converter.	90 <b>MO</b>	Monitoring Output.
74 <b>ART</b>	Address in Real Time.	91 <b>MOSFET</b>	Metal Oxide Semiconductor Field Effect Transistor.
75 <b>ASIC</b>	Application-Specific Integrated Circuit.	92 <b>MSB</b>	Most Significant Bit.
76 <b>BGA</b>	Ball Grid Array.	93 <b>NSW</b>	New Small Wheel.
77 <b>CA</b>	Charge Amplifier.	94 <b>PDO</b>	Peak Detector Output.
78 <b>CMOS</b>	Complementary Metal Oxide Semiconductor.	95 <b>PtP</b>	Pulse to Peak.
80 <b>DAC</b>	Digital to Analog Converter.	96 <b>PtT</b>	Peak to Threshold.
81 <b>DDF</b>	Delayed Dissipative Feedback.	97 <b>ROC</b>	Read Out Controller.
82 <b>DDR</b>	Double Data Rate.	98 <b>SEU</b>	Single Event Upset.
83 <b>DICE</b>	Dual Interlocked Cells.	99 <b>SLVS</b>	Scalable Low Voltage Signaling.
84 <b>EAR</b>	Export Administration Regulations.	100 <b>sTGC</b>	small Thin Gap Chambers.
85 <b>ENC</b>	Equivalent Noise Charge.	102 <b>TAC</b>	Time to Amplitude Converter.
86 <b>ESD</b>	Electrostatic Discharge.	103 <b>TDO</b>	Time Detector Output.
87 <b>FIFO</b>	First In First Out.	104 <b>TID</b>	Total Ionizing Dose.
88 <b>LSB</b>	Least Significant Bit.	105 <b>TMR</b>	Triple Modular Redundancy.
89 <b>Micromegas</b>	Micro Mesh Gaseous Structure	106 <b>ToT</b>	Time over Threshold.
		107 <b>TtP</b>	Threshold to Peak.

## 108 2 Related Documents

- 109 The VMM interfaces directly with 3 custom ASICs and indirectly with one. A brief description  
 110 of the functionality of these ASICs and the relevant printed circuit boards, the specifications  
 111 documents, as well as links to these document are provided below.
- 112 **1. The ReadOut Controller (ROC).** It reads data out of up to 8 VMM chips and provides  
 113 all interface readout control signals:  
 114 [https://edms.cern.ch/file/1470540/1/NSW\\_VMM3\\_ROCReviewFeb2015\\_PDR\\_20150507.pdf](https://edms.cern.ch/file/1470540/1/NSW_VMM3_ROCReviewFeb2015_PDR_20150507.pdf)
- 115 **2. The Slow Control Adapter (SCA).** Used for configuration and monitoring of the VMM.  
 116 <https://espace.cern.ch/GBT-Project/GBT-SCA/default.aspx>

- 117 **3. The Trigger Data Serializer (TDS).** It is used to handle the prompt signals (ToT and  
118 strips) used in the sTGC trigger  
119 [https://indico.cern.ch/event/327350/contribution/2/attachments/635918/875421/sTGC\\_Review\\_largerfigures.pdf](https://indico.cern.ch/event/327350/contribution/2/attachments/635918/875421/sTGC_Review_largerfigures.pdf)
- 121 **4. The Front End Card with 8 vmm (MMFE-8),** is the front end card with 8 VMM chips  
122 (512 channels) used by the Micromegas Detectors  
123 [https://edms.cern.ch/file/1470529/1/NSW\\_MMFE-8-Specification-020515\\_PDR.pdf](https://edms.cern.ch/file/1470529/1/NSW_MMFE-8-Specification-020515_PDR.pdf)
- 124 **5 The Address in Real Time (ART) ASIC** receives synchronously with the BC clock the  
125 ART signals from up to 32 VMM, encodes the strip address of those VMM with a hit, appends  
126 the BCID and transmits the data to the MM trigger processor.  
127 [https://edms.cern.ch/file/1472976/1/NSW\\_ART\\_ASIC\\_specs\\_PDR\\_2015\\_2.docx](https://edms.cern.ch/file/1472976/1/NSW_ART_ASIC_specs_PDR_2015_2.docx)
- 128 **6 The ART Data Driver Card (ADDC)** is the PCB housing the ART ASIC and GBT  
129 chipset.  
130 [https://edms.cern.ch/file/1470535/1/NSW\\_ADDC\\_document\\_v1.0\\_PDR\\_2\\_2015.pdf](https://edms.cern.ch/file/1470535/1/NSW_ADDC_document_v1.0_PDR_2_2015.pdf)
- 131 **7 sTGC Analog Requirements for the New Small Wheel VMM3 ASIC**  
132 [https://edms.cern.ch/file/1536160/1/VMM3\\_Analog\\_Requirements\\_sTGC\\_EDMS\\_SpecsDocument\\_20150814.docx](https://edms.cern.ch/file/1536160/1/VMM3_Analog_Requirements_sTGC_EDMS_SpecsDocument_20150814.docx)

### 134 **3 Description of Component or Facility**

135 The VMM is composed of 64 linear front-end channels. A block diagram of one of the identical  
136 channels is shown in Fig. 1. Each channel integrates a low-noise charge amplifier (CA) with  
137 adaptive feedback, test capacitor, and adjustable polarity (to process either positive or negative  
138 charge) optimized for a capacitance of 200 pF and a peaking time of 25 ns. The input MOSFET  
139 is a p-channel with gate area  $L \times W = 180 \text{ nm} \times 10 \text{ mm}$  (200 fingers, 50  $\mu\text{m}$  each) biased at a drain  
140 current  $ID = 2 \text{ mA}$ ; this corresponds to an inversion coefficient  $IC \approx 0.22$ , a transconductance  
141  $g_m \approx 50 \text{ mS}$ , and a gate capacitance  $C_g \approx 11 \text{ pF}$ . The filter (shaper) is a third-order designed in  
142 delayed dissipative feedback (DDF) [1], has adjustable peaking time in four values (25, 50, 100,  
143 and 200 ns) and stabilized, band-gap referenced, baseline. The DDF architecture offers higher  
144 analog dynamic ranges, making possible a relatively high resolution at input capacitance much  
145 smaller than 200 pF. The gain is adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).

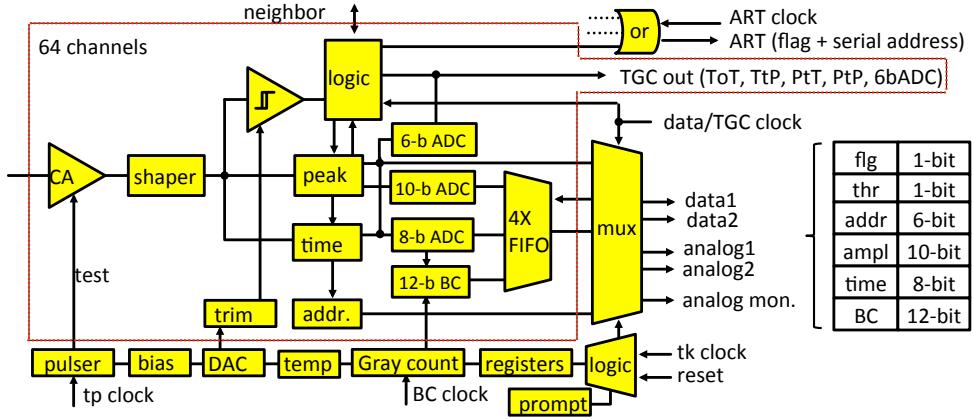


Figure 1: Architecture of VMM2.

146 Next to the shaper are the sub-hysteresis discriminator [2] with neighboring and trimming,  
 147 the peak detector and the time detector. The sub-hysteresis function allows discrimination of  
 148 pulses smaller than the hysteresis of the comparator circuit. The threshold is adjusted by a  
 149 global 10-bit DAC and an individual channel 4-bit trimming DAC. The neighbor channel logic  
 150 forces the measurements of channels neighboring a triggered one, even if the channel does not  
 151 have a signal over the set threshold. The neighbor logic extends also the two neighboring  
 152 chips through bidirectional IO. The peak detector measures the peak amplitude and stores it  
 153 in an analog memory. The time detector measures the peak timing using a time-to-amplitude  
 154 converter (TAC), i.e. a voltage ramp that starts at the time of the peak and stops either when  
 155 ena is lowered or at a clock cycle of the BC clock, depending on the mode of operation as  
 156 described below. The TAC value is stored in an analog memory and the ramp duration is  
 157 adjustable in four values (125 ns, 250 ns, 500 ns, 1  $\mu$ s). The peak and time detectors are followed  
 158 by a set of three low-power ADCs (a 6-bit, a 10-bit, and a 8-bit), characterized by a domino  
 159 architecture [3] but of new concept. These ADC are enabled depending on the selected mode of  
 160 operation.

161 The ASIC can operate in either a two phase analog mode (not used in NSW), or in a  
 162 continuous , simultaneous read/write mode. In the two phase mode data are registered while  
 163 the VMM is in acquisition mode and then read out after the system is switched to the read out  
 164 mode. Acquisition is re-enabled after the readout phase is completed. In continuous mode the  
 165 simultaneous read/write of data assures dead-timeless operation that can handle rates up to the  
 166 maximum of 1 MHz per channel, expected at the NSW. The ASIC has four independent output  
 167 data paths:

- 168 1. Multiplexed analog amplitude and time stamp
- 169 2. Digitized (10-bit amplitude, 8-bit vernier time stamp) in a 2-bit (DDR readout) digital  
 170 multiplexed mode in either a short four-word buffer existing already in VMM2 or a buffered
- 171 3. Address in Real Time (ART) used in the VMM trigger
- 172 4. Direct SLVS outputs of all 64 channels in parallel in one of five selectable formats, used in  
 173 the sTGC trigger

<sup>174</sup> The overall connection scheme of these data paths with the rest of the NSW readout and trigger  
<sup>175</sup> components is shown in Figure 2 and a detailed description of all modes of operation will be  
<sup>176</sup> described in Section 11.

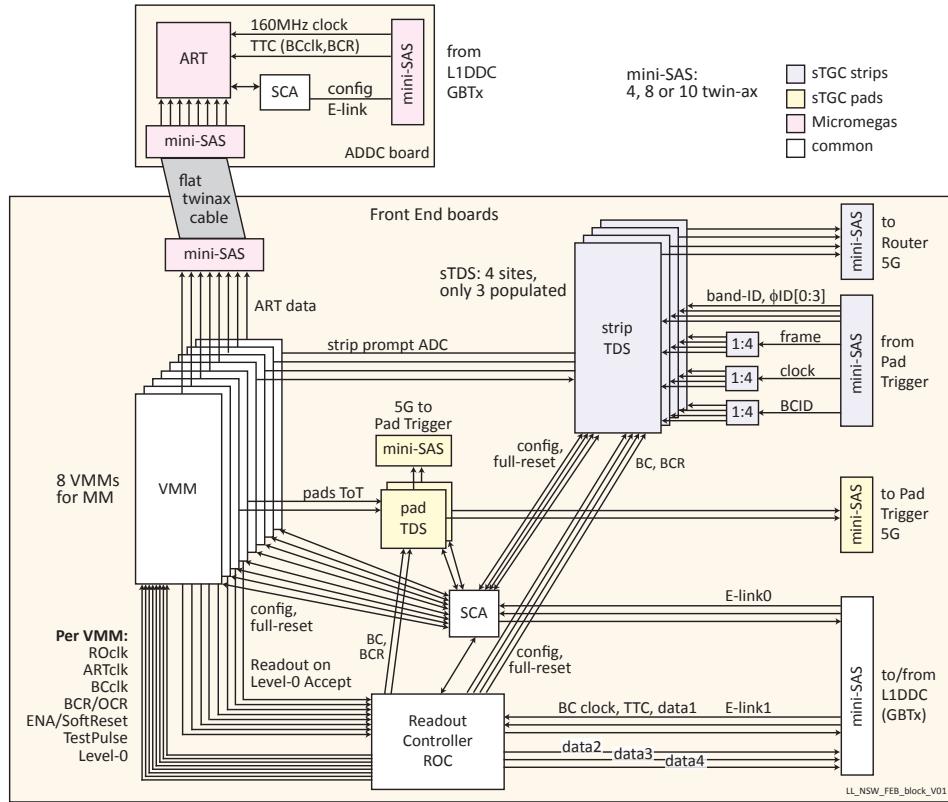


Figure 2: Overall connection diagram of the VMM.

<sup>177</sup> Finally, the ASIC includes global and acquisition resets, an adjustable pulse generator connected to the injection capacitor of each channel, adjustable with a global 10-bit DAC, and  
<sup>178</sup> triggered with the external clock tp, a threshold generator adjustable with a global 10-bit DAC,  
<sup>179</sup> a band-gap reference circuit, a temperature sensor. It also integrates analog monitor capability  
<sup>180</sup> to directly measure the global DACs, the band-gap reference, a temperature sensor, the analog  
<sup>181</sup> baseline, the analog pulse, and the channel threshold (after trimming). An analog buffer can be  
<sup>182</sup> enabled using the bits sbfm. The monitor is controlled with global register bits scmx, sm0-sm5  
<sup>183</sup> and channel register bit smx. The analog monitor can be routed to the pdo output using the  
<sup>184</sup> register bit sbmx.  
<sup>185</sup>

## <sup>186</sup> 4 Signal Processing requirements

<sup>187</sup> Both MicroMegas and sTGC chambers of the NSW Upgrade will use the VMM as their front  
<sup>188</sup> end processing ASIC. In this section are specified the analog requirements for the VMM for both  
<sup>189</sup> detectors. There are several changes w.r.t. VMM2 as a result of the beam, lab and chamber  
<sup>190</sup> measurements, and as a result of extensive discussions and studies done jointly by the detector

<sup>191</sup> and electronics team.

## <sup>192</sup> 4.1 MicroMegas Detectors

<sup>193</sup> The Micromegas signals from the anode strips (negative polarity signals) depending on the  
<sup>194</sup> chosen gas gain and shaper integration time can be up to a maximum 250 fC, but typically half  
<sup>195</sup> or even one fourth of the maximum. The input current waveform is shown in Figure 3.

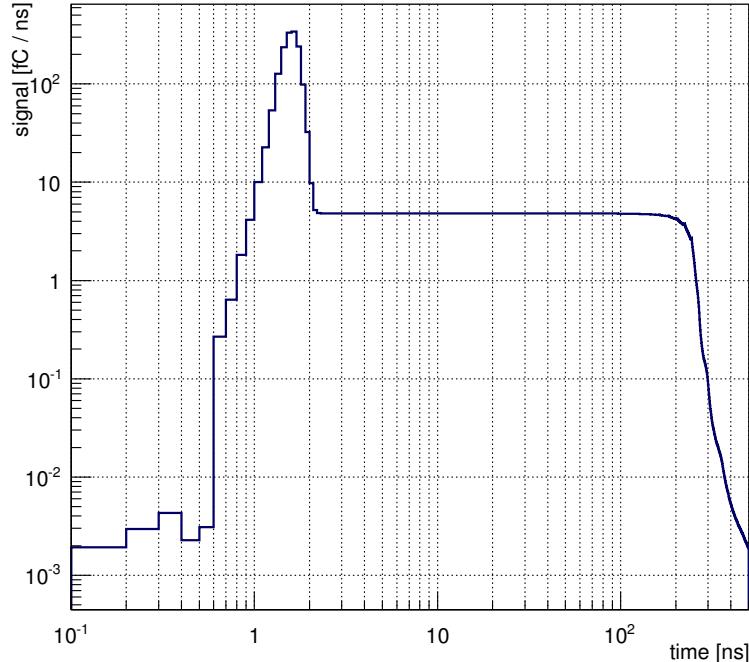


Figure 3: Simulated current induced by the motion of electrons and positive ions during the avalanche formation within the 128  $\mu\text{m}$  amplification region of micromegas (the actual input to the VMM is of negative polarity).

<sup>196</sup> The fast electron current is followed by the positive ion current. One can notice two features.  
<sup>197</sup> Since the ions are moving in a constant electric field the current is uniform. Because of the short  
<sup>198</sup> distance to the wire mesh (128  $\mu\text{m}$ ) the total signal duration is  $\sim$ 200 ns [4]. In addition to  
<sup>199</sup> the current waveform and maximum input charge, the other relevant parameter is the electrode  
<sup>200</sup> (anode strip) capacitance which varies from about 50 to 200-300 pF depending on the length of  
<sup>201</sup> the strips.

## <sup>202</sup> 4.2 sTGC Detectors

<sup>203</sup> For sTGC chambers, there are 3 different types of active elements on a detector: Strips, wires  
<sup>204</sup> and pads. All 3 are read out via the VMM. Strips provide the precision coordinate measurement  
<sup>205</sup> for track reconstruction, wires the second coordinate and pads are used for triggering purposes

requiring a 3 out of 4 coincidence between the signals of pads in consecutive layers. The wire signals are negative while both the strip and pad sigmas are positive. Hence the need for the VMM to handle both polarities. A typical current waveform from an sTGC detector is shown in Figure 4. The total charge and the long ion tail impose specific requirements on the processing of the sTGC signals and are outlined below.

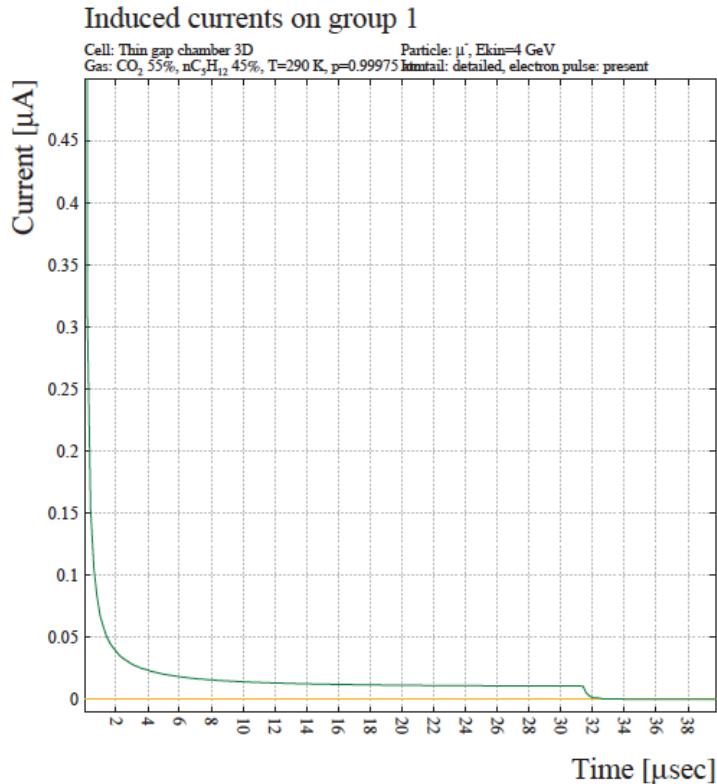


Figure 4: Simulated current induced by the motion of electrons and positive ions in an sTGC detector.

### 4.3 Wire Signals

1. The VMM should recover from wire signals of  $\langle Q_w \rangle = 6 \text{ pC}$  within 200 ns .
2. The linearity is not a critical factor here; however it is desirable for the linearity up to 2 pC to be known in order to apply offline corrections.

### 4.4 Pad Signals

1. In ADC mode, the VMM should recover from pad signals of  $\langle Q_p \rangle = \langle Q_w \rangle / 2 = 3 \text{ pC}$  within 250 ns .
2. The linearity is not a critical factor here; however it is desirable for the linearity up to 2 pC to be known in order to apply offline corrections.
3. In direct-timing-only mode (Time-over-Threshold and 6-bit ADC):

- 221       (a) if the pulse charge is less than 6 pC , the dead time shall be 60 ns after the trailing  
222       edge of the ToT pulse or 60 ns after the readout of the last bit.  
223       (b) if the pulse charge is more than 6 pC , the dead time increases with the charge and  
224       at 50 pC is expected to reach  $\approx 1 \mu\text{s}$  from the peak.

225     **4.5 Input Capacitance and Rate per VMM**

- 226     1. The capacitance of the largest pad on sTGC detectors will be 2 nF or less, defining the  
227       maximum capacitance the VMM must work within the requirements set out in the pre-  
228       ceding sections, in particular in terms of dead time and recovery time.  
229     2. The expected/estimated maximum rate at luminosity of  $7 \times 10^{34}$  is 0.8 MHz per VMM  
230       channel for pads and 0.9 MHz per VMM channel for strips. An average strip multiplicity  
231       of 4.7 is assumed in this, including from neighbor-on mode.

232     **5 Physical Description of the VMM**

233     The VMM is a fully custom ASIC fabricated in the 130 nm IBM 8RF-DM. process. In this  
234       section the current version, VMM2, is described since the final design is not yet available. It  
235       should be noted that the vast majority of the features, pin assignment and layout will be identical  
236       in the final version with only a very small number of pins (less than 6 out of 400) will be different.  
237     In what follows the VMM2 device will be described with the new features included when known,  
238       and the possible changes pointed out. The document will be updated as the new information  
239       becomes available.

240     The VMM2 is packaged in a 400 ball, 1 mm pitch BGA. The device size is  $21 \times 21 \text{ mm}^2$ .  
241       consistent with the pitch of the Micromegas detectors. The layout size is  $13.518 \times 8.384 \text{ mm}^2$   
242       and the die size is  $13.599 \times 8.464 \text{ mm}^2$ . The die layout is shown in Fig. 5. With the addition of  
243       the Level-0 buffer the die size is expected to increase by about 1 mm in its long side. Although  
244       it is possible to accommodate the few new pins required in the same 400 ball BGA, we are  
245       examining the possibility of using a higher ball count package in order to strengthen the power  
246       distribution, especially in the mixed signal supply. Again the overall layout will follow the one  
247       of the current device. The ball assignment is shown in Fig. 6, and the detailed pin list and their  
248       function in Table 1.

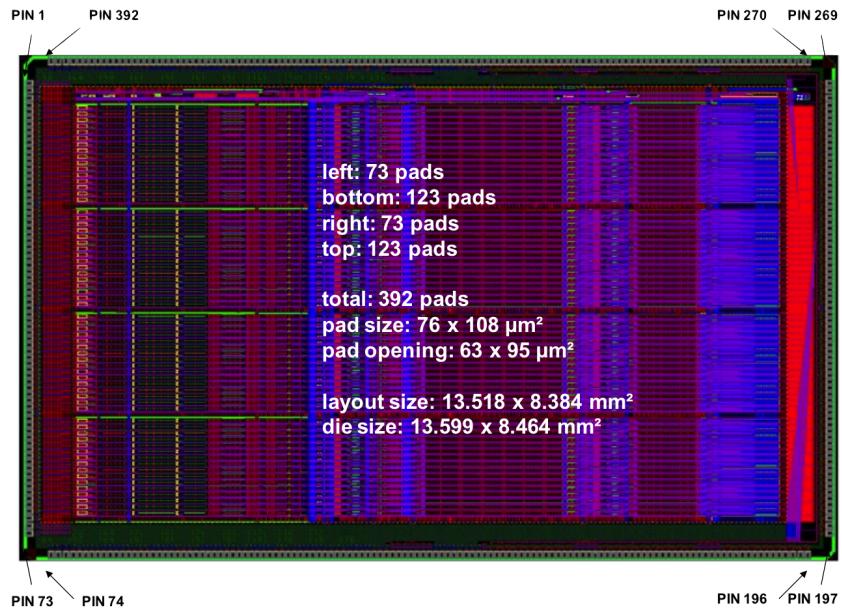


Figure 5: VMM2 die layout

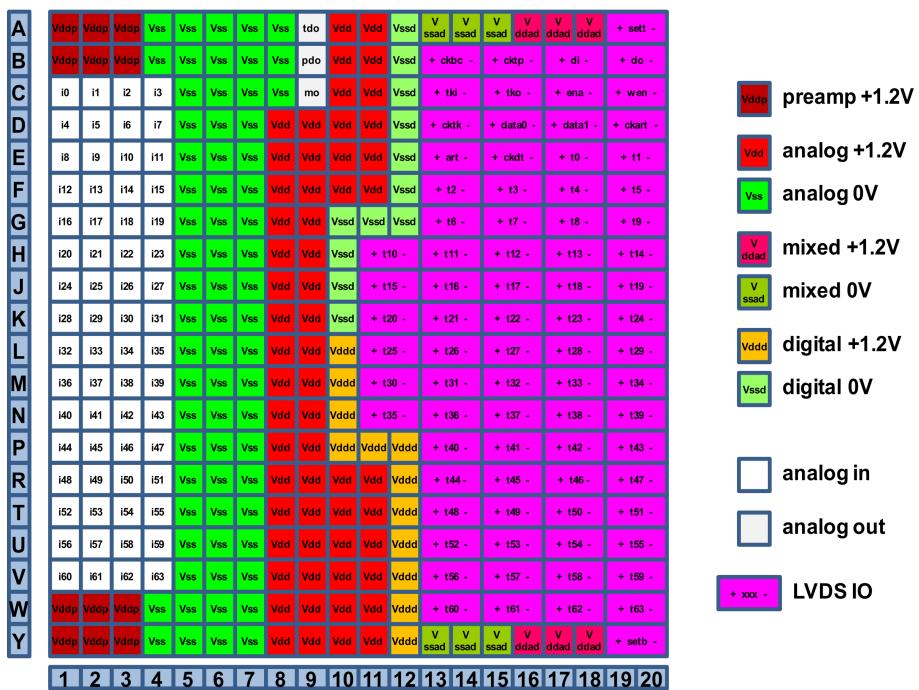


Figure 6: VMM2 pinout (top view)

## Specification for VMM

Table 1: Pad/Pin or Connector Assignments

<b>BGA Ball Assignment</b>	
<b>Ball/Pin name</b>	<b>Description-Comments</b>
Vdd,Vss	Analog supplies 1.2 V and grounds 0 V – 123 pins total, max current 400 mA
Vddd, Vssd	Mixed-signal (ADC) supplies 1.2 V and grounds 0 V – 12 pins, max current ~200 mA
Vddd, Vssd	Digital supplies 1.2 V and grounds 0 V 21 pins
Vddp	Charge amplifier supplies 1.2 V 9 pins, max current ~150 mA
i0-i63	Analog inputs ESD protected
mo	monitor multiplexed analog output
pdo	Peak Detector multiplexed output Not used by NSW
tdo	Time detector multiplexed analog output Not used by NSW
sett	Ch 0 neighbor trigger SLVS
ckbc	Bunch Crossing clock SLVS, Advances 12-bit Gray-code BC counter
cktp	Test Pulse Clock SLVS
di	Configuration data input CMOS in VMM3
do	Configuration data output CMOS in VMM3
tki	Level Zero (L0) Token input in analog mode
tko	Token output Used in analog mode only
ena	Acquisition start/stop: <ul style="list-style-type: none"> <li>• ena high, wen low: acquisition is enabled <ul style="list-style-type: none"> <li>• internally enabled after 40 ns from ena high</li> <li>• in two-phase (analog) mode is acquisition</li> <li>• in continuous (digital) mode is acquisition and readout</li> </ul> </li> <li>• ena low, wen low: in two phase (analog) is readout</li> <li>• ena pulse, wen high: configuration mode</li> </ul>
wen	Configuration enable <ul style="list-style-type: none"> <li>• wen high: configuration mode</li> <li>• wen pulse: acquisition reset (also resets BC counter)</li> </ul>
cktk	Token and configuration clock
data0	Flag and first data line in digital DDR mode (flag and address in analog mode)
data1	Second data line in digital DDR mode
ckart	Address in Real Time (ART) clock
art	ART output
ckdt	Data out and 6-bit ADC clock
ttp0-ttp63	Direct digital outputs
setb	ch63 neighbor trigger

249 **6 Manufacturer**

250 **6.1 Wafer Processing**

251 The VMM will be fabricated in the IBM 120 nm 8RF-DM CMOS process through MOSIS.  
252 Because of its size it is more economical to be submitted in a custom dedicated run even for  
253 prototypes. The wafers will be thinned to 0.010" (250  $\mu$  m), diced, inspected, and sorted to  
254 waffle packs.

255 **6.2 Packaging**

256 As mentioned in section 6 the VMM2 is packaged in a 400 ball BGA with 1 mm pitch. The  
257 design of the new substrate will start immediately after the design is completed in consultation  
258 with the groups designing the front end cards, and the packaging house. The new BGA may have  
259 a higher ball count and, necessarily, smaller pitch in order to strengthen the power distribution.  
260 The implications of this change are being studied and a decision will be made before the final  
261 design review. We are in contact with two new packaging vendors, IMEC and Signetics. They  
262 both agreed to accept the project in spite of the low (by industry standards) volume of 50,000  
263 chips at production.

264 **6.3 Export License Issues**

265 The design does include the PROMPT circuit. The appropriate office at BNL has determined  
266 that the VMM does not need Export Administration Regulations (EAR) license and, therefore,  
267 it can be freely distributed to all of our NSW collaborators.

268 **7 Power**

269 The VMM is designed to operate at a nominal voltage of 1.2 V . It requires four different supplies  
270 in order to minimize the contribution to the Equivalent Noise Charge (ENC) of the digital and  
271 mixed analog-digital circuits. These four power supplies are:

- 272 • **Vddp:** Charge amplifier supply connected to the sources of the p-channel input MOSFETs
- 273 • **Vdd:** Powers all other analog circuits
- 274 • **Vddad:** Mixed Analog–Digital (ADC)
- 275 • **Vddd:** Supplies the digital circuits and SLVS drivers

276 Table 2 summarizes the requirements and tolerances for the four supplies. The power dissipation  
277 depends on the selected functionality and mode of operation. It ranges from 500 mW to 800 mW.  
278 For example the SLVS outputs can be disabled when not needed, e.g., in Micromegas operation  
279 or the wire readout in the sTGC detectors.

Table 2: VMM Power Supply Requirements

Supply	Voltage[V]	Ripple	Max Current [mA]
Vddp	$1.2 \pm 5\%$	$< 10 \mu\text{V rms}, 1\text{--}10 \text{ MHz}$	150
Vdd	$1.2 \pm 5\%$	$< 100 \mu\text{V rms}, 1\text{--}10 \text{ MHz}$	400
Vddad	$1.2 \pm 5\%$	$< 100 \mu\text{V rms}, 1\text{--}10 \text{ MHz}$	200
Vddd	$1.2 \pm 5\%$	$< 1 \text{ mV rms}, 1\text{--}10 \text{ MHz}$	

## 280 8 Cooling

281 As mentioned already the VMM power dissipation depends on the features used with a maximum  
 282 of  $\sim 1 \text{ W}$ . Although not excessive, enclosed in a Faraday cage in the high density environment  
 283 of the NSW (especially in the case of Micromegas detectors), cooling of the VMM chips is  
 284 mandatory. A system with water as coolant is being designed by the teams working on the  
 285 detectors.

The IBM CMOS8RF Design Manual specifies the operating temperature range to be from  $-55^\circ\text{C}$  to  $12^\circ\text{C}$ . However device life time degrades rapidly at high temperatures. The case temperature should be kept below  $50^\circ\text{C}$  and preferably in the range  $30\text{--}50$  and should be verified and compared to the junction temperature provided by the VMM ASIC. The VMM includes a temperature sensor which can be read out by programming the monitor output and digitized by the SCA setting (in configuration mode)  $\text{scmx} = 0$ ,  $\text{sm5-sm0} = 000100$  (see Table 5). The die temperature is approximately given by given by:

$$^\circ\text{C} = 725 - \frac{V_{\text{sensor}}}{1.85}$$

where  $V_{\text{sensor}}$  is the temperature sensor reading in mV. The case temperature of a single-chip

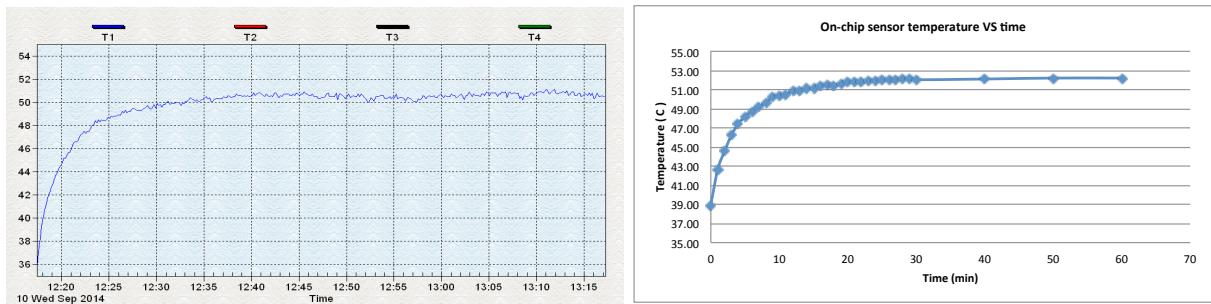


Figure 7: Left plot, the VMM case temperature. Right plot, the junction temperature as a function of time after turn-ON

286  
 287 board was measured from turn ON until thermal equilibrium and was compared with the die  
 288 temperature. The results are shown in Fig.7. The difference of about  $2^\circ\text{C}$  is consistent with the  
 289 typical junction to case thermal resistance for BGA devices of similar size,  $\sim 1^\circ\text{C/W}$ .

## 290 9 Input and Output

291 The input and output connections of the VMM are shown in Table 3.

## 292 10 Detailed Functional Description and Specifications

293 As mentioned already the VMM has four independent data paths and can operate in one of two  
 294 modes, two-phase (analog) and continuous (digital). Configuration of the ASIC is yet another  
 295 mode. In the following sections these modes and the relevant specifications will be described in  
 296 detail.

### 297 10.1 Configuration Process

298 The ASIC can be put in configuration mode by having the *wen* signal high and the *ena* low.  
 299 When in the configuration mode, the ASIC registers are accessible through the token clock *cktk*  
 300 and the data inputs *di*. The data transmitted are shifted at the falling edge of *ck* and latched  
 301 when the *wen* is low. The written configuration is available at the *do* output for daisy-chain  
 302 configuration. The timing diagram is shown in Figure 8.

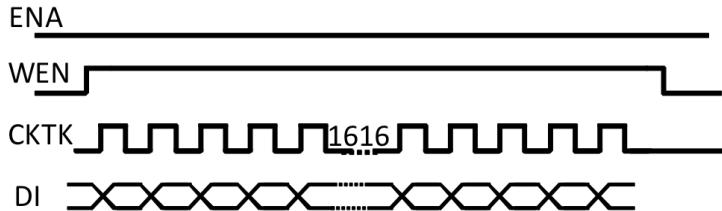


Figure 8: Configuration timing diagram of VMM.

303 The configuration is a single string of 1616-bits of which 80-bits are the global registers and  
 304 1536 are channel registers. Each of the 64 channels has a 24-bit configuration. The list of  
 305 registers is shown in Tables 5,6. The first bit to write is the channel 63 last bit and the last to  
 306 write is the global *spg* register. The sequence is shown in Table 4

Table 4: Sequence of Configuration Registers of the VMM.

Register Type	Sequence
global registers	[spg sdp sbmx sbft sbfp sbfm slg sm5:sm0 scmx sfa sfam st1:0 sfm sg2:0 sng stot sttt ssh stc1:0 sdt9:0 sdp9:0 sc010b:sc110b sc08b:sc18b sc06b:sc26b s8b s6b spdc sdcks sdcka sdck6b sdrv stpp res00 res01 res1 res2 res3 nu nu]
channel register (64×)	[sp sc sl st sm sd0:sd3 smx sz010b:sz410b sz08b:sz38b sz06b:sz26b nu nulast]

Table 3: Input and Output Signals of the VMM. The already known changes in VMM3 are shown in bold.

Name, Position	Connection	In, Out or I/O	Type of Signal or Max/Min	Description
sett A19-20	VMM	I/O	SLVS	Channel 0 force-neighbor signal
setb Y19-20	VMM	I/O	SLVS	Channel 63 force-neighbor signal
ckbc B13-14	ROC	In	SLVS	Bunch crossing clock of 40 MHz
cktp B15-16	ROC	In	SLVS	Test pulse clock
cktk D13-14	ROC	In	SLVS	Token and configuration clock
ckdt E15-16	ROC	Out	SLVS	Data output and 6-bit ADC clock
ckart D19-20	ROC	In	SLVS	ART clock
di B17	SCA/VMM	In	<b>CMOS</b>	Configuration data input
<b>chipSelect</b> B18	SCA	In	<b>CMOS</b>	Chip Select
do B19	VMM	Out	<b>CMOS</b>	Configuration data output
<b>ckspi</b> B20	SCA	In	<b>CMOS</b>	Input SPI clock
t0-t63 E17-W20	TDS	Out	SLVS	Direct digital outputs
mo C9	SCA	Out	0-1 V	Analog output for calibration
tki C13-14	ROC	In	SLVS	Token input (analog mode), L0 (digital mode)
tko C15-16		Out	SLVS	Token output (analog mode)
ena C17-18	SCA	In	SLVS	Acquisition start/stop
wen C19-20	SCA	In	SLVS	Configuration control
art E13-14	ART2GBT	Out	SLVS	Address in Real Time

Table 5: Global Configuration Registers of the VMM.

Global bits (defaults are 0)	Description
spg	input charge polarity ([0] negative, [1] positive)
sdp	disable-at-peak
sbmx	routes analog monitor to PDO output
sbft [0 1], sbfp [0 1], sbfm [0 1]	analog output buffers, [1] enable (TDO, PDO, MO)
slg	leakage current disable ([0] enabled)
sm5-sm0, scmx	monitor multiplexing. <ul style="list-style-type: none"> <li>• Common monitor: scmx, sm5-sm0 [0 000001 to 000100], pulser DAC (after pulser switch), threshold DAC, band-gap reference, temperature sensor)</li> <li>• channel monitor: scmx, sm5-sm0 [1 000000 to 111111], channels 0 to 63</li> </ul>
sfa [0 1], sfam [0 1]	ART enable (sfa [1]) and mode (sfam [0] timing at threshold, [1] timing at peak)
st1,st0 [00 01 10 11]	peaktime (200, 100, 50, 25 ns )
sfm [0 1]	leakage current disable ([0] enabled)
sg2,sg1,sg0 [000:111]	gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)
sng	neighbor (channel and chip) triggering enable
stot [0 1]	timing outputs control 1 <ul style="list-style-type: none"> <li>• stpp,stot[00,01,10,11]: TtP,ToT,PtP,PtT</li> <li>• TtP: threshold-to-peak</li> <li>• ToT: time-over-threshold</li> <li>• PtP: pulse-at-peak (10ns)</li> <li>• PtT: peak-to-threshold</li> </ul>
sttt [0 1]	timing outputs enable
ssh [0 1]	sub-hysteresis discrimination ([1] enable)
stc1,stc0 [00 01 10 11]	TAC slope adjustment (125, 250, 500, 1000 ns )
sdt9-sdt0 [0:0 through 1:1]	coarse threshold DAC
sdp9-sdp0 [0:0 through 1:1]	test pulse DAC
sc010b,sc110b	10-bit ADC conversion time
sc08b,sc18b	8-bit ADC conversion time
sc06b, sc16b, sc26b	6-bit ADC conversion time
s8b	8-bit ADC conversion mode
s6b	6-bit ADC enable (10-bit and 8-bit disable)
spdc	ADCs enable
sdcks	dual clock edge serialized data enable
sdcka	dual clock edge serialized ART enable
sdck6b	dual clock edge serialized 6-bit enable
sdrv	tristates analog outputs with token, used in analog mode
stpp [0 1]	timing outputs control 2

Table 6: Channel Configuration Registers of the VMM.

<b>Channel bits (defaults are 0)</b>	<b>Description</b>
sp [0 1]	input charge polarity ([0] negative, [1] positive)
sc [0 1]	large sensor capacitance mode ([0] $<\sim 30\text{ pF}$ , [1] $\sim 30\text{ pF}$ )
sl [0 1]	leakage current disable [0=enabled]
st [0 1]	1.2 pF test capacitor [1=enabled]
sm [0 1]	mask enable [1=enabled]
sd0-sd3 [0:0 through 1:1]	trim threshold DAC, 1 mV step ([0:0] trim 0 V, [1:1] trim -15 mV )
smx [0 1]	channel monitor mode ( [0] analog output, [1] trimmed threshold))
sz010b, sz110b, sz210b, sz310b, sz410b	10-bit ADC zero
sz08b, sz18b, sz28b, sz38b	8-bit ADC zero
sz06b, sz16b, sz26b	6-bit ADC zero

## 307 10.2 Two-Phase Analog Mode

308 In two-phase (analog) mode, which is the mode originally implemented in VMM1, the ASIC  
 309 operates in two separate phases: acquisition with *ena* high and readout with *ena* low. During  
 310 the acquisition phase the events are processed and stored in the analog memories of the peak  
 311 and time detectors. As soon as a first event is processed, a flag is raised at the digital output  
 312 *data0*. Once the acquisition is complete the ASIC can be switched to the readout phase and the  
 313 readout proceeds injecting a token at the token input *tki*. The first set of amplitude and time  
 314 voltages is made available at the analog outputs *pdo* and *tdo*. Analog buffers can be enabled  
 315 using the bits *sbfp* and *sbft*. The address of the channel is serialized and made available at the  
 316 output *data0* using six data clocks. The next channel is read out by advancing the token with  
 317 the token clock. The token is sparse, passed only among those channels with valid events. If,  
 318 after the token clock occurs, the *data0* goes low, the readout is complete and the token is routed  
 319 to the output *tko* for the readout of the next chip. This allows a daisy-chained readout with a  
 320 single token input. Fig. 9 shows the complete timing diagram of the analog mode operation.

321 This mode will not be used in the NSW, but is being left in subsequent versions as an  
 322 option. It should be noted that the two trigger paths, the 64-channel parallel outputs as well as  
 323 the ART stream are active in this mode as well. The flag of the ART can be used, for example,  
 324 as a fast OR of all 64-channels whereas the prompt parallel outputs can be used to implement  
 325 more sophisticated trigger algorithms. If not needed the parallel SLVS outputs can be disabled  
 326 with significant savings in power consumption and noise immunity from digital activity.

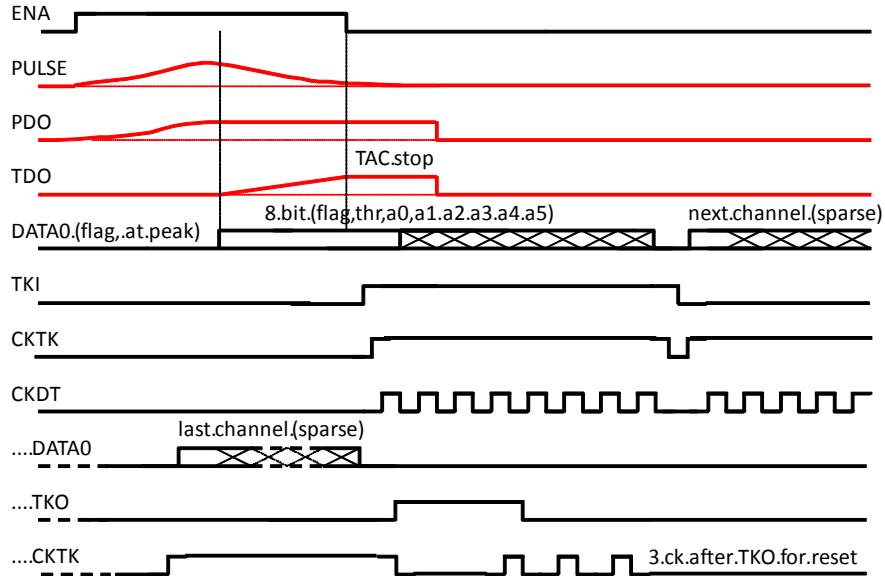


Figure 9: Data Readout with PDO,TDO and external ADC (2-phase mode)

### 327 10.3 Continuous (digital) Mode

328 In direct-output mode the 64 channel digital outputs ttp are activated and provide one of four  
 329 different timing pulses: time-over-threshold (ToT), threshold-to-peak (TtP), peak-to-threshold  
 330 (PtT), or a 10 ns pulse occurring at peak (PtP), and can be set using the global bits stot and  
 331 stpp. The channel self resets at the end of the timing pulse, thus providing continuous and  
 332 independent operation of all 64-channels. Alternatively, if the bits spdc and s6b are both set  
 333 high, the peak detector converts the voltage into a current that is routed to the 6-bit ADC.  
 334 The 6-bit ADC provides a low-resolution A/D conversion of the peak amplitude in a conversion  
 335 time of about 25 ns from the peak time. The conversion time and the baseline (zeroing) are  
 336 adjustable using the global bit set sc6b (the conversion time is the number of data clocks set  
 337 by the sc6b bits) and the channel bit set sz6b respectively. The serialized 6-bit data is made  
 338 available at the channel output immediately after an event flag which occurs at the peak time.  
 339 The flag is lowered at the next clock cycle of the data clock, and the 6-bit ADC data is shifted  
 340 out after that, either at each clock cycle or at each clock edge of the data clock depending on  
 341 the global bit sdck6b. The channel reset occurs after the last bit has been shifted out.

342 In continuous (digital) mode (bit *spdc* high, bit *sttts* low, bit *s6b* low) the peak and time  
 343 detectors convert the voltages into currents that are routed to the 10-bit ADC and 8-bit ADC  
 344 respectively. The 10-bit ADC provides a high resolution A/D conversion of the peak amplitude  
 345 in a conversion time of about 200 ns from the occurrence of the peak. The conversion time  
 346 and baseline (zeroing) are adjustable using the global bit set sc10b (the conversion time is a  
 347 200 ns base plus a 60 ns increment for the MSB and LSB phases, set by the sc10b bits) and  
 348 the channel bit set sz10b respectively. The 8-bit ADC provides the A/D conversion of the peak  
 349 timing (measured using the TAC) from the time of the peak to a stop signal. The TAC stop  
 350 signal occurs at a next clock cycle of a shared 12-bit Gray-code counter which is incremented  
 351 using the external clock signal BC. The counter value at the TAC stop time is latched into a local

352 12-bit memory, thus providing a total of 20-bit deep timestamp with a nanosecond resolution.  
 353 The conversion time and baseline (zeroing) are adjustable using the global bit set *sc8b* (the  
 354 conversion time is a 100 ns base plus a 60 ns increment for the MSB and LSB phases, set by the  
 355 *sc8b* bits) and the channel bit set *sz8b* respectively. The channel is reset once both the 8-bit and  
 356 10-bit conversions are complete and the digital values are latched in digital memories. Thus, in  
 357 continuous (digital) mode a total of 38-bits are generated for each event. The first bit is used  
 358 as a readout flag, the second is the threshold crossing indicator (allows discrimination between  
 359 above-threshold and neighbor events). Next is a 6-bits word for the channel address, followed by  
 360 10-bits associated with the peak amplitude, and 20-bits associated with the timing. The digital  
 361 output bit assignment is summarized also on the table of Figure 1. At this point two modes  
 362 should be distinguished. The non-ATLAS mode described in the following subsection, and the  
 363 ATLAS-specific to be used in NSW which will be described in Section 11.

### 364 10.3.1 Non-ATLAS Continuous Mode

365 The mode, already existing in VMM2, where the 38-bit word is stored in a 4-events deep deran-  
 366 domizing FIFO (there is one such FIFO per channel) and it is read out using a token-passing  
 367 scheme where the token is passed first-come first-serve only among those FIFOs that contain  
 368 valid events. The first token is internally generated as needed (i.e. the *tki* and *tko* IOs are not  
 369 used) and advanced with the token clock. The data in the FIFOs is thus sequentially multi-  
 370 plexed to the two digital outputs *data0* and *data1*. The first output *data0* is also used as a flag,  
 371 indicating that events need to be read out from the chip. The external electronics releases a sync  
 372 signal using the token clock as well (i.e. the token clock provides both advancement and data  
 373 output synchronization), after which the 38-bit data is shifted out in parallel to the *data0* and  
 374 *data1* outputs using either 19 clock cycles or 19 clock edges of the external data clock, depending  
 375 on the global bit *sdcks*. The timing diagram relevant to this mode is shown in Figure 10

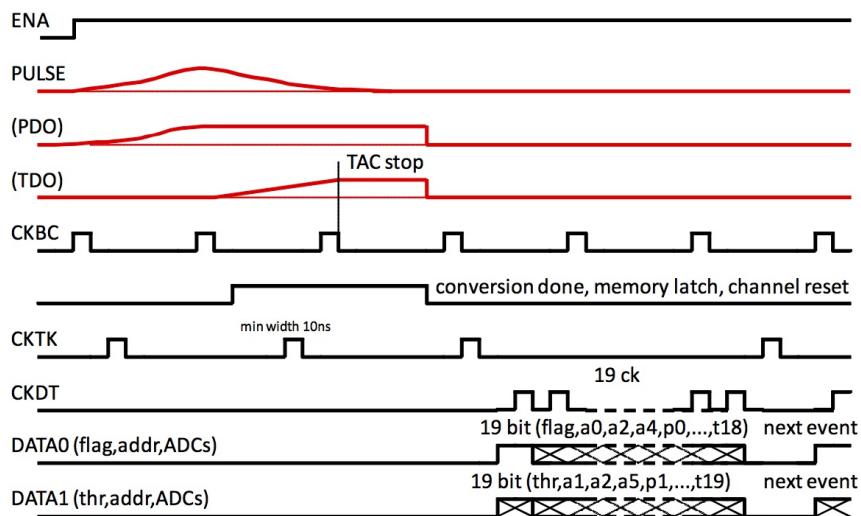


Figure 10: Data Readout with ADCs (continuous mode, 1 bit/ck).

## 376 11 NSW-specific Readout

377 For the NSW the readout requirements are significantly more complex requiring Level-0 in-VMM  
 378 buffering (or the single-level now being considered by the ATLAS TDAQ group) since the VMM  
 379 output bandwidth is not sufficient for the rates expected in some regions of the sTGC detectors.  
 380 The requirements for such a readout have been established by the Readout Working group and  
 381 are included in the "Requirements for the NSW VMM3 readout ASIC and the Readout Controller  
 382 ASIC Design Review Report"

383 [https://edms.cern.ch/file/1470540/1/NSW\\_VMM3\\_ROCReviewFeb2015\\_PDR\\_20150507.pdf](https://edms.cern.ch/file/1470540/1/NSW_VMM3_ROCReviewFeb2015_PDR_20150507.pdf)

384 For completeness these specifications are repeated with notes where modifications are nec-  
 385 essary and/or proposed.

### 386 11.1 Summary of requirements and external constraints

#### 387 General requirements

- 388 1. Level-0 rate: up to 1 MHz (Phase 2)
- 389 2. Level-0 latency: up to 10  $\mu$ s fixed latency (Phase 2)
- 390 3. There is no simple dead time for Level-0; the complex dead time parameters are unknown.
- 391 4. Since several BCs may be read out per Level-0 trigger, a BC may belong to more than one  
   trigger.
- 392 5. Level-1 rate: Phase 1: up to 100 kHz Phase 2: up to 400 kHz
- 393 6. Level-1 latency: Phase 1: 2.5  $\mu$ s fixed latency Phase 2: up to 60  $\mu$ s, variable latency
- 394 7. Configurable E-link speeds: 80, 160 or 320 Mb/s
- 395 8. Configuration registers and state machines must use TMR for SEU protection
- 396 9. The number of bunch crossings read out for a trigger must be configurable from 1 to 8.
- 397 10. A mechanism to completely identify the detector source of the data, independent of cable  
   connections, must be provided.
- 398 11. The VMM and ROC will be configured via an SCA ASIC.
- 399 12. The ROC should generate test pulse trigger for the VMM in response to a TTC test pulse  
   bit.
- 400 13. In response to the test pulse input, the VMM should generate the test pulse on the next  
   BC clock.
- 401 14. Radiation tolerance. See: "New Small Wheel Radiation and Magnetic Field Environ-  
   ment" [5].
- 402 15. The VMM and ROC must provide an SEU flag or counter to be read, reset, by the SCA.
- 403 16. Resets: full reset (via pin and on power up); reset all but configuration registers (See  
   Section - NOT KNOWN TO THIS DOC.)
- 404 17. The ITAR fuse from CERN must be placed in both the VMM and the ROC in order to  
   be free of export restrictions.

#### 412 VMM specific requirements

- 413 1. Max VMM output BW: 800 Mb/s (640 Mb/s, net with 8b/10b encoding)
- 414 2. The VMM configuration/monitor path must be operable independently of the acquisition  
   state.
- 415 3. The VMM3 must provide a buffer overflow counter (per channel or per VMM?) to be read  
   by the SCA.
- 416 4. Each VMM must have a dedicated (i.e. not shared) configuration connection to the SCA.

- 419    5. Each VMM must have a dedicated test pulse trigger pin and a test pulse enable configura-  
 420    tion bit.  
 421    6. The hit output to the Read out Controller must be 8b/10b encoded. There must be at  
 422    least one comma character sent between Level-0 events and they must be sent continuously  
 423    when events are not sent.

424    **Notes:**

- 425    **Item 2.** The VMM configuration/monitoring path, though independent of the acquisition path  
 426    can not be operable while data taking. A configuration operation when VMM is sensitive (i.e.  
 427    is acquiring) would be extremely disruptive, and measurements would be certainly corrupted,  
 428    with settling times typical of the stabilizers in the analog circuits. Considerable changes would  
 429    be needed to attempt protection of the sensitive circuits and alleviate these effects.  
 430    **Item 3.** The buffer overflow is handled by the digital interface (see section on exception mes-  
 431    sages).  
 432    **Item 5.** The VMM3 does include a dedicated test pulse pin. It should be clarified that the test  
 433    pulse should be aligned with the Bunch Crossing clock.

434    **ROC specific requirements**

- 435    1. TTC information is provided to the ROC via GBT from FELIX  
 436    2. The ROC must provide BCR and BC clock to other on-board ASICs, and, in addition,  
 437       Level-0 Accept, ART clock (160 MHz), and RO (160 MHz) clock to each VMM.  
 438    3. The ROC will receive a 40 MHz BC clock, but needs a PLL to generate clocks for the 80,  
 439       160, 320 Mb/s E-links.  
 440    4. The data sent on the E-links must be 8b/10b encoded with Start-of-Packet and End-of-  
 441       Packet symbols framing the data for one trigger.  
 442    5. Depending on a configuration bit, the ROC will send either the Level-0 Accept or the  
 443       Level-1 Accept signal out as the “Level-0” signal.  
 444    6. The ROC E-links must adhere to SLVS or LVDS standards  
 445    7. When its buffers are nearing full, the ROC must be able to generate the BUSY-ON symbol  
 446       in the Level-1 data flow to FELIX so that FELIX can generate RODBUSY to the Central  
 447       Trigger. BUSY-OFF, with hysteresis, must be generated when the buffers return to a safe  
 448       occupancy.

449    **11.2 VMM**

450    The overall block diagram for the part of the readout in the VMM is shown in Figure 11. It  
 451    consists of FIFOs and logic blocks described below.

452    The existing VMM2 has a 4-deep FIFO per channel, implemented in custom layout. This will  
 453    remain for non-ATLAS users wishing to operate in the existing VMM2 mode. The data (format  
 454    shown in Figure 12) in these FIFOs is a sequence of hits that are transferred to a corresponding  
 455    deep FIFO, implemented with the digital library, for the ATLAS-mode. Note that the 4-deep  
 456    FIFO is filled asynchronously whenever the VMM peak detector finds a peak in its input signal.  
 457    The channel has a minimum 200 ns dead time after a peak is found. Each channel will transfer  
 458    between its FIFOs autonomously.

459    The maximum hit rate per channel is 5 MHz. With a 64-deep “latency” FIFO all hits for a  
 460    period of 12.8  $\mu$ s can be buffered, provided that the hits are read out at a rate of least 5 MHz.

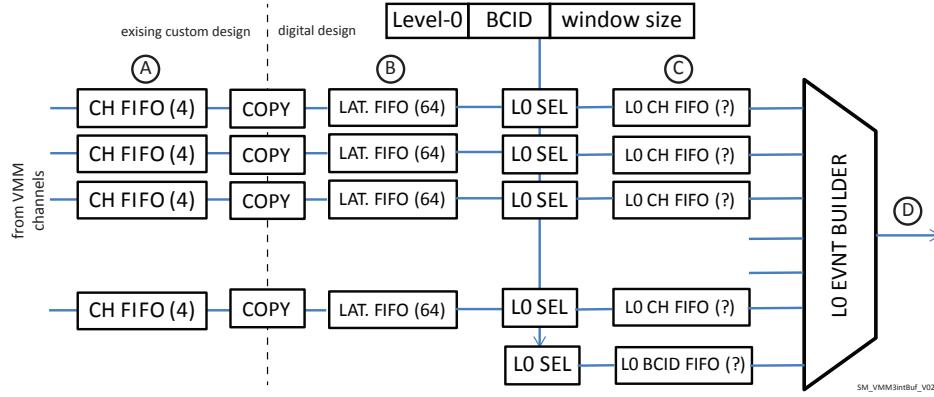


Figure 11: VMM3 internal buffers for Level-0 event output. The formats of the data at points A, B, C and D are shown in the figures following.

hit data	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
	F	N	Chan# (6)						ADC (10)										TDC (8)								BCID (12)											

LL\_format\_fromVMM2\_v01

Figure 12: Data format from the VMM custom logic (Point A in Figure 11) “N” indicates that the hit is because the neighboring channel was above threshold. “F”, flag, is always 1.

- 461 Since Level-0 Accepts can occur for consecutive bunch crossings, the read rate must be 40 MHz.  
 462 Therefore overflow of the latency FIFOs cannot occur for Level-0 latencies smaller than 12.8  $\mu$ s,  
 463 unless the readout of the FIFOs stops (see below). The data format (“B”) in the latency FIFO  
 464 is shown in Figure 13. Since there is one FIFO for every channel, the channel number need not  
 465 be stored.

chan FIFO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	P	N	ADC (10)						TDC (8)								BCID (12)															

LL\_format\_LatFIFO\_V01

Figure 13: Format of the data in the Level-0 latency FIFO (Point B in Figure 11) “P” is a parity bit.

### 466 11.2.1 Level-0 data selector

- 467 Each channel has a Level-0 Selector circuit which is connected to the output of the channel’s  
 468 latency FIFO. The selector finds events within the BCID window (maximum size of 8 BCs) of a  
 469 Level-0 Accept and copies them to the L0 Ch FIFO. The latency FIFO operates as a first-word-  
 470 fall-through FIFO so that the FIFO output can be examined before it is discarded or copied.  
 471 Since the maximum window size, 8 BCs, i.e. 200 ns, is less than the minimum dead time of a  
 472 VMM channel, 200 ns, there can be at most one hit per channel in a trigger time window.  
 473 The selector compares the BCID field of the hit data in the FIFO (when the FIFO is not  
 474 empty) with the content of a global BCID counter. This counter is offset by the Level-0 latency  
 475 (less the number of BCs in the readout window before the triggering BCID) from the BCID

476 counter used to tag hits when their peak is detected. In this way it indicates the BCID at the  
 477 time of tagging, even though it is being examined after the Level-0 latency.

- 478 • On every BC clock, if the hit data becomes older than the Level-0 window, the data is  
 479 flushed from the latency FIFO.
- 480 • If a Level-0 Accept is received for the given BCID and the BCID field of the hit data is  
 481 inside the Level-0 window the hit data is copied to the following Level-0 FIFO.
- 482 • If a channel's L0 Sel circuit does not find a hit with a BCId falling within the window, a  
 483 ‘no data’ item (first bit equal 0) is passed to the L0 Ch FIFO for that BCID.
- 484 • Therefore all L0 Ch FIFOs receive for each Level-0 Accept either a single ‘hit data’ or a  
 485 ‘no data’ item and therefore all will simultaneously overflow when they are full (provided  
 486 that the FIFOs are also read simultaneously). The L0 Ch FIFOs are effectively a single  
 487 wide FIFO.
- 488 • Note that a hit may be copied more than once if more than one Level-0 Accept occurs  
 489 within a BCID window.

490 The 24-bit item for a valid hit and for “no data” (format “C”) is shown in Figure 14. For  
 491 valid hit data the L0 Sel circuit also calculates a 3-bit relative BCId with respect to the BCId.  
 492 The value of this relative BCId is 3 if the BCId in the data found in the latency FIFO and  
 493 the BCId associated with the Level-0 Accept are equal. The parity bit is the parity bit read  
 494 from the latency FIFO, checked and recalculated for Format “C”. If the parity check failed, the  
 495 recalculated parity bit is inverted to force detection of a parity error by the downstream logic.  
 496 A parity error counter is also incremented.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
hit data	1	P																						N rel BCID
no data	0	P	0																					undefined
msg	0	P	1	R																				msg TBD (20)
BCID FIFO	V	P	V'	orb																				LL_format_L0FIFO_V02

Figure 14: Format of the data in the Level-0 select output derandomizer FIFO (Point C in Figure 11)

497 For each Level-0 Accept, the BCID and a 2-bit orbit count associated with the Level-0  
 498 Accept are entered into a 16-bits wide FIFO, the L0 BCID FIFO (see Figure 11) together with  
 499 a parity bit, P, and two overflow condition bits, V, V' (see Figure 14). If writing the items for  
 500 the current Level-0 Accept caused the L0 Ch FIFOs to become full, the Overflow bit, V, in the  
 501 BCID item is set and further writing to the L0 Ch FIFOs is suspended until their level falls  
 502 below a lower level. Note that the BCID FIFO is deeper than the L0 Ch FIFOs so writing to  
 503 the BCID FIFO on every Level-0 Accept continues, but with the overflow bit set to indicate  
 504 that there are no corresponding items in the L0 Ch FIFOs. If writing the BCID FIFO would  
 505 cause an overflow, the second Overflow status bit (V') is set and subsequent writing to the BCID  
 506 FIFO is suspended for the next ‘Nskip’ Level-0 Accepts. This is at least ‘Nskip’  $\mu$ s and allows  
 507 time for several events to be transferred out of the BCID and L0 Chan FIFOs.

508 **Automatic suspension of noisy channels** can be based on the result of counting hits  
 509 during a certain time interval or for a number of consecutive Level-0 Accepts. This requires the  
 510 implementation of counters that are incremented for hits and are decremented in absence of hits

511 during a certain time interval or for a number of Level-0 Accepts. A more straightforward option  
 512 would be to monitor the filling degree of the latency FIFOs and to shut off a channel once its  
 513 latency buffer is filled to a configurable level. A natural place for monitoring the filling degree  
 514 would be the copy stage. Once the latency FIFO is filled to the maximum level, data should  
 515 still be copied to the FIFO, but seen as invalid data by the L0 Sel and be discarded once the  
 516 BCId is earlier than the earliest BCId of the search window. To make this possible an additional  
 517 bit is needed for each item entered in the L0 Ch FIFO indicating that the channel is inactive  
 518 or active (so the FIFO would need to be 33-bits wide). The channel could become active again  
 519 once the filling degree of the latency FIFO falls below a second level. By an appropriate choice  
 520 of the levels the probability of an overflow condition of the L0 Ch FIFOs can be made small.

521 A data format is also defined for message data. It could be used to pass a message to the  
 522 L0 Ch FIFO indicating the shutting off of a channel instead of transferring the “invalid data  
 523 format”.

### 524 11.2.2 Level-0 event building

525 For each Level-0 Accept, the outputs of the BCId FIFO and of the L0 Ch FIFOs are read in  
 526 round-robin manner, starting with the BCId FIFO. Only valid data is forwarded to the event  
 527 builder stage. To achieve synchronous overflow of all L0 Ch FIFOs the data of these FIFOs is  
 528 transferred synchronously into registers which are then read in sequence by the Event Builder.

529 The format of the Level-0 Event Builder output, the data sent to the Read out Controller,  
 530 is shown in Figure 15. The header is always sent, even when there are no following hits. The  
 531 truncation bit, “T”, indicates that the number of hits exceeded the (configurable) maximum for  
 532 a VMM and that further hits for this Level-0 trigger have been discarded. It is set in the last  
 533 hit that is transferred.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
header	O	P	orb		BCID (12)																											
hit data	1	P	O	T	Chan# (6)						ADC (10)										TDC (8)								N	rel BCID		
msg	1	P	1	R	R	msg ID				msg TBD (23)																						

LL\_format\_VMM3out\_V03

Figure 15: Format of the data sent to the ROC ASIC (Point D in Figure 11) Zero or more hits may follow the header.

534 Once the overflow bit, “V”, in the BCID word is active, only the header is output; the  
 535 BCId read from the BCId FIFO is the first BCId for which the overflow occurred. To make  
 536 this possible the depth of the BCId FIFO has to be at least one word larger than that of the  
 537 L0 Ch FIFOs. For outputting 64 32-bit words output via a link with an effective bandwidth  
 538 of 512 Mb/s, 4  $\mu$ s is needed, i.e. 160 bunch crossings. In this time, for Phase 2, on average  
 539 four Level-0 Accepts would occur, but in theory up to 160 could occur. Complex dead time  
 540 would reduce this, but the complex dead time parameters for Phase 2 are not known. However,  
 541 since the complex dead time parameters are not known, possible BCID FIFO overflows must be  
 542 handled. If a BCID word written into the FIFO would cause the BCID FIFO to be full, it is  
 543 written with the overflow bit, V’, set (Figure 14). The Level-0 Event Builder sends a message  
 544 word indicating this overflow. The ROC then knows not to expect data from this VMM for the  
 545 next ‘Nskip’ Level-0 Accepts.

546 Event building in one stage at an average Level-0 Accept rate of 1 MHz requires that a  
547 complete round-robin cycle on average should be completed in  $1\ \mu\text{s}$ , i.e. in 15 ns per step. Event  
548 building in two stages would allow reducing this to 30 ns, i.e. a 40 MHz clock can be used.

549 In order to optimize the depths of all FIFOs a simulation is required. For this, a model  
550 for the input rates of the VMM is needed. Small clusters of strips or wires are typically hit,  
551 but larger clusters may be hit in case of e.g.  $\delta$ -ray or neutron production. Initially a Poisson  
552 distribution for the time distribution of Level-0 Accepts can be used, but for a more detailed  
553 simulation the complex dead time and the LHC bunch structure needs to be taken into account.  
554 A simulation of the logic is being developed by the Brasov group.

555 **11.2.3 Transfer from VMM to Readout Controller**

556 The data transfer from VMM to Readout Controller is via two serial lines (even bits on one, odd  
557 bits on the other) running at 160 MHz with Double Data Rate (DDR) giving a total bandwidth  
558 of 640 Mb/s. Two lines are used to reduce the clock rate. The Readout Controller supplies the  
559 clock for this transfer. 8b/10b encoding is used with one or more comma characters transmitted  
560 continuously between Level-0 events. The 8b/10b encoding reduces the effective bandwidth to  
561 512 Mb/s. Figure (NOT KNOWN TO THIS DOC) in Section (NOT KNOWN TO THIS DOC)  
562 shows the Level-0 VMM output bandwidths needed by the various VMMs, assuming 40 bits  
563 per hit. The 512 Mb/s VMM output capacity is clearly sufficient. (The readout clock input of  
564 the VMM can be up to 200 MHz, but this would require modifying the CERN ePLL to produce  
565 200 MHz output.)

566 **11.2.4 VMM clock domains**

567 40 MHz (BC clock): Front-end, Latency FIFOs, Level-0 Selection, Level-0 FIFOs (in port)  
568 160 MHz (VMM Readout clock): Level-0 FIFOs (out port), Event Builder

569 **11.3 Trigger Paths**

570 The VMM, in addition to the information recorded at Level-1 (or Level-0), provides trigger  
571 primitives for both Micromegas and sTGC detectors. In each case an independent trigger data  
572 path provides information to the trigger processor at the bunch crossing frequency. In the next  
573 two subsections a short description, the requirements, and implementation of the two data paths  
574 will be discussed.

575 **11.3.1 Micromegas Trigger Primitive**

576 The Micromegas Detector in the NSW has a total of  $\sim 2$  million channels that would make it  
577 impossible to have a trigger system using information from these channels in parallel and in  
578 real time. The Micromegas trigger concept takes advantage of the fine pitch (0.5 mm) of the  
579 detectors in the following way. Each VMM provides, at a single dedicated digital output art,  
580 the address of the first on-chip above-threshold event, called address in real time (ART). The  
581 system, thus, is equivalent to a trigger system with segmentation of 3.2 cm( $64 \times 0.5$  mm) with  
582 spatial resolution of order 300  $\mu\text{m}$  sufficient for the angular resolution required in order to reject  
583 candidates that are not consistent with those originating at the interaction point. This way the  
584 trigger channel count is reduced to  $\sim 32,000$  channels.

585      The ART mode is enabled with the bit *sfa*. Either at the pulse threshold crossing (bit *sfram*  
 586      low) or at the pulse peak (bit *sfram* high) a flag is released at the art output. The flag is followed  
 587      by the serialized address of the event. Also in this case the address is released either at each  
 588      clock cycle or at each clock edge of the external ART clock, depending on the global bit *sdcka*.

589    **ART Requirements/Properties**

- 590      • Arbitration logic blocks other than the first hit occurring 2 or more ns later
- 591      • The ART stream clock frequency is 160 MHz and is provided in each VMM of a front end  
 592      board by a dedicated SLVS line from the ROC serving the front end board.
- 593      • It can be optionally clocked at both edges of the clock for an effective rate of 320 MHz .
- 594      • The ART must be aligned to the ART clock.
- 595      • It can optionally be provided at threshold crossing or at peak found. In the NSW imple-  
 596      mentation we choose the former. It reduces the latency by about the peaking time and at  
 597      the same time allows the use of longer integration time which results in lower electronic  
 598      noise and higher charge collection. Furthermore, for the trigger path, amplitude slue is  
 599      not an issue.
- 600      • While the direct outputs are active simultaneously with all modes of operation they are  
 601      not needed in Micromegas. It must be possible to turn off the SLVS drivers in order to  
 602      reduce power consumption and the possibility of digital interference with the front end  
 603      operation.

604    The ART latency is the sum of several delays

- 605      1. Time from instantaneous charge event to 1% of the peak is  $\sim 10$  ns
- 606      2. Time from pulse peak to peak found  $\sim 5$  ns
- 607      3. Digital latency from comparator firing to leading edge of ART is  $\sim 5$  ns
- 608      4. Digital latency from peak found to leading edge of ART is  $\sim 5$  ns

609    Or  $\sim 15$  ns for the threshold crossing option or  $\sim 20$  ns + peaking time if the peak detect is  
 610    chosen. The above assumes a typical case of input capacitance of 200 pF and a load of 20 pF at  
 611    the digital output.

612    **11.3.2 sTGC Trigger Primitives**

613    The sTGC detector trigger concept uses projective, overlapping cathode pads to define a candi-  
 614    date track segment by a 3 out of four coincidence in both quadruplets in a sector. The projective  
 615    tower defines then bands of strips to be read out and sent to the sTGCtrigger logic IThe pad sig-  
 616    nals operate in the direct-output mode in which the 64 channel digital outputs ttp are activated  
 617    and provide one of four different timing pulses:

- 618      • Time-over-threshold (ToT)

- Threshold-to-peak (TtP)
- Peak-to-threshold (PtT)
- A 10ns pulse occurring at peak (PtP)

The mode can be set using the global bits *stot* and *stpp*. The channel self resets at the end of the timing pulse, thus providing continuous and independent operation of all 64 channels. Alternatively, if the bits *spdc* and *s6b* are both set high, the peak detector converts the voltage into a current that is routed to the 6-bit ADC. The 6-bit ADC provides a low-resolution A/D conversion of the peak amplitude in a conversion time of about 25 ns from the peak time. The conversion time and the baseline (zeroing) are adjustable using the global bit set *sc6b* (the conversion time is the number of data clocks set by the *sc6b* bits) and the channel bit set *sz6b* respectively. The serialized 6-bit data is made available at the channel output immediately after an event flag which occurs at the peak time. The flag is lowered at the next clock cycle of the data clock, and the 6-bit ADC data is shifted out after that, either at each clock cycle or at each clock edge of the data clock depending on the global bit *sdck6b*. The channel reset occurs after the last bit has been shifted out.

Because of the large area of some pads and the high rate dead time per channel with an effect in efficiency is of concern for the sTGC trigger system and therefore choice of the direct output format is important. We summarize here the requirements of the digital part (see section 4 for the analog requirements):

### sTGC digital trigger requirements/properties

- While the direct outputs are active simultaneously with all modes of operation they are not needed in readout of the sTGC strips and wires. It must be possible to turn off the SLVS drivers in order to reduce power consumption and the possibility of digital interference with the front end operation.
- The 6-bit stream clock frequency is 160 MHz and is provided in each VMM of a front end board by a dedicated SLVS line from the ROC serving the front end board.
- It can be optionally clocked at both edges of the clock for an effective rate of 320 MHz .

The direct mode latency can be calculated from the following:

1. Time from instantaneous charge event to 1% of the peak is  $\approx 10\text{ns}$
2. Timex from pulse peak to peak found  $\sim 5\text{ ns}$
3. Digital latency from threshold- comparator to leading edge of ToT is  $\sim 4\text{ ns}$
4. Digital latency from peak found to leading edge of 6-bit ADC is  $\sim 4\text{ ns}$

Therefore for ToT the total latency is 14 ns for ToT or 18 ns + peaking time for the 6-bit ADC option. The dead time because of the 10-bit ADC latency is  $\sim 200\text{ ns}$  after the peak. However it is possible to interrupt the 6-bit ADC conversion when the signal drops below threshold (the earliest the channel can be reset) thus providing a lower resolution peak value with the minimum dead time.

## 656 12 Radiation Tolerance and SEU

657 The VMM ASIC is expected to be exposed at a total ionization 100 krad according to the  
 658 simulations done [6]. Deep sub-micron technologies are known to be immune to much higher TID  
 659 doses because of increasingly thinner oxide layers which can trap increasingly smaller amounts of  
 660 charge. Although not expected to be a problem, VMM3 will be tested for TID tolerance in the  
 661  $^{60}\text{Co}$  source irradiation facility at BNL. However single event upsets (SEU) become increasingly  
 662 more serious as the technology feature size decreases because of the smaller capacitance in the  
 663 storage elements that need smaller energy depositions in order to flip their state. In the VMM  
 664 there are two types of storage elements that require SEU protection, the configuration register,  
 665 and the state machine control logic. In the data domain perhaps the 12-bit BCID register (under  
 666 discussion) whereas the FIFOs need not be protected as an occasional data corruption is not an  
 667 issue. To mitigate the SEU effects in the VMM storage elements two different techniques are  
 668 used:

- 669 1. Dual Interlocked Cells (DICE) for the protection of the configuration register, and
- 670 2. The more common Triple Modular Redundancy (TMR) for the state machines and possibly  
 671 the BCID register

672 The DICE uses redundancy to significantly reduce susceptibility to an upset. D flip flops based on  
 673 the dual interlocked cell latches have redundant storage nodes and restore the cell original state  
 674 when an SEU error is introduced in a single node [7]. The scheme fails if multiple nodes are upset  
 675 but this is far less likely, especially at the rather modest neutron levels of  $\sim 10^{12} n/\text{cm}^2/\text{year}$   
 676 at luminosity  $7 \times 10^{34} \text{s}^{-1} \text{cm}^{-2}$ . The TMR technique is used to protect the small number (less  
 677 than 20) storage elements of the state machines. At the measured upset cross sections of order  
 678  $10^{-14} \text{cm}^2$  the upset probability is of order one tenth of an upset per VMM per year.

679 The first version of the VMM was tested in the NSCR Demokritos Tandem accelerator. The  
 680 VMM1 was irradiated in the area of the configuration registers for  $\sim 44 \text{ h}$   $n$  of energy range  
 681  $\sim 18\text{-}22 \text{ MeV}$  achieving an integrated  $n$  flux of  $3.1 \times 10^{11} \text{ncm}^{-2}$ . The measured cross-section  
 682 found to be  $(4.1 \pm 0.7) \times 10^{-14} \text{cm}^2/\text{bit}$ . This shows a probability of  $\sim 3 \times 10^{-8} \text{SEU/s}$  for the  
 683 NSW expected  $n$  flux.

## 684 13 Testing, Validation and Commissioning

685 The production testing of the VMM will be done along with the functional testing of the ASIC.  
 686 The testing will be based in the noise, alive channels and functionality that will be defined  
 687 as crucial for the ASIC validation before mounted to the boards. An automated test pattern  
 688 generator can be used to test the packaged chips on the bench-top with a dedicated test PCB.  
 689 The chips will be categorized based on the criteria to “Good”, “Good as Spare” and “Rejected”.

## 690 14 Reliability Matters

### 691 14.1 Consequences of Failures

692 The consequences of VMM failures are easily deduced from the system architecture and overall  
 693 NSW design. In increasing severity they are:

- 694 • Occasional inoperative individual channels due to a variety of reasons have little impact  
695 on the quality of data. An isolated channel will result in reduced (local) spatial resolution  
696 in both the Micromegas and sTGC detectors, while two or more adjacent channel failures  
697 will have a (local) effect in efficiency as well
- 698 • Failure of a VMM will result in the loss of information from all 64 channels. In the case of  
699 the Micromegas detectors this would result in a dead segment 3.5 cm in radius of a single  
700 plane of a given sector. In the case of sTGC, because of the larger pitch, it would result  
701 in a significantly larger loss depending on the type of readout affected (strips, pads, wires,  
702 as well as the location in a sector).

703 **14.2 Prior Knowledge of Expected Reliability**

704 No such knowledge exists at this point. .

705 **14.3 Measures Proposed to Insure Reliability of Component and/or System**

706 The assembled front end cards will undergo burn-in following guidelines described in the IBM  
707 8RF Design Manual, with perhaps modifications to be determined.

708 **14.4 Quality Control to Validate Reliability Specifications during Production**

709 The production devices will be tested in an automated station to be designed and fabricated by  
710 the Tomsk group in collaboration with BNL. The goal will be to identify fully operational units,  
711 failed ones to be discarded and functional ones with issues that might be useable if necessary.  
712 The exact test protocol and parameters that will determine usability will be determined as we  
713 gain more experience with the VMM2 and VMM3 prototypes.

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