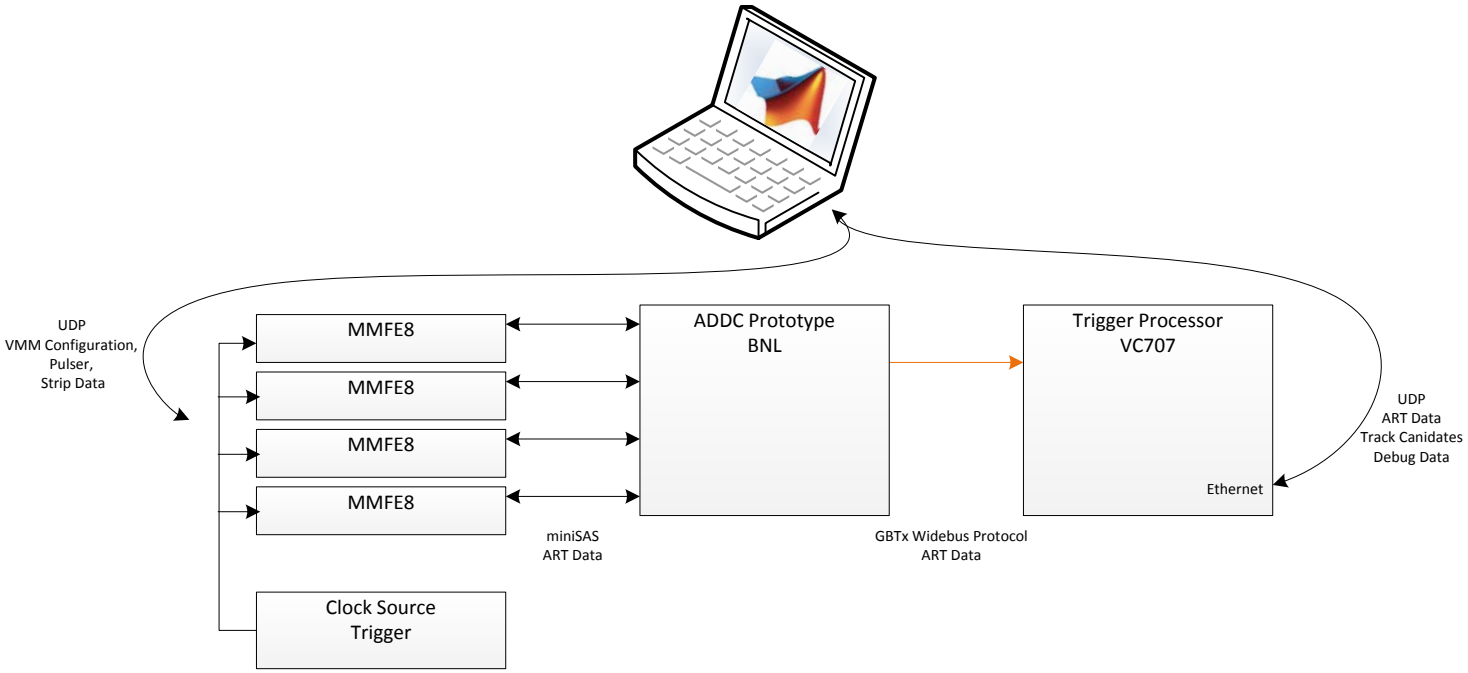
MM Trigger Processor Update

ART Data Path Testing



Current Activities

- Preparation for vertical slice integration
- Algorithm implementation and modifications for timing closure
- Interface to the ancillary functions
- VHDL simulations and code optimizations (Alex)