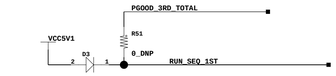
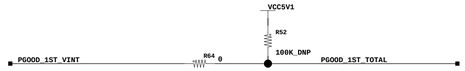
ADDC Schematic INDEX

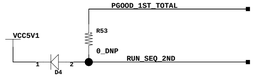
CHECKED, 3/3/2013

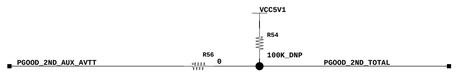
First Stage — VCCINT(1V), MGTAVCC(1V)



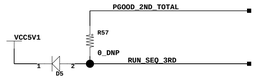


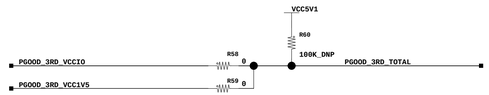
Second Stage — VCCMGTAVTT(1V2), VCCAUX(1V8)



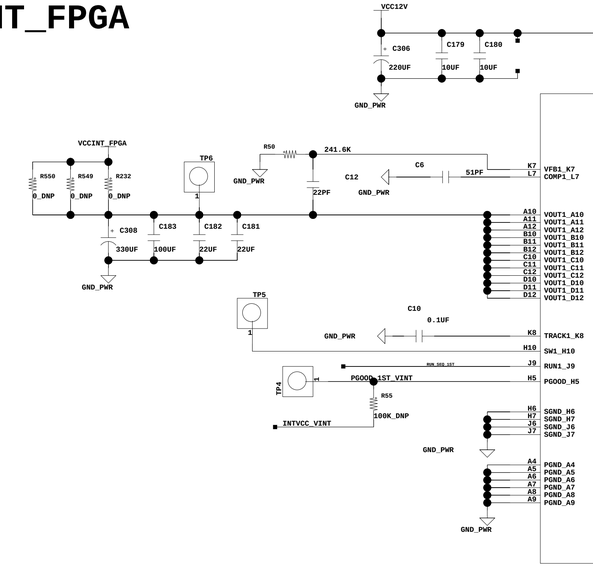


Third Stage — VCCIO(3V3,2V5,1V5), VCCA(1V5)

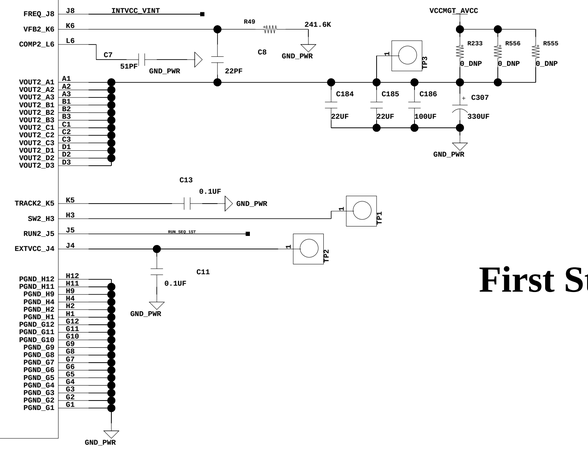




VCCINT_FPGA 1.0V

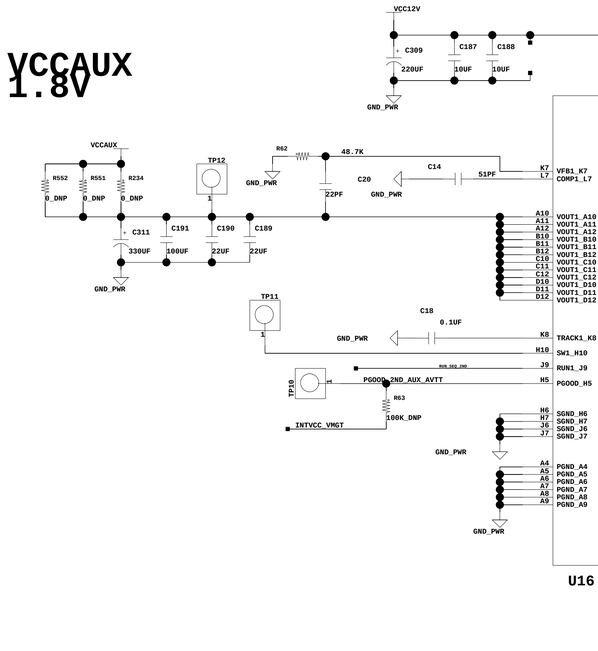


VCCMGT_AVCC 1.0V

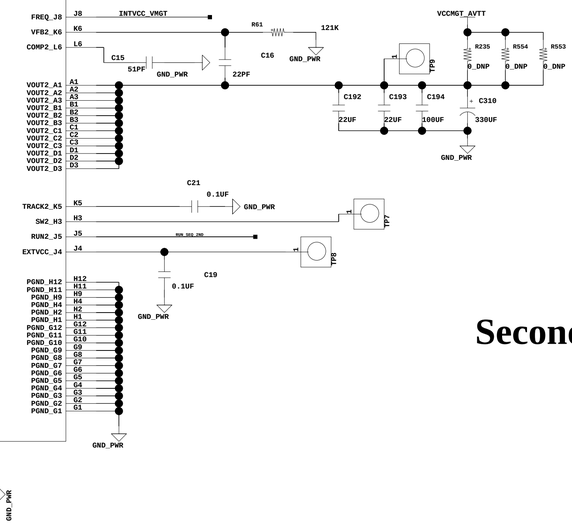


First Stage

VCCAUX 1.8V



VCCMGT_AVTT 1.2V



Second Stage

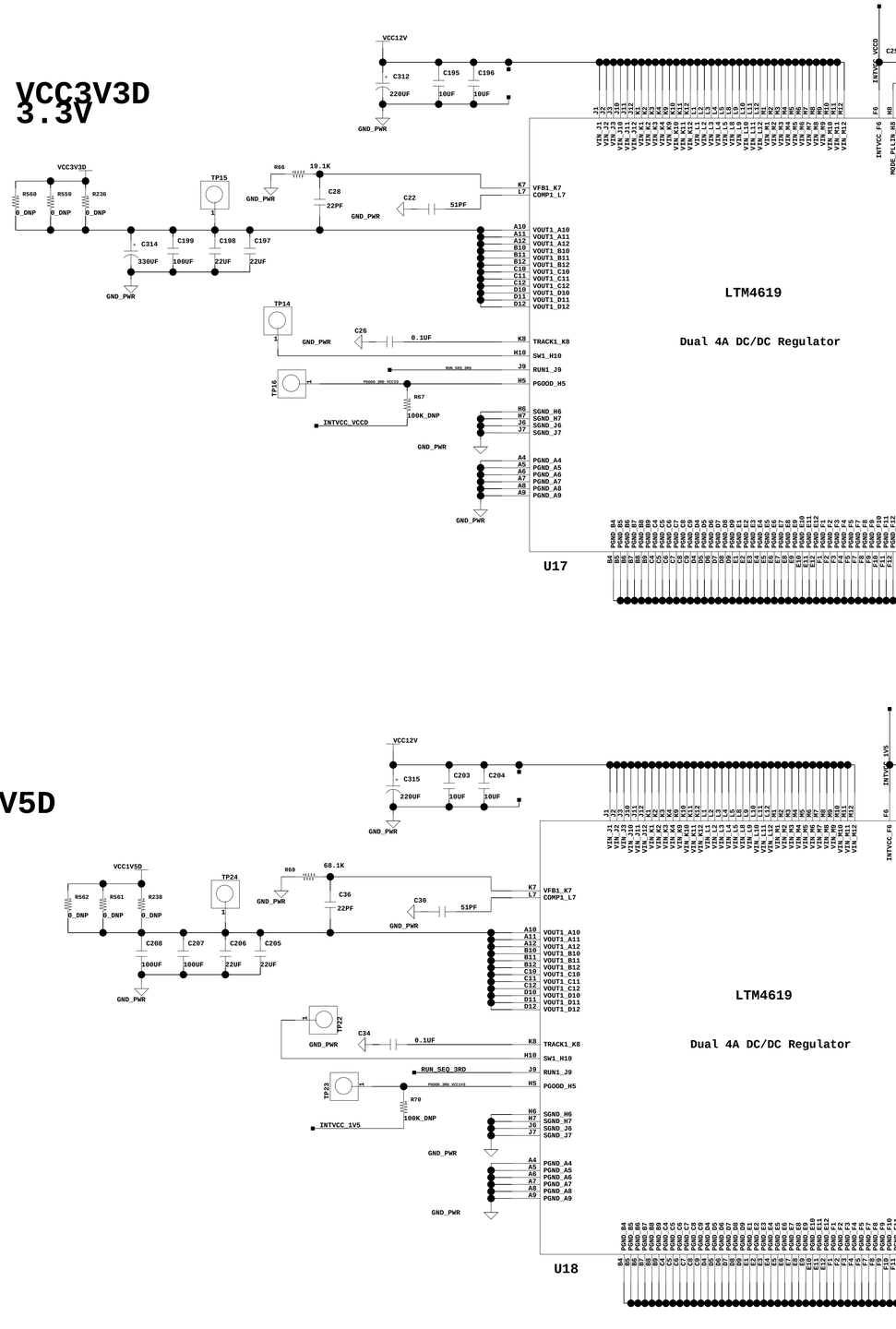
COMPANY	
TITLE	
SIZE D REV	SHEET PWR1 OF N
DRAWN	DATE

NOTE

Third Stage

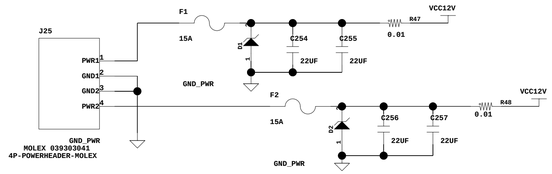
CHECKED, 3/3/2013

VCC3V3D
3.3V

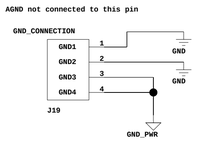


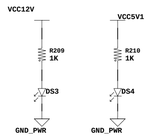
NOTE

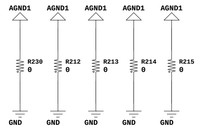
COMPANY	
TITLE	
SIZE D REV	SHEET PWR2 OF N
DRAWN	DATE

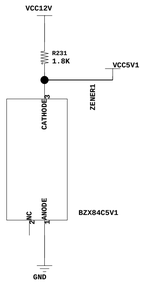


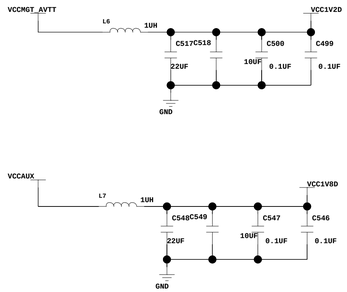
This power connector mate with MOLEX 39014040









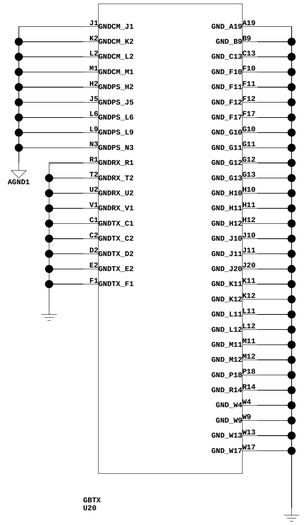


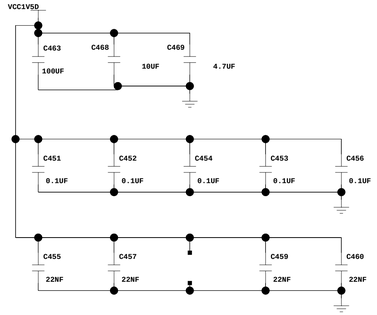
NOTE

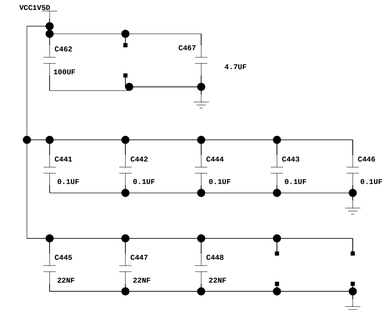
COMPANY	
TITLE	
SIZE D REV	SHEET PWR-COMN N
DRAWN	DATE

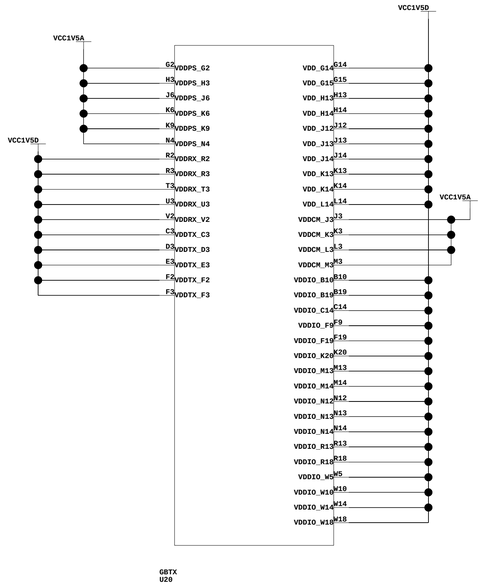
CHECK voltage and filter once again

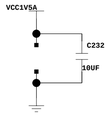
3/3/2013

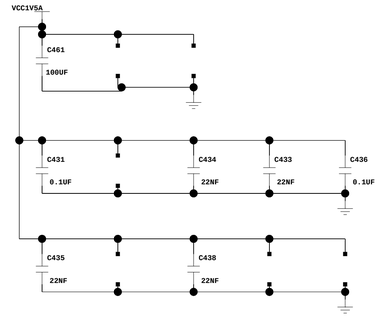








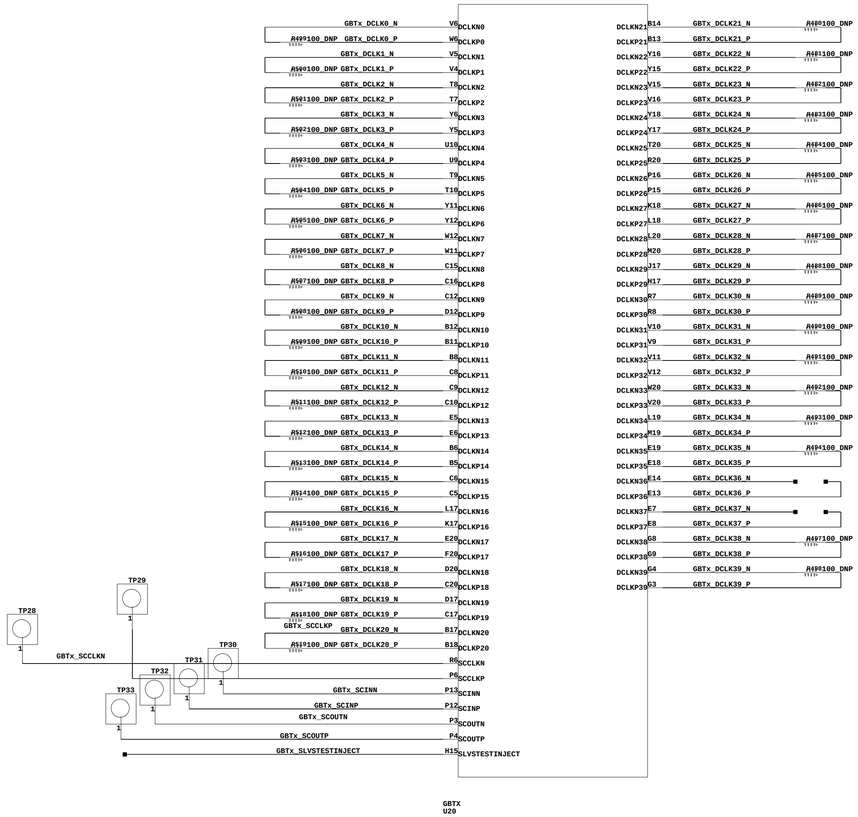


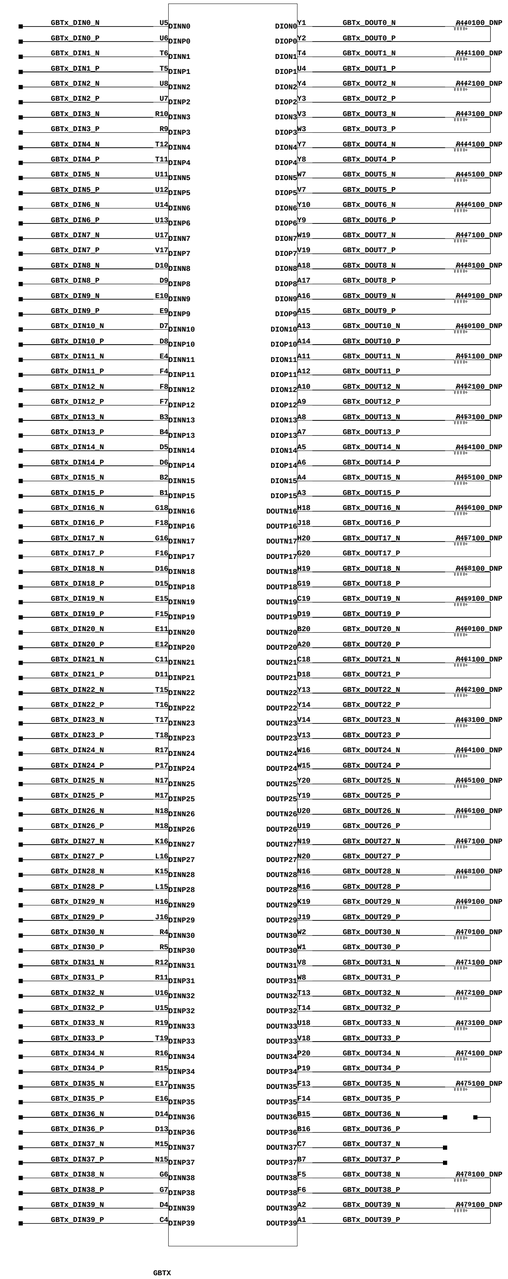


NOTE

COMPANY	
TITLE	GBTx_PWR_GND
SIZE D REV	SHEET OF N
DRAWN	DATE

CHECKED, 3/3/2013

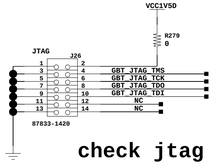




SC test connections check again

NOTE

COMPANY	
TITLE	
SIZE D REV	SHEET GBTx_06 N
DRAWN	DATE

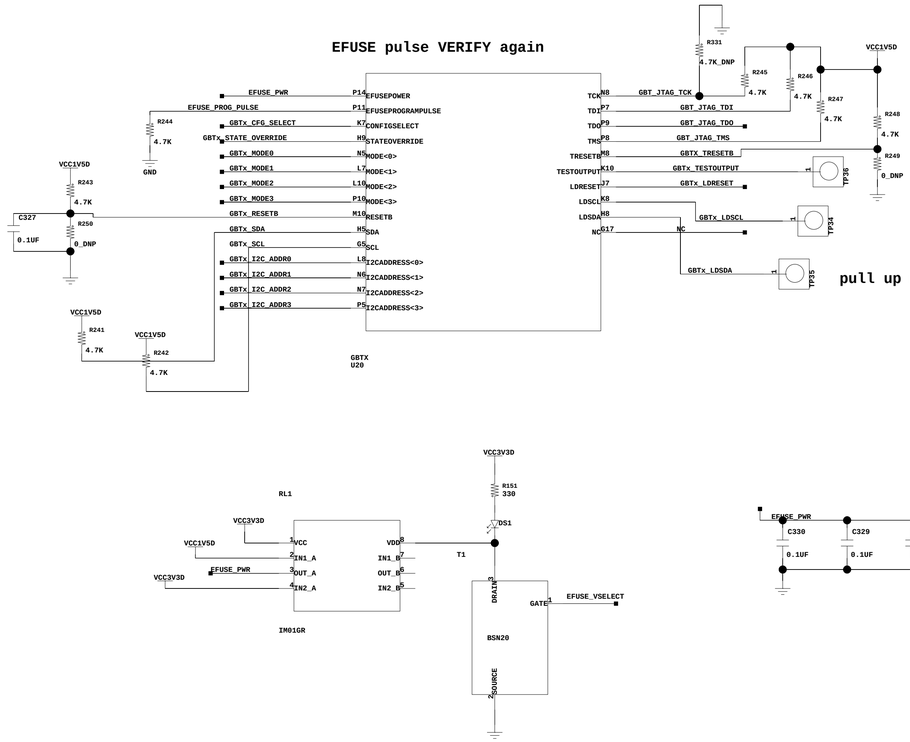


check jtag voltage for GBT

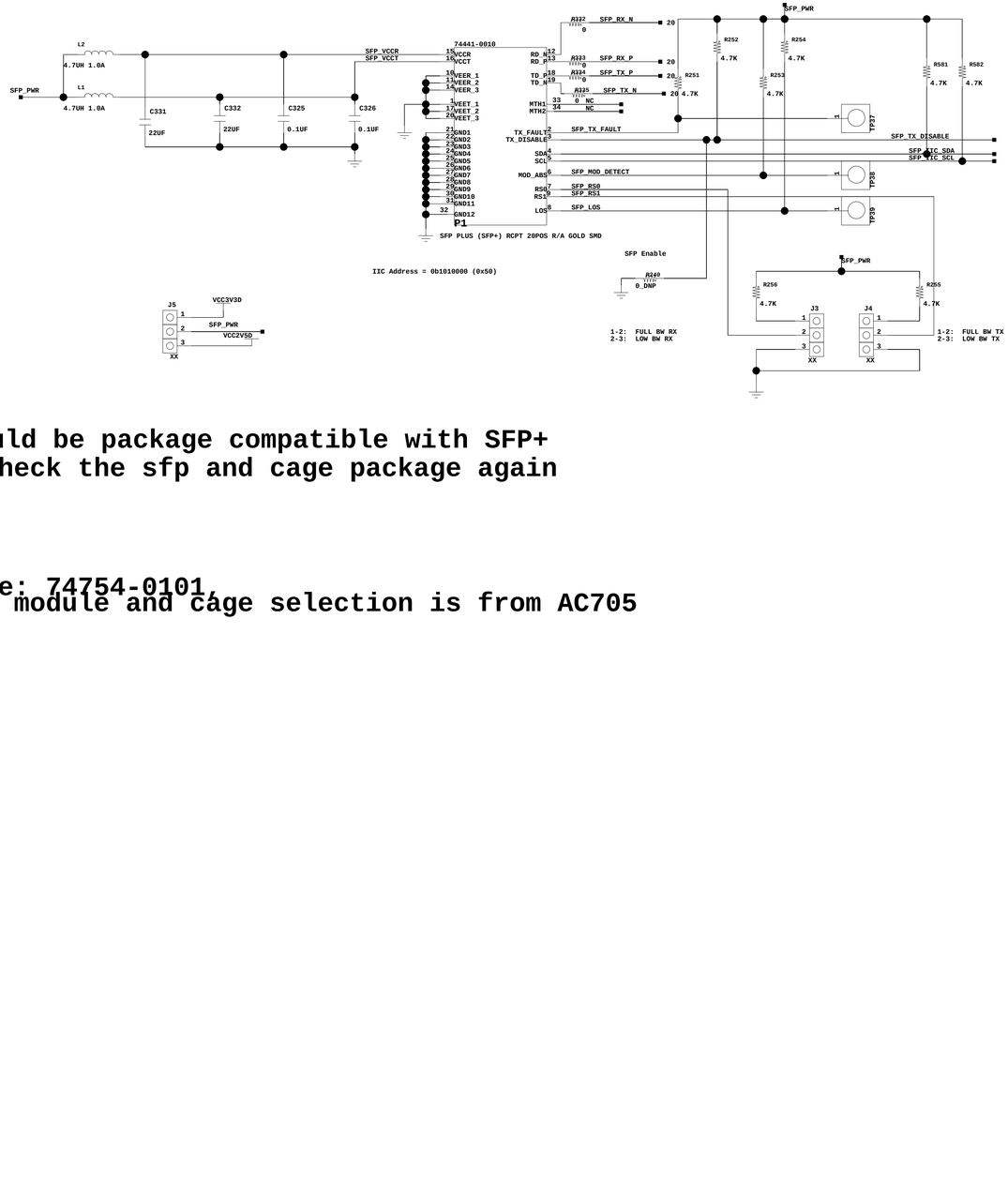
SFP+ power selectable, 2.5V, 3.3V

EFUSE PWR CHECK AGAIN

EFUSE pulse VERIFY again



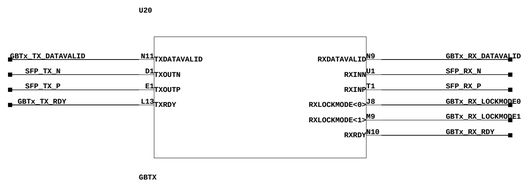
pull up near FPGA side



VTRX should be package compatible with SFP+
Be careful to check the sfp and cage package again

cage: 74754-0101
the module and cage selection is from AC705

efuse pwr relay, programming under 3.3v



NOTE

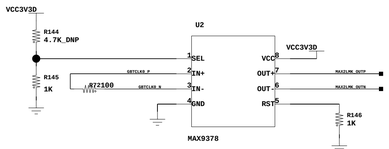
COMPANY

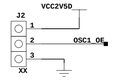
TITLE

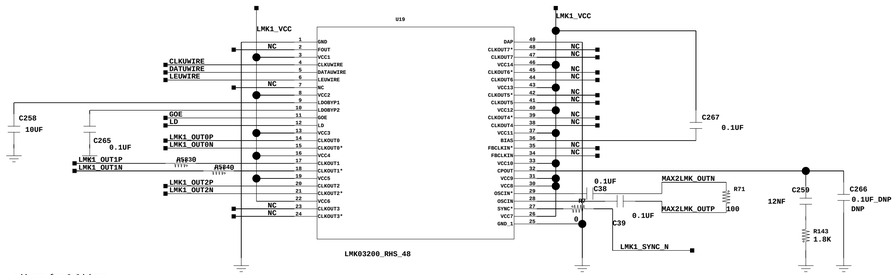
SIZE D REV SHEET GBTx_RX_CFG

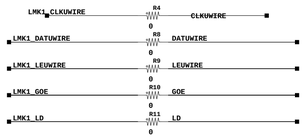
DRAWN DATE

CHECKED, 3/3/2013





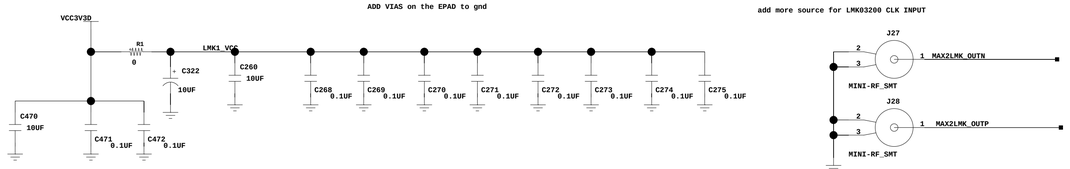




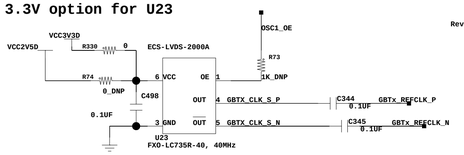
add cap for 3v3d here

ADD VIAS on the EPAD to gnd

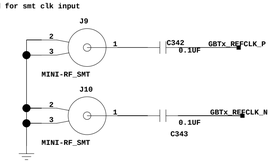
add more source for LMK03200 CLK INPUT



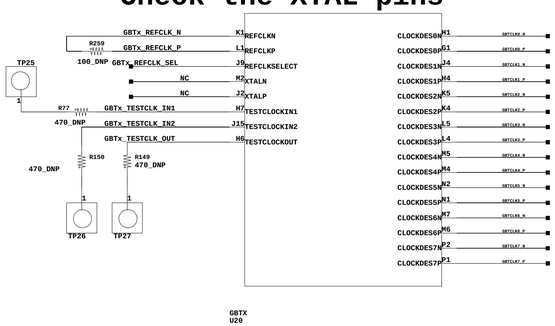
ADD 3.3V option for U23



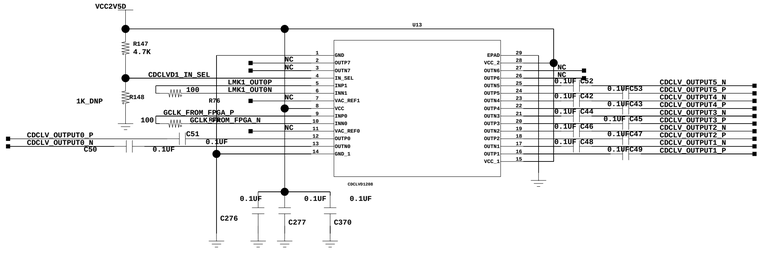
Revised for smt clk input

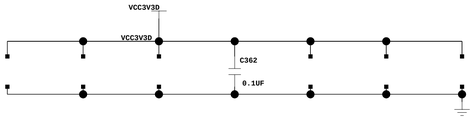


Check the XTAL pins



ADD TEST POINT FOR GBTCLK1_





use SN65LVDT122PW as clock slvs backup

NOTE

COMPANY

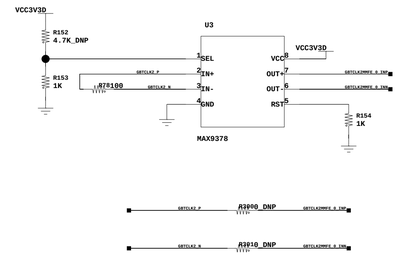
TITLE

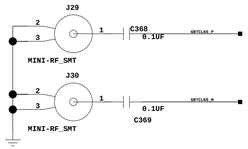
SIZE D REV SHEET OF N

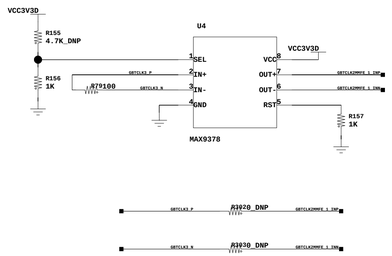
DRAWN DATE

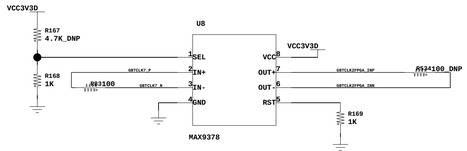
CLK_GBTX_LMK03200

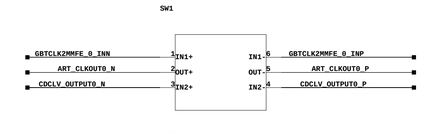
CHECKED, 3/3/2013

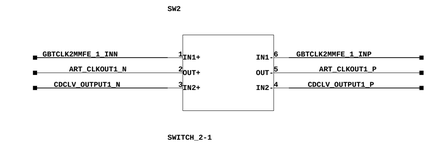


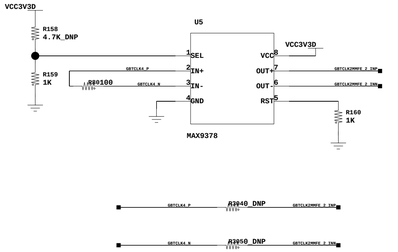


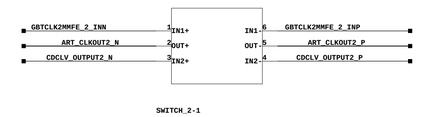


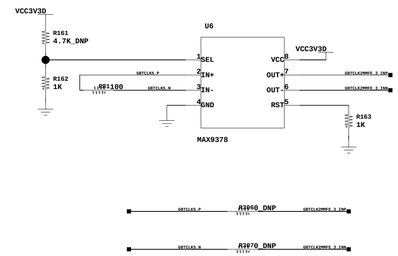


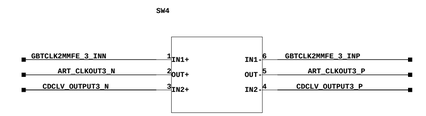


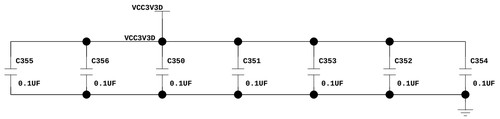












NOTE

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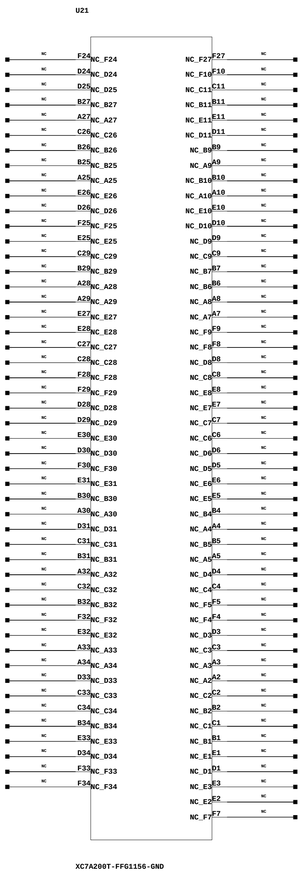
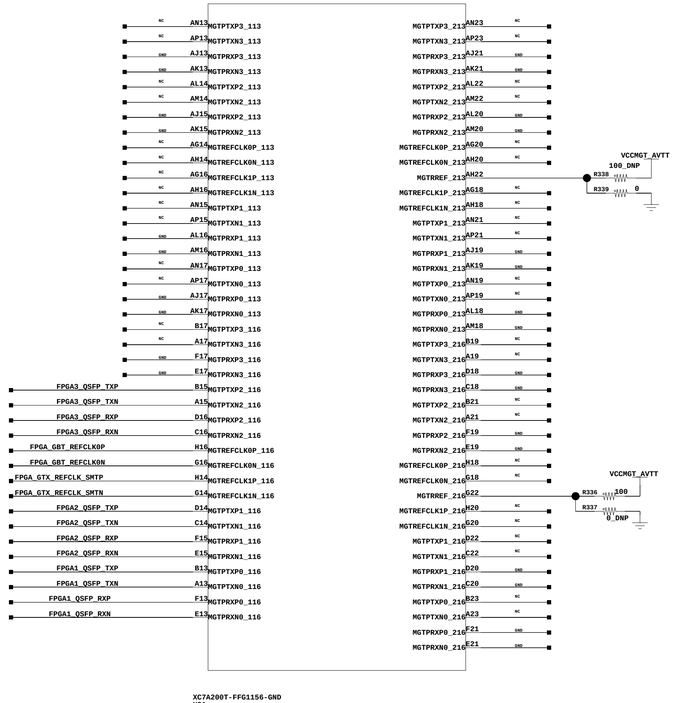
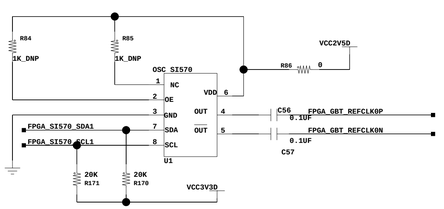
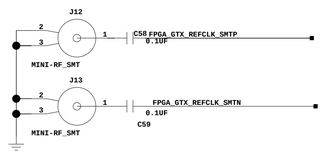
TITLE	
SIZE D REV	SHEET CLK_MAX9378_B:1output
DRAWN	DATE

CHECKED, 3/3/2013







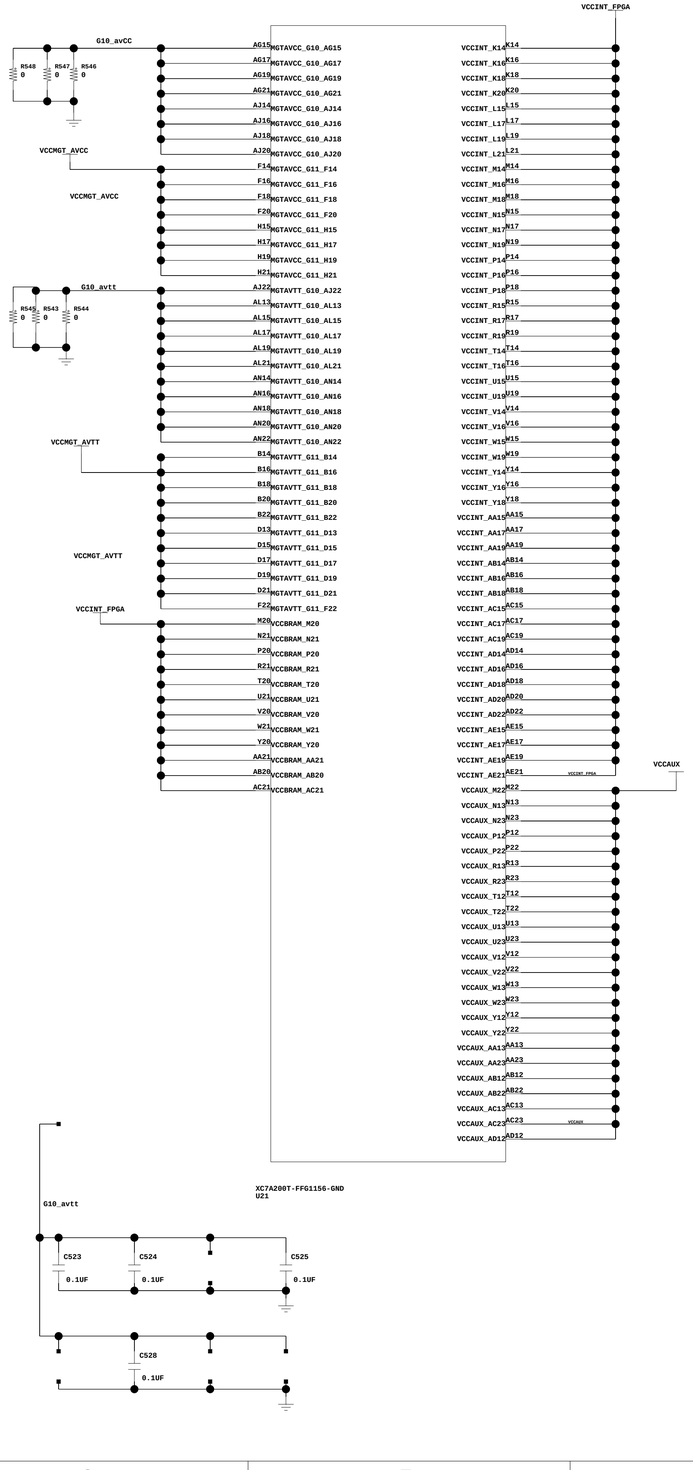


NOTE

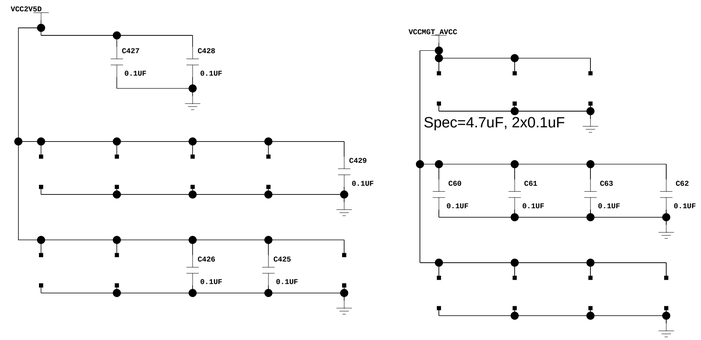
COMPANY				
TITLE				
SIZE	D	REV	SHEET	FPGA_NET_GNDNNC
DRAWN			DATE	

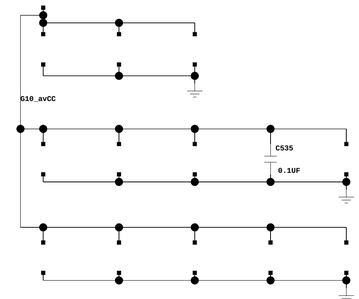
CHECKED, 3/3/2013

Consider use only 1 bank of MGT



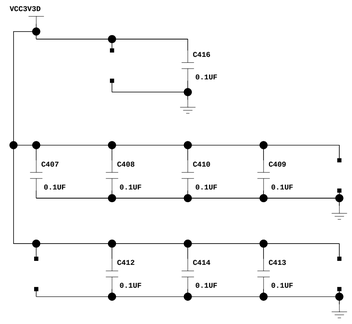
Place MGT 0.1uF caps within the FPGA via field on the bottom of the board, one for each MGT power pin/GND pin pair

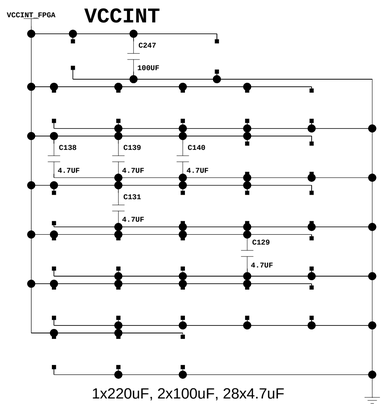




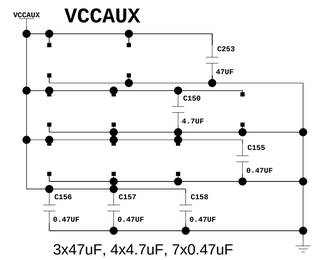
USE VCCINT FOR VCCBRAM

Adjust the Filter cap value in PCB layout

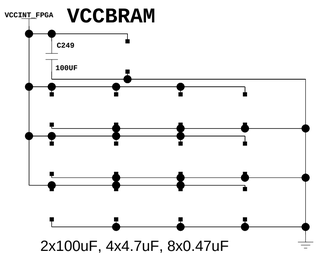




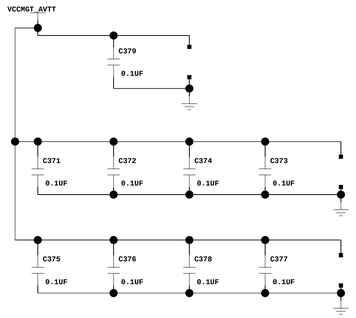
1x220uF, 2x100uF, 28x4.7uF

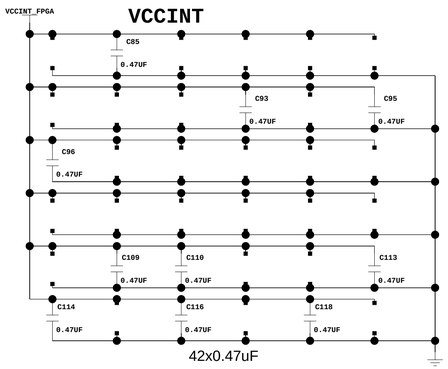


3x47uF, 4x4.7uF, 7x0.47uF



2x100uF, 4x4.7uF, 8x0.47uF





42x0.47uF

NOTE

COMPANY

TITLE

SIZE D REV SHEET FPGA_PWR_N

DRAWN DATE

CHECKED, 3/3/2013

JTAG: 1 for FPGA, 1 for GBTX

DX is not used

4. CHECK THE cfg of FPGA again

CHECK THE 3v3d bank

check the voltage for a7 jtag

XC7A200T-FFG1156-GND
U21

MASTER SPI: M[2:0]=001

U21

XC7A200T-FFG1156-GND

TLK2501_RCP_64

CLOSE TO PIN55, PIN57

CLOSE TO TLK2501 VDD PINS

S25FL256S

COMPANY	
TITLE	
SIZE D REV	SHEET FPGA_CFG_BANK0_14
DRAWN	DATE

NOTE

ADD vcc1V5 in this bank

ARTBANK_VCCO
VCCO_12_AJ27
VCCO_12_AK34
VCCO_12_AL31
VCCO_12_AM28
VCCO_12_AN25
VCCO_12_AP32
IO_0_12 AJ24
IO_L1P_T0_12 AL34 ART_DIN20_P
IO_L1N_T0_12 AM34 ART_DIN20_N
IO_L2P_T0_12 AJ33 ART_DIN28_P
IO_L2N_T0_12 AJ34 ART_DIN28_N
IO_L3P_T0_DQS_12 AN34 ART_DIN30_P
IO_L3N_T0_DQS_12 AP34 ART_DIN30_N
IO_L4P_T0_12 AK33 ART_ELINK_OUT2_P
IO_L4N_T0_12 AL33 ART_ELINK_OUT2_N
IO_L5P_T0_12 AN33 ART_DIN31_P
IO_L5N_T0_12 AP33 ART_DIN31_N
IO_L6P_T0_12 AL32 ART_DIN23_P
IO_L6N_T0_VREF_12 AM32 ART_DIN23_N
IO_L7P_T1_12 AJ31 ART_DIN21_P
IO_L7N_T1_12 AK32 ART_DIN21_N
IO_L8P_T1_12 AM31 ART_DIN22_P
IO_L8N_T1_12 AN32 ART_DIN22_N
IO_L9P_T1_DQS_12 AJ30 ART_DIN20_P
IO_L9N_T1_DQS_12 AK31 ART_DIN20_N
IO_L10P_T1_12 AN31 ART_DIN27_P
IO_L10N_T1_12 AP31 ART_DIN27_N
IO_L11P_T1_SRCC_12 AJ29 ART_ELINK_IN3_P
IO_L11N_T1_SRCC_12 AK30 ART_ELINK_IN3_N
IO_L12P_T1_MRCC_12 AL30 ART_CLKIN3_P
IO_L12N_T1_MRCC_12 AM30 ART_CLKIN3_N
IO_L13P_T2_MRCC_12 AL28 ART_CLKIN2_P
IO_L13N_T2_MRCC_12 AL29 ART_CLKIN2_N
IO_L14P_T2_SRCC_12 AJ28
IO_L14N_T2_SRCC_12 AK28
IO_L15P_T2_DQS_12 AP29 ART_DIN26_P
IO_L15N_T2_DQS_12 AP30 ART_DIN26_N
IO_L16P_T2_12 AM29
IO_L16N_T2_12 AN29
IO_L17P_T2_12 AN28 ART_DIN25_P
IO_L17N_T2_12 AP28 ART_DIN25_N
IO_L18P_T2_12 AK27 ART_ELINK_OUT1_P
IO_L18N_T2_12 AL27 ART_ELINK_OUT1_N
IO_L19P_T3_12 AJ25 ART_DIN16_P
IO_L19N_T3_VREF_12 AK25 ART_DIN16_N
IO_L20P_T3_12 AJ26 ART_DIN17_P
IO_L20N_T3_12 AK26 ART_DIN17_N
IO_L21P_T3_DQS_12 AM26 ART_DIN18_P
IO_L21N_T3_DQS_12 AN26 ART_DIN18_N
IO_L22P_T3_12 AM27 ART_DIN19_P
IO_L22N_T3_12 AN27 ART_DIN19_N
IO_L23P_T3_12 AL25 ART_ELINK_IN1_P
IO_L23N_T3_12 AM25 ART_ELINK_IN1_N
IO_L24P_T3_12 AP25 ART_DIN24_P
IO_L24N_T3_12 AP26 ART_DIN24_N
IO_25_12 AL24

GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND
U21

U21
ARTBANK_VCCO
VCCO_13_AC25
VCCO_13_AD32
VCCO_13_AE29
VCCO_13_AF26
VCCO_13_AG33
VCCO_13_AH30
IO_0_13 AD23
IO_L1P_T0_13 AF34 ART_DIN4_P
IO_L1N_T0_13 AG34 ART_DIN4_N
IO_L2P_T0_13 AD33 ART_DIN5_P
IO_L2N_T0_13 AD34 ART_DIN5_N
IO_L3P_T0_DQS_13 AH33 ART_DIN6_P
IO_L3N_T0_DQS_13 AH34 ART_DIN6_N
IO_L4P_T0_13 AE33 ART_DIN7_P
IO_L4N_T0_13 AF33 ART_DIN7_N
IO_L5P_T0_13 AG32 ART_DIN0_P
IO_L5N_T0_13 AH32 ART_DIN0_N
IO_L6P_T0_13 AE32 ART_DIN1_P
IO_L6N_T0_VREF_13 AF32 ART_DIN1_N
IO_L7P_T1_13 AD31 ART_DIN2_P
IO_L7N_T1_13 AE31 ART_DIN2_N
IO_L8P_T1_13 AD30 ART_DIN3_P
IO_L8N_T1_13 AE30 ART_DIN3_N
IO_L9P_T1_DQS_13 AD28 ART_ELINK_IN2_P
IO_L9N_T1_DQS_13 AD29 ART_ELINK_IN2_N
IO_L10P_T1_13 AG31 ART_ELINK_OUT3_P
IO_L10N_T1_13 AH31 ART_ELINK_OUT3_N
IO_L11P_T1_SRCC_13 AF29 ART_CLKIN0_P
IO_L11N_T1_SRCC_13 AF30 ART_CLKIN0_N
IO_L12P_T1_MRCC_13 AG29
IO_L12N_T1_MRCC_13 AG30
IO_L13P_T2_MRCC_13 AH28
IO_L13N_T2_MRCC_13 AH29
IO_L14P_T2_SRCC_13 AE28 ART_CLKIN1_P
IO_L14N_T2_SRCC_13 AF28 ART_CLKIN1_N
IO_L15P_T2_DQS_13 AD26 ART_ELINK_IN0_P
IO_L15N_T2_DQS_13 AE26 ART_ELINK_IN0_N
IO_L16P_T2_13 AC26 ART_DIN12_P
IO_L16N_T2_13 AC27 ART_DIN12_N
IO_L17P_T2_13 AG27 ART_DIN13_P
IO_L17N_T2_13 AH27 ART_DIN13_N
IO_L18P_T2_13 AE27 ART_DIN14_P
IO_L18N_T2_13 AF27 ART_DIN14_N
IO_L19P_T3_13 AG26 ART_DIN15_P
IO_L19N_T3_VREF_13 AH26 ART_DIN15_N
IO_L20P_T3_13 AE23 ART_DIN8_P
IO_L20N_T3_13 AF23 ART_DIN8_N
IO_L21P_T3_DQS_13 AG24 ART_DIN9_P
IO_L21N_T3_DQS_13 AH24 ART_DIN9_N
IO_L22P_T3_13 AC24 ART_DIN10_P
IO_L22N_T3_13 AD24 ART_DIN10_N
IO_L23P_T3_13 AF25 ART_DIN11_P
IO_L23N_T3_13 AG25 ART_DIN11_N
IO_L24P_T3_13 AD25 ART_ELINK_OUT0_P
IO_L24N_T3_13 AE25 ART_ELINK_OUT0_N
IO_25_13 AF24

GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

U21
ARTBANK_VCCO
VCCO_15_M28
VCCO_15_N25
VCCO_15_P32
VCCO_15_R29
VCCO_15_T26
VCCO_15_U33
IO_0_15 T24
IO_L1P_T0_AD0P_15 R26
IO_L1N_T0_AD0N_15 P26
IO_L2P_T0_AD8P_15 N26
IO_L2N_T0_AD8N_15 M27 FPGA_TP1
IO_L3P_T0_DQS_AD1P_15 U25 FPGA_TP2
IO_L3N_T0_DQS_AD1N_15 T25 FPGA_TP3
IO_L4P_T0_15 P24 GCLK_FROM_FPGA_P
IO_L4N_T0_15 N24 GCLK_FROM_FPGA_N
IO_L5P_T0_AD9P_15 U26
IO_L5N_T0_AD9N_15 U27
IO_L6P_T0_15 R25 GBTx_DCLK30_P
IO_L6N_T0_VREF_15 P25 GBTx_DCLK30_N
IO_L7P_T1_AD2P_15 T27 L1DDC_ELINK_IN1_P
IO_L7N_T1_AD2N_15 R27 L1DDC_ELINK_IN1_N
IO_L8P_T1_AD10P_15 N27 L1DDC_ELINK_OUT1_P
IO_L8N_T1_AD10N_15 N28 L1DDC_ELINK_OUT1_N
IO_L9P_T1_DQS_AD3P_15 T28 L1DDC_ELINK_IN2_P
IO_L9N_T1_DQS_AD3N_15 R28 L1DDC_ELINK_IN2_N
IO_L10P_T1_AD11P_15 N29 L1DDC_ELINK_OUT4_P
IO_L10N_T1_AD11N_15 M29 L1DDC_ELINK_OUT4_N
IO_L11P_T1_SRCC_15 U29 LMK1_OUT1P
IO_L11N_T1_SRCC_15 T29 LMK1_OUT1N
IO_L12P_T1_MRCC_15 P28 FPGA_SYSTEM_CLKP
IO_L12N_T1_MRCC_15 P29 FPGA_SYSTEM_CLKN
IO_L13P_T2_MRCC_15 R30 L1DDC_ELINK_CLK_P
IO_L13N_T2_MRCC_15 P30 L1DDC_ELINK_CLK_N
IO_L14P_T2_SRCC_15 U30
IO_L14N_T2_SRCC_15 T30
IO_L15P_T2_DQS_15 M30 L1DDC_ELINK_IN4_P
IO_L15N_T2_DQS_ADV_B_15 M31 L1DDC_ELINK_IN4_N
IO_L16P_T2_A28_15 R31 L1DDC_ELINK_IN3_P
IO_L16N_T2_A27_15 P31 L1DDC_ELINK_IN3_N
IO_L17P_T2_A26_15 N31 L1DDC_ELINK_OUT3_P
IO_L17N_T2_A25_15 M32 L1DDC_ELINK_OUT3_N
IO_L18P_T2_A24_15 U31 L1DDC_ELINK_OUT2_P
IO_L18N_T2_A23_15 U32 L1DDC_ELINK_OUT2_N
IO_L19P_T3_A22_15 T32 MAX_FPGA_DCLK36_P
IO_L19N_T3_A21_VREF_15 R32 MAX_FPGA_DCLK36_N
IO_L20P_T3_A20_15 N32 GBTCLK2FPGA_INP
IO_L20N_T3_A19_15 N33 GBTCLK2FPGA_INN
IO_L21P_T3_DQS_15 T33 SN65LVDT122_FPGA_DCLK38_P
IO_L21N_T3_DQS_A18_15 R33 SN65LVDT122_FPGA_DCLK38_N
IO_L22P_T3_A17_15 N34 SN65LVDT122_FPGA_DCLK39_P
IO_L22N_T3_A16_15 M34 SN65LVDT122_FPGA_DCLK39_N
IO_L23P_T3_FOE_B_15 U34
IO_L23N_T3_FWE_B_15 T34 FPGA_TP4
IO_L24P_T3_RS1_15 P33
IO_L24N_T3_RS0_15 P34
IO_25_15 U24

GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

U21
VCC1V5D
VCCO_16_G33
VCCO_16_H30
VCCO_16_J27
VCCO_16_K24
VCCO_16_K34
VCCO_16_L31
IO_0_16 L23 GBTx_TX_DATAVALID
IO_L1P_T0_16 N24 GBTx_TX_RDY
IO_L1N_T0_16 P24 GBTx_RX_DATAVALID
IO_L2P_T0_16 K23 GBTx_RX_LOCKMODE0
IO_L2N_T0_16 L23 GBTx_RX_LOCKMODE1
IO_L3P_T0_DQS_16 G24 GBTx_RX_RDY
IO_L3N_T0_DQS_16 G25 GBTx_LDRESET
IO_L4P_T0_16 K25 GBTx_LDSCL
IO_L4N_T0_16 J25 GBTx_LDSDA
IO_L5P_T0_16 M25 GBTx_TRESETB
IO_L5N_T0_16 L25 GBTx_TESTOUTPUT
IO_L6P_T0_16 J24 EFUSE_PROG_PULSE
IO_L6N_T0_VREF_16 H24 GBTx_CFG_SELECT
IO_L7P_T1_16 H27 GBTx_STATE_OVERRIDE
IO_L7N_T1_16 G27 GBTx_MODE0
IO_L8P_T1_16 H26 GBTx_MODE1
IO_L8N_T1_16 G26 GBTx_MODE2
IO_L9P_T1_DQS_16 L27 GBTx_MODE3
IO_L9N_T1_DQS_16 K27 GBTx_SDA
IO_L10P_T1_16 K26 GBTx_SCL
IO_L10N_T1_16 J26 GBTx_I2C_ADDR0
IO_L11P_T1_SRCC_16 L28 GBTx_I2C_ADDR1
IO_L11N_T1_SRCC_16 K28 GBTx_I2C_ADDR2
IO_L12P_T1_MRCC_16 J28 GBTx_I2C_ADDR3
IO_L12N_T1_MRCC_16 H28
IO_L13P_T2_MRCC_16 L29 GBTx_TESTCLK_IN1
IO_L13N_T2_MRCC_16 K29 GBTx_TESTCLK_IN2
IO_L14P_T2_SRCC_16 K30 GBTx_TESTCLK_OUT
IO_L14N_T2_SRCC_16 J30
IO_L15P_T2_DQS_16 G29 GBTx_REFCLK_SEL
IO_L15N_T2_DQS_16 G30 EFUSE_VSELECT
IO_L16P_T2_16 K31 GBTx_SCCLKP
IO_L16N_T2_16 J31 GBTx_SCCLKN
IO_L17P_T2_16 H31 GBTx_SCINP
IO_L17N_T2_16 G31 GBTx_SCINN
IO_L18P_T2_16 L29 GBTx_SCOUTP
IO_L18N_T2_16 L30 GBTx_SCOUTN
IO_L19P_T3_16 H32 FPGA_SLVSTESTIN2ECT
IO_L19N_T3_VREF_16 G32
IO_L20P_T3_16 K33 GBTx_RESETB
IO_L20N_T3_16 J34
IO_L21P_T3_DQS_16 H33
IO_L21N_T3_DQS_16 G34
IO_L22P_T3_16 L32
IO_L22N_T3_16 K32
IO_L23P_T3_16 J33
IO_L23N_T3_16 H34
IO_L24P_T3_16 L33
IO_L24N_T3_16 L34
IO_25_16 M26

GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

VCC1V5D
R286 4.7K
R287 4.7K

VCC2V5D
VCC1V2D
VCC1V8D
R568 0
R567 0_DNP
R566 0_DNP
R565 0_DNP
ARTBANK_VCCO

FPGA_SLVSTESTINJECT
R281 0
GBTx_SLVSTESTINJECT

VCC1V5D
C473 0.1UF
C474 0.1UF
C476 0.1UF
C475 0.1UF
C477 0.1UF

U21
A31 VCCO_17_A31
B26 VCCO_17_B28
C25 VCCO_17_C25
D32 VCCO_17_D32
E29 VCCO_17_E29
F26 VCCO_17_F26

GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

VCC3V3D
R288 4.7K_DNP
R289 1K
U28
SEL
IN+
IN-
GND
VCC
OUT+
OUT-
RST
GBTx_DCLK38_P
GBTx_DCLK38_N
AS27100
MAX_FPGA_DCLK36_P
MAX_FPGA_DCLK36_N
AS26100_DNP
R290 1K
MAX9378
GEOMETRY.HEIGHT=50.00mil

VCC3V3D
R291 4.7K_DNP
R292 1K
U29
GBTx_DCLK37_P
GBTx_DCLK37_N
MAX_FPGA_DCLK37_P
MAX_FPGA_DCLK37_N
R293 1K
MAX9378
GEOMETRY.HEIGHT=50.00mil

VCC3V3D
C357 0.1UF
C358 0.1UF

FPGA_TP1
R579 1K
DS10
FPGA_TP2
R580 1K
DS11
FPGA_TP3
R575 1K
DS6
FPGA_TP4
R576 1K
DS7

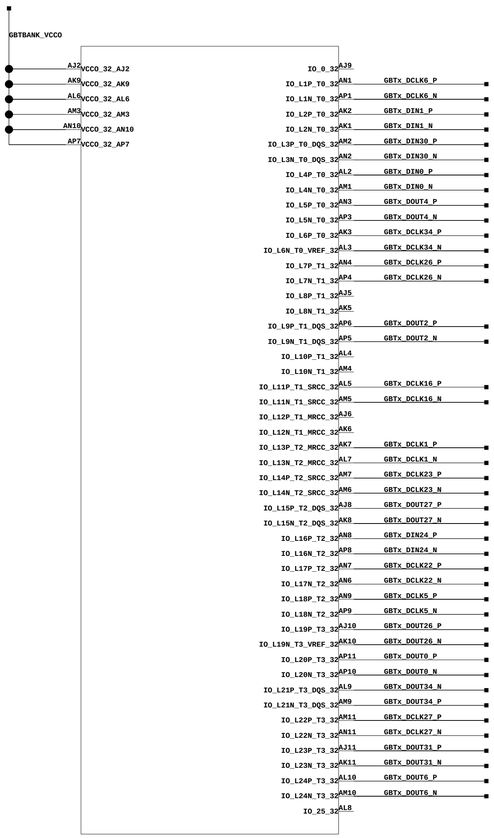
check package of sn65lvdt122 again

U32
GBTx_DCLK38_N
GBTx_DCLK38_P
R3131K
VCC3V3D
R3154.7K
VCC3V3D
R3164.7K
GBTx_DCLK39_P
GBTx_DCLK39_N
1B
2A
3S0
4DE
5S1
6A
7B
8GND
VCC16
VCC15
1Y
1Z
2DE
2Z
2Y
9GND
VCC3V3D
SN65LVDT122_FPGA_DCLK38_P
SN65LVDT122_FPGA_DCLK38_N
R3174.7KVCC3V3D
SN65LVDT122_FPGA_DCLK39_N
SN65LVDT122_FPGA_DCLK39_P
AS28100_DNP
AS29100_DNP
SN65LVDT122

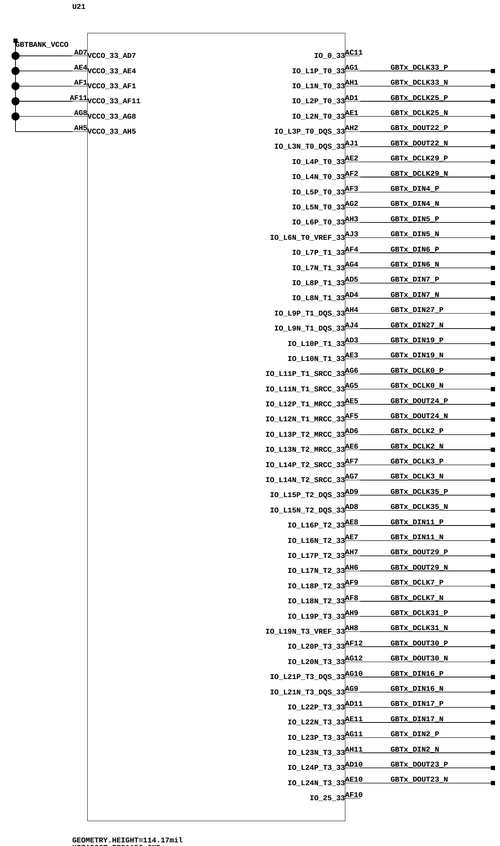
VCC3V3D
C346 0.1UF
C347 0.1UF

NOTE

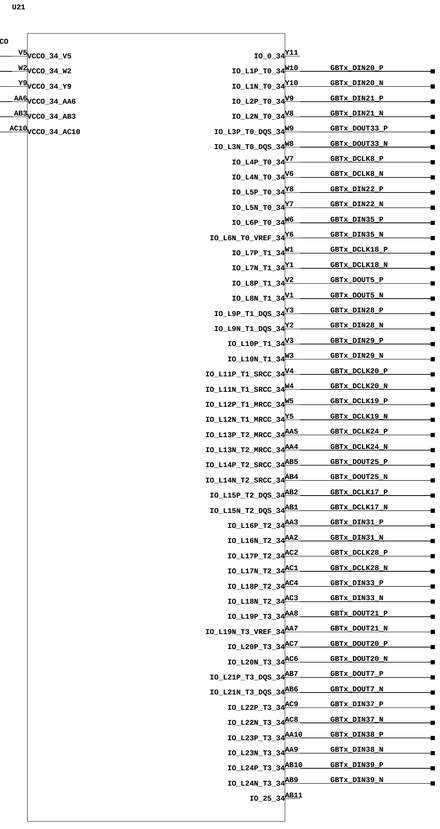
COMPANY	
TITLE	
SIZE	D
REV	
SHEET	OF
N	
DRAWN	
DATE	



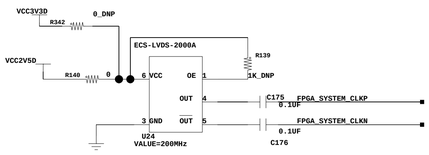
GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

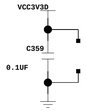


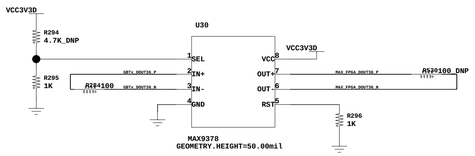
GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

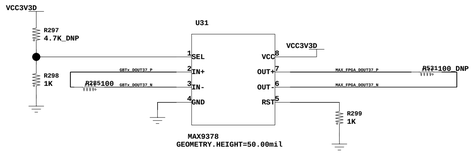


GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

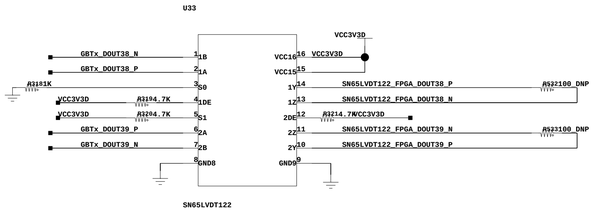


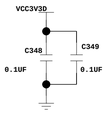


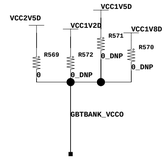




May add a resistor for s0





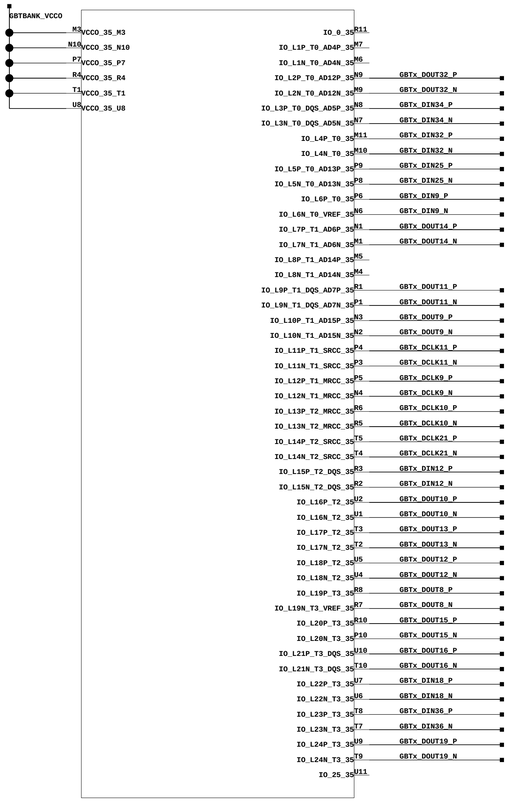


NOTE

COMPANY	
TITLE	
SIZE D REV	SHEET FPGA_BANK32_B3_34
DRAWN	DATE

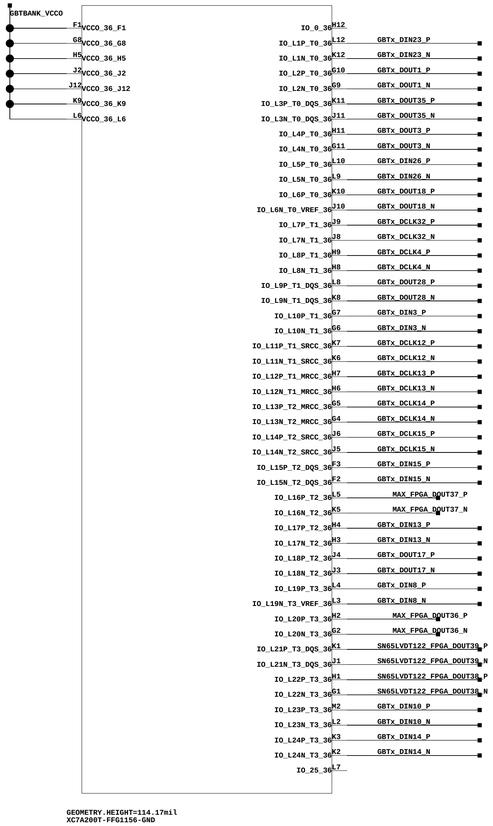
ADD some test points and leds here

U21



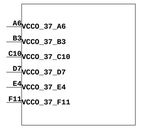
GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

U21



GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

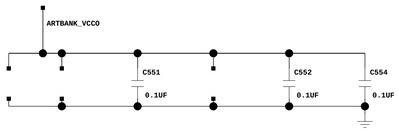
U21

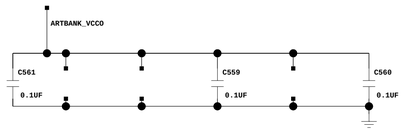


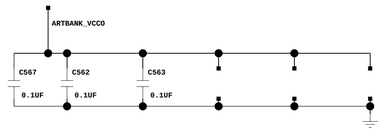
GEOMETRY.HEIGHT=114.17mil
XC7A200T-FFG1156-GND

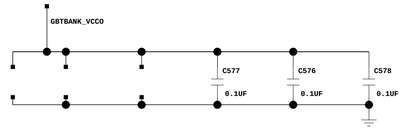
NOTE

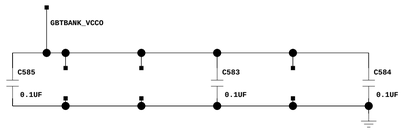
COMPANY	
TITLE	
SIZE D REV	SHEET FPGA_BANK35_B6_37
DRAWN	DATE

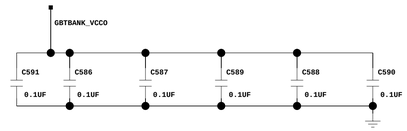


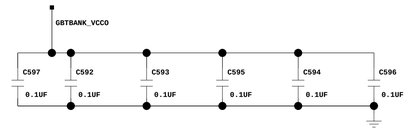












NOTE

COMPANY

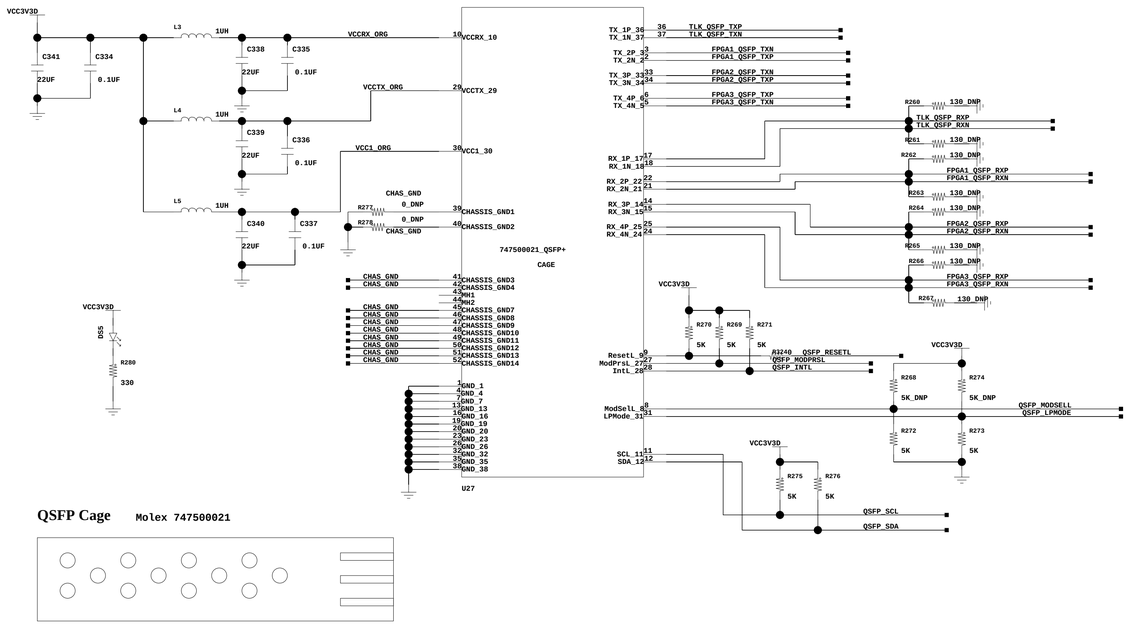
TITLE

SIZE D REV SHEET FPGA_BANKVO_BAP

DRAWN DATE

REVISED, 3/31/2013

QSFP Cage from Molex 747500021
QSFP connector from Molex 0755860011 38 positions
QSFP module from Avago: AFBR-79EIDZ

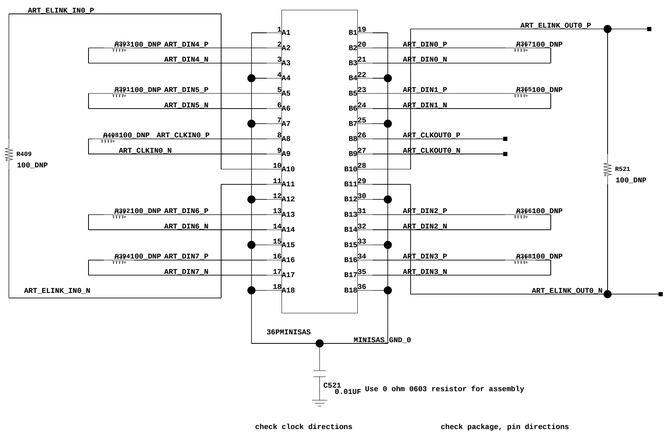


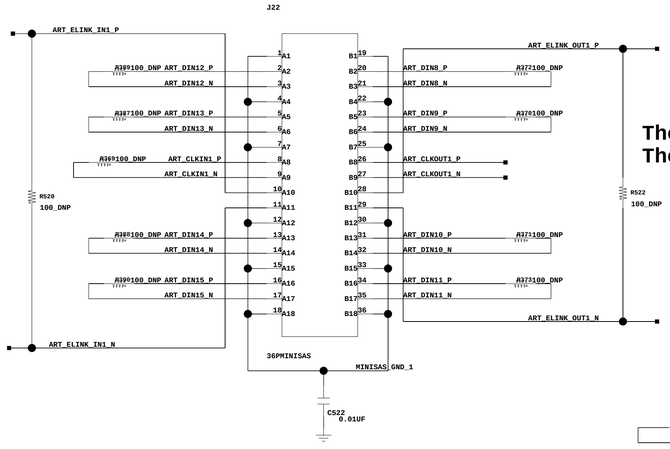
QSFP Cage Molex 747500021

NOTE

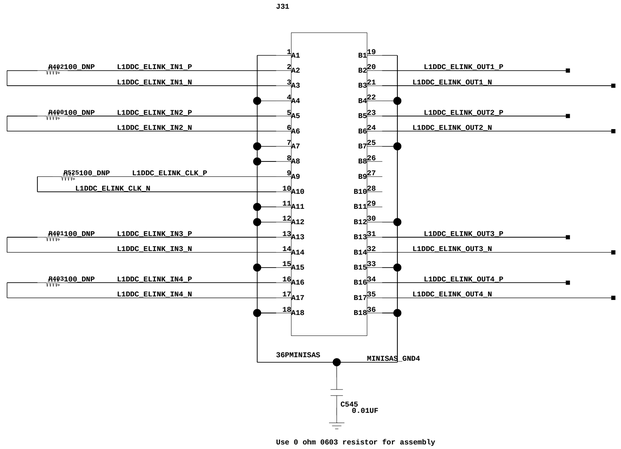
COMPANY
TITLE
SIZE D REV SHEET QSFP OF N
DRAWN DATE

CLKOUT: FROM ADDC TO MMFE-8
CLKIN: FROM MMFE-8 TO ADDC



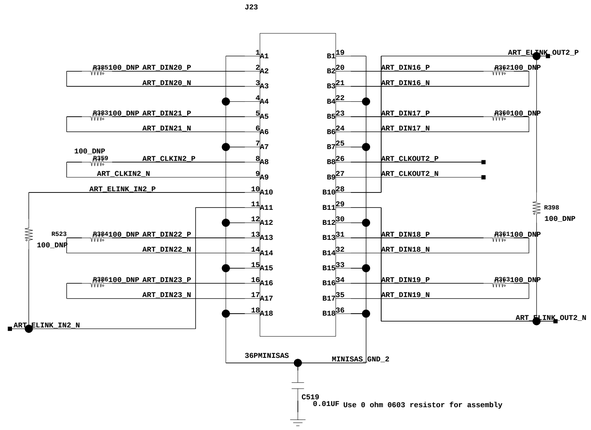


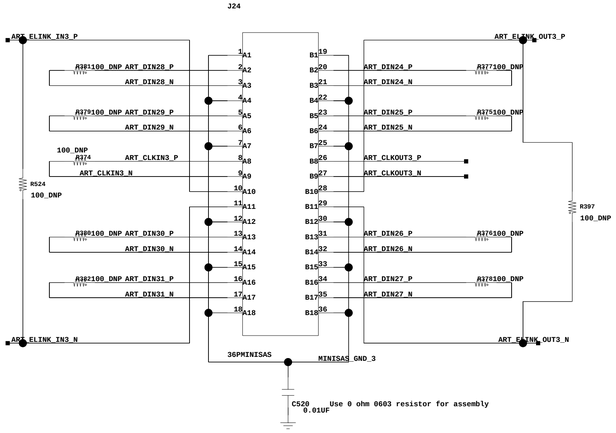
The e-link capacitors may chaged to 0R0
The termination resistors place near FPGA side



Connector: Molex 75783-0125

Cable: 8F36-AAA105-0.50, 50cm





NOTE

COMPANY

TITLE

SIZE D REV SHEET MINISAS_CONNN

DRAWN DATE

Schematic Ends

Ref Pages BELOW

Remindings:

1. **ADD silkscreen for resistor selection**
2. **Check the package drawed by my self...**
3. **ADD Capacitors for OSCs and convertor chips**
4. **CHECK THE cfg of FPGA again**