ATLAS NSW Electronics Specification
Component or Facility Name: TDS

Trigger Data Serializer for the ATLAS NSW Upgrade

Version: V 1.0

Abstract

This document describes the design specifications for the sTGC Trigger Data Serializer (TDS) ASIC to be used in the ATLAS NSW muon detector upgrade. TDS is a high-speed low-latency low-power-consumption radiation-tolerant serializer. It is responsible for preparing sTGC trigger data for both pads and strips, performing pad-strip matching, and serializing trigger data for transmission to the circuits on the rim of the NSW detector. We have designed and fabricated a prototype to test the TDS high-speed serializer part and a first prototype of the TDS ASIC with all of its functionality implemented. Both prototypes met our expectations. However there are some changes for the TDS specifications after the first prototype and that requires a second prototype.

Revision History			
Rev. No.	***Proposed Date*** / ***Approved Date***	***Description of Changes*** *(Include section numbers or page numbers if appropriate)*	***Proposed By: author*** / ***Approved By: reviewer***
0.0	P: date A: date	Initial draft	P: name A: name
		List only versions that are submitted for approval. If there is more than one author or reviewer, list each with a "P:" or "A:" as appropriate.	

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1 Conventions and Glossary

sTGC: small-strip Thin Gap Chamber
NSW: New Small Wheel
TDS: Trigger Data Serializer
Pad-TDS: TDS that handles sTGC pad detector signals
Strip-TDS: TDS that handles sTGC strip detector signals
TOT: time over threshold
BCID: bunch crossing ID

2 Related Documents

1) *TDSVII_pads_map.xlsx* shows the map between pads on ASIC and external signals/power/ground and is attached with this document.
2) *TDSVII_i2c_register.pdf* shows the details for all programmable registers and is attached with this document.
3) *pad-trigger interface protocol.pdf* shows the protocol between pad-trigger logic and strip-TDS ASIC.
4) Specifications of the 1st TDS prototype:

   https://indico.cern.ch/event/385326/contribution/1/attachments/768906/1054604/TDS_Specification_V7.pdf
5) Talks about the serializer-core ASIC design and test results:

   https://indico.cern.ch/event/327350/contribution/4/attachments/635920/875425/SER_TestResults_Liang_nSW_ASIC_Review_21July2014.pdf
6) Talks about the TDS-V1 specifications and design:

   https://indico.cern.ch/event/327350/contribution/2/attachments/635918/875422/sTGC_Review_doc.pdf

   https://indico.cern.ch/event/327350/contribution/2/attachments/635919/875424/TDS_ATLAS_Review_July21.pdf
7) Talks about the wire-bonded TDS-V1 ASIC test results:

   http://indico.cern.ch/event/354058/session/0/contribution/8/attachments/701564/963197/TDS_status_report_20150209.pdf

   https://indico.cern.ch/event/382360/contribution/0/attachments/762188/1045635/2015.03.20_NSW_TDSv1_TestStatus_Liang.pdf

   https://indico.cern.ch/event/394321/contribution/2/attachments/789444/1082048/TDS_ATLAS_June2015.pdf

3 Description of Component or Facility

The TDS ASIC is responsible for preparing trigger data for both sTGC pads and strips, performing pad-strip matching, and serializing data for transmission to the circuits on the rim of the NSW detector. The chip has two different running modes: one to deal with sTGC pads (denoted as “pad-TDS”) and the other to deal with sTGC strips (denoted as “strip-TDS”). The two modes are selected via a hardware pin on the sTGC frontend board. Strip pulse heights are captured by the VMM frontend Amplifier-Shaper-Discriminator (ASD) chip and sent to strip-TDS. Meanwhile discriminated pad signals are assigned to their bunch crossing,

and the binary pattern of hit pads is serialized by pad-TDS and sent to the pad trigger electronic board on the rim of the NSW. Three-out-of-four coincidences are made in pad trigger electronics in each sTGC quadruplet; this track road information is sent to the strip-TDS to choose a band of strips to be sent to the on-rim router electronics. The frontend electronics chain is shown in Figure 1.

TDS will be fabricated in the IBM 130 nm CMOS process. In total 2048 strip-TDS ASICs and 768 pad-TDS ASICs are needed. The main challenges for the TDS ASIC design are: 1) the output data need to be sent at a rate of 4.8 Gbps; 2) the overall latency should be less than 100 ns for pad-TDS and 150 ns for strip-TDS; 3) the power consumption should be less than 1 W per chip; 4) the ASIC needs to be radiation-tolerant; 5) Each strip-TDS needs to handle 128 strips, while each pad-TDS handles up to 104 pads.

We designed and fabricated a serializer-core chip to test the TDS high-speed serializer part. The high-speed serializer is based on the CERN GBT serializer, but we have made three modifications: 1) Modifying user clock to load data at 160 MHz instead of 40 MHz; 2) loading 30 bits instead of 120 bits at each user clock cycle; (3) changing the metallization technology from LM to DM. The serializer-core chip was packaged in QFN and the test results indicate that it satisfies our requirements.

We also designed and fabricated a TDS-V1 ASIC with all TDS functionalities implemented. The chip can handle 128 strips and up to 96 pads. Test results using wire-bonded dies mounted on PCB indicate that they function properly. The V1 chips are packaged in a 400-pins BGA package and due to delays on the packaging process, we are still testing packaged chips mounted on PCB.

After the fabrication of the TDS-V1 ASIC, there are some specification changes. They include: 1) add channel-by-channel timing delay for each channel for pad-TDS; 2) change the interface from the pad-trigger logic to the strip-TDS; 3) integrate the configuration and integration part into the logic part; 4) change the output format for the strip-TDS to the router.

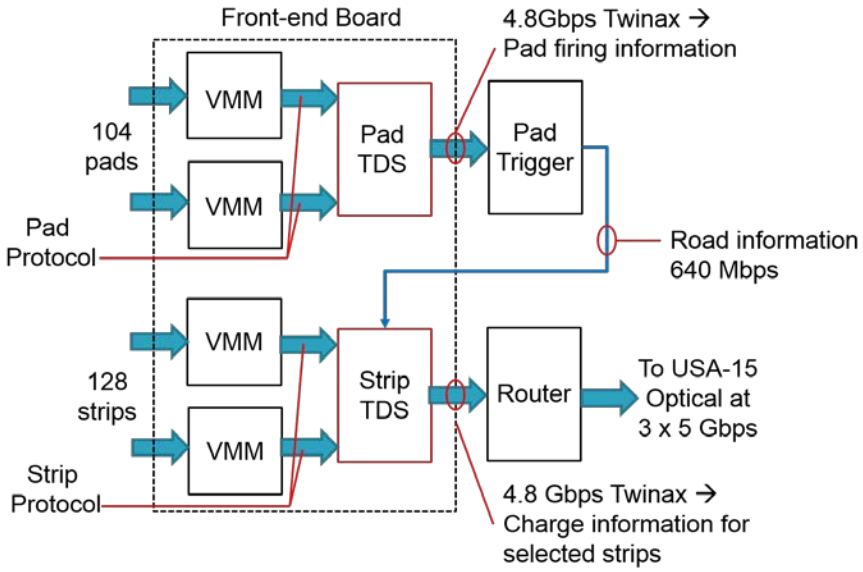


Figure 1: Location of the TDS ASIC on the sTGC frontend electronics chain.

Figure 2 shows the block diagram of the strip-TDS ASIC. The design is divided into three major parts: VMM interface, Preprocessor, and Serialization. The VMM interface reads in the VMM output data, stores them in 4-depth ring buffers together with BCID in each channel and waits for track road information from the pad trigger logic board. The Preprocessor performs BCID and pad-strip matching, and selects strips within the pad road for transmission to the router. The Serialization part prepares the trigger data in the right format and serializes them for transmission to the router board. A signal flow of strip-TDS is shown in Figure 3.

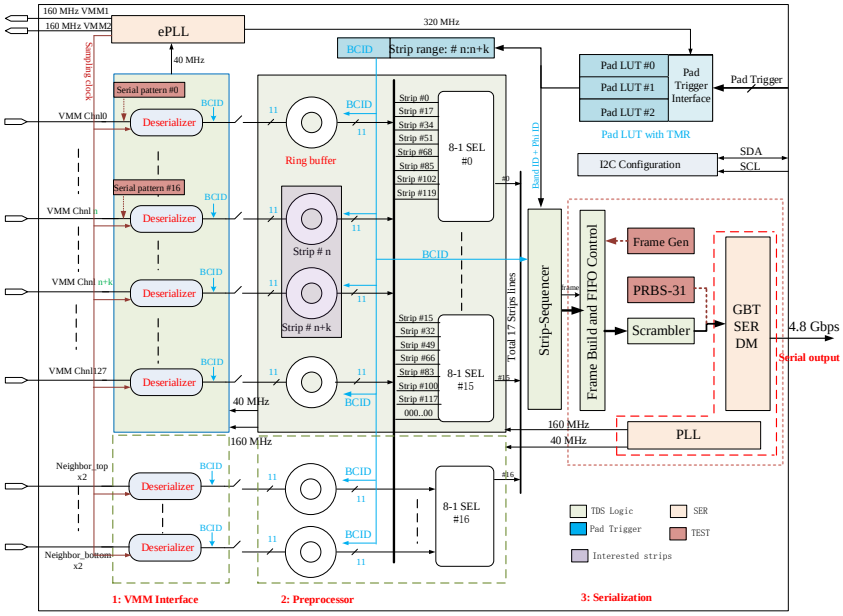


Figure 2. Block diagram of the strip-TDS ASIC.

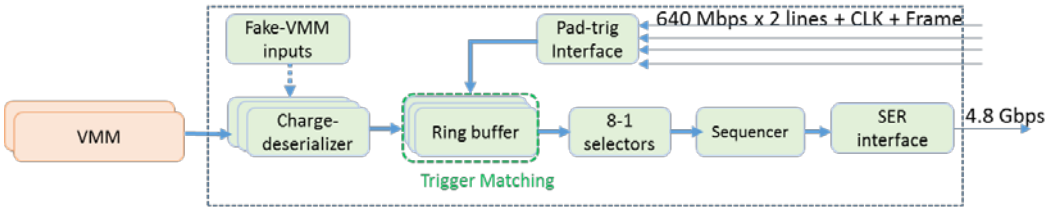


Figure 3. Signal flow in the strip-TDS ASIC.

The block diagram of the pad-TDS ASIC is shown in Figure 4. The design is also divided into three parts: VMM interface, Preprocessor, and Serialization. The inputs from VMM to pad-TDS are pulses (e.g., TOT or a fixed width pulse). Pad-TDS tags the arrival time of a hit by sampling the associated global BCID counter, as shown in Figure 5. The sampled BCID will be stored in a 2-depth ring buffer for each channel. At the end of each BC, pad-TDS will perform BCID comparison between the current BCID and the BCIDs stored in each channel buffer to determine the channel firing status. The firing status of a channel is 1-bit yes/no information, and these information will be collected and sent in serial to the pad-trigger logic board on the rim at 4.8 Gbps.

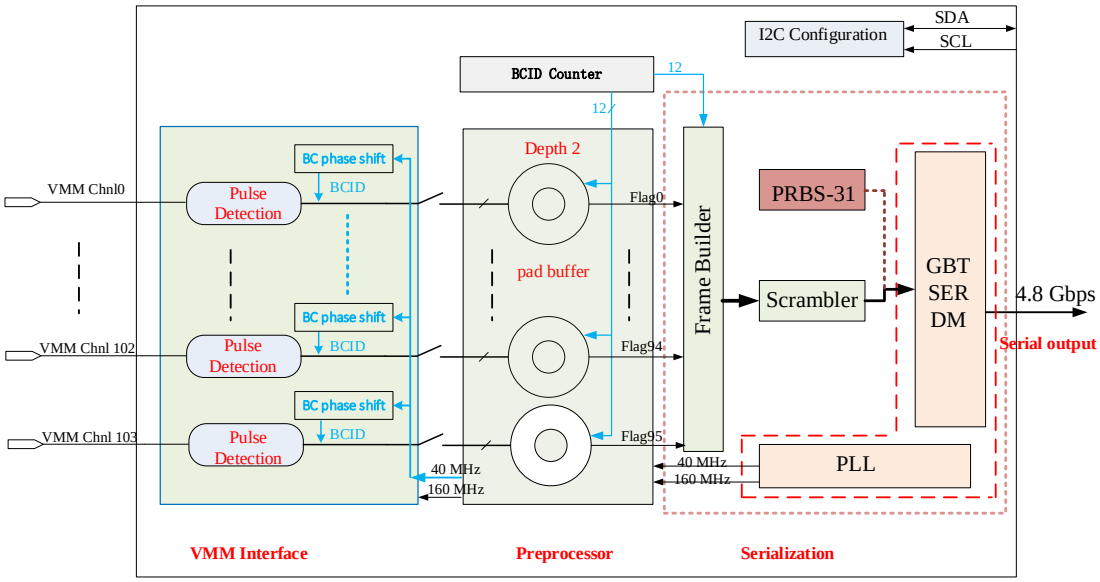


Figure 4. Block diagram of the pad-TDS ASIC.

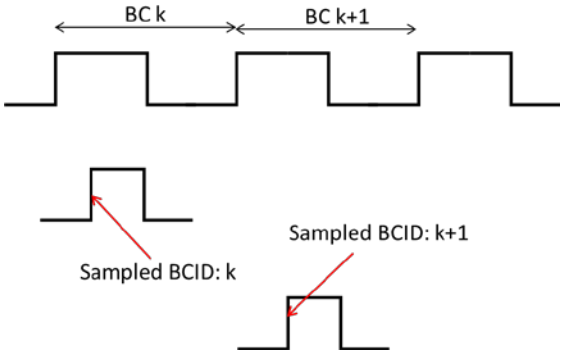


Figure 5. Illustration of the pad-hit detection and BCID assignment.

4 Interfaces

As shown in Figure 1, both pad-TDS and strip-TDS receive signals from two VMM ASICs. Pad-TDS sends the pad firing status together with BCID to the pad trigger logic board while strip-TDS receives the road information from the pad trigger logic board. The strip-TDS output will be sent to the router board. The specifications for the VMM, pad trigger logic board, and the router board are listed in Table 4.1.

Table 4.1: Components which Interface to This Component

Name of Component	Name of Component Specification
VMM ASIC	VMM Front End Specification https://indico.cern.ch/event/385326/contribution/3/attachments/768909/1054607/VMM_specifications_20150424.pdf
pad trigger logic board	https://indico.cern.ch/event/354058/session/1/contribution/15/attachments/701568/963203/PadTriggerLogicBoard.pdf
router board	https://indico.cern.ch/event/354058/session/1/contribution/14/attachments/701569/963204/Design_review_report_021015REVIEW.pdf

5 Physical Description

A preliminary layout of the TDS-V2 ASIC is shown in Figure 6. The silicon design area is 5.2mm × 5.2mm. The size is mainly due to the large number of physical pads each ASIC needs to handle and also the density of detector channels. TDS will be packaged in a wire-bonded 2cm × 2cm 400-pins BGA. In order to reduce the size of the chip, the pads (each one has a size of 95μm × 62μm) are staggered in two rows. The distance between two rows is 255 μm and the pitch size between two pads in the same row is 73 μm. The pin assignment of the TDSVII die is provided in "*TDSVII_pads_map.xls*". A screen shot view of the pad floorplan is shown in Figure 7.

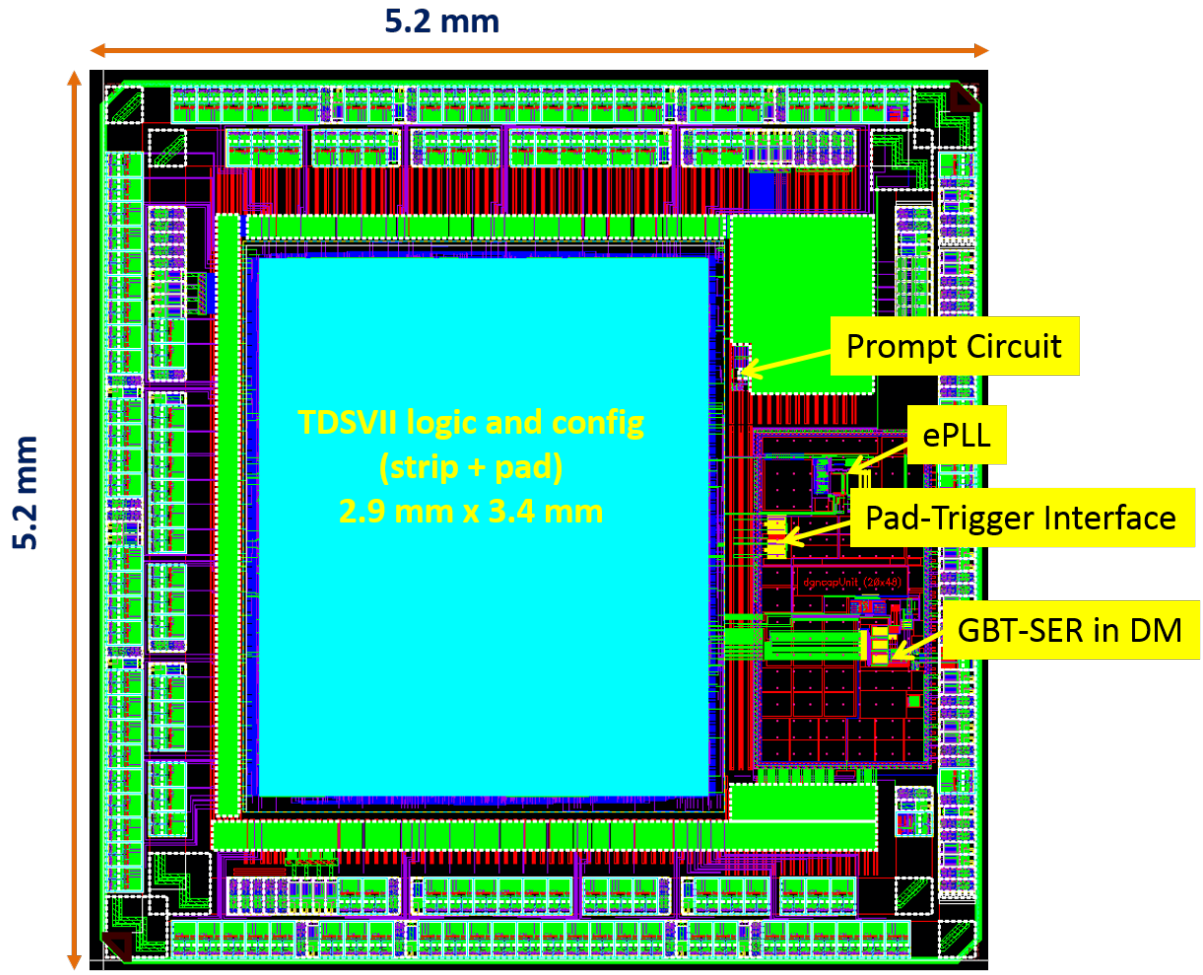


Figure 6: A preliminary layout of the TDS-V2 ASIC. Five different blocks are clearly seen in the picture: 1) the logic and config part is the part that is responsible for all TDS logics, configuration and monitoring, it is implemented with the Cadence digital process; 2) the prompt circuit is required to meet the export control requirements and the design is provided by BNL; 3) ePLL is used for providing phase adjustable 160 MHz to VMMs and the design is provided by CERN; 4) the pad-trigger interface circuit accepts and decodes the pad trigger road information and is based on hand-layout to meet the speed requirement; 5) GBT-SER in DM is the high-speed serializer part that is based on the CERN GBT design but with three significant modifications.

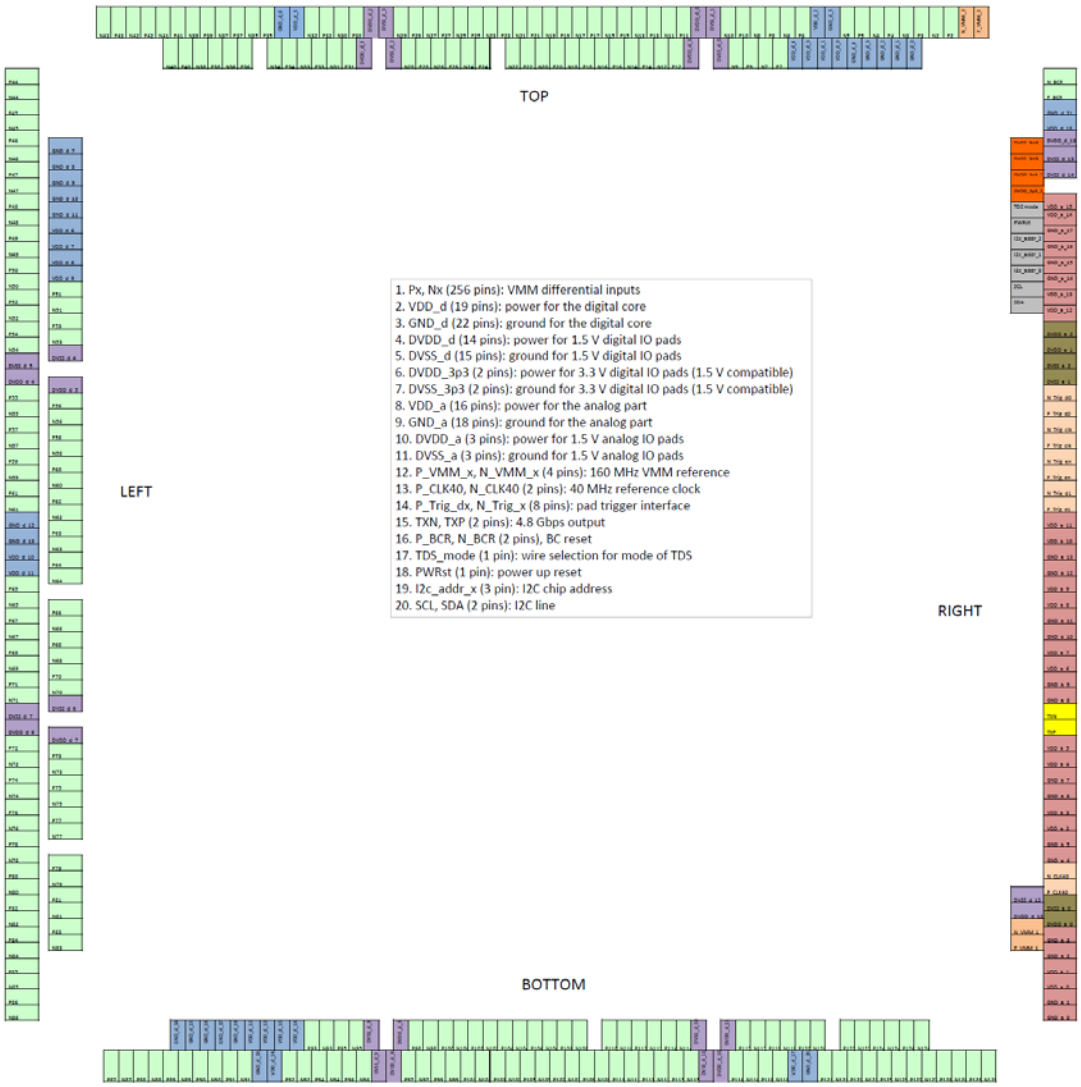


Figure 7: Physical pad floorplan for TDS-V2 ASIC (see “TDSVII_pads_map.xls” for details).

6 Manufacturer

TDS ASIC will be fabricated in the IBM 130 nm CMOS process with a sub-category 8RF-DM323, which has 3 thin metal layers, 2 thick metal layers, and 3 thick metal layers used for RF purpose (DM323). The choice is made to have the final production on the same wafer with other NSW ICs. The PROMPT circuitry is included in the design for the export control purpose.

7 Power

We will use 1.5 V for both analog and digital parts and the maximum current is expected to be 300 mA for the analog part and 400 mA for the digital part based on the simulation. We have measured the power consumption for the high-speed serializer and found the measured and simulated power consumption agree with each other.

Table 7.1: Power Requirements

Name	Max/Nom/Min V or I Supplied	Nom/Max I for Voltage Source	Max/Min V for Current Source	Other Requirements
Analog power	Max: 1.6 Volt Nom: 1.5 Volt (~300 mA) Min: 1.45 Volt			
Digital power	Max: 1.6 Volt Nom: 1.5 Volt (~400 mA) Min: 1.45 Volt			

8 Cooling

ATLAS will provide water cooling for all NSW ASICs during the normal operation.

9 Input/Output

There are 400 pins in total for this ASIC, Table 9.1 lists detailed information for each pin.

Table 9.1: Input and Output Signals

Name	In, Out or I/O	Type of Signal or Max/Min	Input or Output Impedance	Description
P/N[127:0]	In	SLVS		128 chnls VMM inputs; padTDS shares chnl0-103;
P/N_VMM_[1:0]	Out	SLVS		Two 160 MHz clock to VMM charge output
P/N_CLK40	In	SLVS		40 MHz reference input to SER
TXP/N	Out	CML		4.8 Gbps serializer output
P/N_Trig_en	In	SLVS		Frame of pad trigger logic to stripTDS
P/N_Trig_clk	In	SLVS		320 MHz clock of pad trigger logic to stripTDS
P/N_Trig_d[1:0]	In	SLVS		Two data lines of pad trigger logic to stripTDS
SCL	In	LVCMOS15		I2C
SDA	In/Out	LVCMOS15		I2C
I2c_addr[2:0]	In	LVCMOS15		I2C chip address
P/N_BCR	In	SLVS		BCID reset
TDS_mode	In	LVCMOS15		Mode selection of pad/strip TDS
PWRst	In	LVCMOS15		Power up reset

10 Detailed Functional Description and Specification

10.1 General features

10.1.1 Overview of characteristics

1) Supply: 1.5 Volt
2) IO standard: SLVS (CERN IP) for differential; 1.5 Volt CMOS for single-ended
3) Serial output: 4.8 Gbps, CML
4) Reference Clock input: 40 MHz
5) Reset: power up reset or soft rest via I2C
6) Configuration port: I2C (slave, 7 bits mode)
7) Package: 400-pin wire-bond BGA
8) Two modes: strip/pad mode is selected via an IO pin instead of a register
9) BCR is provided as a hardware pin
10) SEU protection: TMR is done for following parts: Serializer, Serial protocol logic, BCID, BC clock generator, BC clock phase shift, matching window of strip channel, all configuration registers, pad trigger LUT.

10.1.2 Configuration parameters

The parameters of TDS-V2 are configured via the I2C interface. The I2C interface in TDSVII works in slave mode with a 7-bit chip address. All configurable parameters are listed below:

1) Strip/Pad TDS BCID offset, BCID rollover value: 12 bits each
2) Strip/Pad TDS BC clock phase: 4 bits
3) Strip TDS matching window size: 4 bits
4) Strip/Pad TDS enable/disable channel: 128 bits
5) Strip TDS pad Look up Table: 16 (depth) x 15 (width) bits
6) Pad TDS delay tune for individual channel: 5 bits x 104
7) Configuration parameters on ePLL (160 MHz to VMM), GBT SER
8) Test commands: self-Test, bypass-trigger, TDS serial protocol test, PRBS-31 test.
9) Soft Reset command: Reset logic, reset ePLL, reset SER
10) SEU error flag: TDS will make 64 bits CRC to monitor potential SEU flips for all parameters from 1-9
11) Monitoring information of Strip TDS VMM channel 0, 64: 19 bits x 2
12) Monitoring of Strip TDS pad trigger interface: 25 bits
13) Monitoring of Locking status of ePLL, SER

In total, there are ~1300 bits for parameters from 1) to 9), and all these parameters are SEU protected with TMR, which gives about ~5000 bits configuration bits in total.

Detailed description of configuration parameters can be found in "*TDSVII_i2c_register.pdf*".

10.2 Strip-TDS

10.2.1 VMM interface

1) Number of input VMM channels: 128 differential pairs

Covering the channels of two VMMs.

2) VMM input signal standard: SLVS (CERN IP)
   Embedded 100-Ohm termination resistor, and can accept a wide common-mode voltage from 0.2 V to 1 V with a typical swing of ± 200 mV.
3) VMM will use the 160 MHz clock provided by TDS to send 6-bit charge information to TDS. TDS has two phase-programmable 160 MHz clocks for the corresponding two VMMs. Each clock can be configured to take into account trace differences from two input VMMs to the TDS. The programmable phase is provided by an embedded CERN ePLL IP, with a programmable phase step of 400 ps. TDS samples the VMM 6-bit charge via dual edges of its local 160 MHz, and correct programmable phases of the 160 MHz VMM used will help avoid timing violations.
   In the final version of VMM, a test pattern will be provided. One can make use of the test pattern from VMM to determine the correct phases for the 160 MHz clocks to VMMs. Besides, TDS always passes the sampled charges together with BCID for two channels (channel 0 and channel 64) to monitoring registers. One can refer to the values in these monitoring registers while tuning the phases of 160 MHz for VMM. All registers are accessible via the I2C bus.
4) The output standard of the 160 MHz clock to VMM: SLVS.
   Signal swing is: -0.2V - +0.2V. AC coupling and proper bias on the side to VMM will migrate the common mode voltage differences.
5) Figure 8 shows the serial protocol of VMM 6-bit charge output. TDS will assign BCID based on the leading edge of the VMM charge output, which corresponds to the peaking time of charge in VMM. The local BCID can be synchronized globally with a programmable 12-bit BCID phase offset and 6.25 ns step phase shift of the BCID clock (a total of 4 phases available in 25 ns). Besides, there is also a programmable 12-bit BCID rollover value, which sets the maximum of BCID.
6) There is no need to adjust the signal arrival time for different strips on one strip-TDS chip, but a programmable matching window is provided in each TDS, from 25 ns to 50 ns with a step of 6.25 ns, to compensate for the signal delays to and through the VMM chip.
7) Due to the layout of the wires inside the sTGC detector, it can take more than 25 ns to collect the charge of a muon hitting in the middle of two wires. The matching window is most likely to be set to a number greater than 25 ns. In case of the matching window is larger than 25 ns, a BCID extension flag will be assigned. For example, as illustrated in Figure 9, when using a 31.25 ns matching window, a VMM hit in the first 6.25 ns of one BC will be assigned to the current BC, but will also be given an extension flag indicating that it might also belong to the previous BCID. In other words, TDS uses 13 bits to indicate the arrival time of a hit: 12 bits BCID plus one flag bit. A hit with BCID k+1 and a valid flag means that it may belong to BC k+1 (the hit occurs in BC k+1 and arrives very early) or belong to BC k (the hit occurs in BC k but takes more than 25 ns to collect its charge).
8) For the first 14 strip channels, each channel has a VMM 6-bit charge test pattern for self-testing purpose. A trigger-matching scheme is also provided to shift the charge out through the Preprocessor and Serializer.

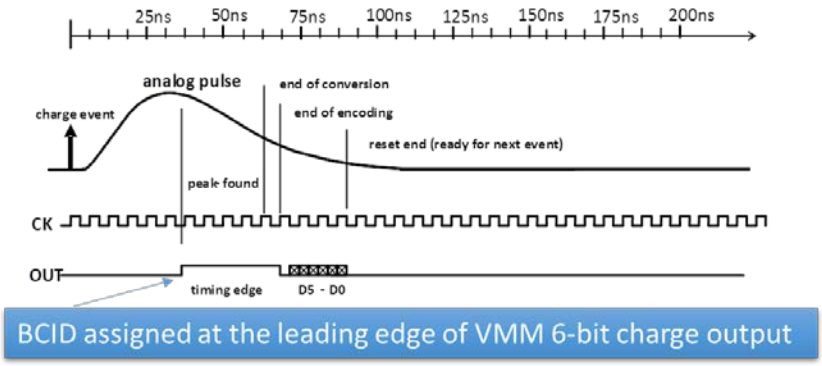


Figure 8: VMM 6-bit charge output protocol.

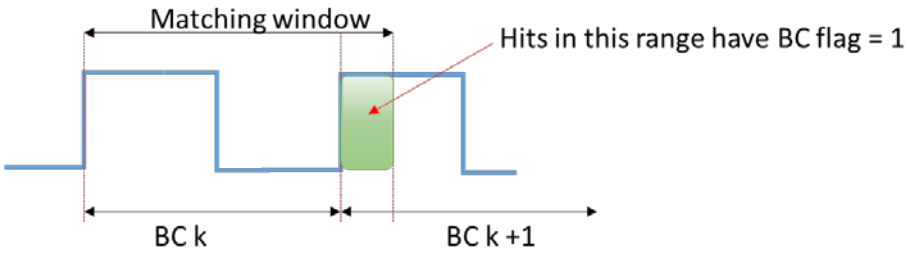


Figure 9. Matching window and BC flag.

10.2.2 Preprocessor

9) A ring buffer is used for each strip channel to buffer VMM inputs while waiting for the decision from the pad-trigger. It is assumed that the arrival time for the pad-trigger signal is later than the arrival time for strips. The contents inside the ring buffer for each hit is: 6-bit charge + 1 bit BCID flag + 12-bit BCID.
   Each ring buffer has a depth of 4 and can store charge and BCID information for 4 hits. In order to not keep hits occurred a long time ago, there is an 8-bit programmable timer to clear old contents inside each ring buffer. The timer works at 40 MHz. A NULL (BCID: 0xFFF, charge: 0, flag: 0) will be written into the ring buffer each cycle set by the timer. The ring buffer is shift-register-based, and a new write command will pushed the oldest hit out, as shown in Figure 10.

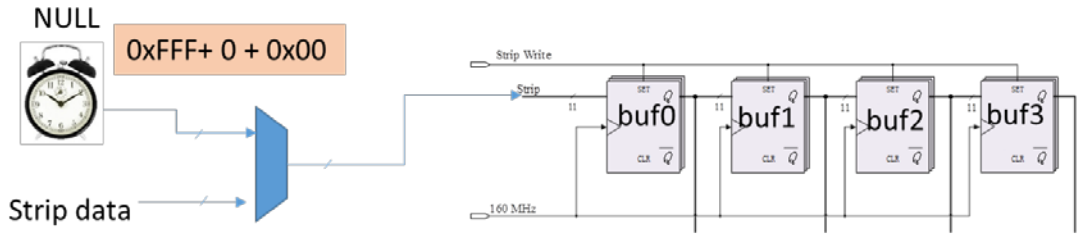


Figure 10. Illustration of strip-TDS channel buffer and old hit removal scheme.

10) Since one pad road can cross two TDSs, we need to read out data from both TDSs in that case. Besides the 7-bit road ID, the pad logic also needs to send one extra bit to indicate which TDS to be read out, thus we have 8 bits for band ID.

11) Pad road information from the pad trigger logic is delivered to each strip-TDS via four lines: frame, clock, and two data lines. All lines are differential and in LVDS standard. Figure 11 shows the protocol for communication between pad-trigger logic board and strip-TDS. A detailed timing requirement on the pad-trigger interface is provided in "*pad-trigger interface protocol.pdf*".

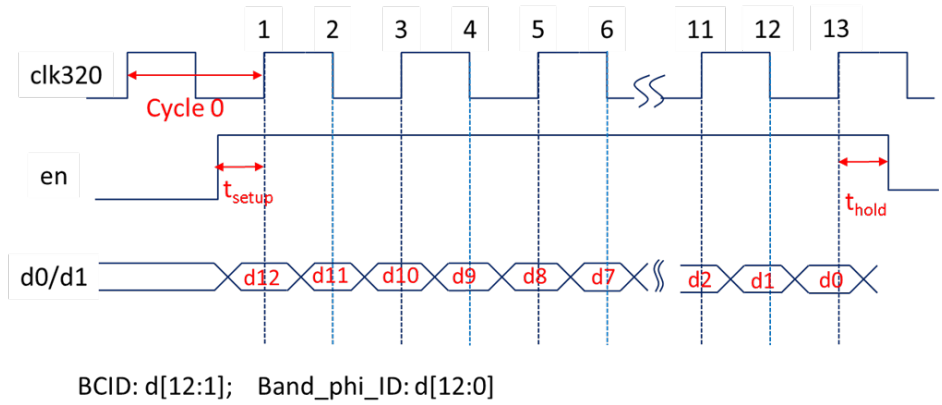


Figure 11. Trigger road protocol between the pad-trigger logic board and strip-TDS.

Clock (*clk320*): 320 MHz,
Frame line (*en*): indicates the starting of the bits by staying valid at the rising edge of clock.
Data lines (*d0/d1*): 640 Mbps each (320 MHz DDR), one line is dedicated for BCID information and the other is for band ID (8 bits) and phi ID (5 bits). TDS also passes the information from the two data lines to monitoring registers to allow us to check its contents.
On the sTGC frontend board, clock, frame and BCID lines are shared for all TDSs and will be distributed to each TDS via a fan-out chip, while the band-phi ID line is dedicated for each TDS. There might be additional delay imposed by the fan-out chip on the clock, frame and BCID lines with respect to the band-phi ID line. One can check monitoring registers to see if there are any timing violations.

12) Each TDS has a LUT that contains the starting channel number for at most 16 roads. The address for the element of each LUT is 8-bits band-ID and the content is 7-bits starting strip address. The LUT size is 15 bits width × 16 depth. TMR is used to reduce effects from SEU.

13) After it decodes the starting strip address, TDS will search for a range of 17 strips (including four neighboring channels: two from the top and two from the bottom), and match the pad trigger BCID with the BCIDs of hits stored in the ring buffer for each channel. Figure 12 illustrates the process of trigger BCID matching in a strip-TDS channel, contents in the buffer are loaded per trigger request, and BCID are checked for all contents in parallel.
If the matching window is set to 25 ns, exact BCID matching is performed; otherwise, the flag bit mentioned in 7) will be taken in account. For the latter case, if the pad trigger BCID is k, hits with BCID k+1 and a valid flag bit are also considered to be valid matches. In case there are multiple matches in the buffer, the newest one will be picked.
Since one hit can cause several neighbor strips to fire, in order to reduce the traffic, we use seventeen 8-to-1 selectors as shown in Figure 2 so that any fired strip belongs to one

cluster will be processed by different 8-to-1 selectors. All 128 channels are arranged to seventeen 8-to-1 selector by every 17 channels. The Strip-Sequencer circuit will make sure that the selected channels from these 8-to-1 selectors have the natural channel sequence.

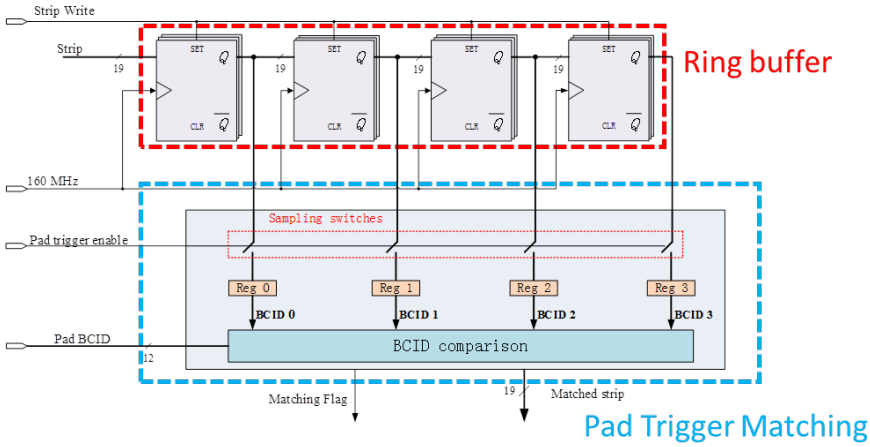


Figure 12. Pad trigger matching in a selected strip-TDS channel.

14) Depending on the firing status of the 17 strips, either the first 14 strips or the last 14 strips will be selected for read out, as shown in Figure 13. The total output data has a size of 104 bits. They will be sent in 4 consecutive packets with 30 bits per packet at 4.8 Gbps. With 4 header bits for each packet, the overall data that need to be transmitted are 120 bits and thus the overall transmission time is 25 ns. When there are no data, TDS will send four consecutive 30-bit NULL packets. The header for a data packet is "1010", whereas the header of a NULL packet is "1100". Router will make use of the difference in these header bits for its cutting-through switching algorithm to quickly throw away NULL packets.

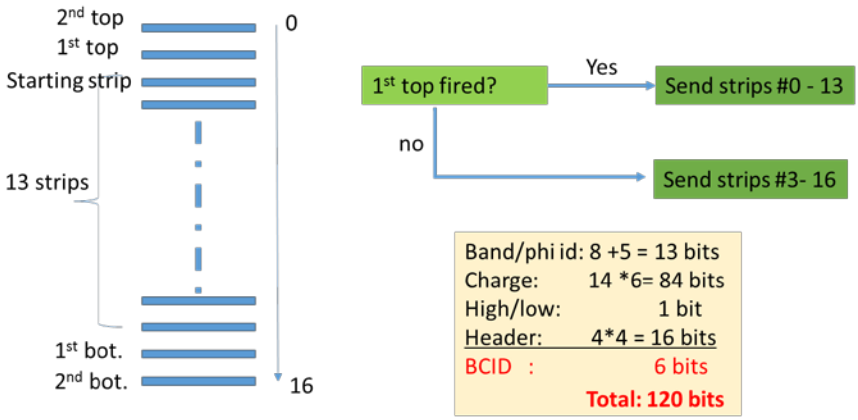


Figure 13. Algorithm for selection of 14 strips out of a total of 17 strips in a trigger.

15) TDS can be configured to bypass the pad-trigger matching and send out data for 14 strips out of the 128 channels, as shown in Figure 14. In case there are more than 14 matched strips, only the first 14 strips will be selected via the 8-1 priority selectors. This functionality is mainly for testing purpose when no pad-trigger logic is available.

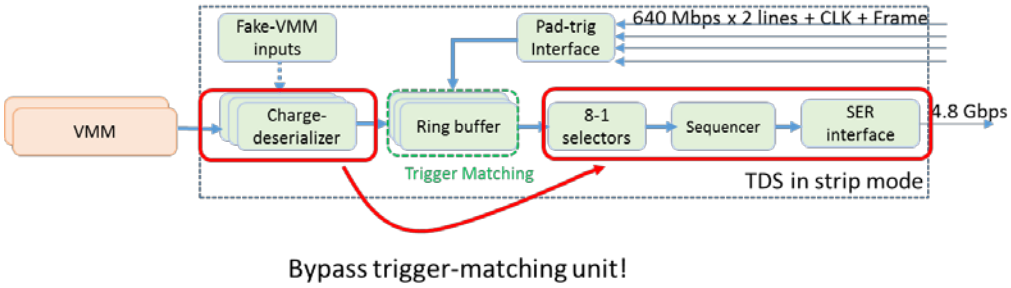


Figure 14. Bypassing pad trigger matching unit in strip-TDS for test purpose.

10.2.3 Serialization

16) The CERN-GBT serializer was converted to IBM 8RF-DM and modified to load 30 bits at 160 MHz instead of 120 bits at 40 MHz. We have built a serializer-core prototype and also used it in our 1st TDS prototype and observed good performance for both prototypes.

17) The 120 bits data is arranged in 4 consecutive 30-bit packets. A data frame starts with a 4-bit header "1010", and a NULL starts with "1100", as shown in Figure 15.

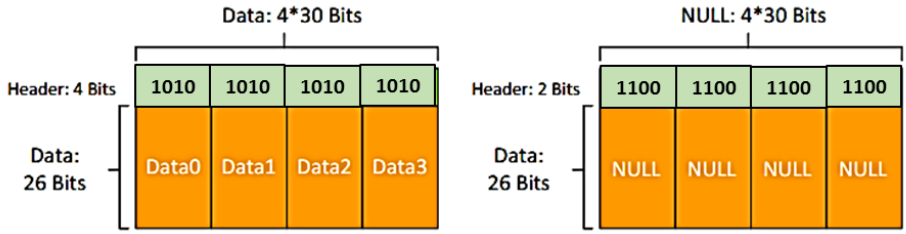


Figure 15. strip-TDS to Router serial protocol.

18) We use a scrambler for the DC-balancing purpose. The polynomial used for the scrambler algorithm is: 1+x^39+x^58, which is the IEEE standard for 10 G Ethernet [1], as shown in Figure 16.

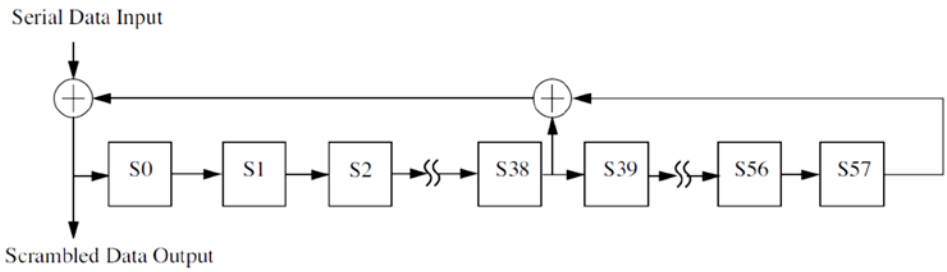


Figure 16. Scrambling scheme in strip-TDS serial output.

19) To test the protocol of the TDS outputs to the router, TDS can be configured to generate fake strip data. Counters are used in the data fields of a packet while the NULL is constant: 0xBA1176.

20) To test the serial link performance, the TDS can be configured to output PRBS-31. This is useful for eye-diagram observation and bit error evaluation of the link.

21) No CRC bits will be sent with the strip data. To check the link of strip-TDS to Router, one can set TDS to a test mode with fake strip data and the fake data are sent according to

the serial protocol. The link on the Router side can be trained and Router can also forward the fake data to USA15 for further check the data transmission.

10.3 Pad-TDS

22) Each pad-TDS handles a total of 104 pads with SLVS input and can also accept the VMM's "LVDS"-like input.

23) Each pad-TDS has a 12-bit BCID offset. Pad-TDS makes use of the BCID offset to synchronize its BCID to the global LHC clock. In addition, there is also a BCID rollover register, which sets the maximum BCID counter value.

24) There is a local BC clock for each pad channel and that clock can be configured to different phase shifts with respect to the global BC clock at a step size of 3.125 ns for a total time shift range of 25 ns. This is mainly used to compensate cable length differences from the pad detector to the VMM. The local BCID counter shares the same BCID offset and BCID rollover value with the global BCID counter in the pad-TDS.

The principle of the pad-TDS local BC phase shift circuit is shown in Figure 17. The circuit is made up of two branches, denoted as "Rising edge branch" and "Falling edge branch". The two branches are the same except the Rising edge branch is driven by the rising edge of 160 MHz and the Falling edge branch is driven by inversion of the 160 MHz. Each branch has a loop of four-tap shift registers and with proper selection of initial values of each tap (*d0-d3*), the branch can be programed to generate a 40 MHz clock with a phase shift step of one cycle of 160 MHz (6.25 ns), as shown in Figure 18. Since the two branches are driven by rising and falling edges of the 160 MHz respectively, the two branches in together can be programmed to generate a BC clock with a phase shift step of 3.125 ns. An additional bit (*d4*) is used to select outputs between these two branches. Figure 19 illustrates the principle of the two branches working together for a 3.125 ns phase shift.

In conclusion, there will be five bits (*d0-d4*) used for local BC phase shift, and the correspondence of configuration bits and the phase shift value is list below.

The phase shift circuit is protected with TMR. Moreover, the circuit will automatically check and recover the states every BCR in case of any failure even with TMR.

BC phase	0 ns	3.125 ns	6.25 ns	9.375 ns	12.5 ns
d0-d4	11000	11001	01100	01101	00110
BC phase	15.625 ns	18.75 ns	21.875 ns		
d0-d4	00111	10010	10011		

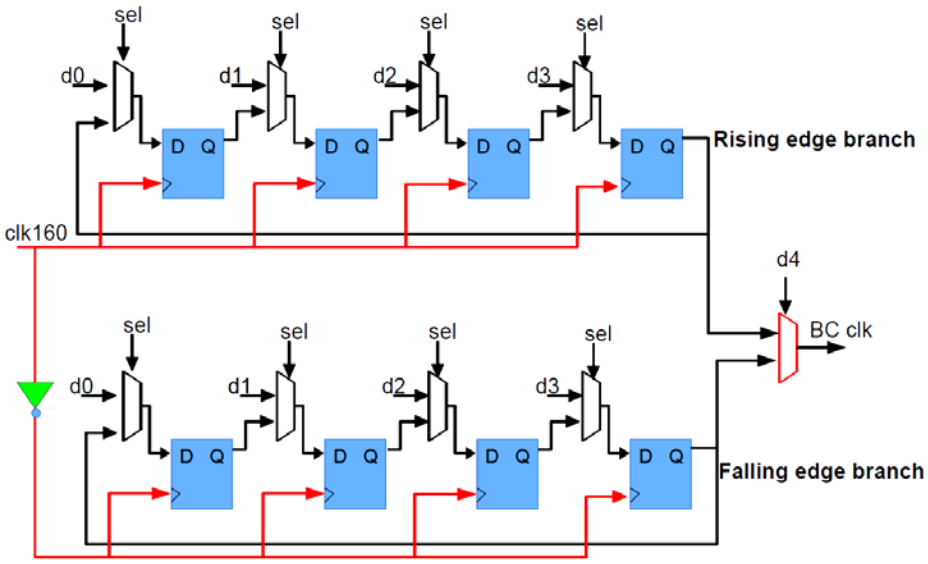


Figure 17. Block diagram of the local BC phase shift circuit in the pad-TDS.

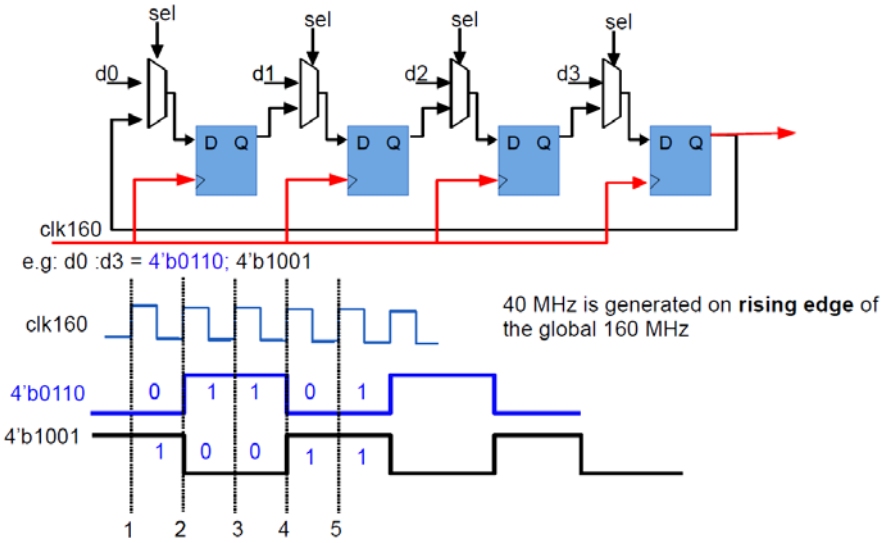


Figure 18. Operation principle of one branch in the local BC phase shift circuit.

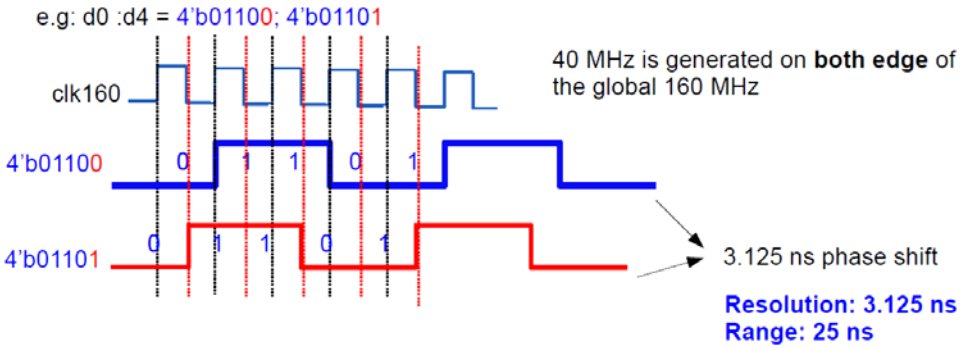


Figure 19. Operation principle of the local BC phase shift circuit.

25) In case a pad fired, the pad-TDS uses the leading edge of the pulse signal to sample the corresponding pad-channel BCID counter, which works with the local BC clock. The sampled BCIDs are kept in the ring buffer. At the end of the global BCID k, TDS will

check the ring buffer of each channel to see if there is a hit with a BCID equals to k. A channel is marked as "yes" as long as there is a match in the ring buffer, otherwise, a "no" will be recorded. Similarly as the strip-TDS, there is also a timer circuit in each channel to prevent a pad hit from occupying the ring buffer for too long time. The timer is programmable with 8 bits counter working at 40 MHz.

26) Pad-TDS uses the same serializer as the one used by the strip-TDS. The pad-TDS data are arranged into 120 bits and transmitted in 25 ns. The format is listed below:

header	Pad-TDS status	BCID
"1010"	104 bits "yes/no"	12 bits

27) All data except the header bits are scrambled to keep DC-balanced. The same scrambler polynomial is used as the one used by the strip-TDS. Again, no CRC fields are available in the transmission.

28) A PRBS-31 generator is also provided for serial link test.

10.4 Programming Model

The TDS is configured via I2C bus, in which TDS is served as a slave with 7-bit chip address. There are about 5000 bits of configuration parameters after TMR, and a detailed register map with respect to the I2C address is provided in "*TDSVII_i2c_register.pdf*".

11 Radiation Tolerance, EMC Issues and Other Special Requirements

The Total Ionization Dose (TID) for the NSW on-detector front-end electronics is about 500 Krad [2]. It has been demonstrated that this level of radiation is not a problem for IBM 130 nm CMOS process [3].

For protection of Single-Event Effect (SEE), all clock trees in the TDS logic part has been tripled for protection against Single Event Transition. And Triple Modular Redundancy (TMR) scheme are applied to protect the chip from effects of Single Event Upset (SEU), this includes all configuration parameters, the BCID counter, Serial protocol logic, BC clock generator, BC clock phase shift, matching window of strip channels, pad trigger LUT, and the loop-back divider in the Serializer. Besides, there are additional logics to monitor the parameters of circuits with feedback loops every cycle of bunch crossing reset. In case these parameters are corrupted from SEU even with TMR protection, the monitoring circuit will auto correct them at the next bunch-crossing reset.

12 Testing, Validation and Commissioning

Describe testing procedures that will be used to demonstrate that the fabricated component meets the specifications. This should include radiation testing if radiation tolerance is one of the requirements. Specify the testing features included in the system in view of easily test and qualify the component during production (e.g. BIST included in ASICs or systems).

It is not required to complete this section prior to the first specification review but it should be completed prior to the PDR. Prior to the FDR, the production testing must be described, and prior to the PRR, commissioning plans must be included.

13 Reliability Matters

13.1 Consequences of Failures

Describe the consequences to the detector of a failure of one unit of this component, e.g. x% of the sub-detector channels will be lost, or one stave or petal could overheat causing delamination of its component parts. The severity of the consequences will determine the level of reliability required and the level to be validated by QA and QC procedures defined in Sections 12.4 and 12.5.

13.2 Prior Knowledge of Expected Reliability

We have built a prototype of the high speed serializer and also a first prototype of TDS ASIC with all functionality implemented. No unexpected design issues have been observed so far.

13.3 Measures Proposed to Insure Reliability of Component and/or System

Include such measures as conservative design techniques (give specific examples), redundancy and possibilities to replace failed part. If failed part could be replaced, estimate the difficulty and time involved for installing replacements,

13.4 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

Describe what stress tests will be applied during the development period to validate the reliability of this component. Give a brief outline of any appropriate reliability theory being used. These tests could involve destructive tests.

It is not required to complete this section prior to the first specification review but it must be completed prior to the PDR. It is strongly recommended that these plans be reviewed and approved prior to the actual PDR to avoid the possibility of failing the PDR and thus delaying the fabrication or construction of the prototype parts,

13.5 Quality Control to Validate Reliability Specifications during Production

Describe what stress tests will be applied during production, possibly on a sampling basis, to validate the reliability of production units. These could likely be destructive tests. Specify the required sampling percentage of production units.

It is not required to complete this section prior to the first specification review but it must be completed prior to the FDR. It is strongly recommended that these plans be reviewed and approved prior to the actual FDR to avoid the possibility of failing the FDR and thus delaying the fabrication or construction of the pre-production parts,

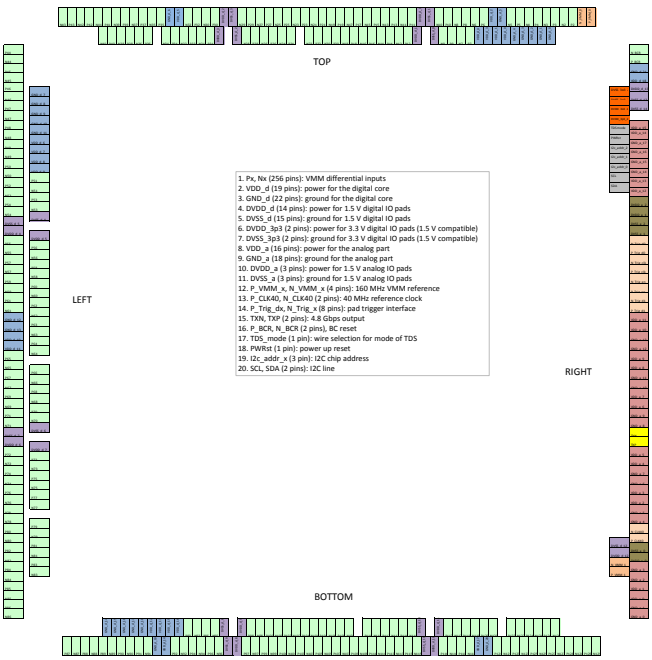
14 References

[1]. IEEE Standard for Ethernet, Section Four, IEEE Standard 802.3, 2012

[2]. Ryan Edgar, available via: https://indico.cern.ch/event/433775/#preview:1628709

[3]. F. Faccio, G. Cervelli, “Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors”, *IEEE Trans. On Nuclear Sci.* vol. 50, no. 6, pp. *2413*-2420, Dec. 2005

Bonding pads for the 2nd TDS prototype



I2C addr.	R/W	Size (byte)	Memory addr.	Bit Map
0	R/W	4	bit[31 : 0]	[31 : 20] BCID offset; [19 : 8] BCID rollover value; [7 : 4] BC clock phase, 6.25 ns step; 0 deg: 4'b0011; 90 deg : 4'b0110; 180 deg: 4'b1100; 270 deg: 4'b1001 [3 : 0] strip TDS matching window, from 25 ns to 50 ns, 6.25 ns step. 25 ns : 4'b0000; 31.25 ns: 4'b0001; 37.5 ns: 4'b0011; 43.75 ns: 4'b0111; 50 ns: 4'b1111;
1	R/W	2	bit[47 : 32]	[47 : 43] Phase of 160 MHz to VMM #1 [42 : 38] Phase of 160 MHz to VMM #0 [37 : 34] GBT SER PLL current set [33 : 32] GBT SER PLL low-pass filter resistor set
2	R/W	16	bit[175: 48]	[175: 48] disable set for channel #127-0 (MSB-LSB)
3	R/W	16	bit[303:176]	[190:176] strip TDS trigger road LUT 0 [206:192] strip TDS trigger road LUT 1 [222:208] strip TDS trigger road LUT 2 [238:224] strip TDS trigger road LUT 3 [254:240] strip TDS trigger road LUT 4 [270:256] strip TDS trigger road LUT 5 [286:272] strip TDS trigger road LUT 6 [302:288] strip TDS trigger road LUT 7
4	R/W	16	bit[431:304]	[318:304] strip TDS trigger road LUT 8 [334:320] strip TDS trigger road LUT 9 [350:336] strip TDS trigger road LUT a [366:352] strip TDS trigger road LUT b [382:368] strip TDS trigger road LUT c [398:384] strip TDS trigger road LUT d [414:400] strip TDS trigger road LUT e [430:416] strip TDS trigger road LUT f
5	R/W	16	bit[559:432]	[436: 432] delay for pad chnl #0 [444: 440] delay for pad chnl #1 [452: 448] delay for pad chnl #2 [460: 456] delay for pad chnl #3 [468: 464] delay for pad chnl #4 [476: 472] delay for pad chnl #5 [484: 480] delay for pad chnl #6 [492: 488] delay for pad chnl #7 [500: 496] delay for pad chnl #8 [508: 504] delay for pad chnl #9 [516: 512] delay for pad chnl #10 [524: 520] delay for pad chnl #11 [532: 528] delay for pad chnl #12 [540: 536] delay for pad chnl #13

				[548: 544] delay for pad chnl #14 [556: 552] delay for pad chnl #15
6	R/W	16	bit[687:560]	[564: 560] delay for pad chnl #16 [572: 568] delay for pad chnl #17 [580: 576] delay for pad chnl #18 [588: 584] delay for pad chnl #19 [596: 592] delay for pad chnl #20 [604: 600] delay for pad chnl #21 [612: 608] delay for pad chnl #22 [620: 616] delay for pad chnl #23 [628: 624] delay for pad chnl #24 [636: 632] delay for pad chnl #25 [644: 640] delay for pad chnl #26 [652: 648] delay for pad chnl #27 [660: 656] delay for pad chnl #28 [668: 664] delay for pad chnl #29 [676: 672] delay for pad chnl #30 [684: 680] delay for pad chnl #31
7	R/W	16	bit[815:688]	[692: 688] delay for pad chnl #32 [700: 696] delay for pad chnl #33 [708: 704] delay for pad chnl #34 [716: 712] delay for pad chnl #35 [724: 720] delay for pad chnl #36 [732: 728] delay for pad chnl #37 [740: 736] delay for pad chnl #38 [748: 744] delay for pad chnl #39 [756: 752] delay for pad chnl #40 [764: 760] delay for pad chnl #41 [772: 768] delay for pad chnl #42 [780: 776] delay for pad chnl #43 [788: 784] delay for pad chnl #44 [796: 792] delay for pad chnl #45 [804: 800] delay for pad chnl #46 [812: 808] delay for pad chnl #47
8	R/W	16	bit[943:816]	[820: 816] delay for pad chnl #48 [828: 824] delay for pad chnl #49 [836: 832] delay for pad chnl #50 [844: 840] delay for pad chnl #51 [852: 848] delay for pad chnl #52 [860: 856] delay for pad chnl #53 [868: 864] delay for pad chnl #54 [876: 872] delay for pad chnl #55 [884: 880] delay for pad chnl #56 [892: 888] delay for pad chnl #57 [900: 896] delay for pad chnl #58 [908: 904] delay for pad chnl #59 [916: 912] delay for pad chnl #60 [924: 920] delay for pad chnl #61

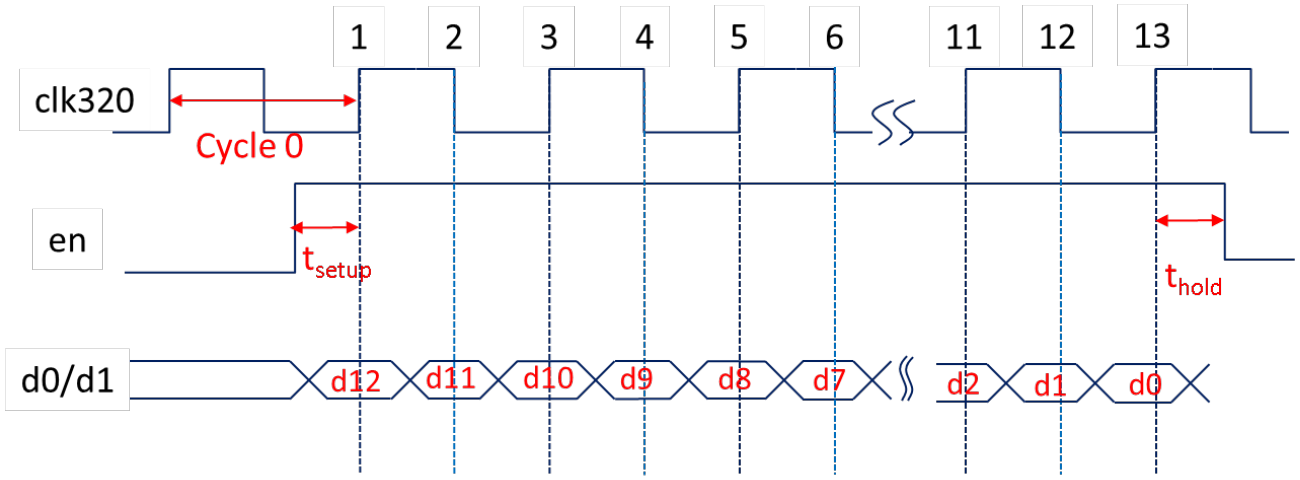
				[932: 928] delay for pad chnl #62 [940: 936] delay for pad chnl #63
9	R/W	16	bit[1071:944]	[948: 944] delay for pad chnl #64 [956: 952] delay for pad chnl #65 [964: 960] delay for pad chnl #66 [972: 968] delay for pad chnl #67 [980: 976] delay for pad chnl #68 [988: 984] delay for pad chnl #69 [996: 992] delay for pad chnl #70 [1004:1000] delay for pad chnl #71 [1012:1008] delay for pad chnl #72 [1020:1016] delay for pad chnl #73 [1028:1024] delay for pad chnl #74 [1036:1032] delay for pad chnl #75 [1044:1040] delay for pad chnl #76 [1052:1048] delay for pad chnl #77 [1060:1056] delay for pad chnl #78 [1068:1064] delay for pad chnl #79
10	R/W	16	bit[1199:1072]	[1076:1072] delay for pad chnl #80 [1084:1080] delay for pad chnl #81 [1092:1088] delay for pad chnl #82 [1100:1096] delay for pad chnl #83 [1108:1104] delay for pad chnl #84 [1116:1112] delay for pad chnl #85 [1124:1120] delay for pad chnl #86 [1132:1128] delay for pad chnl #87 [1140:1136] delay for pad chnl #88 [1148:1144] delay for pad chnl #89 [1156:1152] delay for pad chnl #90 [1164:1160] delay for pad chnl #91 [1172:1168] delay for pad chnl #92 [1180:1176] delay for pad chnl #93 [1188:1184] delay for pad chnl #94 [1196:1192] delay for pad chnl #95
11	R/W	8	bit[1263:1200]	[1204:1200] delay for pad chnl #96 [1212:1208] delay for pad chnl #97 [1220:1216] delay for pad chnl #98 [1228:1224] delay for pad chnl #99 [1236:1232] delay for pad chnl #100 [1244:1240] delay for pad chnl #101 [1252:1248] delay for pad chnl #102 [1260:1256] delay for pad chnl #103
12	R/W	4	bit[1295:1264]	[1271:1264] reset SER if equals 0x14 reset logic if equals 0x06 reset ePLL if equals 0x20 [1276:1272] {bypass_trigger, bypass_scrambler, test_frame2Router_enable, stripTDS_globaltest, PRBS_en }

				[1283:1280] prompt circuit: b3 :b0 [1287:1284] bypass prompt if equals 0xF [1295:1288] timer
13	R	16		8-bit CRC polynomial 0x97 for a total of 1296 bits [7 : 0] 8-bit CRC of memory bits [80: 0] [15 : 8] 8-bit CRC of memory bits [161: 81] [23 : 16] 8-bit CRC of memory bits [242: 162] [31 : 24] 8-bit CRC of memory bits [323: 243] [39 : 32] 8-bit CRC of memory bits [404: 324] [47 : 40] 8-bit CRC of memory bits [485: 405] [55 : 48] 8-bit CRC of memory bits [566: 486] [63 : 56] 8-bit CRC of memory bits [647: 567] [71 : 64] 8-bit CRC of memory bits [728: 648] [79 : 72] 8-bit CRC of memory bits [809: 729] [87 : 80] 8-bit CRC of memory bits [890: 810] [95 : 88] 8-bit CRC of memory bits [971: 891] [103: 96] 8-bit CRC of memory bits [1052: 972] [111:104] 8-bit CRC of memory bits [1133:1053] [119:112] 8-bit CRC of memory bits [1214:1134] [127:120] 8-bit CRC of memory bits [1295:1215]
14	R	6		[1 : 0] lock of SER (MSB), lock of ePLL (LSB) [26: 8] monitoring of strip TDS channel #0 [46:28] monitoring of strip TDS channel #64
15	R	4		[12: 0] strip TDS trigger BAND and Phi ID [27:16] strip TDS trigger BCID

Interface between pad-trigger logic and the strip-TDS

- Source synchronization with a DDR clock (clk320 MHz) and data enable (en);
- Data line (d0 and d1) rate is: 640 Mbps;
- d0 is for BCID (12 bits), d1 is for Band-phi ID (13 bits), MSB coming out first.

The timing diagram of the protocol is shown as follows:



BCID: d[12:1]; Band_phi_ID: d[12:0]

For the above timing diagram:

1) The first bit is captured at rising edge of clk320 after “en” becomes valid.
2) A total of 13 bits (d[12:0]) will be captured via dual edges of clk320.
3) There is flexibility on width of “en”: “en” can starts valid at any time in “Cycle 0” as long as the setup time (t_{setup}) is meet; “en” can also extend until the rising edge following edge 13, but it should stay valid for at least the time of t_{hold}.

The interface inside TDS will capture the corresponding BCID and Band-phi ID from the two lines, and output this information with a trigger request.