ATCA platform certification for NSW Trigger Processor

Preliminary -

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1. General

In general terms, all necessary I/O data paths must be tested and verified in hardware as well as configuration and ATCA management functionality. This includes testing all data paths for ancillary functions, TTC, monitoring, and optical i/o for interfacing to detector data and sector logic[1]. Another critical aspect of the hardware testing is temperature tests at a representative power load. Full trigger algorithm implementation is not the scope of the initial board test, however, emulating the power consumption of the final application, as realistic as possible, is important to characterize the system thermal characteristics. It is not necessary that all functions performed in firmware need to be tested and verified in hardware. In many cases, it will be sufficient to estimate the resources required for some functionality in order to verify that the FPGA resources are sufficient. If it appears that the FPGA resources will come close to being fully utilized, then detailed implementation must be done.

2. Test-stand Hardware Infrastructure

2.1 Powered ATCA Crate

Details on Crate here

2.2 Shelf Manager

Details

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2.3 Rear Transition Module

Can we use the Stoneybrook RTM for both LAr carrier and SRS?

Does Sorin have a RTM we can use for testing?

2.4 ATCA based Ethernet Switch - ??

Do we need a switch blade?

2.5 AMC Optical Front End Emulator (Xilinx Eval Board)- ??

Not needed if we use a loopback method

2.6 Anything else - ??

3. Hardware Tests

These tests are listed in order from lowest level to highest level in terms of functionality. All described functionality must be fully tested and verified.

3.1 Smoke test

3.1.1 Tests

- Power up test to insure all power supply voltages on Carrier and Mezzanine are correct. Power supply currents should be measured.

3.2 IPMC / MMC Management and Monitoring.

3.2.1 Tests

- Carrier and AMC power on/off through IPMC/MMC
- JTAG connectivity from IPMC to carrier and AMC
- e-keying with real port descriptors for carrier/IPMC and AMC/MMC
- Carrier sensor read out.

3.2.2 LAr Notes

The ATLAS/LAPP IPMC software will probably not support the AMC MMC e-keying by June. We will bypass this with on board jumpers on the LAr carrier for v1.

3.2.3 SRS Notes

The SRS team will focus on implementing the specific panel development in ATLAS DCS System (WinCC) fwATCA framework. Until that is being done, web-based shelf-manager communication may be used instead.

IPMC / MMC can perform power-up/down, FPGA reboot, carrier and mezzanine sensor readout, FPGA IPMI extension (access to Virtex-7 XADC/Sys Monitor for temperature and internal voltage sensing, access to microPods I2C sensors, etc. – pending firmware implementation)

3.3 Clock network / Jitter-cleaner.

3.3.1 Tests

- Eyescans of all high speed (XAUI, GBT) channels in parallel at the design frequency and as high as we can go up to roughly 10.3 Gbps.
- Test the clock recovery from the optical links and local cleaning through the PLLs using a GBT implementation and external GBT source .

3.4 FPGA Configuration

The main FPGA configuration is done through the IPMC in the Shelf Manager and produces a JTAG stream to configure the Carrier's FPGA. The Carrier then passes JTAG configuration data to the FPGAs on the Mezzanine cards.

3.4.1 Tests

- Configuration using the dedicated JTAG connector
- Configuration using IPMC Ethernet (to be used in situ in USA-15)
- FPGA power-up configuration from BPI flash.

3.4.2 LAr Notes

Software for IPMC Ethernet configuration may not be ready by June. Also, no shelf manager/backplane combinations which support JTAG connectivity to any blade slots have been found.

3.4.3 SRS Notes

On the SRS carrier, the JTAG passes through a small (Spartan6) FPGA which is connected to the carrier IPMC, as well as the two carrier FPGAs,

therefore JTAG configuration can be performed either via IPMC (via Base Ethernet link) or via an RTM Ethernet connection (bypassing IPMC). In both cases, firmware and software need to be developed.

3.5 SDRAM

Both hardware options will include SDRAM on the ATCA carrier board. This is currently not a requirement of the Trigger Processor however it may be utilized as the design progresses.

3.5.1 Tests

- Verify operation of the SDRAM on the ATCA carrier

3.5.2 SRS Notes

The SRS Carrier has been tested with 2GByte SO-DIMM DDR3 RAM

3.6 Blade-to-blade communication

Blade-to-blade communication is not a requirement of the Trigger Processor

3.6.1 LAr Notes

LAr has no blade-to-blade communication, except through the XAUI or GbE hub switch

3.6.2 SRS Notes

The SRS Carrier includes LVDS(52) and GTx(4) through full mesh backplane which will be tested.

3.7 Rear transition module

It is not a Trigger Processor requirement to have communication through the rear transition module, however the available signals could be used as the connection to FELIX and also provide Ethernet communication.

3.7.1 Tests

- IBERT on all available SFP connections on the rear transition module up to the limit of carrier FPGA (5-6Gbps)

3.7.2 LAr Notes

LAr carrier has 8 SFP/GBT in v1, but this will be reduced to 5 in v2 and beyond. It also has one more SFP/GbE on the RTM for all versions. (For v1, it will also have a dedicated RJ45 to the IPMC.)

3.7.3 SRS Notes

The SRS carrier has 16 GTH signals through the rear transition module. These SFP connections are typically being used for 1Gb Ethernet or 10GbEthernet (XAUI).

3.8 Lateral sTGC and MM communication

In order to merge track candidates found by the MM and sTGC algorithms, it is a Trigger Processor requirement to have communication between the MM FPGA and sTGC FPGA. With 22 bits per track candidate, and a possible 8 candidates per bunch crossing the throughput requirement for this lateral communication is 4.4 Gbs

3.8.1 Tests

- Test all signals that are to be used for lateral communication. These should be checked in both directions and their data rate vs BERR should be measured. Maximum bit rate per LVDS line should be established and verified to meet the Trigger Processor requirements.

3.8.2 LAr Notes

On the LAr AMC, the sTGC FPGA and MM FPGA communicate through signals that pass through the carrier FPGA. There are currently 8 LVDS signals per AMC that could probably be increased to 16.

3.8.3 SRS Notes

On the SRS AMC, the sTGC FPGA and MM FPGA sit on the same PCB. There are 64 LVDS signals between them.

3.9 AMC to Carrier Communication

There is no Trigger Processor requirement for AMC to Carrier communication; however this could be used to move some of the ancillary functions from the AMC to the carrier card.

3.9.1 Tests

- Test all signals that are to be used for lateral communication. These should be checked in both directions and their data rate vs BERR should be measured. Maximum bit rate should be established.

3.9.2 LAr Notes

All of the AMC to carrier LVDS signals will be used for the lateral communication. There are 8 GTH/X connections: 4 XAUI, 3 "GBT" and 1 GbE that can be used for AMC to carrier communication. All are known to be functional.

3.9.3 SRS Notes

The SRS has 50 LVDS, and 8 GTH per mezzanine that can be used for AMC to carrier communication.

3.10 TTC and FELIX

The TTC and FELIX functionality will be verified as part of the clock / jitter cleaner tests. There is no need to use the FELIX protocol for this test.

3.11 AMC Optical I/O

For each Trigger Processor FPGA, it is a requirement to have 32 optical receivers for front-end data and 14 optical transmitters to sector logic. Additionally, one transceiver could be used as a connection to FELIX. These links will be configured to run at mixed speeds.

The tests may be conducted, for example, by looping outputs back to inputs and doing BERR testing on all available channels. Trigger algorithms are not needed for this test. The test could alternatively use a separate board to transmit and receive test data thus completely decoupling the device under test from the test-stand emulator.

3.11.1 Tests

- Test all available links up to 10 Gbs
- Test at a mixed speed configuration emulating the use in experiment (32 downlinks at 4.8/5.5-6 Gbps (MM/sTGC case), 14 uplinks at 6.4 Gbps(?) (Sector Logic) and 4 duplex 4.8Gbps (FELIX))

3.11.2 LAr Notes

The LAr AMCs have 48 transceivers that have been tested to 10 Gbps.

3.11.3 SRS Notes

The SRS AMC includes 36 transceivers.

3.12 ATCA Thermal Testing

A critical aspect of the hardware testing is temperature tests at high power load. Full trigger algorithm implementation is not the scope of the initial board test. However, emulating the power consumption of the final application, as realistic as possible, is an interesting case from the point of view of heat dissipation and power supply stress.

3.12.1 Tests

- Monitor temperature and link errors with the AMC in a simulated environment. The FPGA should be configured with a 'power equivalent' implementation along with a representation of the expected optical link requirement (32 downlinks at 4.8/5.5-6 Gbps (MM/sTGC case), 14 uplinks at 6.4 Gbps(?) (Sector Logic) and 4 duplex 4.8Gbps (FELIX)). The crate configuration and cooling should also be representative of the final design.

3.12.2 LAr Notes

For the LAr-based cards, we plan to run all 48 AMC microPod channels, the XAUI links and the GBT links at expected frequencies, along with some logic processing to be defined (probably eyescan and microblaze). There are temperature sensors in the Xilinx chips and the microPods and we have on board I2C temperature and current monitors on the carrier.