Trigger Processor Implementation

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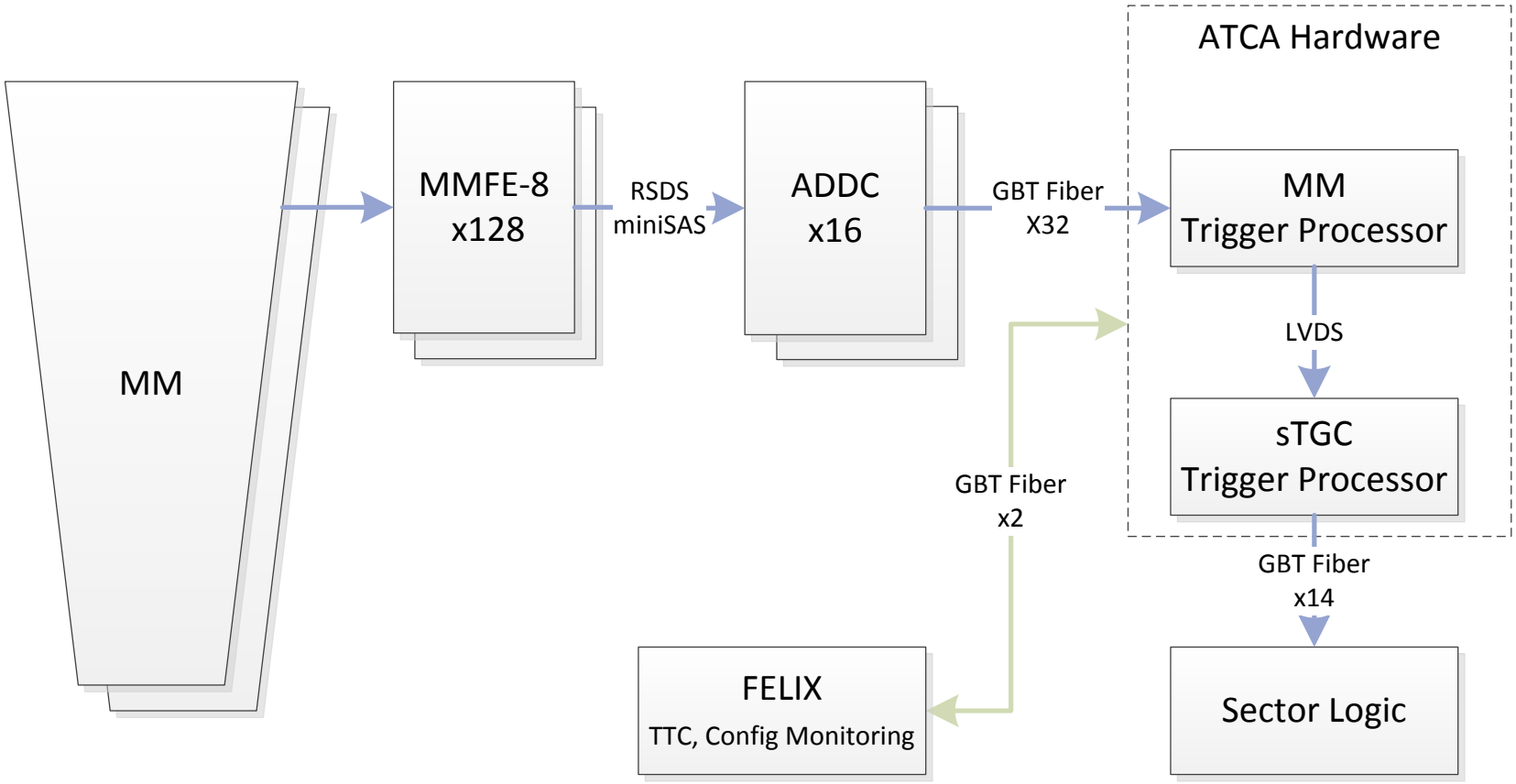
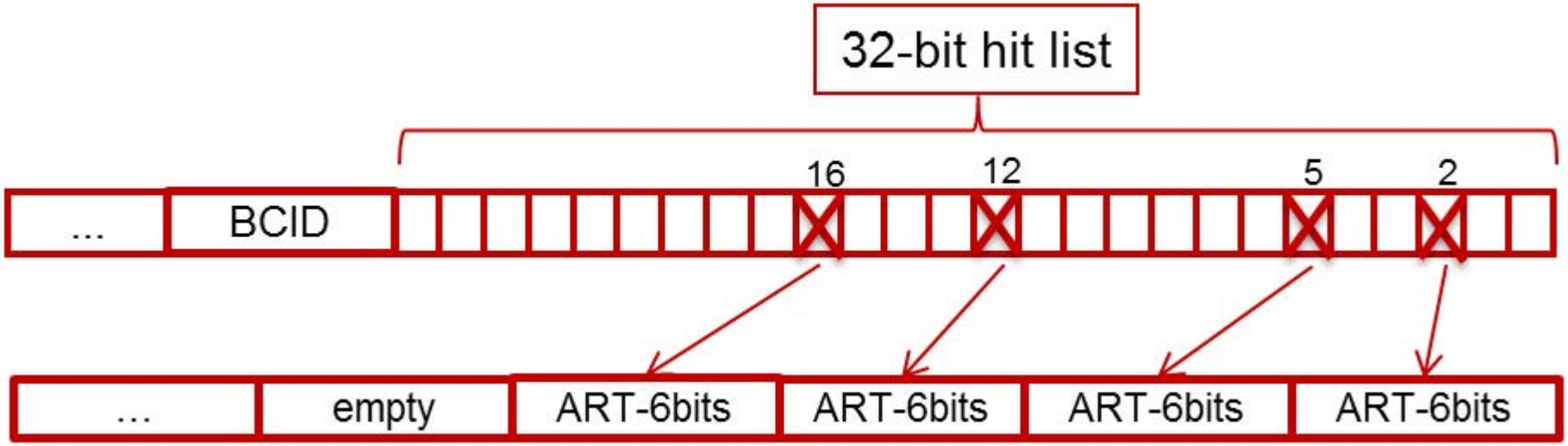
ART Data/Trigger Processor Overview

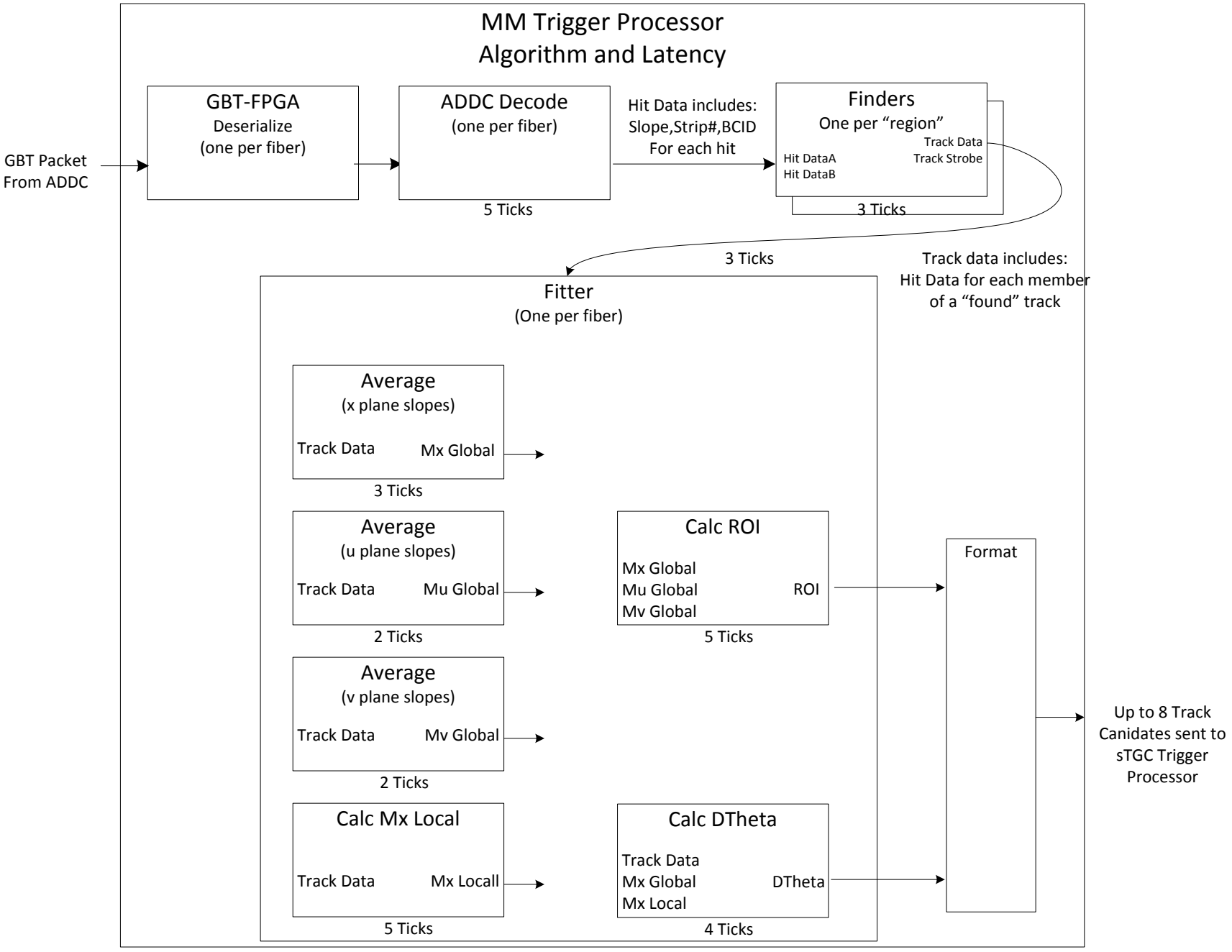


ADDC GBT Data Packet

- Each ADDC will service 2 sets of 32 VMMs and have 2 fiber outputs using the GigaBit Transceiver (GBT) architecture. One fiber per 32 VMMs
- The GBT packet in widebus mode will provide 112 data bits at a rate of 4.8 Gbs and arrives once every bunch crossing
  - HIT_CNT = 4-bit number of hits (range 0 - 8; 9 - 15 invalid)
  - ART_DATA = 6-bit triggered VMM strip number
  - ARTDATA_PARITY = 8-bit parity, one per hit
  - HIT_LIST= The triggered state of each of the 32 VMMs will be represented as a single bit in this 32-bit field.

ADDC GBT Data Packet



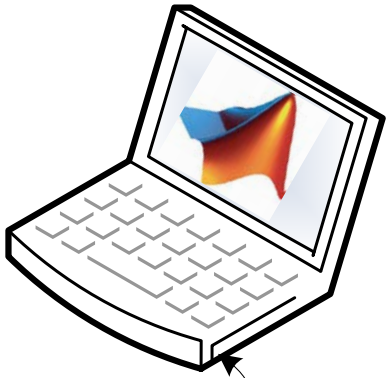


Algorithm Critical path total 20 clock ticks

Implementation

- 320 MHz Internal Clock
- 1/16th sector slice, containing all elements of algorithm implemented
- Modelsim used for simulation
- Xilinx Vivado 14.4 used for synthesis and PAR
- No timing errors in algorithm
- Extrapolated resource estimate
  - 70% targeting a ‘485
  - 50% targeting a ‘690.
- Source code on SVN

Development Platform



GBT Protocol Optical Loopback
ADDC ART Data Format
x2

Microblaze Soft Processor

Ethernet
ttyUSB

AXI Master

AXI

ADDC Emulator

AXI Slave

ADDC
ART Data

Configuration and Monitoring

AXI Slave

Monitoring

GBT FPGA
(HDL)

ADDC
ART Data

ADDC
ART Data

Bypass

Trigger Processor

ADDC
ART Data

Track Canidates
Debug Data

VC707 Virtex 7 FPGA
(XC7VX485T)

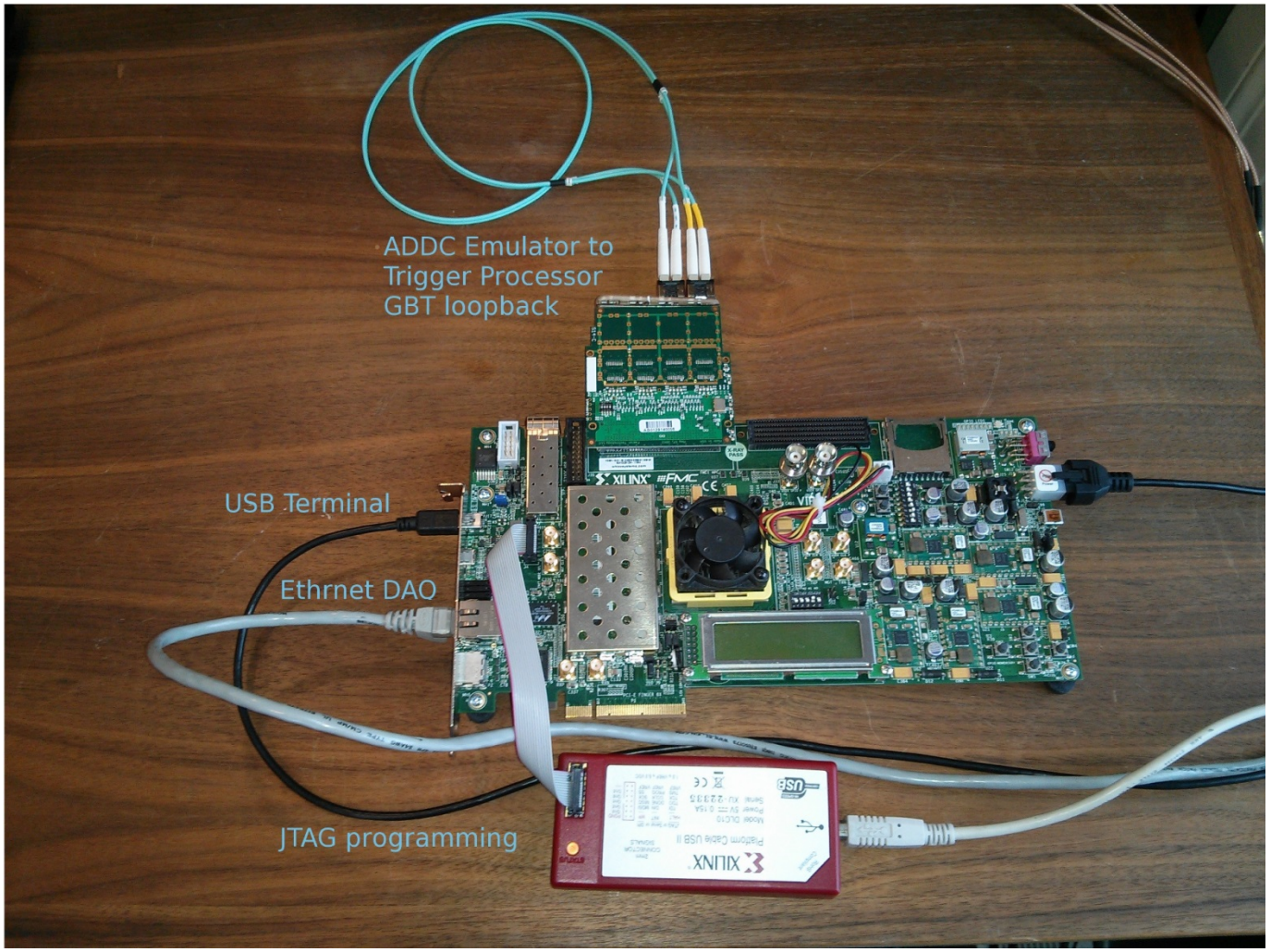
Development Platform

- Matlab used for all data formatting, communication and analysis
- Communication uses TCP/IP on Mircroblaze with AXI interface to Programmable Logic
- ADDC Emulator
  - Generates GBT packets from track data files
  - Currently lives in Trigger Processor FPGA
- GBT Loopback
  - Option to bypass
  - Implementation uses code from the CERN GBT-FPGA project

Development Platform

- Algorithm hardware results comparable to computer simulation
  - Currently working on increasing the bit resolution of some variables, This will likely increase latency by 6 – 9 ns
- Initial data communication with BNL ADDC verified

Development Platform

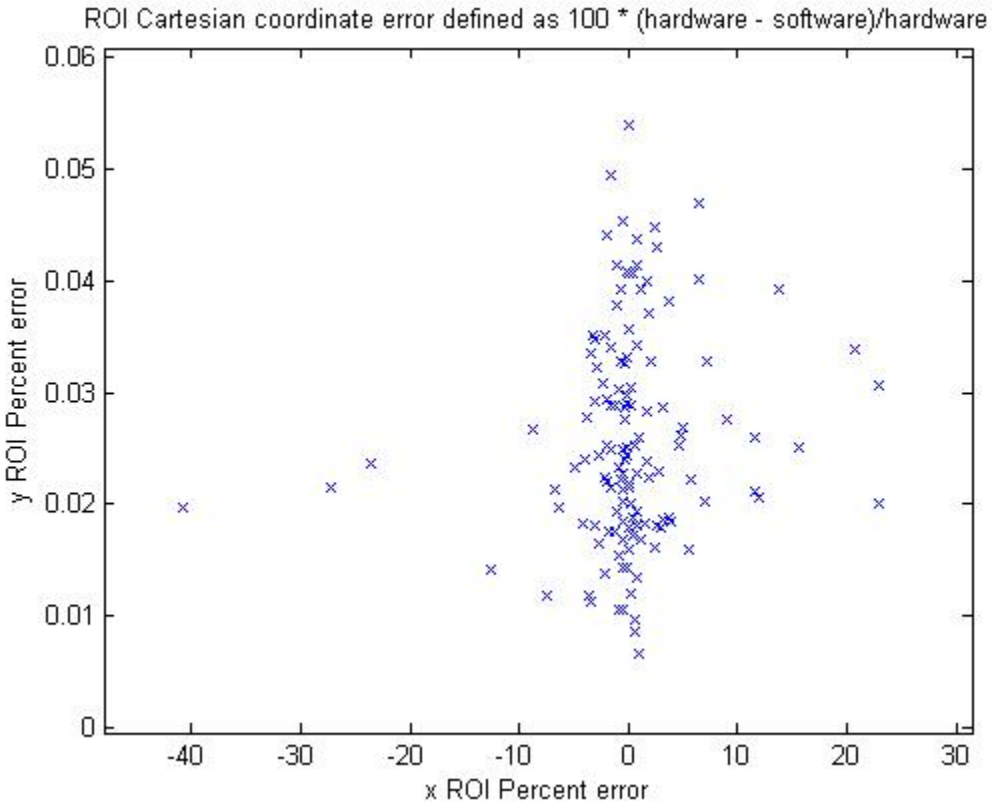


Ancillary functions

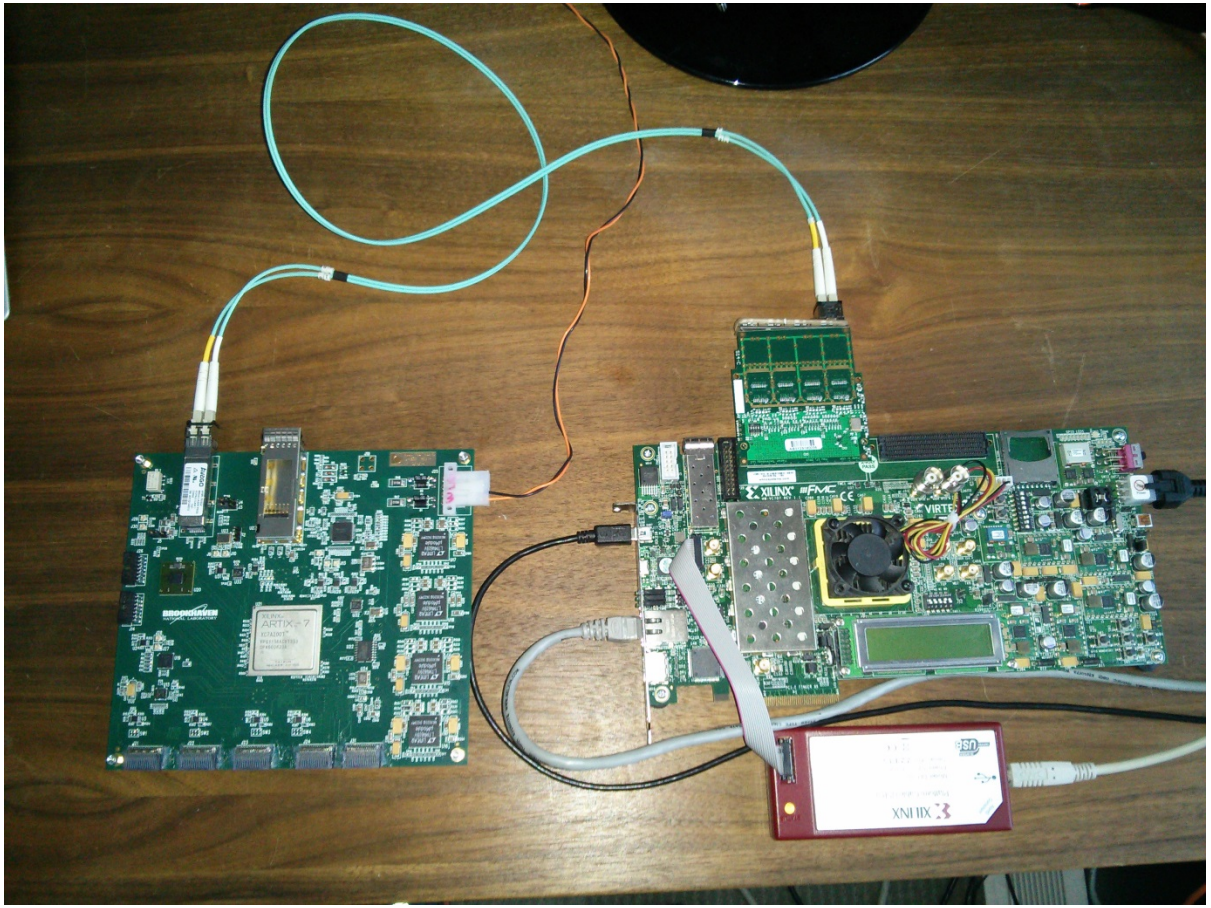
- Ancillary functions common to both MM and sTGC can be shared as well-defined packages.
- Ancillary functions Include
  - Timing and Trigger control (TTC)
  - Level-1 pipeline and derandomizer
  - read/write of configuration parameters
  - monitoring
  - playback for debugging
  - Segment output to Sector Logic
  - Segment output to "other" detector's trigger processor
- Three groups will participate in writing the firmware:
  - Harvard
  - Illinois
  - Weizmann

Backup

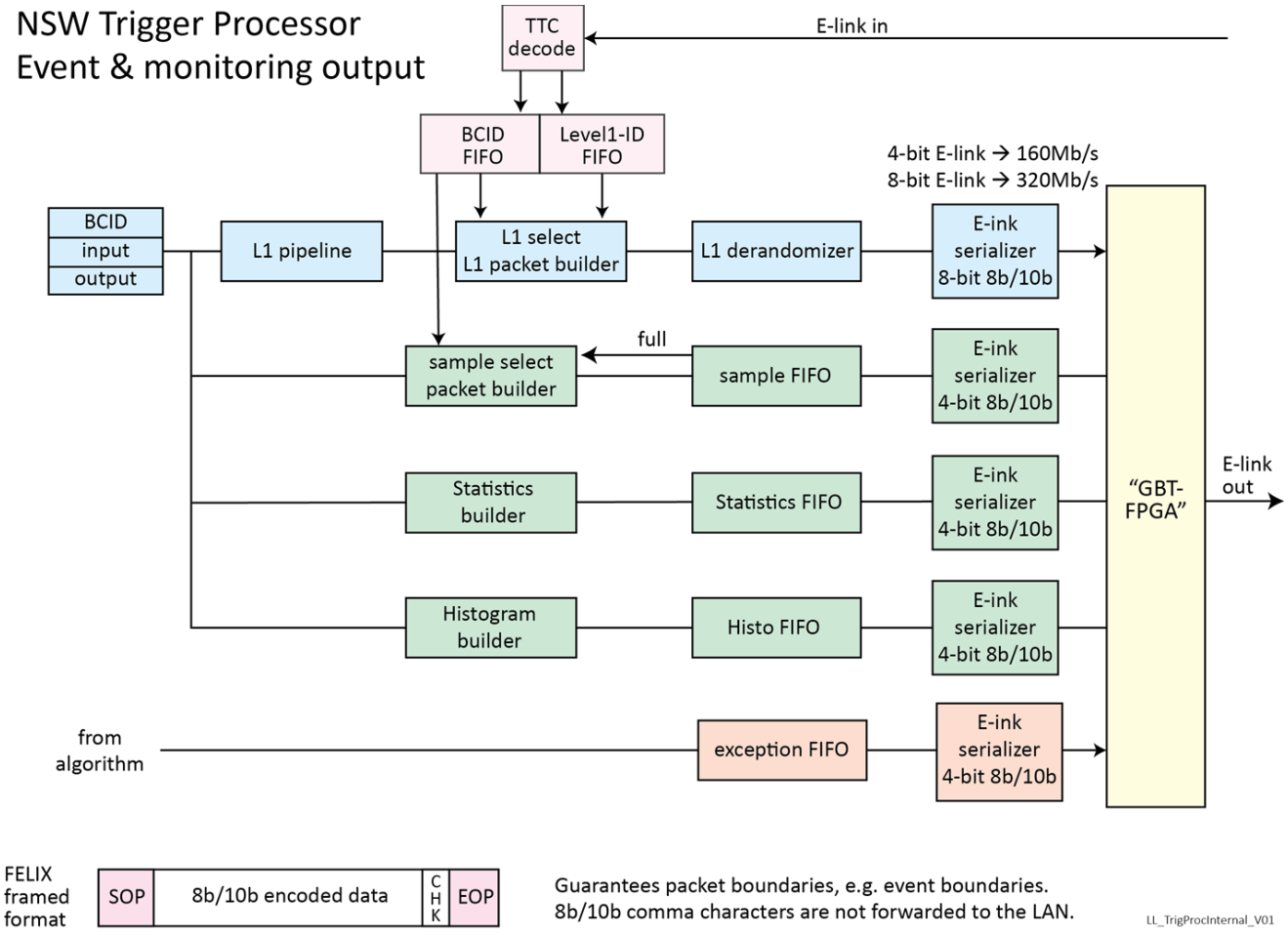
Hardware / Software Example Comparisons



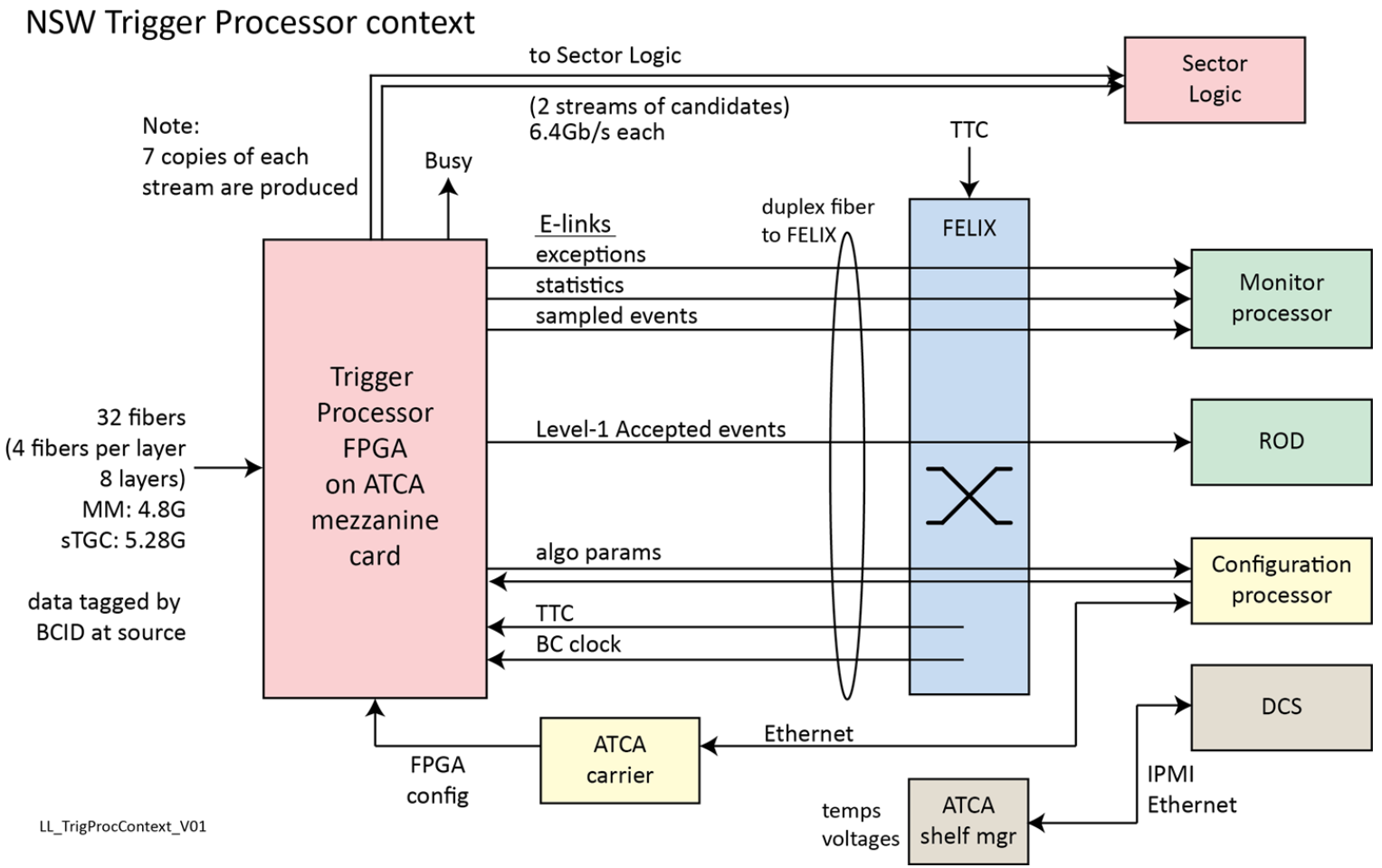
Trigger Processor with ADDC



Monitoring Functions



Data Path


NSW Trigger Processor context
to Sector Logic
Sector Logic
(2 streams of candidates)
6.4Gb/s each
Note:
7 copies of each
stream are produced
Busy
TTC
duplex fiber
to FELIX
FELIX
E-links
exceptions
statistics
sampled events
Monitor processor
Trigger Processor FPGA on ATCA mezzanine card
32 fibers
(4 fibers per layer
8 layers)
MM: 4.8G
sTGC: 5.28G
data tagged by
BCID at source
Level-1 Accepted events
ROD
algo params
Configuration processor
TTC
BC clock
DCS
Ethernet
ATCA carrier
FPGA config
IPMI Ethernet
temps
voltages
ATCA shelf mgr
LL_TrigProcContext_V01