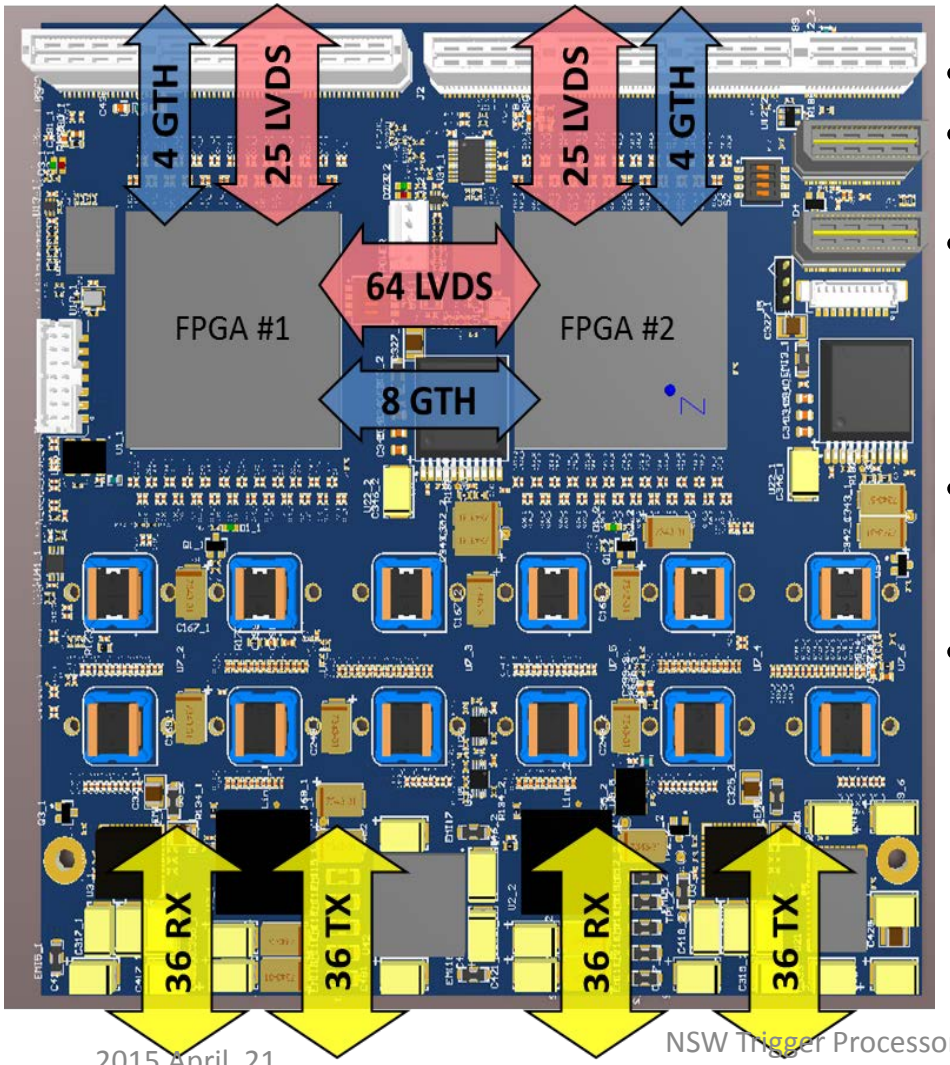
NSW Trigger Processor Hardware Platform Test Plans and Status

2015, April 21

Nathan Felt, Sorin Martoiu

High Density Optical Mezzanine for ATCA-SRS

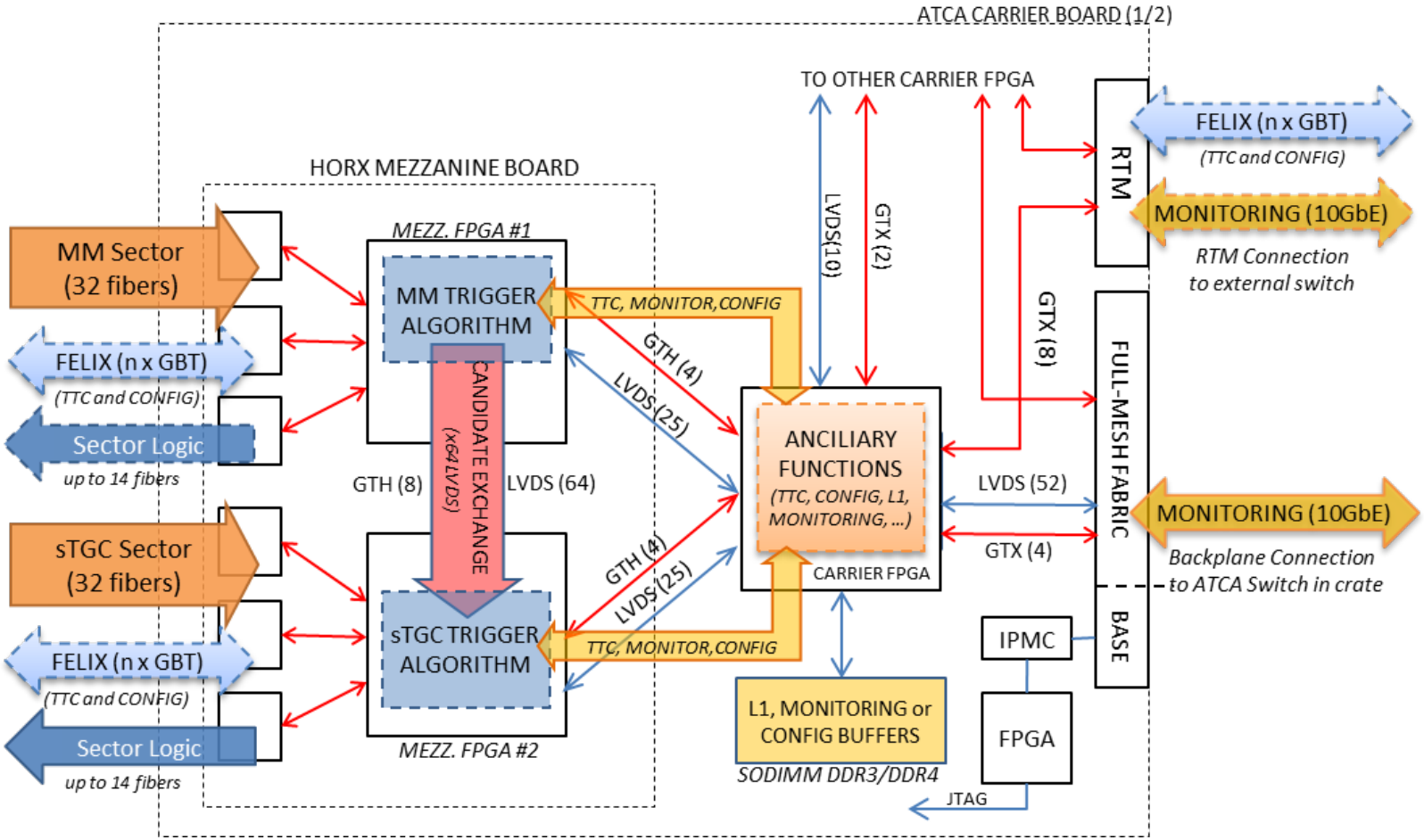


- Dimensions: 145mm x 146 mm
- FPGA: 2 x Virtex-7 (415T, 485T, 550T, 690T)
- Front-End:
  - 72 RX + 72 TX Optical Fibers (36/36 each FPGA)
  - 12 x Avago MicroPod modules (up to 12.5Gbps)
- Inter-FPGA interface
  - 64 LVDS inter-FPGA
  - 8 GTH inter-FPGA
- Carrier interface:
  - 50 LVDS to blade
  - 8 GTH to blade
  - Separate System and GTH clocks
  - Power (12V) and management (IPMI, JTAG)

Trigger Processor
ATCA Hardware Testing

- Housekeeping
  - Power, Configuration, Monitoring
- Communication
  - GTH, LVDS
- Environment
  - Thermal testing

ATCA-SRS Carrier /AMC as a Trigger Processor



Housekeeping

- Carrier and AMC power on/off through IPMC/MMC
- e-keying with real port descriptors for carrier/IPMC and AMC/MMC
- Carrier sensor read out.
- Configuration
  - Remote and local JTAG configuration
  - FLASH Programming and power-up configuration

Communication
Rear Transition Module

A RTM is not a Trigger Processor requirement, however could be used as the connection to FELIX and also provide Ethernet communication.

- BERT on all available SFP connections on the rear transition module up to the limit of carrier FPGA (5-6Gbps)

Communication
Lateral sTGC - MM

In order to merge track candidates found by the MM and sTGC algorithms, it is a Trigger Processor requirement to have communication between the MM FPGA and sTGC FPGA. The throughput requirement is 4.4 Gbs. The latency of the lateral communication may impact the total latency and should be considered.

- BERT on all LVDS lateral communication signals.

Communication
AMC to Carrier

There is no Trigger Processor requirement for AMC to Carrier communication, however this could be used to move some of the ancillary functions from the AMC to the carrier card.

- BERT on all signals from AMC FPGA to Carrier FPGA

Communication
AMC MicroPod Optical I/O

Each Trigger Processor FPGA is required to have 32 optical receivers for front-end data and 14 optical transmitters to sector logic. Additionally, one transceiver could be used as a connection to FELIX. These links will be configured to run at mixed speeds.

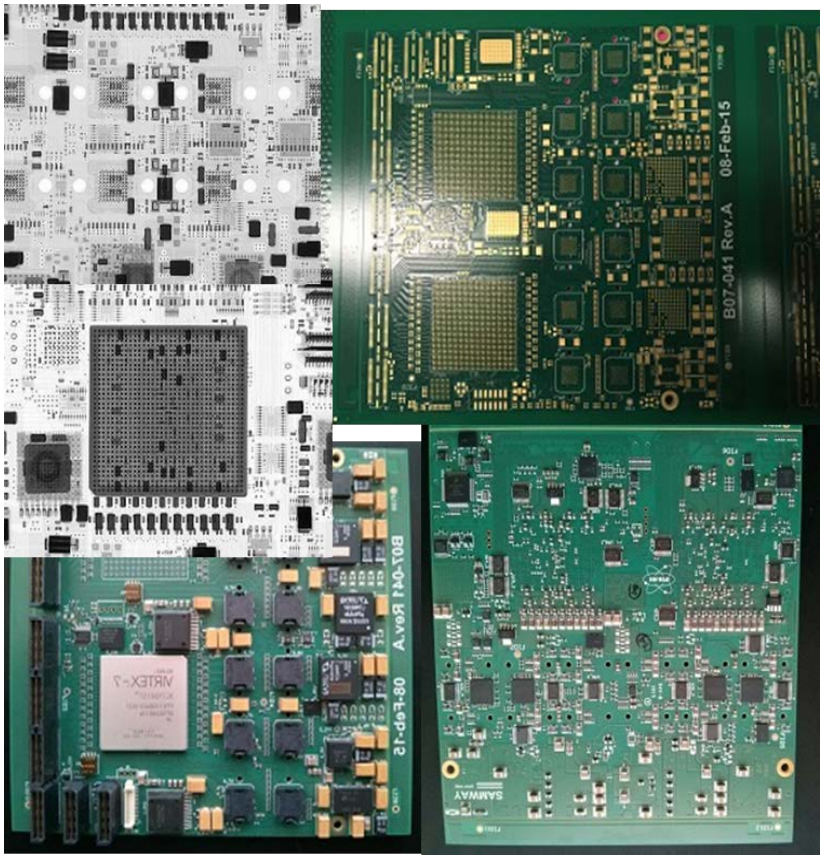
- Test all links up to 10 Gbs.
- Test microPod links at mixed speeds.

ATCA Thermal Testing

A critical aspect of the hardware testing is temperature tests at high power load. Full trigger algorithm implementation is not required but should include a power equivalent implementation.

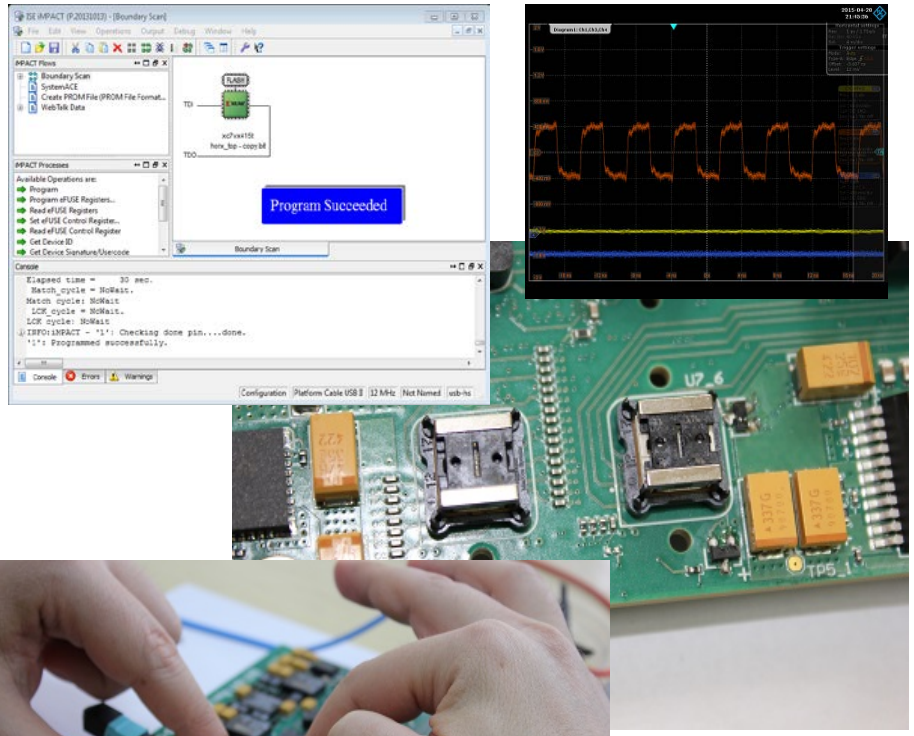
- Monitor temperature and link errors with the AMC in a worst case simulated environment.

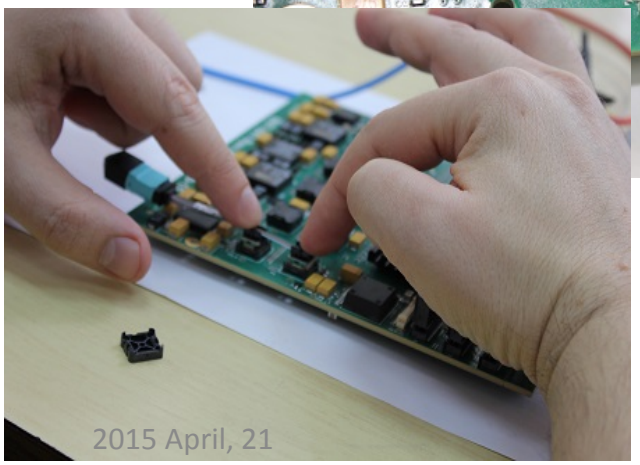
Prototype Production



- Prototype took longer than expected
- PCB was delayed and eventually produced by different manufacturer
- Assembly job went at the back of the queue (high volume order in front of us)
- No contingency plan here - wait more…
- Finally on our table last Friday

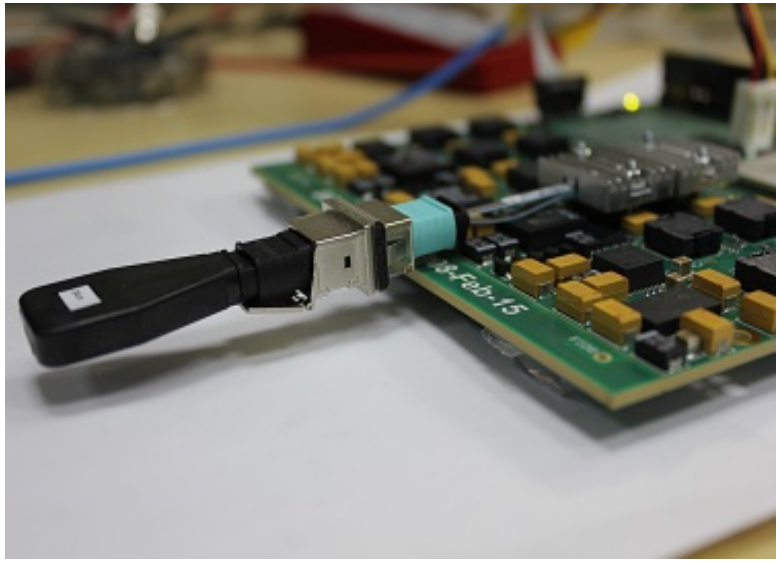
Prototype Setup and First Verifications





- ✓ All power rails were verified initially without load
- ✓ Verified JTAG access to FPGA
- ✓ Verified programming to and configuration from on-board BPI Flash
- ✓ Initial verification of clocks, PLLs, on-board I2C communication
- ✓ Installed first MicroPods on the board; verified if our custom heatsinks make enough pressure for good connectivity.

First Optical Tests



MGT/BERT Settings | DRP Settings | Port Settings | RX Margin Analysis

	GTH_X1Y16	GTH_X1Y17	GTH_X1Y18	GTH_X1Y19
MGT Settings				
MGT Alias	GTH0_118	GTH1_118	GTH2_118	GTH3_118
Tile Location	GTH_X1Y16	GTH_X1Y17	GTH_X1Y18	GTH_X1Y19
MGT Link Status	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps
PLL Status	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED
Loopback Mode	None	None	None	None
Channel Reset	Reset	Reset	Reset	Reset
TX/RX Reset	TX Reset / RX Reset	TX Reset / RX Reset	TX Reset / RX Reset	TX Reset / RX Reset
TX Polarity Invert	☑	☐	☐	☐
TX Error Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	250 mV (0000)	250 mV (0000)	250 mV (0000)	250 mV (0000)
TX Pre-Cursor	0.00 dB (00000)	0.00 dB (00000)	0.00 dB (00000)	0.00 dB (00000)
TX Post-Cursor	0.00 dB (00000)	0.00 dB (00000)	0.00 dB (00000)	0.00 dB (00000)
RX Polarity Invert	☐	☐	☐	☐
Termination Voltage	Programmable	Programmable	Programmable	Programmable
RX Common Mode	800 mV	800 mV	800 mV	800 mV
BERT Settings				
TX Data Pattern	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit
RX Data Pattern	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit
RX Bit Error Ratio	2,284E-014	2,284E-014	2,285E-014	2,285E-014
RX Received Bit Count	4,378E013	4,378E013	4,377E013	4,377E013
RX Bit Error Count	0,000E000	0,000E000	0,000E000	0,000E000
BERT Reset	Reset	Reset	Reset	Reset
Clocking Settings				
TXUSRCLK Freq (MHz)	312,56	312,56	312,56	312,56
TXUSRCLK2 Freq (MHz)	312,56	312,56	312,56	312,56
RXUSRCLK Freq (MHz)	312,56	312,56	312,56	312,56
RXUSRCLK2 Freq (MHz)	312,56	312,56	312,56	312,56

- First IBERT tests with optical loopback at 10Gbps are ok.
- We are setting up a testbench setup for covering a set of frequencies on all optical links