Stony Brook Update

1. Ethernet Test board
2. OTC V2
3. ATCA carrier

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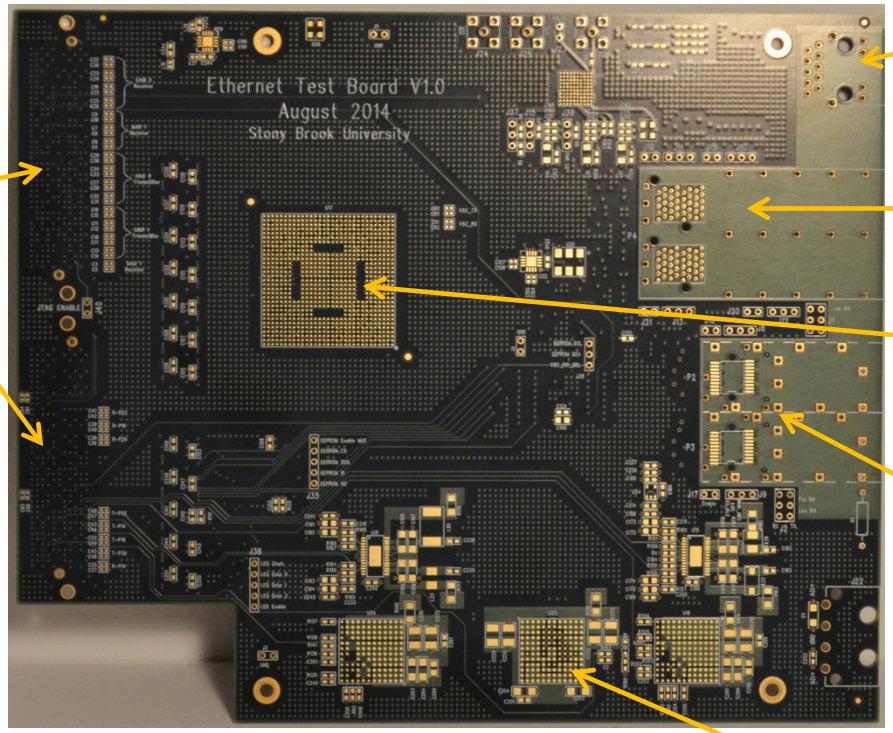
ETB progress

- test board for Ethernet (Intel FM2112/4112)
  - Layout completed; Board produced; being assembled



RJ45 (simulate IPMC connection)

FMC connections to Xilinx VC707 evaluation board:
4 x GbE to switch
2 x XAUI to switch
2 x GbE direct to SFP
2 x GbE in loopback
and control lines

2x2 SFP+ to switch

Intel FM2112/ 4112

2 SFP+ direct to VC707

Power Supplies

  - Begin testing in October

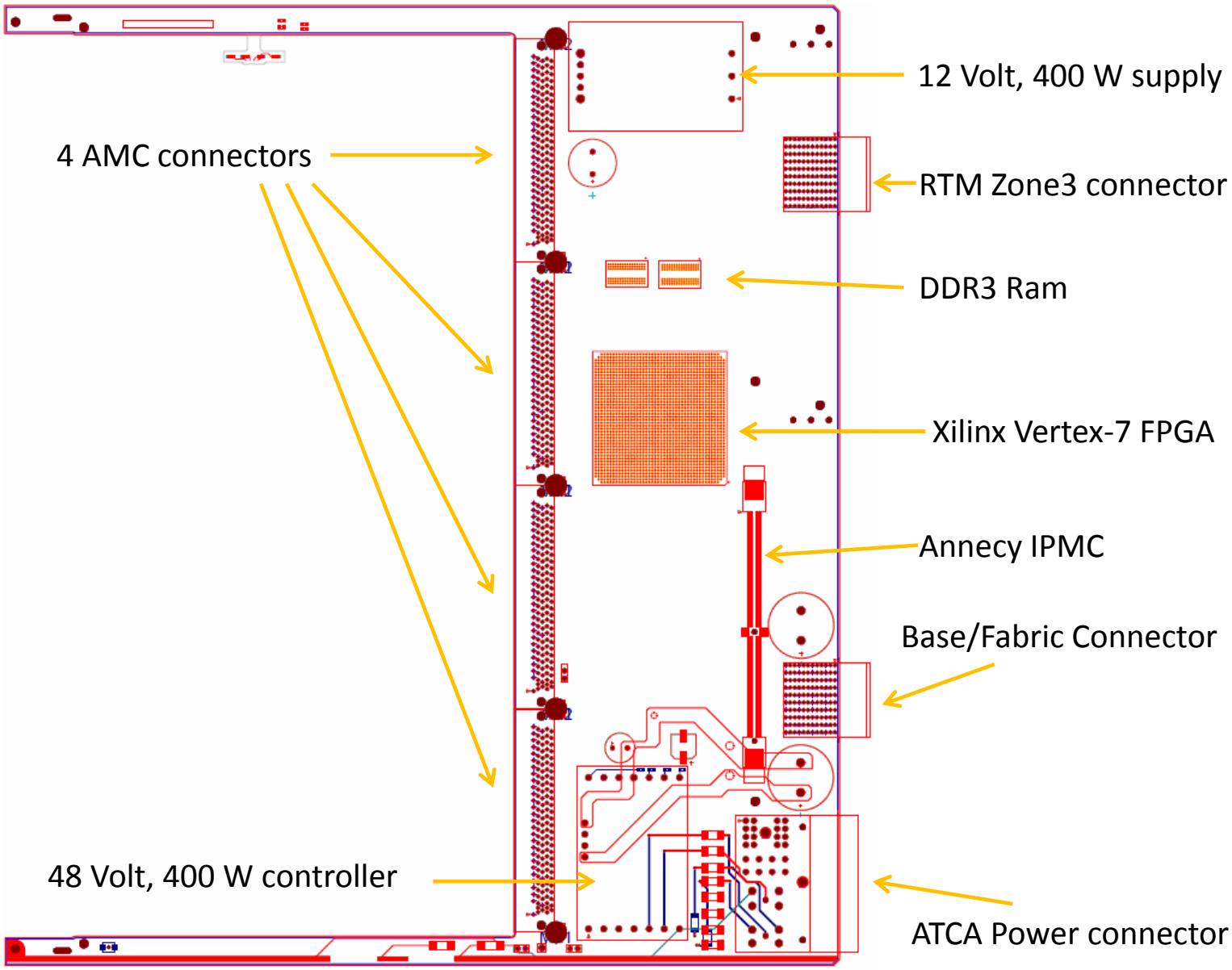
Version 2 Optical Test card

- 15 boards back from fabrication
- Parts for 10 boards available
- Assembly will start next week, with 2 week delivery

Version 1 ATCA Carrier card

- Schematic essentially complete
  - Includes the FPGA but not the Ethernet Switch
  - Have routed all Ethernet through the FPGA
  - Has full XAUI and GBT connections
  - Will require RTM for GBT SFP+ cages
  - Vitesse VSC8221 switch chip is possible backup to Intel
  - Schematics needs through review before starting layout in October
    - Expect about 3 months for board layout, fabricate and assembly
  - Add the switch once testing looks reasonable
    - Probably on RTM because of space limitations

ATCA initial parts layout – just starting



Connections planned for the V1 ATCA carrier

ATCA v1

4 identical AMC slots (next page)
2x GbE to Base interface, 1 GbE to RTM
2x XAUI to Fabric
4x (8x for layout tests) GBT to RTM

ATCA infrastructure (w/jumper bypass for testing)
Xilinx Virtex-7 485-1927 FPGA
    GbE (plan: v1 only then switch on RTM), XAUI, GBT

Clocks
    125 MHz GbE
    156.25 MHz (XAUI and also to AMC)
    40.079 MHz (oscillator)
    “ATLAS” recovered clock
  Last two clocks through a CDCM6208V2RGZT cleaner

ATCA to AMC Interface

AMC Port	Default	ATCA Src	Type
0	GbE	FPGA	Serial Tx/Rx
8-11	XAUI	FPGA	"
12	GBT	FPGA	"
13	GBT	FPGA	"
18	user	FPGA	LVDS 1.8 V
19	user	FPGA	"
20	user (GBT?)	FPGA	Serial Tx/Rx
FCLKA	ATLAS Clk	Cleaner	LVDS
TCLKA	156.25 MHz	Osc.	LVDS

The protocols on the serial tx/rx can be changed but clock reference frequencies have some constraints

Serial Tx/Rx are 100 Ω, decoupled on receiver side

LVDS is DC coupled, unterminated

RTM (v1)

- 4 x SFP for GBT
- 4 x SFP for GBT layout testing
- 1 x SFP for GbE

ATCA and RTM Documentation forthcoming