ATLAS NSW Electronics Specification
Component or Facility Name: ART ASIC

"Address in Real-Time" Concentrator ASIC

Version: V 1.1

Abstract

The ART ASIC is part of the trigger uplink path of the MicroMega chambers, part of the NSW detector. The ASIC receives the prompt "Address in Real-Time" (ART) data generated by 32 VMM front-end chips which consists of the address of the first arriving hit in each 64-channel front-end IC for a given bunch crossing, selects up to 8 individual data samples for each bunch-crossing and sends the data to USA15 via one GBT chip configured to operate in parallel mode without Forward Error Correction (FEC).

All items in orange are template descriptions to be replaced in actual specifications. The term "component" will be widely used in these descriptions and that should be taken to be an individual component (e.g. an IC), a card or electronics module (e.g. a power supply), a facility (e.g. DCS) or a service (e.g. grounding and shielding).

If any section does not apply to what is being specified, please do not delete the section, but rather enter "Not Applicable" as the content of the section.

Specifications must be reviewed and approved at a Specification Verification Review (SVR) by a committee formed by the ATLAS review office in collaboration with the NSW project leader and electronics coordinator. Any later changes must be approved by the ATLAS review office who may call for a re-review depending upon the degree of the changes.

In addition to the SVR, three types of design reviews are referenced in this specification template. They are the Preliminary Design Review (PDR), Final Design Review (FDR) and Production Readiness Review (PRR), all of which will be organized by the ATLAS review office in collaboration with the NSW project leader and electronics coordinator. The PDR must be held prior to the fabrication of the first prototype. Further PDRs may be required prior to fabrication of revised prototypes depending upon the degree of changes. The decision for this will be made by the ATLAS review office in collaboration with the NSW project leader and electronics coordinator. The FDR must be held prior to the fabrication of the pre-production units and the PRR must be held prior to start of the production units.

Revision History			
Rev. No.	***Proposed Date*** ***Approved Date***	***Description of Changes*** *(Include section numbers or page numbers if appropriate)*	***Proposed By: author*** ***Approved By: reviewer***
1.0	P: 06/02/2015 A:	Initial specification document submitted to EDMS	P: S. Martoiu A:
1.1	P: 15/09/2015 A:	Current version	P: S. Martoiu A:

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1 Conventions and Glossary

ART – Address in Real-Time

ASIC – Application-Specific Integrated Circuit

BC – Bunch-Crossing

BCID – Bunch-Crossing Identification Number

DDR – Double Data Rate

NSW – New Small Wheel

SEU – Single Event Upset

SLVS – Scalable Low Voltage Signaling

TMR – Triple Modular Redundancy

2 Related Documents

All documents (other than references) linked to this specification. If this specification is for a component that integrates other NSW components or complex commercial components, include in this list all specifications for these components being integrated.

3 Description of Component or Facility

The scheme for readout of trigger data for the MicroMegas detector in NSW is shown in the block diagram in Figure 1.

For the Micromegas detector, the trigger data is generated by considering only the first arriving hit in each 64-channel front-end IC for a given bunch crossing. The strip address of the hit (Address-in-Real-Time) is promptly produced by the VMM chip in serial form.

The Address-in-Real-Time words generated by the front-end ASIC (VMM) are sent to the trigger processor in USA15 via optical links in two steps. First, the ART from each of 32 front-end VMMs (four Front End boards) is serially transmitted, point-to-point, to a companion digital ASIC on the trigger data driver card; from there it is sent to USA15. The ASIC performs the following functions:

- Deserialize the ART stream and phase-align the hits to the BC clock.
- Identify the strip addresses of up to a fixed number of hits by means of cascaded priority encoders.
- Append the 5-bit geographical VMM ASIC address to the strip address of each hit.
- Send the ART addresses and the 12-bit BCID to a GBT configured to operate in parallel mode without Forward Error Correction (FEC).

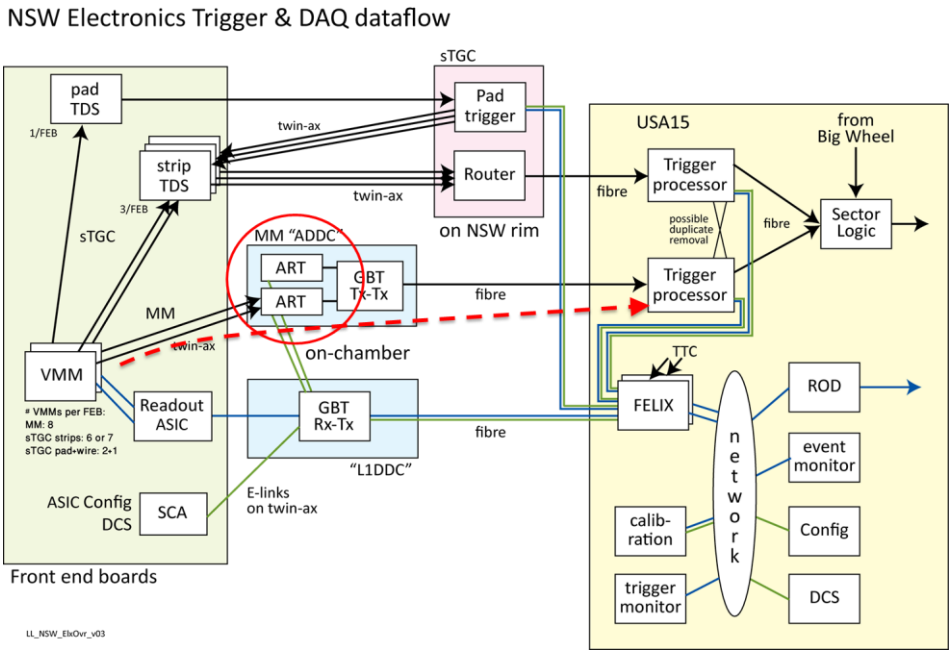

Figure 1. Block diagram of the Trigger and DAQ NSW electronics. The MicroMegas trigger path is designated with the red dotted arrow. The ART ASICs (red circle) are collecting trigger data (Address in Real Time) from the front-end VMM ASIC and formatting the output to the GBT chip. The information travels on fibers up to the Trigger Processors located in USA15.

There are a total of 512 ART data driver cards. Using the dual Versatile Transmitter (VTTx) significantly reduces the cost per link. The absence of the downlink, however, requires that the ART ASIC receive its TTC and clock signals from the Level-1 event readout downlink and that the ART GBT transmitter also be configured via that downlink.

4 Interfaces

This component interfaces to other components listed in Table 4.1.

Table 4.1: Components which Interface to This Component

Name of Component	Name of Component Specification
VMM ASIC	VMM Datasheet [1]
GBT ASIC	GBTx Manual [2]
SCA ASIC	GBT-SCA Manual [3]

5 Physical Description

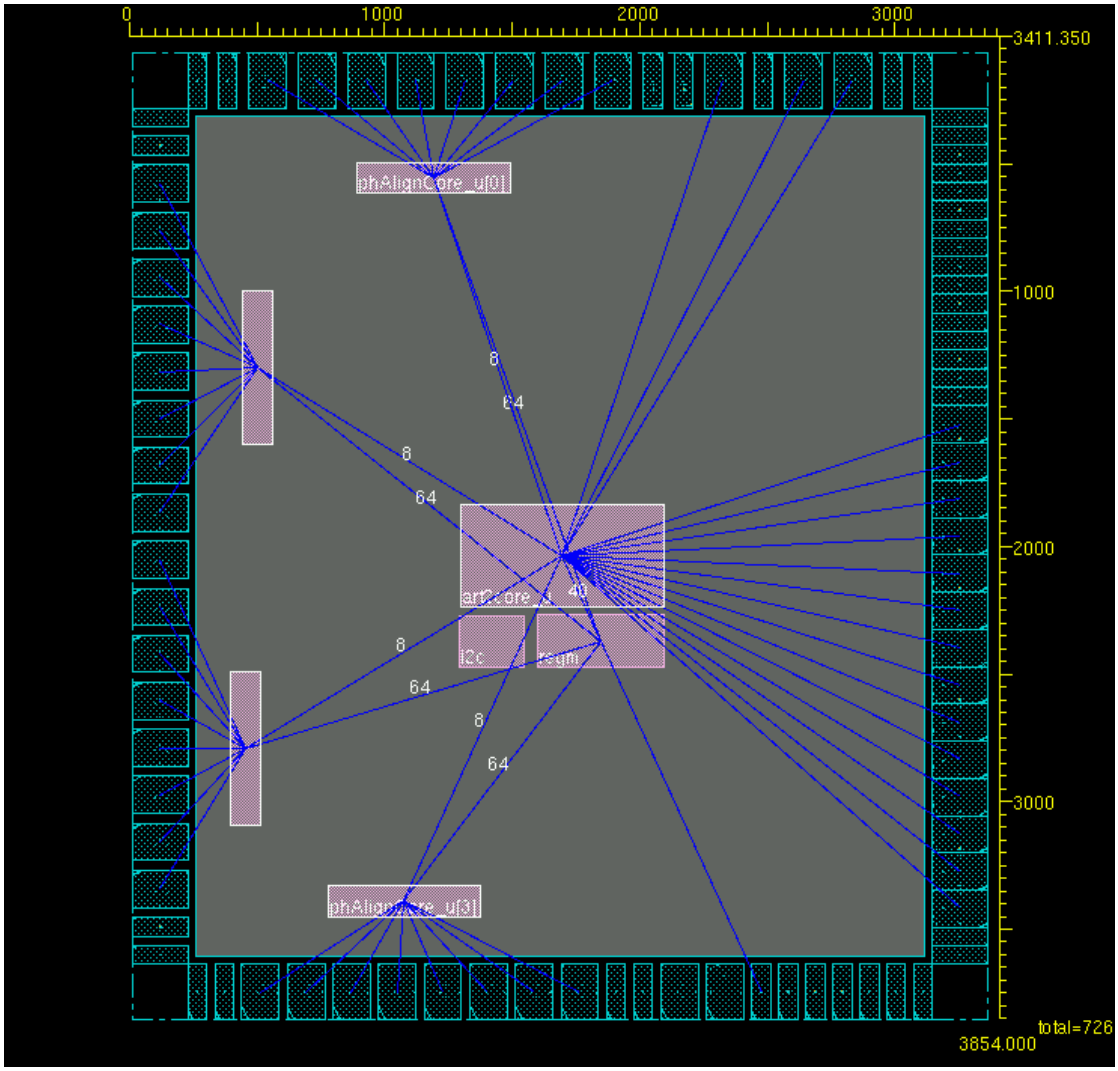

Figure 2. Floorplan of the ART ASIC

State the physical description of the component: unpackaged IC, packaged IC, PCB, rack mounted module, etc. If specifying a facility, state the area served by the facility, e.g. for the Grounding and Shielding Plan, state the part of the detector for which it applies.

- For an unpackaged IC, include a figure showing its size and pad arrangement and a table with pad assignments.
- For a packaged IC, include the type and size of package, a figure showing the pin arrangement and a table with pin assignments.
- For a PCB, include a figure showing its size and connectors and connection points and a table listing the connection assignments.
- For a rack mounted module or an enclosed unit, include a figure outlining the unit with its size and connections and a table listing the connection assignments.
- For a component that integrates other NSW components or complex commercial components, include a list of all these components being integrated.

The final size may not be known at the time of the first specification review but an estimate should be given. Actual size specified by the time of the PDR, FDR and PRR.

Table 5.1: Pad/Pin or Connector Assignments

Name or Number	Description
Name or number from Figure 5.1	Very brief description of connection.

6 Manufacturer

GlobalFoundries GF_8RF-DM (former IBM CM8RF-DM)

7 Power

Table 7.1: Power Requirements

Name	Max/Nom/Min V or I Supplied	Nom/Max I for Voltage Source	Max/Min V for Current Source	Other Requirements
VDD	1.4V/1.5V/1.6V	~100mA (tbc)		

8 Cooling

The ASIC is specified by design to work at temperatures between 0 and 125 degrees Celsius. Given the low power consumption, no special cooling is foreseen. The final cooling requirements will be reviewed once a real-size detector module is available ("Module-0").

A water cooling system is provided in situ for all NSW electronics.

9 Input/Output

Table 9.1: Input and Output Signals

Name	In, Out or I/O	Type of Signal	Source/ Destination	Description
ART_IN_P/N[31:0]	Input	SLVS	VMM (MMFE8)	ART input from VMMs
GBT_OUT_P/N[13:0]	Output	SLVS	GBTx (ADDC)	Data output to GBT
BCR_P/N	Input	SLVS		BCR input (optional)

ELINK_TTC_CLK	Input	SLVS	GBTx(L1DDC)	TTC E-Link clock
ELINK_TTC_DATA	Input	SLVS	GBTx(L1DDC)	TTC E-Link data
CLK40_P/N	Input	SLVS	GBTx (ADDC)	40MHz clock
CLK160_P/N	Input	SLVS	GBTx (ADDC)	160MHz clock
RESET	Input	CMOS	SCA (ADDC)	ASIC Reset
I2C_SCL	Input	CMOS	SCA (ADDC)	I2C clock (from SCA)
I2C_SDA	Bidir	CMOS	SCA (ADDC)	I2C data (from/to SCA)
TEST_MODE	Input	CMOS	-	Test interface (tbc)
SEU	Output	CMOS	SCA (ADDC)	SEU flag

10 Detailed Functional Description and Specification

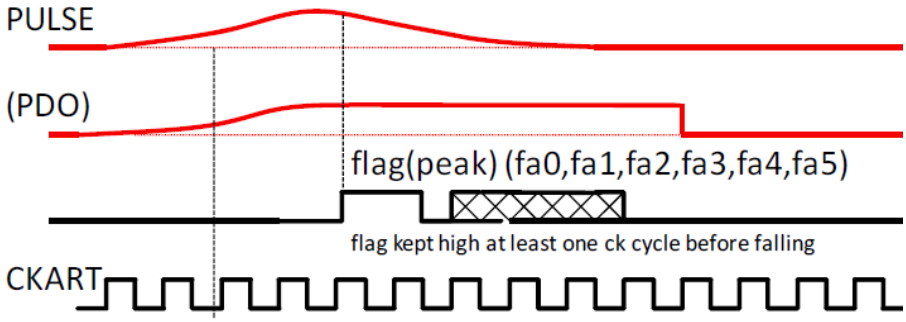

Figure 3. The ART signal [1]

The ART signal generated by the VMM front-end ASIC (Figure 3) consists of a flag pulse, followed by 6 bits which indicate the address of the strip that received a hit. The internal circuitry of the VMM selects always the first channel that was hit, when more channels receive a signal nearly at the same time. The ART circuit is triggered either by the threshold crossing of the strip signal or by the peak detection circuit. For minimum latency, the threshold crossing will be used in the experiment. In DDR mode, the flag is high for two falling edges of the 160 MHz clock and kept low until the next rising edge of the clock. The 6 address bits are then serialized on each edge of the clock. Following the ART address, the ART circuit is internally reset for approximatively 10ns.

For the purpose of this discussion, a simplified version of the ART signal is shown in Figure 4, where the flag is reduced to a single bit of the 160 MHz DDR stream which is immediately followed by the 6 ART address bits. Since this signal is triggered asynchronously, the start of the ART signal may appear at any 160 MHz DDR tick, inside the 40 MHz BC clock window (see Figure 4).

The ART ASIC will register all ART signals starting anywhere inside one BC window. In Figure 4 the boundary between BC windows is represented by blue lines. The ART ASIC looks initially at the presence of flags. All ART flags which occurred in the 25 ns time window between time 0 and time 1 are therefore known at time (1). The ASIC can perform the selection of the hits immediately, even before some of the ART signals have completed (i.e. some of the 6 ART data bits are still flowing out of the VMM chips). Half BC is reserved for the hit selection operation. At time 1.5 (half BC time later) the hit selection is performed and the result is presented on the output bus. If there are more than

8 VMMs issuing ART signals in the same BC window, the ART ASIC will select only 8 of them, based on a priority scheme which is detailed later.

At time (2) all the bits of the ART addresses are recorded and can be presented at the output. Therefore the ART ASIC generates the data to the GBT chip in two steps, at time (1.5) and time (2), corresponding to the 80Mbps transfer mode.

As it will be detailed in the following chapter, simulations performed for worst case of the technology showed that the hit selection operation can be performed in about 3-4 ns, which is considerably shorter than the 0.5 BC. Despite that, the latency cannot be shortened further because the deserialization step might not be completed in time for signals which burst at the very end of the BC window.

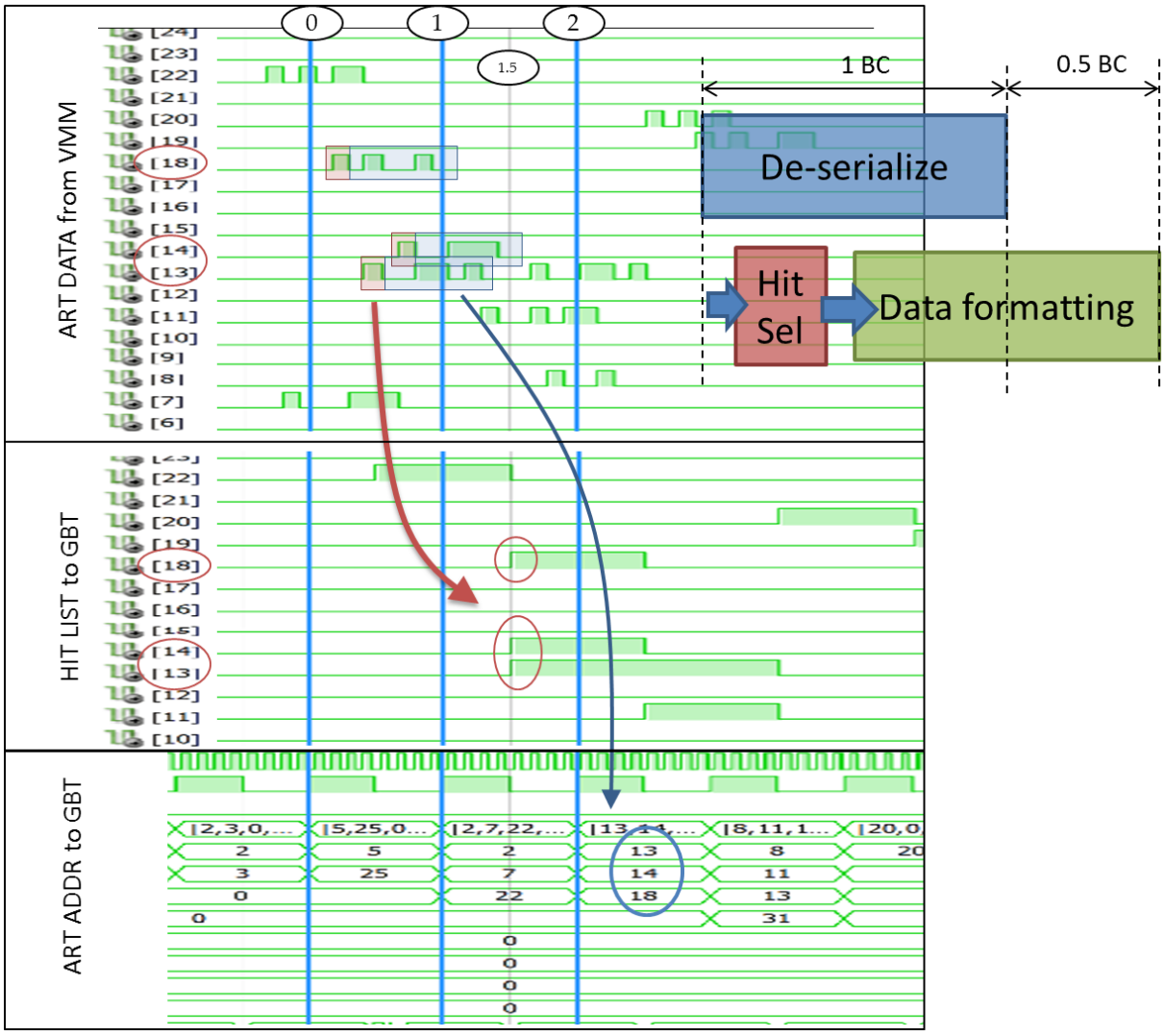

Figure 4. Theory of operation of the ART ASIC. Hit selection (red) is performed in parallel with ART data de-serialization (blue).

For transfer rates of 160 or 320 Mbps, the data flow to the GBT will be segmented in 4 or 8 steps (see Figure 5). This gives the possibility to lower further the latency by segmenting the data such that the information which is available earlier (i.e. first bits of the ART address) is serialized first. In this way, the data can be transferred to the GBTx while ART is still de-serializing the ART stream. For example, in 320Mbps mode, the Hit Selection operation presumably takes one 160 MHz DDR tick (3.125 ns) and it is

immediately followed by the transfer of the hit information, which takes 4 ticks. By the time this transfer ends, the de-serialization of the ART data is half way completed, therefore first bits of each of the 8 ART addresses are already available for transfer.

Taking into account the time at which the GBTx registers the data from the ART ASIC, in 160Mbps and 320Mbps modes, the latency can be shortened by 0.5 BC and 0.75 BC, respectively, compared to the 80Mbps mode.

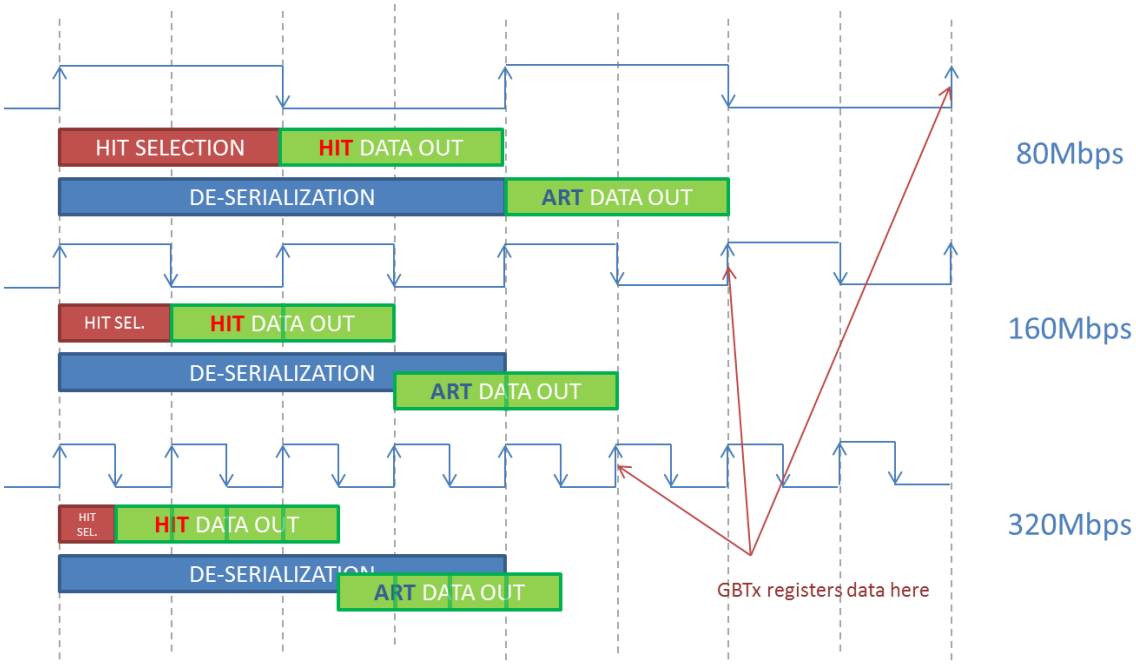

Figure 5. Optimal latency for the three possible output data rates

The implementation of the ART ASIC will target the use of 320 Mbps mode. This will give the best performance results while minimizing the number of IO pads. Considering all corners and worst conditions, the Hit Selection will probably not meet the optimal 3 ns propagation delay, therefore the latency of the ART ASIC will be limited to 1.25 BC.

10.1 Programmable Delays

The purpose of the Programmable Delay block is to be able to skew the input signals to avoid setup or hold violations on the local clock phase, and adjust the ART stream to the correct clock phase. The preferred option is to use the CERN's DLL-based Phase Aligner IP core [4] which will eliminate the spread of the delay parameter with respect to process variations and operating conditions. The future VMM3 chip may integrate the option to register the entire ART signal to the 160 MHz ART clock. In this case, the automatic phase adjustment mode of the Phase Aligner core can be used, which does not require any user interaction.

The PhaseAligner IP has 8 data lines (Figure 6), therefore 4 core instances are needed for the 32 ART inputs of the ASIC.

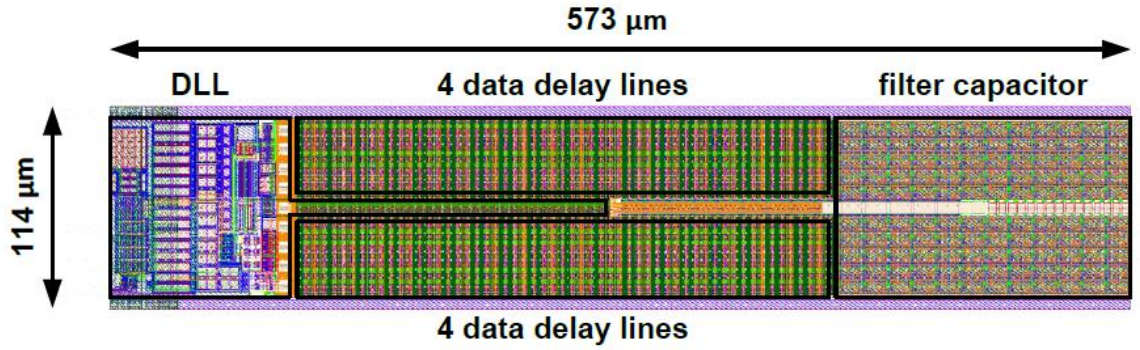

Figure 6. Layout of the CERN PhaseAligner IP [4].

10.2 ART De-serializer Circuit

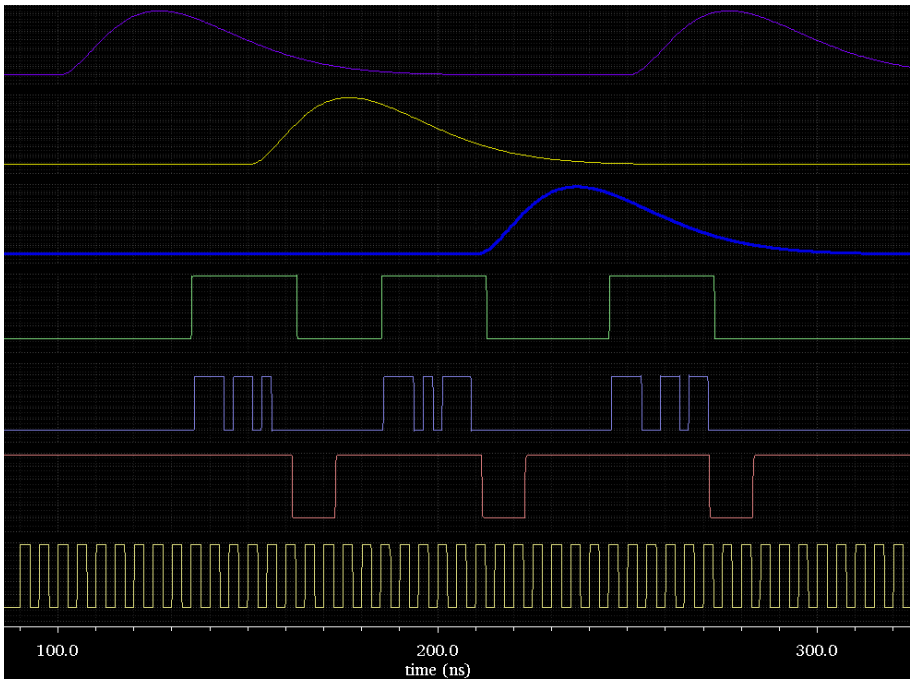

Figure 7. Simulated ART signal (curtesy of Gianluigi De Geronimo)

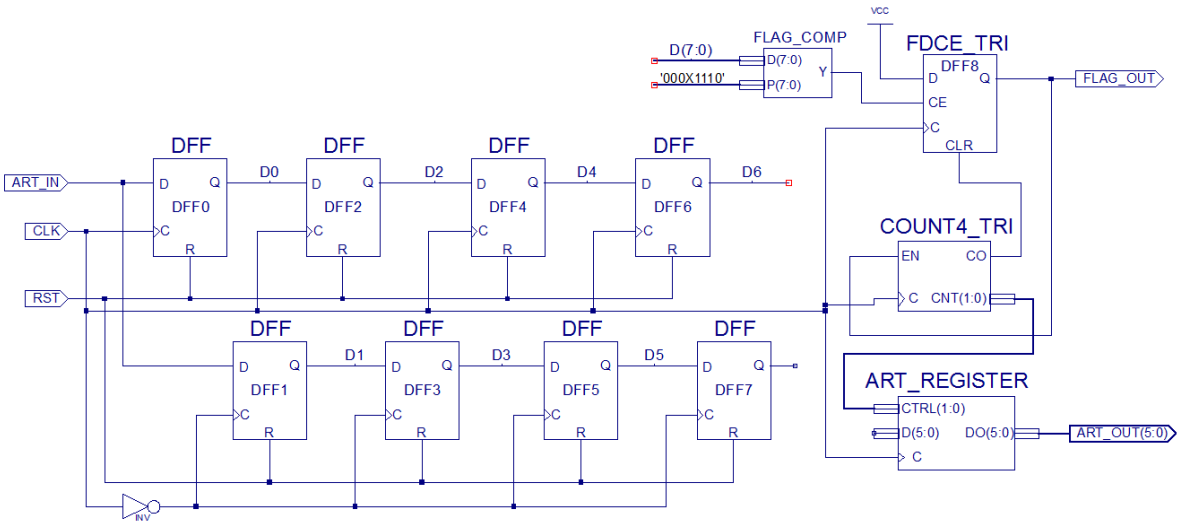

Figure 8. Schematic view of the ART de-serializer.

A sequence of simulated ART signals is given in Figure 7. The flag pulse precedes the serialized address data. In DDR mode, the flag pulse raises asynchronously to the CKART clock and is kept high through the next two falling edges of the 160MHz CKART clock, being lowered by the second falling edge. Optionally, the rising edge of the flag can be registered to the CKART clock. A 10ns reset period is applied after each ART sequence.

A schematic view of the ART de-serializer circuit is given in Figure 8. Flip-flops DFF0 to DFF7 form an 8-bit DDR shift register which de-serialize the incoming data stream. The first ART data bit is streamed at the following rising edge of CKART. The comparator *flag_comp* searches for the "000X1110" pattern[1] which indicate the presence of a flag pulse. A control flip-flop (DFF8) is triggered and kept high for 4 clock cycles (25ns) by a 2 bit counter (*COUNT4_TRI*). This signal is supplied to the hit selection circuitry which registers it on the 40 MHz BC clock domain.

The 2-bit counter also controls the output latches of the de-serializer circuit (*ART_REGISTERS)* to extract the 6-bit ART data from the DDR shift register at the appropriate moments. The circuit also calculates a parity bit which is transmitted to the GBTx chip together with the ART data (the parity circuit is not shown in Figure 8).

The 8-bit search pattern (i.e. "000X1110" or "00001110") is unique, i.e. there are no ART data symbols which can trigger a false flag. The pattern is controlled by two 8-bit configuration registers (FLAG_MASK and FLAG_PATTERN) which allow for full flexibility.

The FDCE_TRI and COUNT4_TRI (Figure 8) are forming the control logic of the circuit and are therefore triplicated in order to mitigate Single Event Upsets. The other registers belong to the data path and do not need triplication. The parity error may be generated due to a SEU.

10.3 Programmable Deadtime

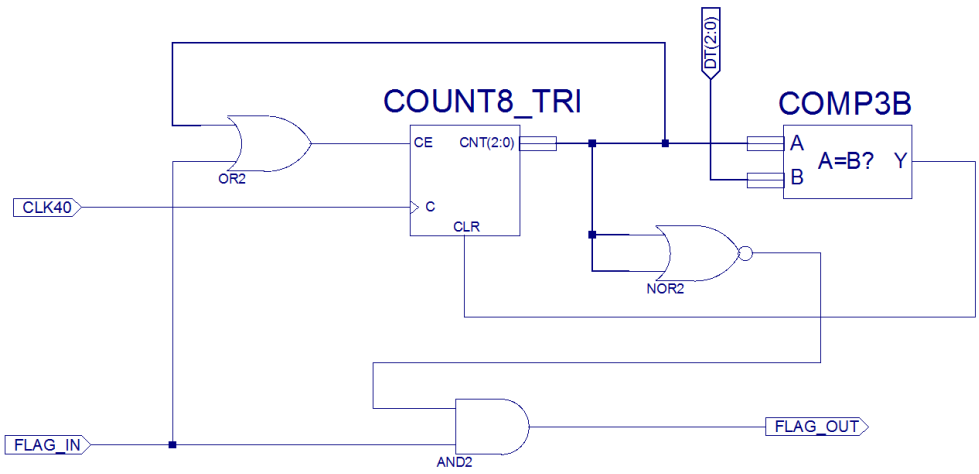

Figure 9. Schematic view of one channel of the Programmable Deadtime circuit.

[1] "X" indicates a don't care bit. The flag signal is raised asynchronously to the ART clock, therefore the rising edge of the signal may be registered on any clock edge. If the flag signal is registered at the falling clock edge internally by the VMM, this bit is replaced by a "0".

This block creates an artificial deadtime for each VMM channel which is controllable via configuration. Subsequent data on a particular channel is ignored for a number between 0 and 7 BCs.

The block consists of a 3-bit counter which is triggered by the flag output of the deserializer circuit of the corresponding channel and operates on the 40 MHz BC clock (see Figure 9). The counter counts up to the programmable value then is reset to 0. Counting is not resumed until the next flag signal. The channel is gated during the time the counter value is different than 0.

In the rare event of a radiation induced SEU, the circuit may introduce a spurious deadtime window or extend a deadtime window which is in progress. Triplication may be needed to avoid spurious triggering of the deadtime counters.

10.4 Hit selection circuit

A few possible models for the hit selection circuitry were evaluated. The best results were obtained with the Hit selection circuit based on cascaded priority encoders as shown in figure 4. The first priority encoder will select the first ART flag (i.e. the most significant bit which is not zero from the 32-bit ART flag word). The result expressed in one-hot 32-bit format is subtracted from the initial ART flag word, and the result is presented to the following stage. The second priority encoder will therefore select the second non-zero bit from the ART flag word. The operation is cascaded 8 times to select a maximum of 8 non-zero flags. The one-hot result of each stage can be or-ed together to result a 32-bit hit list of the selected hit flags. This 32-bit word describes unambiguously the information that is required to be passed to the trigger processor (i.e. the addresses of the VMMs who issued an ART signal).

If absolute address numbers for each VMM hit are required instead, binary decoders have to be implemented for each of the 8 outputs, and the sum of non-zero bits has to be computed and attached to the output stream. These operations may have an impact on the propagation delay parameter.

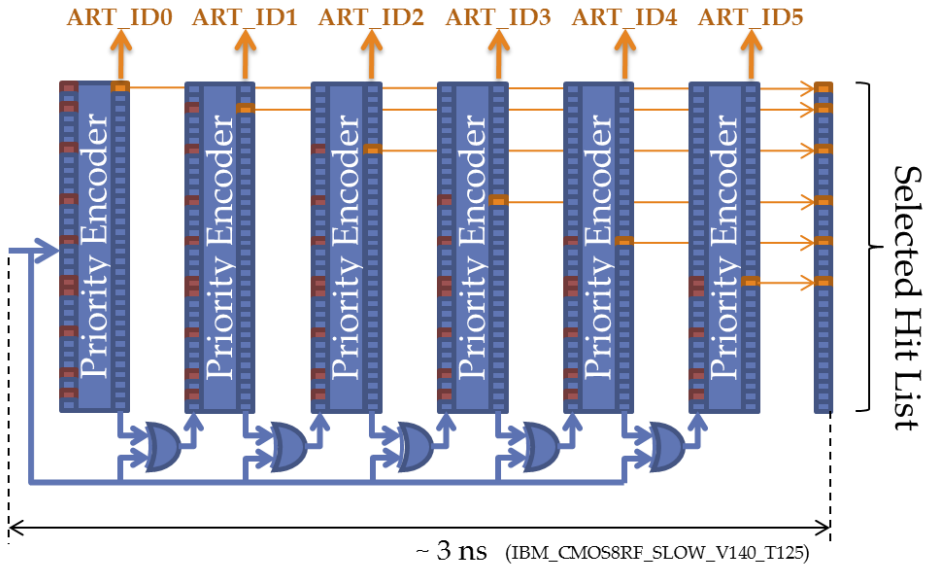

Figure 10. Hit selection circuitry based on priority encoders

10.5 Output Logic

The ART ASIC will transmit to the Trigger Processor the following information:

- Addresses of up to 8 VMM channels which had a hit in a particular BC
- The strip address of each of the 8 or fewer hits recovered from the ART stream (ART Data - Address-in Real-Time).
- 12 bit BCID for checking the synchronization.
- Other information (error flags, parity bits)

As described earlier, the information is transmitted to the GBTx chip in two steps. First, the selected VMM hit list is available (Hit Information), based on the flag bits issued by any of the 32 VMM chips at the input of the ASIC. Half BC later the corresponding ART Data is transmitted to the output, consisting of 8 x 6-bit strip addresses. The Wide Bus mode of the GBTx chip allows for 112 bits to be transmitted in a 25 ns (BC) window. 56 bits are allocated for each of the two transmission steps. For the 320 Mbps mode, the 56 bits are segmented in 4 transfers, respectively, but the overall data segmentation into Hit Information and ART Data remains the same.

The Hit Information may be transmitted in two modes:

- Hit Map option consists of a 32-bit word where each bit corresponds to one of the 32 VMMs connected to the ART ASIC. All bits corresponding to the VMMs which were selected by the Hit Selection circuit in a given BC are set to "1", while the others are kept low.
- Hit Address option identifies with a 5-bit number (VMM channel ID - 0..31) each VMM which was selected by the priority encoder. 8 x 5-bit addresses are transmitted at any given BC. Considering that the hit list is ordered, a value of 0 in any position other than the first can indicate the end of list. An extra bit has to be used to signal the case where the list is empty.

In both cases, the 12-bit BCID is transmitted together with the Hit Information. The Hit Map option has 12 spare bits. These bits can be used to transmit a fixed word as frame delimiter (e.g. "1010"). The other 8 bits may be used to transmit error flags from the core logic (i.e. error indicators from the 8 binary encoders attached to each priority encoder in the hit selection logic).

Optionally, the Hit Map may be unfiltered, carrying the hit or no hit information for all the 32 VMM connected to the ART ASIC. This mode may be useful for debugging spurious front-end activity. Only the first 8 hits will have the ART address data transmitted.

The Hit Addresses option has 3 spare bits which can be used as frame indicator (i.e. "01") and an error flag (ER).

Table 2. Output Data format

Hit Information Format:

Hit list	1	0	1	0	BCID[11:0]	ERR_FLAGS [7:0]	HIT_LIST[31:0]
Hit addresses	0	1	ER	EY	BCID[11:0]	8 x VMMID[4:0]	

ART DATA Format:

	8 x ARTDATA[5:0]	PARITY[7:0]

ER = Error flag
EY = Empty flag

For the second transfer step (i.e. corresponding to the falling edge of the BC clock), the 8 x 6-bit ART addresses use 48 bits, while the remaining 8 bits are used for parity bits computed by the deserialization logic. The implementation of the ASIC will target the 320 Mbps transfer mode. In order to take advantage of the optimum latency scheme possible in this transfer mode (see Section **Error! Reference source not found.**), the transfer of the ART Data fields is segmented such that the bits which arrive first at the ART ASIC are serialized first to the GBTx chip (**Table 3**).

Table 3. Segmentation of the ART Data transfer for optimum latency performance

Transfer #	1							2							3							4			
Ch #	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	PARITY
Bit Range	[0:1]	[0:1]	[0:1]	[0:1]	[0:1]	[0:1]	[0:1]	[0:1]	[2:3]	[2:3]	[2:3]	[2:3]	[2:3]	[2:3]	[2:3]	[2:3]	[4:5]	[4:5]	[4:5]	[4:5]	[4:5]	[4:5]	[4:5]	[4:5]	[0:7]

On the other side of the fiber, at the Trigger processor side, the data is rearranged due to the way GBT transmits the data. The mapping between the format on the ART ASIC side and what is received at the Trigger Processor side is given in Appendix 1 and Appendix 2.

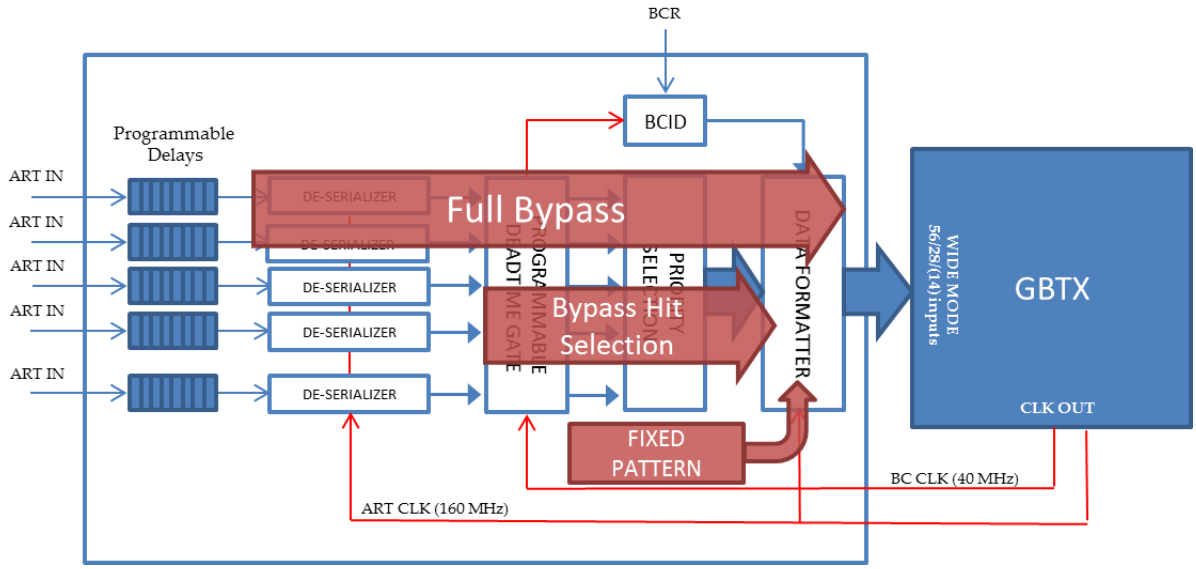

Figure 11. Bypass and test modes

Besides the normal operation modes, the ASIC will implement test modes where various parts of the system are bypassed or fixed or cyclic calibration data is transmitted to the GBTx chip. When possible, these test modes will be identified by different frame header patterns. The test modes are summarized below:

- Full bypass mode (direct connection of the output of programmable delays to the output pads of the ASIC).

- This is used to verify and measure the propagation delay during ASIC initial verification and it is not accessible during normal operation of the ASIC.

- Bypass priority selection on ART data (debug mode)
  - Controlled by a configuration register, the input channels are connected directly to the output logic (8 channels at a time). Except for the frame header pattern, the output format is not altered. This mode can be used for in-system checking of the transmission between VMM chips and ART ASIC and setting the correct propagation delay of the Programmable Delays.

- Fixed output calibration pattern
  - A fixed pattern is sent continuously to the GBTx chip. The pattern is stored in local configuration registers and is accessible via the configuration path. This mode allows for verification of the interface between ART ASIC to GBT. The same mode can be used for in-system geographical identification of individual ART ASICs, by configuring unique patterns for each individual ASIC and observing on which trigger processor channel the pattern is being received.

10.6 TTC Block

The ART ASIC receives the BCR signal from the GBTx chip resident on L1DDC board, via a 160Mbps E-Link (option 1 or 2 in Figure 12). The clock of the TTC E-Link is configured to 40 MHz. The phase of the E-Link signals may not be optimal with respect to the internal clock of the chip. However, the chip will use the internal 160MHz clock to oversample the E-Link signals and readjust the TTC information to the internal 40 MHz BC clock.

E-link option		bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
0	2 bits	L1A	B-chan						
1	4 bits	L1A	BCR	ECR	B-chan				
2	4 bits	L1A	BCR	ECR	Brcst[2]				
3	8 bits	L1A	BCR	ECR	Brcst[2]	Brcst[3]	Brcst[4]	Brcst[5]	B-chan
4	8 bits	L1A	BCR	ECR	Brcst[2]	Brcst[3]	Brcst[4]	Brcst[5]	Brcst[6]

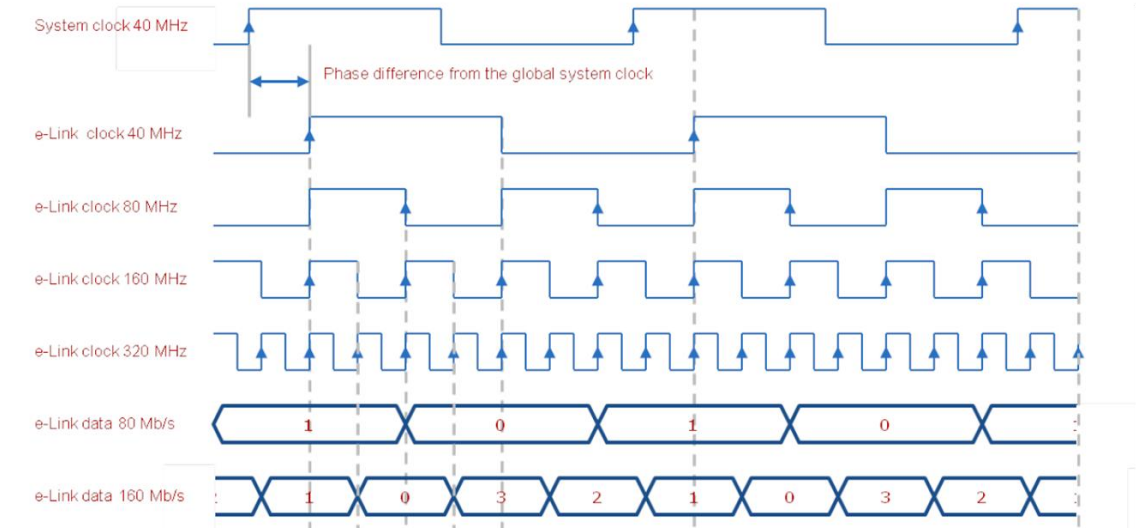

Figure 12. TTC data format sent by FELIX over GBT E-Links (top) and E-Link timing diagram [2] (bottom)

The block diagram of the TTC block is shown in Figure 13. The 40 MHz E-Link clock is present at all times, therefore it is used to recover the relative phase. The timing diagram of the E-Link clock and data signals is given in Figure 12). The clock signal is sampled by a Double Data Rate (DDR) shift register which uses both edges of the internal 160 MHz clock. The 8-bit output of the DDR shift register is registered on the 40 MHz internal reference. Depending on the relative phase between the incoming E-link clock and the internal reference, the output will have different values as in Figure 14. This information is decoded by an Edge Detector circuit which determines which phase of the 160MHz clock is used to sample the E-Link data and at which of the clock edges to sample the complete 4-bit TTC word. The TTC data is then retimed on the internal 40MHz reference clock domain.

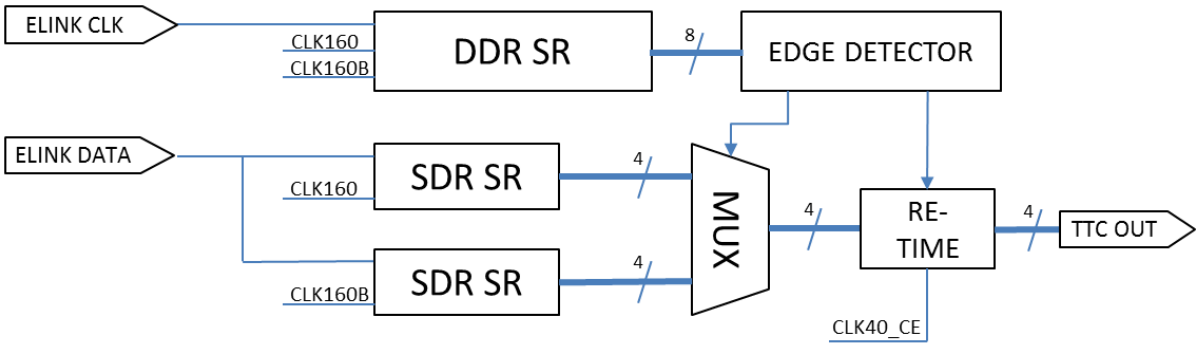

Figure 13. Block diagram of the TTC block.

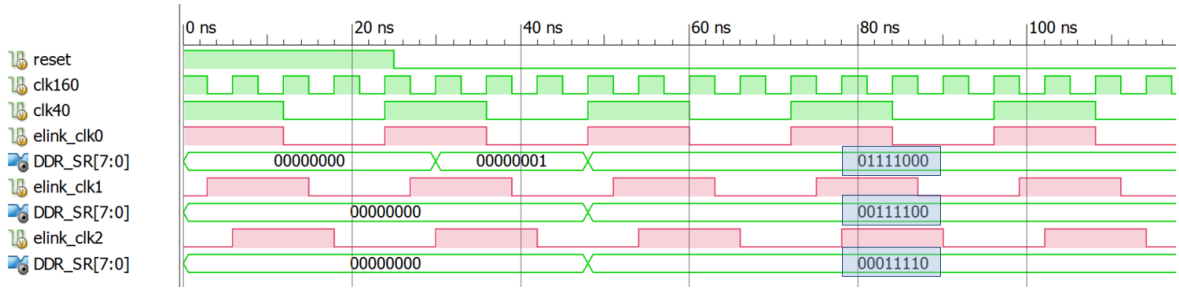

Figure 14. Timing diagram of the TTC DDR Shift Register which is used to find the edge of the incoming clock signal.

The E-Link data signal is sampled by two Single Data Rate (SDR) shift registers on the rising and falling edges of the 160MHz clock, respectively. The Edge Detector circuit determines which phase of the clock to use, as well as the correct word boundary.

In case the phase of the incoming E-Link clock is close to the rising or falling edges of the internal 160 MHz clock, the value at the output of the DDR shift register will fluctuate due to metastability. However, only the bits corresponding to only one of the edges of the clock will fluctuate, the others will be stable. The Edge Detector circuit can be designed to tolerate this situation and recover correctly the TTC data from the E-Link stream.

10.7 I2C Slave and Register Matrix

All programmable parameters of the ART ASIC functionality are stored in a register bank. The register bank will be triple redundant and operate at slower speed (40MHz). The list of registers is given in Table 4.

Table 4. Programmable registers of the ART ASIC

Register Name	Access Type	Addr[2]	Description
FLAG_PATTERN	R/W	0x00	Global programmable search pattern for the flag pulse
FLAG_MASK	R/W	0x01	
BCID_OFFSET_L	R/W	0x02	Fixed offset loaded by BCID counter at BCR [7:0]
BCID_ROLLOVER_L	R/W	0x03	Reset value for the BCID counter corresponding to the orbit time [7:0]
BCID_HIGH	R/W	0x04	Most significative bits of BCID offest and rollover registers ([11 :8]/[11:8])
CONTROL_REG	R/W	0x05	Control Register. Structure is given in Table 5
ARTBYPASS_SEL	R/W	0x06 – 0x0A	Controls which ART channels are transmitted in hit selection bypass mode (8 x 5bit)
PATTERN_DATA	R/W	0x0B – 0x18	Fixed output pattern (112 bits)
SEU_COUNTER_L	R	0x19	SEU counter ([7:0])
SEU_COUNTER_H	R	0x1A	SEU counter ([15 :0])
SRESET_REG	W	0x1F	Soft Reset Register
DELAY_REG	R/W	0x20 – 0x3F	Reserved for Phase Aligner control (tbc)

Table 5. Bit field structure of CONTROL_REG register.

Field	Offset	Width	Access	Reset	Description
cfg_reserved	7	1	R/W	0x0	Reserved
cfg_dout_pattern	6	1	R/W	0x0	Enable fixed pattern output
cfg_dout_artbypass	5	1	R/W	0x0	Enable ART bypass
cfg_dout_hitlist	4	1	R/W	0x0	Enable hit-list mode
cfg_dout_artflags	3	1	R/W	0x0	Send un-filtered flags in flagmask mode
cfg_artmask	0	3	R/W	0x0	Auto-mask value

The Register bank is accessed via an I2C Slave core. The slave is able to write and read the values of individual registers. Also, the core gives read access to the delay setting of the Phase Aligners when used in automatic mode and the SEU counters of the register bank. Special register access will perform Soft Reset of the ASIC core (excluding BCID counter), SEU counters or configuration registers.

[2] Preliminary information.

11 Radiation Tolerance, EMC Issues and Other Special Requirements

The front-end electronics of the NSW detector will have to withstand a total ionization radiation dose below 100 krad [5]. The 130 nm CMOS technology was tested extensively and at much higher TID, and was shown to withstand LHC conditions without the use of special layout techniques. Given the relatively low level of radiation, it is expected that the ASICs will be able to function properly for the entire duration of operation with minimal degradation. However, TID tests of the ASICs may be performed to assess the effects of the total radiation dose expected on the specific design, in particular the possible increase of power consumption due to leakage current.

Table 6. Calculated SEU rates and average time between SEU events (MTBF) based on the radiation data available from simulations [5]

	Number of bits	SEU Rate (SEU/s)	SEU MTBF	SEU MTFB full detector
Deserialization Flip-Flops	192	9.27E-08	125 days	6 hours
Configuration Registers (non-protected)	400 (est.)	1.93E-07	60 days	3 hours
Configuration Registers (TMR)[3]	1200 (est.)	5.80E-07	20 days	1 hour

Single event effects due to instantaneous fluence of ionizing particles, however, must be mitigated with special design techniques like triple redundancy or Hamming encoding, especially for the ASIC configuration registers and internal state machines.

An estimation of SEU rates for the data and configuration logic is given in Table 6. The estimation takes into account the simulated radiation loads for 10 years of operation at R = 2.5 meters[4] given in [5], a SEU cross-section for regular registers of 7.0×10^{-14} cm^2/bit. The yearly runtime used to derive the instantaneous fluence is 10^7 seconds.

SEU effects on the data will most probably have little effect on the overall efficiency. However, simple parity bits are calculated by the input de-serializers circuits and can be used downstream to tag possible data corruption. Table 7 shows the list of logic blocks of the ASIC which will require triple redundancy or another SEU mitigation method.

The ASICs will be tested in radiation taking into account the safety factors according to the ATLAS Policy on Radiation Tolerant Electronics [6] to ensure that possible locking situations are mitigated correctly by the triplication logic.

Table 7. List of logic blocks which will be designed using triple redundancy or other SEU mitigation method.

Block	Data Protection	State Machine Protection
Programmable Delays	No	-
DDR De-serializers	Parity bit	Yes
Programmable Deadtime	-	Yes
Priority Selection	No	-
BCID Counter	Yes	
Output Logic	No	Yes
Register Matrix	Yes	Yes
I2C Slave	Yes	Yes

[3] Single register errors are automatically corrected by the TMR logic.
[4] Value tbd

12 Testing, Validation and Commissioning

Describe testing procedures that will be used to demonstrate that the fabricated component meets the specifications. This should include radiation testing if radiation tolerance is one of the requirements. Specify the testing features included in the system in view of easily test and qualify the component during production (e.g. BIST included in ASICs or systems).

It is not required to complete this section prior to the first specification review but it should be completed prior to the PDR. Prior to the FDR, the production testing must be described, and prior to the PRR, commissioning plans must be included.

13 Reliability Matters

13.1 Consequences of Failures

Failure of one ART ASIC will lead to 0.1% of the MicroMegas channels to be lost. The channels which are lost correspond to one quarter of sector of one detector plane. Tracks can still be reconstructed using the information from the remaining three planes, albeit with degraded efficiency.

Describe the consequences to the detector of a failure of one unit of this component, e.g. x% of the sub-detector channels will be lost, or one stave or petal could overheat causing delamination of its component parts. The severity of the consequences will determine the level of reliability required and the level to be validated by QA and QC procedures defined in sections 12.4 and 12.5.

13.2 Prior Knowledge of Expected Reliability

Based upon industry experience, collaboration experience or personal experience, give an estimate of the reliability of this component.

13.3 Measures Proposed to Insure Reliability of Component and/or System

Include such measures as conservative design techniques (give specific examples), redundancy and possibilities to replace failed part. . If failed part could be replaced, estimate the difficulty and time involved for installing replacements,

13.4 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

Describe what stress tests will be applied during the development period to validate the reliability of this component. Give a brief outline of any appropriate reliability theory being used. These tests could involve destructive tests.

It is not required to complete this section prior to the first specification review but it must be completed prior to the PDR. It is strongly recommended that these plans be reviewed and approved prior to the actual PDR to avoid the possibility of failing the PDR and thus delaying the fabrication or construction of the prototype parts,

13.5 Quality Control to Validate Reliability Specifications during Production

Describe what stress tests will be applied during production, possibly on a sampling basis, to validate the reliability of production units. These could likely be destructive tests. Specify the required sampling percentage of production units.

It is not required to complete this section prior to the first specification review but it must be completed prior to the FDR. It is strongly recommended that these plans be reviewed and approved prior to the actual FDR to avoid the possibility of failing the FDR and thus delaying the fabrication or construction of the pre-production parts,

14 References

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[10] K. Poltorak, F. Tavernier and P. Moreira, "A radiation-hard PLL for frequency multiplication with programmable input clock and phase-selectable output signals in 130 nm CMOS," *2012 JINST 7 C12014*.