LAr Optical Test Card Description
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In this document we describe the AMC-format Optical Test Card (OTC) hardware features. Section 1 provides an overview of the OTC functionality, and descriptions of each major functional block follow in the remaining sections. These remaining sections include the required AMC MMC functions and JTAG and I2C access (Sec. 2), the clocks provided on the OTC and clocks expected to be available through the AMC interface (Sec. 3), the gigabit Ethernet interface (Sec. 4), the multichannel high speed interface (XAUI; Sec. 5), the GBT interfaces (Sec. 6), the 48 channel optical receiver and 48 channel optical transmitter interfaces (μPod; Sec. 7) and the LVDS connectivity (Sec. 8). In each section control and data signals are described. The full connectivity of the onboard FPGA is listed in Appendix A. Other than the brief outline of the MMC functionality in Sec. 2, no description is made of the AMC standard or functions required by the standard.

1. Overview

The main purpose of the OTC is to provide up to 48 channels of optical input to be processed by an onboard FPGA with the results of the processing transmitted on up to 48 channels of optical output. The electro-optical I/O is provided by Avago micropods capable of data rates up to 12.5 Gbps[1]. The micropod electronic data inputs and outputs are connected to a Xilinx Virtex-7 XC7VX485TFFG1927-2 FPGA[2] GTX transceivers. The FPGA provides the processing capacity and the micropod control interface. The optical connections to the micropods are made through two 48 channel MTP connectors on the OTC front panel. The OTC is designed to the AMC full height standard. Thus, in addition to the 48 channels of optical I/O, the OTC provides serial transceiver, generic I/O and clock connectivity through the AMC interface as shown in Table 1 as well as the required AMC management interface.

The serial transceivers for the AMC interface are Xilinx GTX blocks so their configuration is flexible, but the expected OTC primary AMC configuration is one GbE interface, one XAUI interface and up to three ATLAS GBT interfaces. The transceivers signals are 100 Ohm differential pairs. The receive channels are AC coupled on the OTC, and the transmit channels are DC coupled on the OTC with AC coupling expected on the receiving end of the differential pair.

The generic I/O connections are provided via Xilinx Select I/O channels, with the primary configuration expected to be 1.8V LVDS signaling. The Select I/O pins also provide a flexible internal termination scheme. Two clocks are available on the AMC interface, one of which is intended to be derived from the LHC clock. The OTC itself provides three additional clocks including one whose frequency is related to the LHC clock.

[1] There are two speed grades of micropods, one rated to 10.3 Gbps and one to 12.5 Gbps. Tests thus far have used only the slower speed grade micropods. Tests will be made with the higher speed micropods in the coming month.
[2] Pin compatible higher capacity XC7VX550TFFG1927 and XC7VX690TFFG1927 FPGAs with GTH transceivers can be used in place of the XC7VX485TFFG1927. The default speed grade is -2, but -3 parts have also been tested for the 485 series.

The OTC has 512 MB of DDR3 memory (128M x 32 bits) connected to the FPGA. The memory uses two Micron MT41J128M16-125 chips rated at 1600 transfers per second. This chip type is known to the Xilinx Memory Interface Generator (MIG) IP core, and the pin connectivity can be found in Appendix A.

AMC Port(s)	Type	Default Use
0	Serial Transceiver (GTX)	Gigabit Ethernet (GbE)
8 – 11	Serial Transceiver (GTX)	XAUI 10 Gbps Ethernet
12, 13, 20	Serial Transceiver (GTX)	ATLAS GBT
18, 19	Generic I/O (Xilinx Select I/O)	1.8V LVDS, user defined
FCLKA	Synthesized clock	Optical I/O reference
TCLKA	156.25 MHz Oscillator	XAUI reference clock

Table 1: The OTC ports accessible through the AMC interface

2. MMC and I2C and JTAG access

The OTC adheres to the PICMG® AMC.0 R2.0 standard. It includes the mandatory IPMB (I2C), JTAG, hot-swap, LED, MMC and e-keying functionality.

The OTC MMC uses the CERN hardware design[1] implemented directly on the OTC. This gives a more compact design than using the CERN daughter card would. The MMC software is based on the corresponding CERN software, and e-keying descriptors are provided as part of the software customization. Sensor (temperature and voltage) monitoring functionality must be provided through the MMC using data retrieved by the MMC from the FPGA.

In addition to the AMC mandated IPMB I2C functioning, there are two I2C buses on the OTC. One bus connects the MMC to the FPGA and is primarily intended to be used by the MMC to collect sensor data through the FPGA. The second bus connects the FPGA to the clock synthesizer (Sec. 3) and to the micropod receivers and transmitters (Sec. 7). The I2C addresses of the clock synthesizer and micropods are shown in Table 2. The I2C addresses of the FPGA master are defined by firmware.

I2C Address	Device
0x54	Clock Synthesizer (Sec. 3)
0x30	Micropod Rx, U5 (Sec.)
0x31	Micropod Rx, U6
0x32	Micropod Rx, U7
0x33	Micropod Rx, U8
0x28	Micropod Tx, U16
0x29	Micropod Tx, U17
0x2A	Micropod Tx, U18
0x2B	Micropod Tx, U19

Table 2: Addresses of I2C devices on the OTC. The FPGA I2C addresses are defined by whatever firmware is in used.

The MMC also generates an FPGA_RESET signal usable by firmware, a FPGA_PROG signal which forces the FPGA firmware to be reloaded from the flash. There are three general purpose pins driven from the MMC to the FPGA (FPGA_IN0 – FPGA_IN2), and two in the other direction (FPGA_OUT0 and

FPGA_OUT1). Finally, there is an FPGA_DONE signal from the FGPA to the MMC which indicates FPGA firmware loading is complete.

MMC programming: The MMC is programmed through a dedicated JTAG connector (J1). No ability to reprogram the MMC in situ is provided because of potential problems disrupting the IPMB communication between the ATCA carrier and the OTC during MMC programming and inadvertently power cycling the OTC leaving it in an unusable state.

FPGA programming: A second JTAG chain is driven by either the JTAG signal on the AMC interface or by a header (J2) on the OTC and provides the mechanism used to program the FPGA and its flash memory. If the OTC is inserted into an AMC slot, there must be no cable connected to J2, and the FPGA JTAG access can only be made through the AMC JTAG port.

3. Clock Signals

The OTC has five clock sources, three generated on the OTC itself: (1) a 125 MHz oscillator used for the system clock and a GbE clock, (2) a 156.25 MHz oscillator used for a XAUI reference clock, and (3) a 40.079 MHz oscillator used to generate the optical I/O reference clock, and two clocks supplied via the ATCA carrier (4) TCLKA and (5) FCLKA clock ports. When used with the ATCA carrier for the LAr system, the TCLKA signal is a 156.25 MHz signal, and FCLKA is the output of a low jitter clock synthesizer derived from the LHC 40.079 MHz clock which itself is recovered from the GBT signal. TCLKA is intended to provide a common generic data transfer clock (e.g. for XAUI) and FCLKA provides a reference clock for the micropod optical I/O.

The onboard 40.079 MHz oscillator and the FCLKA port drive the two independent clock inputs of a CDCM6208RGZT clock synthesizer. FCLKA is the "primary" channel input, and the onboard oscillator is the "secondary" channel input. The synthesizer has two groups of four outputs[3] which are used to provide the reference clocks for four transceiver quads on the FPGA. Each of the four quads gets a reference clock connection from each of the two groups (i.e. two potentially different reference clocks per quad to allow different transmit and receive speeds for the micropods).

The input select signal REFSEL and the I2C controls of the clock synthesizer are sourced from the FPGA. The synthesizer SYNCHn, RSTn, STATUS0, and STATUS1 synthesizer signals are also connected to the FPGA. The FPGA firmware must ensure that the FPGA pins CLK_SYNCHn (=SYNCHn) and CLK_RSTn (=RSTn) are driven HI for the synthesizer to function, and the appropriate value of CLKSEL (=REFCLK) must be chosen. The onboard 40.079 MHz oscillator input is chosen if CLKSEL=0, otherwise the FCLKA input is used. The default firmware provided in the OTC flash memory configures all outputs of the synthesizer to 5 x 40.079 MHz = 200.395 MHz and uses the onboard oscillator as the source.

The output of the synthesizer, the 125 MHz oscillator, the onboard 156.25 MHz oscillator and the AMC TCLKA signal are connected to the FPGA. The 125 MHz oscillator is used as the system clock. Tables 3

[3] The eight outputs are actually quasi-independent, but for the OTC the natural use is two groups of four with one group used for the input frequency and the second for the output frequency if the two frequencies differ.

and 4 list the connections between the various clock signals and the FPGA system clock and transceiver reference clocks.

Clock Source	FPGA Connection
125 Mhz Oscillator	System clock, Quad 119 MgtRefClk0 (for GbE)
156.25 MHz Oscillator	Quad 213 MgtRefClk0 (XAUI)
AMC TCLKA (156.25 MHz)	Quad 213 MgtRefClk1 (XAUI)
CDCM6208RGZT Synthesizer Outputs (40.079 Osc; AMC FCLKA)	Quads 114, 117, 215, and 218 MgtRefClk0 and MgtRefClk1 (micropod); Quad 119 MgtRefClk1 (for GBT)

Table 3: The correspondence between clock source and FPGA resources

Quad	113	114	115	116	117	118	119	213	214	215	216	217	218	219
REFCLK0	-	S0	-	-	S1	-	GbE	XAUI	-	S2	-	-	S3	-
REFCLK1	-	S4	-	-	S5	-	S7	TCLKA	-	S6	-	-	S7	-

Table 4: Reference clocks provided to the GTX transceivers. The "Sn" notation means the n-th output of the clock synthesizer. The "GbE" notation means the onboard 125 MHz clock, and the "XAUI" notation means the onboard 156.25 MHz clock. A "-" means no direct clock connection, so the reference clock must come from an adjacent quad using the Xilinx "north" and "south" reference clock choice. "S7" appears twice because that output is fanned out to two quads.

4. Gigabit Ethernet Interface

A de facto standard for AMC has a gigabyte Ethernet (GbE) interface available on AMC port 0. This is implemented on the OTC by connecting port 0 to an FPGA serial transceiver. The Xilinx X1_Y24 transceiver in quad 119 is used for this, and the 125 MHz onboard clock required by GbE is connected to the REFCLK0 input for this quad. Ethernet functionality on the port must be provided by the FPGA firmware. An example design is available[2] which uses the Xilinx GbE IP core with software support provided by the LWIP implementation in the Xilinx SDK.

5. Multichannel High Speed Interface (XAUI)

AMC ports 8 – 11 are connected to the four FPGA serial transceivers in quad 213. The onboard 156.25 MHz oscillator is connected to the REFCLK0 input of this quad, and the TCLKA signal on the AMC interface is connected to the REFCLK1 input. Either clock can be selected by firmware as the transceiver reference clock. By default, these ports are intended to be used as a XAUI interface between the OTC and its carrier. However, the transceivers are not XAUI specific, so other protocols (e.g. PCI-e) could be implemented in the FPGA instead of XAUI provided the ATCA carrier uses the same protocol.

6. GBT Interface

AMC ports 12, 13 and 20 are connected to three serial transceivers in quad 119[4]. The 125 MHz oscillator output is connected to REFCLK0, and the output of the clock synthesizer driven by the recovered LHC clock or onboard 40.079 MHz is connected to REFCLK1. Like the XAUI and GbE interfaces,

[4] The fourth transceiver in the quad is used for the GbE interface on port 0 and is described in Sec. 3.

these transceivers are general purpose. The main intent is the use of REFCK1 to provide at least one (and up to three) GBT connection(s) to the ATCA carrier for the interface to the ATLAS TDAQ system.

7. Optical I/O: 48 Channel High Density Transmitter and Receiver (micropod) Interface

The main purpose of the OTC is to receive up to 48 input channels of raw data, process the data in the FPGA, and transmit the results on up to 48 output channels. The input and output are each provided through 4 micropod 12-channel optical receivers (AFBR-78D1SZ) and 4 micropod 12-channel optical transmitters (AFBR-77D1SZ) all of which are in sockets on the OTC and which use a custom heat sink. These I/O channels are connected to 48 transceivers (12 quads) of the FPGA. Each transceiver handles one micropod input and one micropod output channel. The correspondence between the micropod channels and transceivers is shown in Table 5.

The reference clocks for the transceivers come from the outputs of the clock synthesizer. To reduce the fan out demand, only one third of the transceiver quads have their reference clock input pins directly connected to the synthesizer outputs. The other quads must take their reference clock from an adjacent quad using the Xilinx "north clock" and "south clock" reference clock input choice. The clock connections are shown as the "S0" through "S7" entries in Table 4.

Micropod Channel		Xilinx Transceiver	Micropod Channel		Xilinx Transceiver	Micropod Channel		Xilinx Transceiver	Micropod Part/Chan		Xilinx Transceiver
Tx	Rx		Tx	Rx		Tx	Rx		Tx	Rx	
U16/0	U5/0	X1_Y0	U17/0	U6/0	X1_Y12	U18/0	U7/0	X0_Y24	U19/0	U8/0	X0_Y12
1	1	X1_Y1	1	1	X1_Y13	1	1	X0_Y25	1	1	X0_Y13
2	2	X1_Y2	2	2	X1_Y14	2	2	X0_Y26	2	2	X0_Y14
3	3	X1_Y3	3	3	X1_Y15	3	3	X0_Y27	3	3	X0_Y15
4	4	X1_Y4	4	4	X1_Y16	4	4	X0_Y20	4	4	X0_Y8
5	5	X1_Y5	5	5	X1_Y17	5	5	X0_Y21	5	5	X0_Y9
6	6	X1_Y6	6	6	X1_Y18	6	6	X0_Y22	6	6	X0_Y10
7	7	X1_Y7	7	7	X1_Y19	7	7	X0_Y23	7	7	X0_Y11
8	8	X1_Y8	8	8	X1_Y20	8	8	X0_Y16	8	8	X0_Y4
9	9	X1_Y9	9	9	X1_Y21	9	9	X0_Y17	9	9	X0_Y5
10	10	X1_Y10	10	10	X1_Y22	10	10	X0_Y18	10	10	X0_Y6
11	11	X1_Y11	11	11	X1_Y23	11	11	X0_Y19	11	11	X0_Y7

Table 5: The micropod receiver and transmitter channel to Xilinx transceiver connections

8. Generic I/O (LVDS) Interface

AMC ports 18 and 19 are connected to Xilinx Select I/O pins. These can be configured as 1.8V compatible LVDS signals to form standard AMC ports, or they can be user defined for any configuration allowed by Select I/O pins. The signals on port 18 are connected to Xilinx "clock compatible" Select I/O pins. The connections between the ports and the Xilinx FPGA are shown in Table 6.

AMC Port	AMC Signal	Xilinx Pin Name	Xilinx Pin
18	TXP	IO_L12P_T1_MRCC_19	H28
	TXN	IO_L12N_T1_MRCC_19	H29
	RXP	IO_L13P_T2_MRCC_19	K27
	RXN	IO_L13N_T2_MRCC_19	J27
19	TXP	IO_L4P_T0_19	C28
	TXN	IO_L4N_T0_19	B28
	RXP	IO_L5P_T0_19	B26
	RXN	IO_L5N_T0_19	A26

Table 6: The OTC generic I/O connections provided through the AMC connector

References

[1] CERN MMC design document NEED TO FIND

[2] http://sbhep-nt.physics.sunysb.edu/~hobbs/FPGAStuff/OpticalTestCard-f301-s300.zip The xaxiemacif.c file in the Xilinx SDK distribution has to be edited. The version in this zip file has the two edits which involve adding #ifdef statements testing on *XPAR_AXIETHERNET_0_CONNECTED_TYPE*.

Appendix A: FPGA Connections

Pin	Pin Name	Bank	Signal Name	Description
AY31	IO_L9P_T1_DQS_14	14	FPGA_CLK_SYNCn	Synchronize CDCM6208 Clock IC
BA31	IO_L9N_T1_DQS_D13_14	14	FPGA_CLK_RSTn	Reset CDCM6208 Clock IC
AY28	IO_L10P_T1_D14_14	14	FPGA_CLKSEL	0 = local Osc., 1 = AMC_FCLKA
AV29	IO_L14N_T2_SRCC_14	14	FPGA_SCL0	I2C for uPODs and CDCM6208
AN27	IO_L15P_T2_DQS_RDWR_B_14	14	FPGA_SDA0	I2C for uPODs and CDCM6208
AP27	IO_L15N_T2_DQS_DOUT_CSO_B	14	FPGA_SCL1	I2C connection to MMC
AT28	IO_L16P_T2_CSI_B_14	14	FPGA_SDA1	I2C connection to MMC
AT29	IO_L16N_T2_A15_D31_14	14	FPGA_uPOD_RSTn	reset all uPODs (active low)
AP29	IO_L17P_T2_A14_D30_14	14	FPGA_OUT1	GP output to MMC
AP30	IO_L17N_T2_A13_D29_14	14	uPOD_INT0	uPOD interrupt signal
AR28	IO_L18P_T2_A12_D28_14	14	uPOD_INT1	uPOD interrupt signal
AR29	IO_L18N_T2_A11_D27_14	14	uPOD_INT2	uPOD interrupt signal
AN28	IO_L19P_T3_A10_D26_14	14	uPOD_INT3	uPOD interrupt signal
AN29	IO_L19N_T3_A09_D25_VREF_1	14	uPOD_INT4	uPOD interrupt signal
AM30	IO_L20P_T3_A08_D24_14	14	uPOD_INT5	uPOD interrupt signal
AN30	IO_L20N_T3_A07_D23_14	14	uPOD_INT6	uPOD interrupt signal
AK27	IO_L21P_T3_DQS_14	14	uPOD_INT7	uPOD interrupt signal
AK28	IO_L21N_T3_DQS_A06_D22_14	14	FPGA_CLK_STATUS0	CDCM6208 status
AM27	IO_L22P_T3_A05_D21_14	14	FPGA_CLK_STATUS1	CDCM6208 status
AM28	IO_L22N_T3_A04_D20_14	14	FPGA_RESET	input from MMC
AJ29	IO_L23P_T3_A03_D19_14	14	FPGA_OUT0	GP output to MMC
AK29	IO_L23N_T3_A02_D18_14	14	FPGA_IN0	GP input from MMC
AL28	IO_L24P_T3_A01_D17_14	14	FPGA_IN1	GP input from MMC
AL29	IO_L24N_T3_A00_D16_14	14	FPGA_IN2	GP input from MMC
C28	IO_L4P_T0_19	19	LVDS_Tx2p	LVDS connected to AMC Port[19]
B28	IO_L4N_T0_19	19	LVDS_Tx2n	LVDS connected to AMC Port[19]
B26	IO_L5P_T0_19	19	LVDS_Rx2p	LVDS connected to AMC Port[19]
A26	IO_L5N_T0_19	19	LVDS_Rx2n	LVDS connected to AMC Port[19]
H28	IO_L12P_T1_MRCC_19	19	LVDS_Tx1p	LVDS connected to AMC Port[18]
H29	IO_L12N_T1_MRCC_19	19	LVDS_Tx1n	LVDS connected to AMC Port[18]
K27	IO_L13P_T2_MRCC_19	19	LVDS_Rx1p	LVDS connected to AMC Port[18]
J27	IO_L13N_T2_MRCC_19	19	LVDS_Rx1n	LVDS connected to AMC Port[18]
BA18	IO_L1P_T0_34	34	DDRdm0	DDR Memory Interface
BB18	IO_L1N_T0_34	34	DDRdata0	DDR Memory Interface
BC19	IO_L2P_T0_34	34	DDRdata1	DDR Memory Interface
BC18	IO_L2N_T0_34	34	DDRdata2	DDR Memory Interface
BB17	IO_L3P_T0_DQS_34	34	DDRdqs0	DDR Memory Interface
BC17	IO_L3N_T0_DQS_34	34	DDRdqs0n	DDR Memory Interface
BD17	IO_L4P_T0_34	34	DDRdata3	DDR Memory Interface

Pin	Pin Name	Bank	Signal Name	Description
BD16	IO_L4N_T0_34	34	DDRdata4	DDR Memory Interface
BC15	IO_L5P_T0_34	34	DDRdata5	DDR Memory Interface
BD15	IO_L5N_T0_34	34	DDRdata6	DDR Memory Interface
BB16	IO_L6P_T0_34	34	DDRdata7	DDR Memory Interface
AW17	IO_L7P_T1_34	34	DDRdm1	DDR Memory Interface
AY16	IO_L7N_T1_34	34	DDRdata8	DDR Memory Interface
AY18	IO_L8P_T1_34	34	DDRdata9	DDR Memory Interface
AY17	IO_L8N_T1_34	34	DDRdata10	DDR Memory Interface
AW16	IO_L9P_T1_DQS_34	34	DDRdqs1	DDR Memory Interface
AW15	IO_L9N_T1_DQS_34	34	DDRdqs1n	DDR Memory Interface
BA16	IO_L10P_T1_34	34	DDRdata11	DDR Memory Interface
BA15	IO_L10N_T1_34	34	DDRdata12	DDR Memory Interface
AV18	IO_L11P_T1_SRCC_34	34	DDRdata13	DDR Memory Interface
AV17	IO_L11N_T1_SRCC_34	34	DDRdata14	DDR Memory Interface
AU15	IO_L12P_T1_MRCC_34	34	DDRdata15	DDR Memory Interface
BB22	IO_L1P_T0_AD4P_35	35	DDRadr13	DDR Memory Interface
BB21	IO_L1N_T0_AD4N_35	35	DDRadr12	DDR Memory Interface
BC22	IO_L2P_T0_AD12P_35	35	DDRadr11	DDR Memory Interface
BD22	IO_L2N_T0_AD12N_35	35	DDRadr10	DDR Memory Interface
BC20	IO_L3P_T0_DQS_AD5P_35	35	DDRCLKp	DDR Memory Interface
BD19	IO_L3N_T0_DQS_AD5N_35	35	DDRCLKn	DDR Memory Interface
BD21	IO_L4P_T0_35	35	DDRadr9	DDR Memory Interface
BD20	IO_L4N_T0_35	35	DDRadr8	DDR Memory Interface
BA21	IO_L5P_T0_AD13P_35	35	DDRadr7	DDR Memory Interface
BB20	IO_L5N_T0_AD13N_35	35	DDRadr6	DDR Memory Interface
BA20	IO_L6P_T0_35	35	DDRadr5	DDR Memory Interface
BA19	IO_L6N_T0_VREF_35	35	DDRadr4	DDR Memory Interface
AW22	IO_L7P_T1_AD6P_35	35	DDRadr3	DDR Memory Interface
AY22	IO_L7N_T1_AD6N_35	35	DDRadr2	DDR Memory Interface
AV20	IO_L8P_T1_AD14P_35	35	DDRadr1	DDR Memory Interface
AW20	IO_L8N_T1_AD14N_35	35	DDRadr0	DDR Memory Interface
AW21	IO_L9P_T1_DQS_AD7P_35	35	DDRba2	DDR Memory Interface
AY21	IO_L9N_T1_DQS_AD7N_35	35	DDRba1	DDR Memory Interface
AW19	IO_L10P_T1_AD15P_35	35	DDRba0	DDR Memory Interface
AY19	IO_L10N_T1_AD15N_35	35	DDRrasn	DDR Memory Interface
AU22	IO_L11P_T1_SRCC_35	35	DDRcasn	DDR Memory Interface
AV22	IO_L11N_T1_SRCC_35	35	DDRwen	DDR Memory Interface
AU20	IO_L12P_T1_MRCC_35	35	DDRcsn	DDR Memory Interface
AT21	IO_L13P_T2_MRCC_35	35	SYSCLKp	DDR Memory Interface
AU21	IO_L13N_T2_MRCC_35	35	SYSCLKn	DDR Memory Interface
AP21	IO_L15P_T2_DQS_35	35	DDRcke	DDR Memory Interface

Pin	Pin Name	Bank	Signal Name	Description
AP20	IO_L15N_T2_DQS_35	35	DDRodt	DDR Memory Interface
AV14	IO_L13P_T2_MRCC_36	36	DDRdata24	DDR Memory Interface
AW14	IO_L13N_T2_MRCC_36	36	DDRdata25	DDR Memory Interface
AW11	IO_L14P_T2_SRCC_36	36	DDRdata26	DDR Memory Interface
AW10	IO_L14N_T2_SRCC_36	36	DDRdata27	DDR Memory Interface
AY13	IO_L15P_T2_DQS_36	36	DDRdqs3	DDR Memory Interface
BA13	IO_L15N_T2_DQS_36	36	DDRdqs3n	DDR Memory Interface
AY12	IO_L16P_T2_36	36	DDRdm3	DDR Memory Interface
AY11	IO_L16N_T2_36	36	DDRdata28	DDR Memory Interface
BA11	IO_L17P_T2_36	36	DDRdata29	DDR Memory Interface
BA10	IO_L17N_T2_36	36	DDRdata30	DDR Memory Interface
AY14	IO_L18P_T2_36	36	DDRdata31	DDR Memory Interface
BA14	IO_L18N_T2_36	36	DDRrstn	DDR Memory Interface
BB11	IO_L19P_T3_36	36	DDRdm2	DDR Memory Interface
BB12	IO_L20P_T3_36	36	DDRdata16	DDR Memory Interface
BC12	IO_L20N_T3_36	36	DDRdata17	DDR Memory Interface
BD12	IO_L21P_T3_DQS_36	36	DDRdqs2	DDR Memory Interface
BD11	IO_L21N_T3_DQS_36	36	DDRdqs2n	DDR Memory Interface
BB13	IO_L22P_T3_36	36	DDRdata18	DDR Memory Interface
BC13	IO_L22N_T3_36	36	DDRdata19	DDR Memory Interface
BC14	IO_L23P_T3_36	36	DDRdata20	DDR Memory Interface
BD14	IO_L23N_T3_36	36	DDRdata21	DDR Memory Interface
BC10	IO_L24P_T3_36	36	DDRdata22	DDR Memory Interface
BD10	IO_L24N_T3_36	36	DDRdata23	DDR Memory Interface
AG2	MGTXTXP3_113	113	Tx03p	Connection to uPOD_Tx U16
AE6	MGTXRXP3_113		Rx03p	Connection to uPOD_Rx U5
AG1	MGTXTXN3_113		Tx03n	Connection to uPOD_Tx U16
AE5	MGTXRXN3_113		Rx03n	Connection to uPOD_Rx U5
AH4	MGTXTXP2_113		Tx02p	Connection to uPOD_Tx U16
AG6	MGTXRXP2_113		Rx02p	Connection to uPOD_Rx U5
AH3	MGTXTXN2_113		Tx02n	Connection to uPOD_Tx U16
AG5	MGTXRXN2_113		Rx02n	Connection to uPOD_Rx U5
AJ2	MGTXTXP1_113		Tx01p	Connection to uPOD_Tx U16
AJ6	MGTXRXP1_113		Rx01p	Connection to uPOD_Rx U5
AJ1	MGTXTXN1_113		Tx01n	Connection to uPOD_Tx U16
AJ5	MGTXRXN1_113		Rx01n	Connection to uPOD_Rx U5
AK4	MGTXTXP0_113		Tx00p	Connection to uPOD_Tx U16
AK8	MGTXRXP0_113		Rx00p	Connection to uPOD_Rx U5
AK3	MGTXTXN0_113		Tx00n	Connection to uPOD_Tx U16
AK7	MGTXRXN0_113		Rx00n	Connection to uPOD_Rx U5
AC2	MGTXTXP3_114	114	Tx07p	Connection to uPOD_Tx U16

Pin	Pin Name	Bank	Signal Name	Description
Y8	MGTXRXP3_114	114	Rx07p	Connection to uPOD_Rx U5
AC1	MGTXTXN3_114	114	Tx07n	Connection to uPOD_Tx U16
Y7	MGTXRXN3_114	114	Rx07n	Connection to uPOD_Rx U5
AD4	MGTXTXP2_114	114	Tx06p	Connection to uPOD_Tx U16
AA6	MGTXRXP2_114	114	Rx06p	Connection to uPOD_Rx U5
AD3	MGTXTXN2_114	114	Tx06n	Connection to uPOD_Tx U16
AA10	MGTREFCLK0P_114	114	REFCLK_0p	Ref. Clock for Quads 113, 114, 115
AA5	MGTXRXN2_114	114	Rx06n	Connection to uPOD_Rx U5
AA9	MGTREFCLK0N_114	114	REFCLK_0n	Ref. Clock for Quads 113, 114, 115
AB7	MGTREFCLK1N_114	114	REFCLK_4n	Ref. Clock for Quads 113, 114, 115
AB8	MGTREFCLK1P_114	114	REFCLK_4p	Ref. Clock for Quads 113, 114, 115
AE2	MGTXTXP1_114	114	Tx05p	Connection to uPOD_Tx U16
AC6	MGTXRXP1_114	114	Rx05p	Connection to uPOD_Rx U5
AE1	MGTXTXN1_114	114	Tx05n	Connection to uPOD_Tx U16
AC5	MGTXRXN1_114	114	Rx05n	Connection to uPOD_Rx U5
AF4	MGTXTXP0_114	114	Tx04p	Connection to uPOD_Tx U16
AD8	MGTXRXP0_114	114	Rx04p	Connection to uPOD_Rx U5
AF3	MGTXTXN0_114	114	Tx04n	Connection to uPOD_Tx U16
AD7	MGTXRXN0_114	114	Rx04n	Connection to uPOD_Rx U5
W2	MGTXTXP3_115	115	Tx11p	Connection to uPOD_Tx U16
T8	MGTXRXP3_115	115	Rx11p	Connection to uPOD_Rx U5
W1	MGTXTXN3_115	115	Tx11n	Connection to uPOD_Tx U16
T7	MGTXRXN3_115	115	Rx11n	Connection to uPOD_Rx U5
Y4	MGTXTXP2_115	115	Tx10p	Connection to uPOD_Tx U16
U6	MGTXRXP2_115	115	Rx10p	Connection to uPOD_Rx U5
Y3	MGTXTXN2_115	115	Tx10n	Connection to uPOD_Tx U16
U5	MGTXRXN2_115	115	Rx10n	Connection to uPOD_Rx U5
AA2	MGTXTXP1_115	115	Tx09p	Connection to uPOD_Tx U16
V8	MGTXRXP1_115	115	Rx09p	Connection to uPOD_Rx U5
AA1	MGTXTXN1_115	115	Tx09n	Connection to uPOD_Tx U16
V7	MGTXRXN1_115	115	Rx09n	Connection to uPOD_Rx U5
AB4	MGTXTXP0_115	115	Tx08p	Connection to uPOD_Tx U16
W6	MGTXRXP0_115	115	Rx08p	Connection to uPOD_Rx U5
AB3	MGTXTXN0_115	115	Tx08n	Connection to uPOD_Tx U16
W5	MGTXRXN0_115	115	Rx08n	Connection to uPOD_Rx U5
R2	MGTXTXP3_116	116	Tx15p	Connection to uPOD_Tx U17
M8	MGTXRXP3_116	116	Rx15p	Connection to uPOD_Rx U6
R1	MGTXTXN3_116	116	Tx15n	Connection to uPOD_Tx U17
M7	MGTXRXN3_116	116	Rx15n	Connection to uPOD_Rx U6
T4	MGTXTXP2_116	116	Tx14p	Connection to uPOD_Tx U17
N6	MGTXRXP2_116	116	Rx14p	Connection to uPOD_Rx U6

Pin	Pin Name	Bank	Signal Name	Description
T3	MGTXTXN2_116	116	Tx14n	Connection to uPOD_Tx U17
N5	MGTXRXN2_116	116	Rx14n	Connection to uPOD_Rx U6
U2	MGTXTXP1_116	116	Tx13p	Connection to uPOD_Tx U17
P8	MGTXRXP1_116	116	Rx13p	Connection to uPOD_Rx U6
U1	MGTXTXN1_116	116	Tx13n	Connection to uPOD_Tx U17
P7	MGTXRXN1_116	116	Rx13n	Connection to uPOD_Rx U6
V4	MGTXTXP0_116	116	Tx12p	Connection to uPOD_Tx U17
R6	MGTXRXP0_116	116	Rx12p	Connection to uPOD_Rx U6
V3	MGTXTXN0_116	116	Tx12n	Connection to uPOD_Tx U17
R5	MGTXRXN0_116	116	Rx12n	Connection to uPOD_Rx U6
L2	MGTXTXP3_117	117	Tx19p	Connection to uPOD_Tx U17
H8	MGTXRXP3_117	117	Rx19p	Connection to uPOD_Rx U6
L1	MGTXTXN3_117	117	Tx19n	Connection to uPOD_Tx U17
H7	MGTXRXN3_117	117	Rx19n	Connection to uPOD_Rx U6
M4	MGTXTXP2_117	117	Tx18p	Connection to uPOD_Tx U17
J6	MGTXRXP2_117	117	Rx18p	Connection to uPOD_Rx U6
M3	MGTXTXN2_117	117	Tx18n	Connection to uPOD_Tx U17
J10	MGTREFCLK0P_117	117	REFCLK_1p	Ref. Clock for Quads 116, 117, 118
J5	MGTXRXN2_117	117	Rx18n	Connection to uPOD_Rx U6
J9	MGTREFCLK0N_117	117	REFCLK_1n	Ref. Clock for Quads 116, 117, 118
L9	MGTREFCLK1N_117	117	REFCLK_5n	Ref. Clock for Quads 116, 117, 118
L10	MGTREFCLK1P_117	117	REFCLK_5p	Ref. Clock for Quads 116, 117, 118
N2	MGTXTXP1_117	117	Tx17p	Connection to uPOD_Tx U17
K8	MGTXRXP1_117	117	Rx17p	Connection to uPOD_Rx U6
N1	MGTXTXN1_117	117	Tx17n	Connection to uPOD_Tx U17
K7	MGTXRXN1_117	117	Rx17n	Connection to uPOD_Rx U6
P4	MGTXTXP0_117	117	Tx16p	Connection to uPOD_Tx U17
L6	MGTXRXP0_117	117	Rx16p	Connection to uPOD_Rx U6
P3	MGTXTXN0_117	117	Tx16n	Connection to uPOD_Tx U17
L5	MGTXRXN0_117	117	Rx16n	Connection to uPOD_Rx U6
G2	MGTXTXP3_118	118	Tx23p	Connection to uPOD_Tx U17
D8	MGTXRXP3_118	118	Rx23p	Connection to uPOD_Rx U6
G1	MGTXTXN3_118	118	Tx23n	Connection to uPOD_Tx U17
D7	MGTXRXN3_118	118	Rx23n	Connection to uPOD_Rx U6
H4	MGTXTXP2_118	118	Tx22p	Connection to uPOD_Tx U17
E6	MGTXRXP2_118	118	Rx22p	Connection to uPOD_Rx U6
H3	MGTXTXN2_118	118	Tx22n	Connection to uPOD_Tx U17
E5	MGTXRXN2_118	118	Rx22n	Connection to uPOD_Rx U6
J2	MGTXTXP1_118	118	Tx21p	Connection to uPOD_Tx U17
F8	MGTXRXP1_118	118	Rx21p	Connection to uPOD_Rx U6
J1	MGTXTXN1_118	118	Tx21n	Connection to uPOD_Tx U17

Pin	Pin Name	Bank	Signal Name	Description
F7	MGTXRXN1_118	118	Rx21n	Connection to uPOD_Rx U6
K4	MGTXTXP0_118	118	Tx20p	Connection to uPOD_Tx U17
G6	MGTXRXP0_118	118	Rx20p	Connection to uPOD_Rx U6
K3	MGTXTXN0_118	118	Tx20n	Connection to uPOD_Tx U17
G5	MGTXRXN0_118	118	Rx20n	Connection to uPOD_Rx U6
B4	MGTXTXP3_119	119	GbE_Tx3p	connected to AMC_Port[20]
A6	MGTXRXP3_119	119	GbE_Rx3p	connected to AMC_Port[20]
B3	MGTXTXN3_119	119	GbE_Tx3n	connected to AMC_Port[20]
A5	MGTXRXN3_119	119	GbE_Rx3n	connected to AMC_Port[20]
C2	MGTXTXP2_119	119	GbE_Tx2p	connected to AMC_Port[13]
B8	MGTXRXP2_119	119	GbE_Rx2p	connected to AMC_Port[13]
C1	MGTXTXN2_119	119	GbE_Tx2n	connected to AMC_Port[13]
A10	MGTREFCLK0P_119	119	GbECLKp	Ref. Clock for GbE Channels
B7	MGTXRXN2_119	119	GbE_Rx2n	connected to AMC_Port[13]
A9	MGTREFCLK0N_119	119	GbECLKn	Ref. Clock for GbE Channels
C9	MGTREFCLK1N_119	119	REFCLK_8n	Ref. Clock for GbE Channels
C10	MGTREFCLK1P_119	119	REFCLK_8p	Ref. Clock for GbE Channels
E2	MGTXTXP1_119	119	GbE_Tx1p	connected to AMC_Port[12]
C6	MGTXRXP1_119	119	GbE_Rx1p	connected to AMC_Port[12]
E1	MGTXTXN1_119	119	GbE_Tx1n	connected to AMC_Port[12]
C5	MGTXRXN1_119	119	GbE_Rx1n	connected to AMC_Port[12]
F4	MGTXTXP0_119	119	GbE_Tx0p	connected to AMC_Port[0]
D4	MGTXRXP0_119	119	GbE_Rx0p	connected to AMC_Port[0]
F3	MGTXTXN0_119	119	GbE_Tx0n	connected to AMC_Port[0]
D3	MGTXRXN0_119	119	GbE_Rx0n	connected to AMC_Port[0]
AG43	MGTXTXP3_213	213	XAUI_Tx3p	connected to AMC_Port[11]
AE39	MGTXRXP3_213	213	XAUI_Rx3p	connected to AMC_Port[11]
AG44	MGTXTXN3_213	213	XAUI_Tx3n	connected to AMC_Port[11]
AE40	MGTXRXN3_213	213	XAUI_Rx3n	connected to AMC_Port[11]
AH41	MGTXTXP2_213	213	XAUI_Tx2p	connected to AMC_Port[10]
AG39	MGTXRXP2_213	213	XAUI_Rx2p	connected to AMC_Port[10]
AH42	MGTXTXN2_213	213	XAUI_Tx2n	connected to AMC_Port[10]
AF37	MGTREFCLK0P_213	213	XAUICLKp	Ref. Clock for XAUI Channels
AG40	MGTXRXN2_213	213	XAUI_Rx2n	connected to AMC_Port[10]
AF38	MGTREFCLK0N_213	213	XAUICLKn	Ref. Clock for XAUI Channels
AH38	MGTREFCLK1N_213	213	AMC_TCLKAn	Ref. Clock for XAUI Channels
AH37	MGTREFCLK1P_213	213	AMC_TCLKAp	Ref. Clock for XAUI Channels
AJ43	MGTXTXP1_213	213	XAUI_Tx1p	connected to AMC_Port[9]
AJ39	MGTXRXP1_213	213	XAUI_Rx1p	connected to AMC_Port[9]
AJ44	MGTXTXN1_213	213	XAUI_Tx1n	connected to AMC_Port[9]
AJ40	MGTXRXN1_213	213	XAUI_Rx1n	connected to AMC_Port[9]

Pin	Pin Name	Bank	Signal Name	Description
AK41	MGTXTXP0_213	213	XAUI_Tx0p	connected to AMC_Port[8]
AK37	MGTXRXP0_213	213	XAUI_Rx0p	connected to AMC_Port[8]
AK42	MGTXTXN0_213	213	XAUI_Tx0n	connected to AMC_Port[8]
AK38	MGTXRXN0_213	213	XAUI_Rx0n	connected to AMC_Port[8]
AC43	MGTXTXP3_214	214	Tx47p	Connection to uPOD_Tx U19
Y37	MGTXRXP3_214	214	Rx47p	Connection to uPOD_Rx U8
AC44	MGTXTXN3_214	214	Tx47n	Connection to uPOD_Tx U19
Y38	MGTXRXN3_214	214	Rx47n	Connection to uPOD_Rx U8
AD41	MGTXTXP2_214	214	Tx46p	Connection to uPOD_Tx U19
AA39	MGTXRXP2_214	214	Rx46p	Connection to uPOD_Rx U8
AD42	MGTXTXN2_214	214	Tx46n	Connection to uPOD_Tx U19
AA40	MGTXRXN2_214	214	Rx46n	Connection to uPOD_Rx U8
AE43	MGTXTXP1_214	214	Tx45p	Connection to uPOD_Tx U19
AC39	MGTXRXP1_214	214	Rx45p	Connection to uPOD_Rx U8
AE44	MGTXTXN1_214	214	Tx45n	Connection to uPOD_Tx U19
AC40	MGTXRXN1_214	214	Rx45n	Connection to uPOD_Rx U8
AF41	MGTXTXP0_214	214	Tx44p	Connection to uPOD_Tx U19
AD37	MGTXRXP0_214	214	Rx44p	Connection to uPOD_Rx U8
AF42	MGTXTXN0_214	214	Tx44n	Connection to uPOD_Tx U19
AD38	MGTXRXN0_214	214	Rx44n	Connection to uPOD_Rx U8
W43	MGTXTXP3_215	215	Tx43p	Connection to uPOD_Tx U19
T37	MGTXRXP3_215	215	Rx43p	Connection to uPOD_Rx U8
W44	MGTXTXN3_215	215	Tx43n	Connection to uPOD_Tx U19
T38	MGTXRXN3_215	215	Rx43n	Connection to uPOD_Rx U8
Y41	MGTXTXP2_215	215	Tx42p	Connection to uPOD_Tx U19
U39	MGTXRXP2_215	215	Rx42p	Connection to uPOD_Rx U8
Y42	MGTXTXN2_215	215	Tx42n	Connection to uPOD_Tx U19
U35	MGTREFCLK0P_215	215	REFCLK_2p	Ref. Clock for Quads 214, 215, 216
U40	MGTXRXN2_215	215	Rx42n	Connection to uPOD_Rx U8
U36	MGTREFCLK0N_215	215	REFCLK_2n	Ref. Clock for Quads 214, 215, 216
W36	MGTREFCLK1N_215	215	REFCLK_6n	Ref. Clock for Quads 214, 215, 216
W35	MGTREFCLK1P_215	215	REFCLK_6p	Ref. Clock for Quads 214, 215, 216
AA43	MGTXTXP1_215	215	Tx41p	Connection to uPOD_Tx U19
V37	MGTXRXP1_215	215	Rx41p	Connection to uPOD_Rx U8
AA44	MGTXTXN1_215	215	Tx41n	Connection to uPOD_Tx U19
V38	MGTXRXN1_215	215	Rx41n	Connection to uPOD_Rx U8
AB41	MGTXTXP0_215	215	Tx40p	Connection to uPOD_Tx U19
W39	MGTXRXP0_215	215	Rx40p	Connection to uPOD_Rx U8
AB42	MGTXTXN0_215	215	Tx40n	Connection to uPOD_Tx U19
W40	MGTXRXN0_215	215	Rx40n	Connection to uPOD_Rx U8
R43	MGTXTXP3_216	216	Tx39p	Connection to uPOD_Tx U19

Pin	Pin Name	Bank	Signal Name	Description
M37	MGTXRXP3_216	216	Rx39p	Connection to uPOD_Rx U8
R44	MGTXTXN3_216	216	Tx39n	Connection to uPOD_Tx U19
M38	MGTXRXN3_216	216	Rx39n	Connection to uPOD_Rx U8
T41	MGTXTXP2_216	216	Tx38p	Connection to uPOD_Tx U19
N39	MGTXRXP2_216	216	Rx38p	Connection to uPOD_Rx U8
T42	MGTXTXN2_216	216	Tx38n	Connection to uPOD_Tx U19
N40	MGTXRXN2_216	216	Rx38n	Connection to uPOD_Rx U8
U43	MGTXTXP1_216	216	Tx37p	Connection to uPOD_Tx U19
P37	MGTXRXP1_216	216	Rx37p	Connection to uPOD_Rx U8
U44	MGTXTXN1_216	216	Tx37n	Connection to uPOD_Tx U19
P38	MGTXRXN1_216	216	Rx37n	Connection to uPOD_Rx U8
V41	MGTXTXP0_216	216	Tx36p	Connection to uPOD_Tx U19
R39	MGTXRXP0_216	216	Rx36p	Connection to uPOD_Rx U8
V42	MGTXTXN0_216	216	Tx36n	Connection to uPOD_Tx U19
R40	MGTXRXN0_216	216	Rx36n	Connection to uPOD_Rx U8
L43	MGTXTXP3_217	217	Tx35p	Connection to uPOD_Tx U18
H37	MGTXRXP3_217	217	Rx35p	Connection to uPOD_Rx U7
L44	MGTXTXN3_217	217	Tx35n	Connection to uPOD_Tx U18
H38	MGTXRXN3_217	217	Rx35n	Connection to uPOD_Rx U7
M41	MGTXTXP2_217	217	Tx34p	Connection to uPOD_Tx U18
J39	MGTXRXP2_217	217	Rx34p	Connection to uPOD_Rx U7
M42	MGTXTXN2_217	217	Tx34n	Connection to uPOD_Tx U18
J40	MGTXRXN2_217	217	Rx34n	Connection to uPOD_Rx U7
N43	MGTXTXP1_217	217	Tx33p	Connection to uPOD_Tx U18
K37	MGTXRXP1_217	217	Rx33p	Connection to uPOD_Rx U7
N44	MGTXTXN1_217	217	Tx33n	Connection to uPOD_Tx U18
K38	MGTXRXN1_217	217	Rx33n	Connection to uPOD_Rx U7
P41	MGTXTXP0_217	217	Tx32p	Connection to uPOD_Tx U18
L39	MGTXRXP0_217	217	Rx32p	Connection to uPOD_Rx U7
P42	MGTXTXN0_217	217	Tx32n	Connection to uPOD_Tx U18
L40	MGTXRXN0_217	217	Rx32n	Connection to uPOD_Rx U7
G43	MGTXTXP3_218	218	Tx31p	Connection to uPOD_Tx U18
D37	MGTXRXP3_218	218	Rx31p	Connection to uPOD_Rx U7
G44	MGTXTXN3_218	218	Tx31n	Connection to uPOD_Tx U18
D38	MGTXRXN3_218	218	Rx31n	Connection to uPOD_Rx U7
H41	MGTXTXP2_218	218	Tx30p	Connection to uPOD_Tx U18
E39	MGTXRXP2_218	218	Rx30p	Connection to uPOD_Rx U7
H42	MGTXTXN2_218	218	Tx30n	Connection to uPOD_Tx U18
E35	MGTREFCLK0P_218	218	REFCLK_3p	Ref. Clock for Quads 217, 218, 219
E40	MGTXRXN2_218	218	Rx30n	Connection to uPOD_Rx U7
E36	MGTREFCLK0N_218	218	REFCLK_3n	Ref. Clock for Quads 217, 218, 219

Pin	Pin Name	Bank	Signal Name	Description
G36	MGTREFCLK1N_218	218	REFCLK_7n	Ref. Clock for Quads 217, 218, 219
G35	MGTREFCLK1P_218	218	REFCLK_7p	Ref. Clock for Quads 217, 218, 219
J43	MGTXTXP1_218	218	Tx29p	Connection to uPOD_Tx U18
F37	MGTXRXP1_218	218	Rx29p	Connection to uPOD_Rx U7
J44	MGTXTXN1_218	218	Tx29n	Connection to uPOD_Tx U18
F38	MGTXRXN1_218	218	Rx29n	Connection to uPOD_Rx U7
K41	MGTXTXP0_218	218	Tx28p	Connection to uPOD_Tx U18
G39	MGTXRXP0_218	218	Rx28p	Connection to uPOD_Rx U7
K42	MGTXTXN0_218	218	Tx28n	Connection to uPOD_Tx U18
G40	MGTXRXN0_218	218	Rx28n	Connection to uPOD_Rx U7
B41	MGTXTXP3_219	219	Tx27p	Connection to uPOD_Tx U18
A39	MGTXRXP3_219	219	Rx27p	Connection to uPOD_Rx U7
B42	MGTXTXN3_219	219	Tx27n	Connection to uPOD_Tx U18
A40	MGTXRXN3_219	219	Rx27n	Connection to uPOD_Rx U7
C43	MGTXTXP2_219	219	Tx26p	Connection to uPOD_Tx U18
B37	MGTXRXP2_219	219	Rx26p	Connection to uPOD_Rx U7
C44	MGTXTXN2_219	219	Tx26n	Connection to uPOD_Tx U18
B38	MGTXRXN2_219	219	Rx26n	Connection to uPOD_Rx U7
E43	MGTXTXP1_219	219	Tx25p	Connection to uPOD_Tx U18
C39	MGTXRXP1_219	219	Rx25p	Connection to uPOD_Rx U7
E44	MGTXTXN1_219	219	Tx25n	Connection to uPOD_Tx U18
C40	MGTXRXN1_219	219	Rx25n	Connection to uPOD_Rx U7
F41	MGTXTXP0_219	219	Tx24p	Connection to uPOD_Tx U18
D41	MGTXRXP0_219	219	Rx24p	Connection to uPOD_Rx U7
F42	MGTXTXN0_219	219	Tx24n	Connection to uPOD_Tx U18
D42	MGTXRXN0_219	219	Rx24n	Connection to uPOD_Rx U7