



Athena
simulation
data

Formatted
input file
(strip #, time,
FIFO address)

DAQ Interface for
communication

PC

1 FIFO per
VMM

8 FIFOs per
FEB

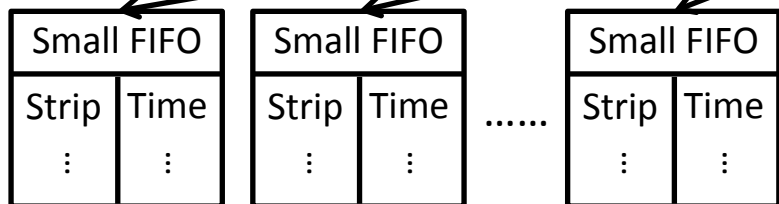
FPGA

Ethernet

Generic
interface

Address
decoder

20 bit
counter @
320 MHz



Time Check

Time Check

Time Check

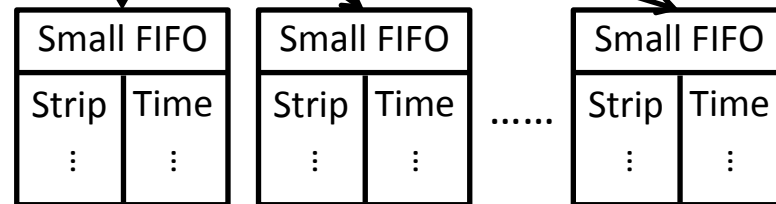
Serializer

Serializer

Serializer

Mini SAS to ADDCs

FEB 0



Time Check

Time Check

Time Check

Serializer

Serializer

Serializer

Mini SAS to ADDCs

FEB 7