**Specifications and Implementation of an ART ASIC prototype for the MicroMegas Trigger system of the NSW Detector**

1. **ART ASIC Specifications** [1]

The scheme for readout of trigger data for the MicroMegas detector in NSW is shown in the block diagram in Fig. 1.

For the Micromegas detector, the trigger data is generated by considering only the first arriving hit in each 64-channel front-end IC for a given bunch crossing. The strip address of the hit (Address-in-Real-Time) is promptly produced by the VMM chip in serial form.

The Address-in-Real-Time words generated by the front-end ASIC (VMM) are sent to the trigger processor in USA15 via optical links in two steps. First, the ART from each of 32 front-end VMMs (four MMFE’s) is serially transmitted, point-to-point, to a companion digital ASIC on the trigger data driver card; from there it is sent to USA15. The ASIC performs the following functions:

* Deserialize the ART stream and phase align the hits to the BC clock.
* Identify the strip addresses of up to a fixed number of hits by means of cascaded priority encoders.
* Append the 5-bit geographical VMM ASIC address to the strip address of each hit.
* Send the ART addresses and the 12-bit BCID to a GBT configured to operate in parallel mode without Forward Error Correction (FEC).

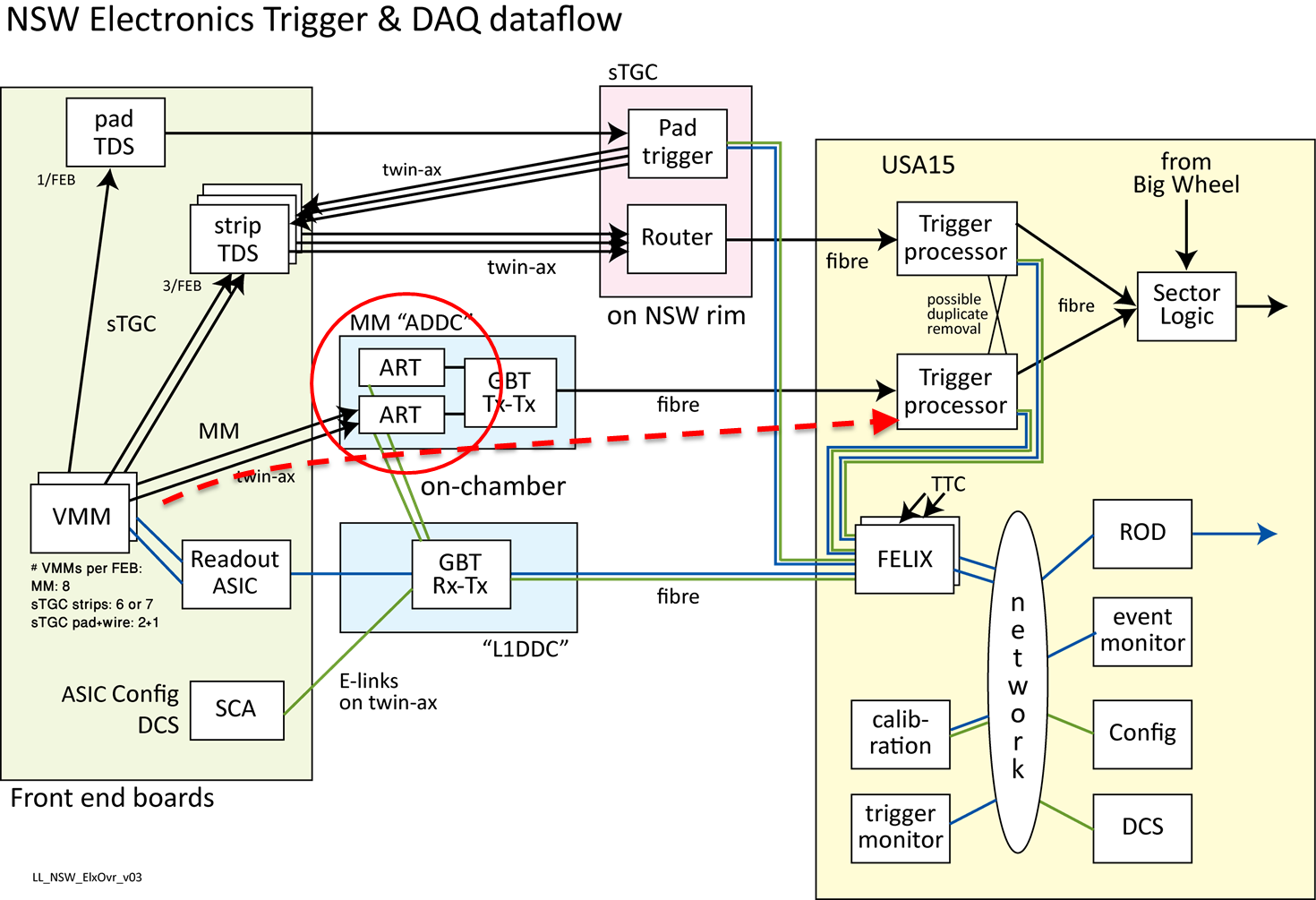


Figure 1. Block diagram of the Trigger and DAQ NSW electronics. The MicroMegas trigger path is designated with the red dotted arrow. The ART ASICs (red circle) are collecting trigger data (Address in Real Time) from the front-end VMM ASIC and formatting theoutput to the GBT chip. The information travels on fibers up to the Trigger Processors located in USA15.

There are a total of 1024 ART data driver cards. Their latency is about 2 BC. Using the dual Versatile Transmitter (VTTx) significantly reduces the cost per link. The absence of the downlink, however, requires that the ART ASIC receive its TTC and clock signals from the Level-1 event readout downlink and that the ART GBT transmitter also be configured via that downlink.

1. **Theory of Operation**



Figure 2. The ART signal

The ART signal generated by the VMM front-end ASIC (figure 2) consists of one bit flag, followed by 6 bits which indicate the address of the strip that received a hit. The internal circuitry of the VMM selects always the first channel that was hit, when more channels receive a signal at the same time. The serialization is done either at the falling edge of a 160 MHz clock or at both clock edges (double data rate). The ART circuitry of VMM has no relation to the 40 MHz BC clock, therefore the ART signal can appear at any moment inside the BC window (see Figure 3).

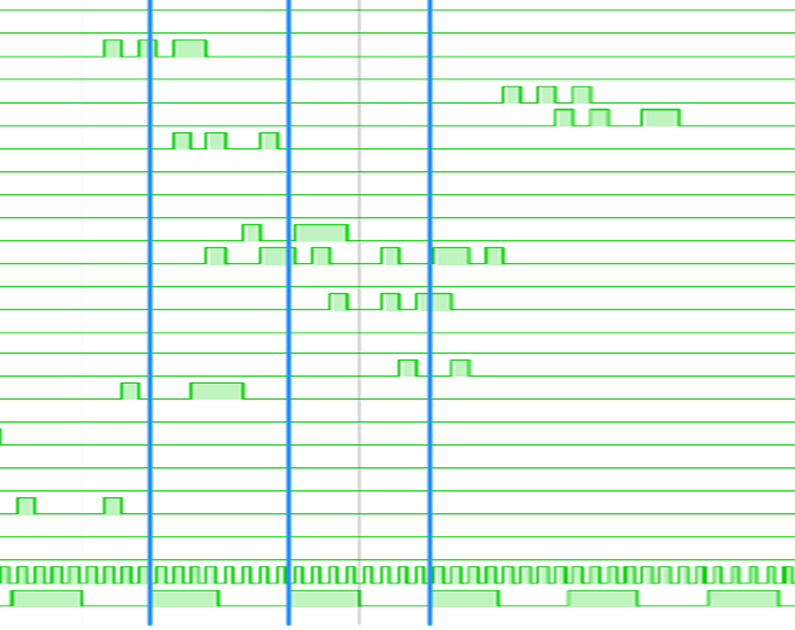


Figure 3. Simulation of ART signals at 160MHz double data rate transfer. The lower two signals are respectively a 320 MHz clock used for simulation and the 40 MHz BC clock

The ART ASIC will register all ART signals coming anywhere inside one BC window. In Figure 4 such the boundary between BC windows are represented with blue lines. The ART ASIC looks initially at the presence of flag bits. All ART flags which occurred between time 0 and time 1 are therefore known at time (1). The ASIC can perform the selection of the hits immediately, even if some of the ART signals have not completed yet (i.e. some of the 6 ART data bits are still flowing out of the VMM chips). Half BC is reserved for the hit selection operation. At time 1.5 (half BC time later) the hit selection is performed and the result is presented on the output bus. If there are more than 8 VMMs issuing ART signals in the same BC window, the ART ASIC will select only the 8 of them, based on a priority scheme which is detailed later.

At time (2) all the bits of the ART addresses are recorded and can be presented at the output. Therefore the ART ASIC generates the data to the GBT chip in two steps, at time (1.5) and time (2), corresponding to the 80MBps transfer mode.

As it will be detailed in the following chapter, simulations performed for worst case of the technology showed that the hit selection operation can be performed in about 3-4 ns, which is considerably shorter than the 0.5 BC. Despite that, the latency cannot be shortened further because the deserialization step might not be completed in time for signals which burst at the very end of the BC window.

If transfer rates of 160 or 320 Mbps are used, the data flow to the GBT will have to be segmented in 4 or 8 steps. In this case, the latency can be shortened by segmenting the data such that the information which is available earlier (i.e. first bits of the ART address) is serialized first.

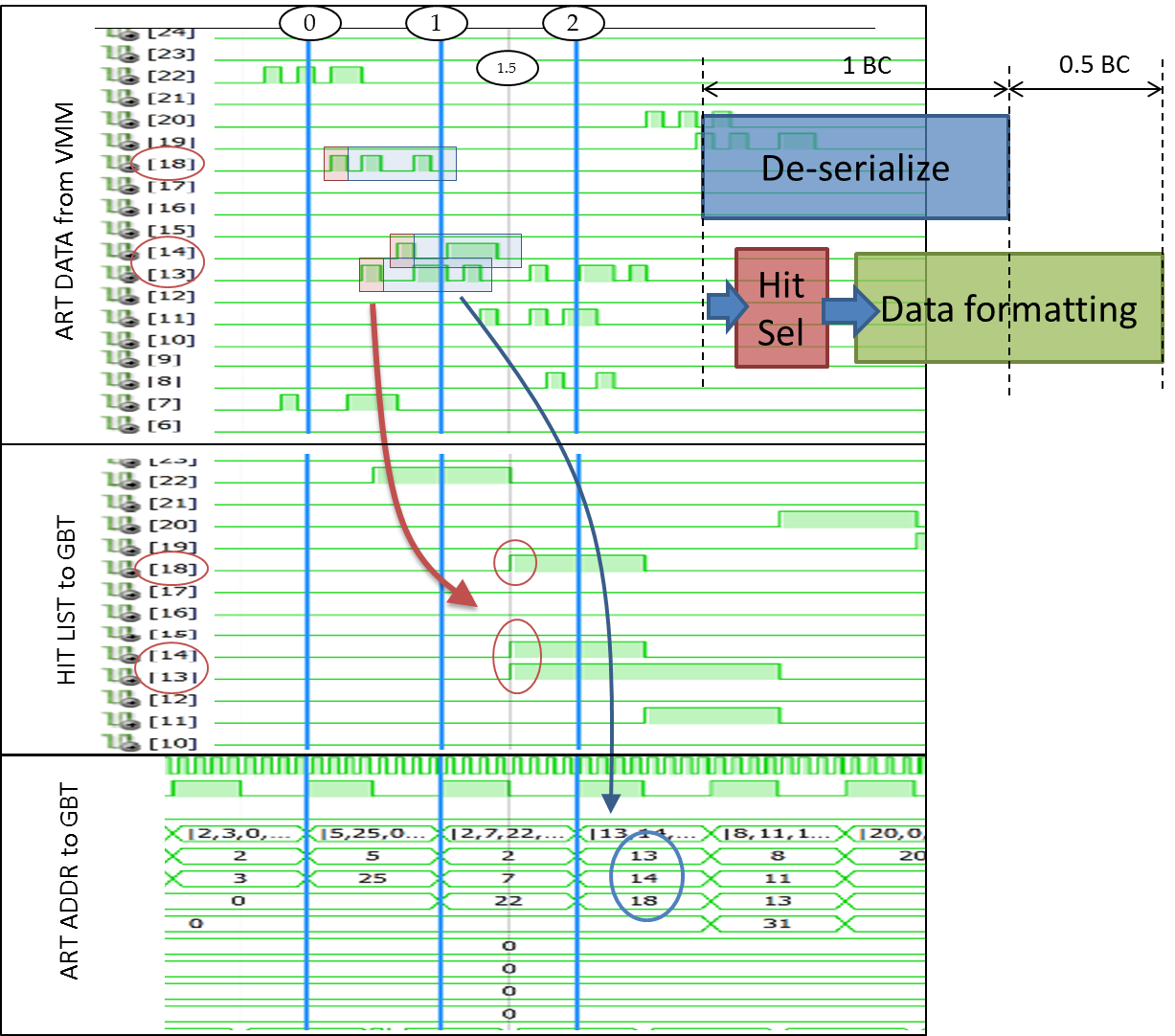


Figure 4. Theory of operation of the ART ASIC. Hit selection (red) is performed in parallel with ART data de-serialization (blue).

* 1. Hit selection circuit

A few possible models for the hit selection circuitry where evaluated. The best results were obtained with the Hit selection circuit based on cascaded priority encoders as shown in figure 4. The first priority encoder will select the first ART flag (i.e. the most significant bit which is not zero from the 32-bit ART flag word). The result expressed in one-hot 32-bit format is subtracted from the initial ART flag word, and the result is presented to the following stage. The second priority encoder will therefore select the second non-zero bit from the ART flag word. The operation is cascaded 8 times to select a maximum of 8 non-zero flags. The one-hot result of each stage can be or-ed together to result a 32-bit hit list of the selected hit flags. This 32-bit word describes unambiguously the information that is required to be passed to the trigger processor (i.e. the addresses of the VMMs who issued an ART signal).

If absolute address numbers for each VMM hit are required instead, binary decoders have to be implemented for each of the 8 outputs, and the sum of non-zero bits has to be computed and attached to the output stream. These operations may have an impact on the propagation delay parameter.

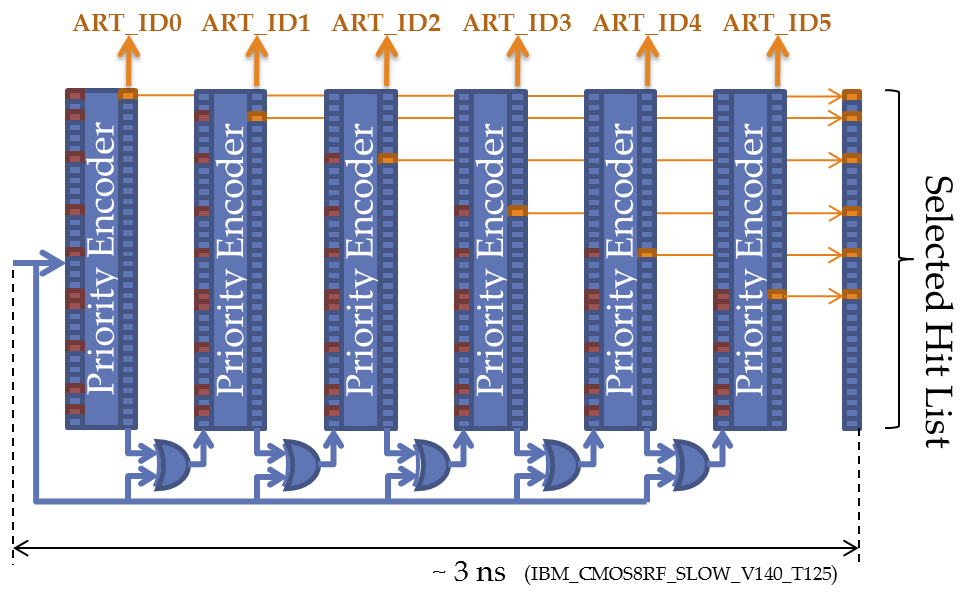


Figure 5. Hit selection circuitry based on priority encoders

* 1. Output Format

The ART ASIC has to transmit to the Trigger Processor the following information:

* Addresses of up to 8 VMM channels which had a hit in a particular BC
* The strip address of each of the 8 or less hits recovered from the ART stream (Address-in Real-Time).
* 12 bit BCID for checking the synchronization.

As it was described earlier, the information is transmitted to the GBtx chip in two steps. First, the selected VMM hit list is available, based on the flag bits issued by any of the 32 VMM chips at the input of the ASIC. Half BC later the corresponding ART addresses are transmitted to the output. In each of the two steps, 56 bits are transmitted to the GBTx chip, corresponding to the 80Mbps transfer mode. For 160 and 320 Mbps modes, the 56 bits are segmented in 2 or 4 transfers, respectively.

There are two options for the output data format. The Hit List option uses 32 bits to encode the VMM hit addresses, as it was described above (see Figure 6). 12 bits are used for BCID while the 12 bits are left for other use. These bits can be used to transmit a fixed word as frame delimiter (eg. “1010”). Other 8 bits may be used to transmit error flags from the core logic (i.e. error indicators from the 8 binary encoders attached to each priority encoder in the hit selection logic.)

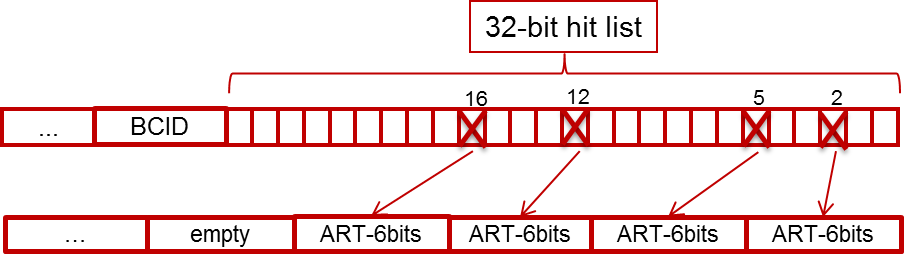


Figure 6. Illustration of the Hit List option

In case the hit addresses are transmitted as 5 bit numbers (VMM channel ID), there is no contingency. Out of the total of 56 bits, 52 are used by the hit addresses and BCID. The remaining 4 bits have to be used to transmit the total number of hits (0 to 8), to avoid the ambiguities in the frequent case where less than 8 hits are registered in a given BC.

For the second transfer (i.e. corresponding to the falling edge of the BC clock), the 8 x 6-bit ART addresses use 48 bit, while 8 bits are used for parity bits computed by the deserialization logic.

**Table 1.** Rising edge data

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **GBTOUT\_RISING[55:0]** | | | |
| calibration | 7 x CALIB\_DATA0[7:0] | | | |
| Hit list | "1010" | BCID[11:0] | ERR\_FLAGS[7:0] | HIT\_LIST[31:0] |
| Hit addresses | HIT\_CNT[3:0] | BCID[11:0] | 8 x VMMIDx[4:0] | |

**Table 2.** Falling edge data

|  |  |  |
| --- | --- | --- |
|  | **GBTOUT\_FALLING[55:0]** | |
| calibration | 7 x CALIB\_DATA1[7:0] | |
| Normal run | ARTDATA\_PARITY[7:0] | 8 x ARTDATAx[5:0] |

HIT\_LIST[31:0] = 32-bit list of flags corresponding to each of the 32 VMMs. 0 - no hit, 1 - hit. A register controls if this is a filtered (i.e. 8 hits max) or an un-filtered copy of the VMM flags registered in a particular BC.

HIT\_CNT[3:0] = number of hits (range 0 - 8; 9 - 15 invalid)

ARTDATA\_PARITY[7:0] = parity bit of the ART data computed by each of the 32 ART de-serializer units. Each bit corresponds to one of the ART data field selected by the priority unit.

* 1. Configuration and Control

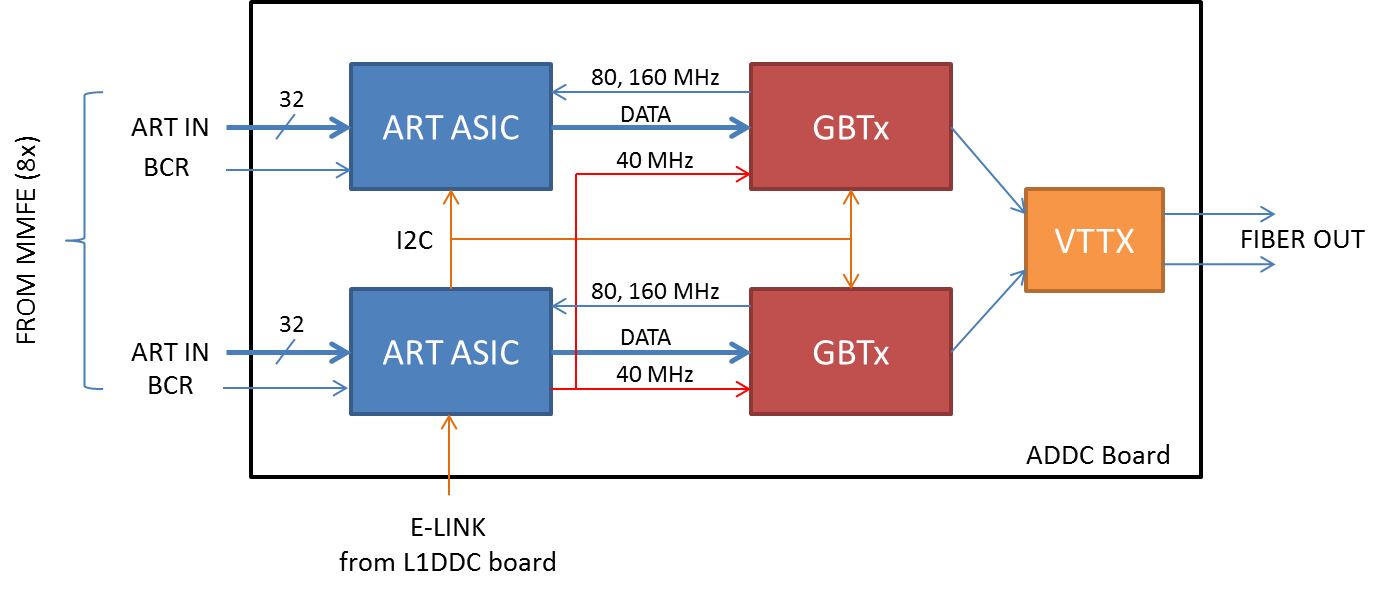


Figure 7. Block diagram of the ADDC board hosting the ART ASICs

On the ART ASIC will be integrated on a front-end board called ADDC. This board will host two ART chips, two GBTx chips and a VtTx electro-optical module.

For configuration purposes there is only one E-link available at the input of the ADDC card. The E-link will be connected to one of the two ART ASICs. This master ASIC will control via I2C the other ART ASIC (slave) as well as the two GBTx chips. The configuration e-link implements HDLC protocol. The higher level protocol used for data communication is defined by the possibilities of the FELIX system. One option is to use a subset of the protocol used by the SCA chip, which is foreseen to be implemented by FELIX.



Figure 8. Channel Layer of the SCA chip [1]

The Bunch Crossing Reset (BCR) signal will be forwarded along with the ART signals from the front-end MMFE board. On the mini-SAS cable used for this link there is one spare differential pair which may be used to feed the 160MHz ART clock from the ART ASIC to the VMMs residing on the MMFE board. This connection is subject to discussion.

* 1. Clocking

The only clock source of the ADDC board is the clock coming via the E-Port (40MHz). This clock is used for the configuration logic (HDLC, register matrix, I2C cores) and is buffered out for the two companion GBTx chips and the slave ART ASIC on the ADDC board. The high-performance PLL and a flexible clock distribution circuitry of the GBTx chip is used to provide clean synthesis clocks (160 MHz, 80 MHz and 40 MHz) for the core logic of the ART ASICs.

Clock domains of the chip are foreseen as follows:

* (dirty) 40 MHz
  + Source: E-Link
  + Skew control: No
  + Sinks: HDLC, I2C Master, I2C Slave, Register Matrix
* 40 MHz
  + Source: GBTx
  + Skew control: Yes (GBTx)
  + Sinks:
    - Logic Core (Hit Selection, Programmable Deadtime)
    - BCID counter
    - Output formatter (80Mbps mode)
* 80/160 MHz
  + Source: GBTx
  + Skew control: Yes (GBTx)
  + Sinks: Output logic (160 and 320Mbps mode)
* 160 MHz (ART)
  + Source: GBTx
  + Skew control: Yes (GBTx)
  + Sinks:
    - ART de-serializers
    - (optional) ART clock output to MMFE
    - (optional) may feed Output Formatter instead of dedicated clock input.

*Optionally, a single 160 MHz clock domain can be used for all core logic (excluding configuration logic which has to use the 40 MHz e-link clock) with multi-cycle clock path for the slower sub-domains (40 MHz and 80 MHz) using clock-enable signals derived from the master BC clock.*

1. **ART ASIC Architecture and Specifications**

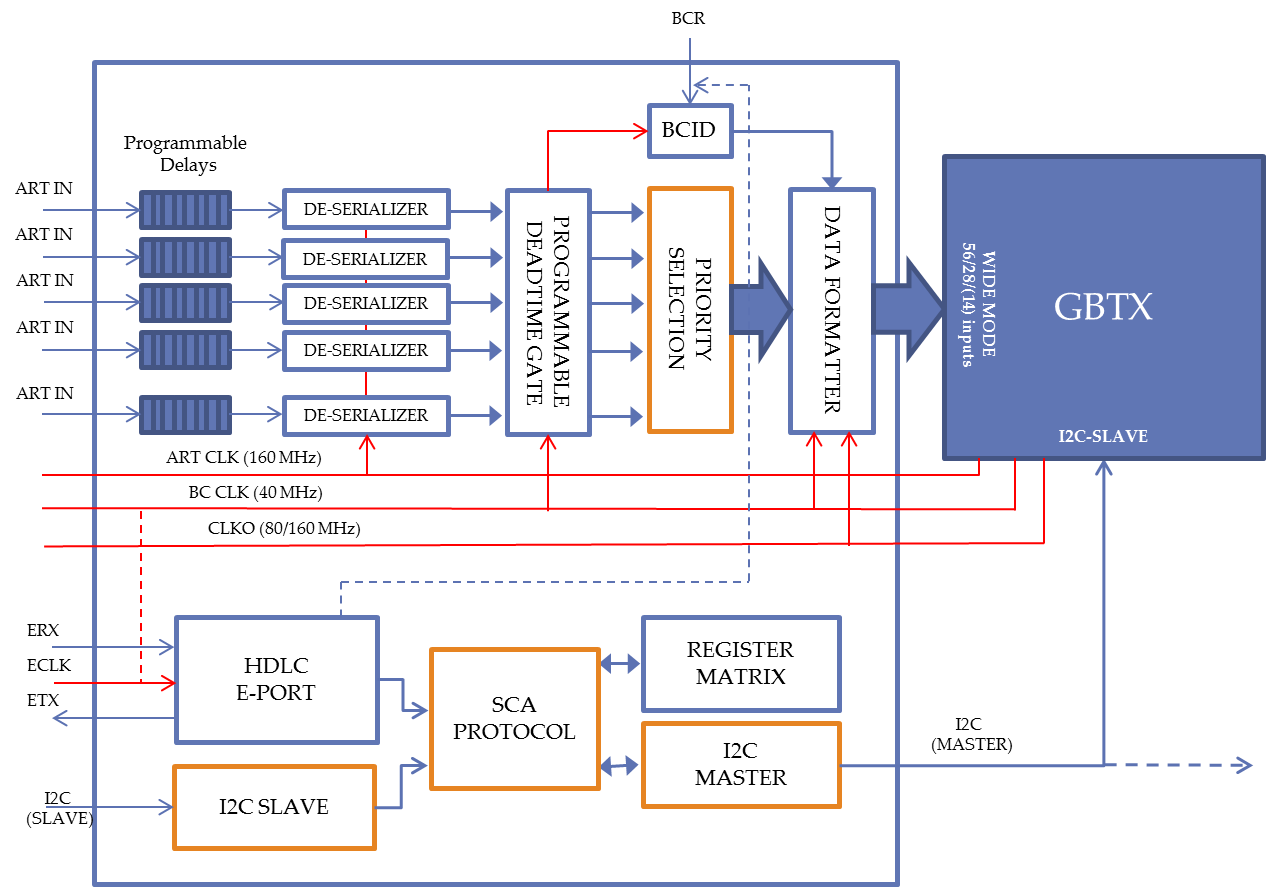


Figure 9. Architecture of the first ART ASIC

* 1. Programmable Delays

The purpose of the block is to be able to skew the input signals to avoid setup or hold violations on the local clock phase.

* Uses regular delay cells, no control loop – subject to process variations
* Individual 8-bit config:
  + Polarity
  + Mute
  + Delay (6 bit – 64 steps)
* MC analysis
  + 200..400 ps delay step
  + < 70% duty cycle distortion

*One option may be to use the CERN’s DLL-based Delay core which will eliminate the spread of the delay parameter. It must be evaluated if this potential benefit justifies the added complexity of the design.*

* 1. DDR De-Serializers
* Separate 160MHz clock domain
* Accepts ART flag on any edge
* Accepts back-to-back transfers
* Computes parity bit
* No triplication of the data registers is required. However the state machine registers must be protected.
  1. Programmable Deadtime
* Artificial deadtime controllable via configuration. Subsequent data on a particular channel may be ignored for a number of BCs.
* Programmable range (global):
  + 0 .. 7 BC
* Triplication may be needed to avoid spurious triggering of the deadtime counters.
  1. Priority Selection
* ART flags are registered on BC clock domain
* Based on cascaded priority encoders
* No triplication needed. Combinatorial logic only. Error flags may be asynchronously computed by the decoding logic and transmitted in the output format.
  1. Data Format
* Data rate:
  + *80 Mbps*
  + 160 Mbps
  + 320 Mbps
* *The 80Mbps mode may be excluded. This would reduce considerably the number of required pads (28 differential TX lines). In addition, reports on the GBtx latency have showed better performance in 160 or 320 Mbps modes* [2]*.*
* Data format options
  + Use hit list (32-bit)
    - Unfiltered hit list (32-bit) may be optionally transmitted. This will carry the information for all the 32 VMM connected to the ASIC. Only the first 8 hits will be have the ART address data transmitted.
  + Use hit addresses (8x5 bit)
* Test and debugging options
  + *~~Hamming encoding on hit list option~~*
  + Bypass mode (direct connection at the output of programmable delays).
    - This is used to verify and measure the propagation delay during ASIC initial verification.
  + Bypass priority selection on ART data (debug mode)
    - Controlled by a configuration register, the input channels are connected directly to the output logic (8 channels at a time). This mode can be used for in-system checking of the transmission between VMM chips and ART ASIC and setting the correct propagation delay of the Programmable Delays.
  + Fixed output calibration pattern
    - verification of the ART ASIC to GBT interface
  + *Cyclic output calibration pattern*
    - *Optional verification of the ART ASIC to GBT interface*
  1. HDLC E-Port and Register Matrix
* HDLC code and SLVS IPs received from CERN (thanks to S. Bonacini and P. Moreira)
* Minor modification: auxiliary channel not implemented to save pads
* Implementation of subset of SCA protocol for data transfer to registers and communication via I2C Master.
* Registers and HDLC core are triplicated
  1. I2C Master
* The I2C Master is used to control the GBTX and the second ART ASIC on the on the same board.
* Triplication is needed
  1. I2C Slave
* The I2C Slave is used to configure the register matrix in slave mode.
* Triplication is needed.

1. **Triple Redundancy**

|  |  |  |
| --- | --- | --- |
| **Block** | **Data Protection** | **State Machine Protection** |
| Programmable Delays | No | - |
| DDR De-serializers | Parity bit | Yes |
| Programmable Deadtime | - | Yes |
| Priority Selection | No | - |
| BCID Counter | Yes (?) |  |
| Output Logic | No | Yes |
| Register Matrix | yes | yes |
| HDLC E-Port | yes | yes |
| I2C Master | yes | yes |
| I2C Slave | yes | yes |

1. **Testability features**
   1. Bypass of core logic.

The outputs of the 32 Programmable Delay Blocks are connected to 32 output pads. This mode can be used for testing the delay blocks and for delay measurement during ASIC verification, prior to board assembly.

* 1. Bypass Priority Selection

The Priority Selection is locked to 8 of the VMM channels, by means of a configuration register. This way, the data from the de-serializers block of the corresponding VMM channel can be read continuously via the GBTx chip. This mode can be used in-system for determining if there are hold or setup time violations due to incorrect phase relationship between the incoming ART data and the local clock phase and adjust the programmable delays accordingly.

* 1. Fixed (or cyclic) output pattern.

This mode may be used in system for determining proper communication between the ART ASIC and the GBTx chip.

* 1. Mask bit for the 32 VMM channels.

1. **Packaging**

The chip has in excess of 250 pads (including 80Mbps output mode). The use of staggered pads has proved to be very problematic for wirebonding on test PCB.

The use of C4 technology may be an option, but this may further complicate testing and packaging of the chip.

The high number of pads and the limited space on the ADDC board might exclude the use of a non-BGA package (e.g. QFN, etc). Given the scarce offer in industry for low volume BGA packaging, this issue may be addressed together with the other chips in the collaboration.

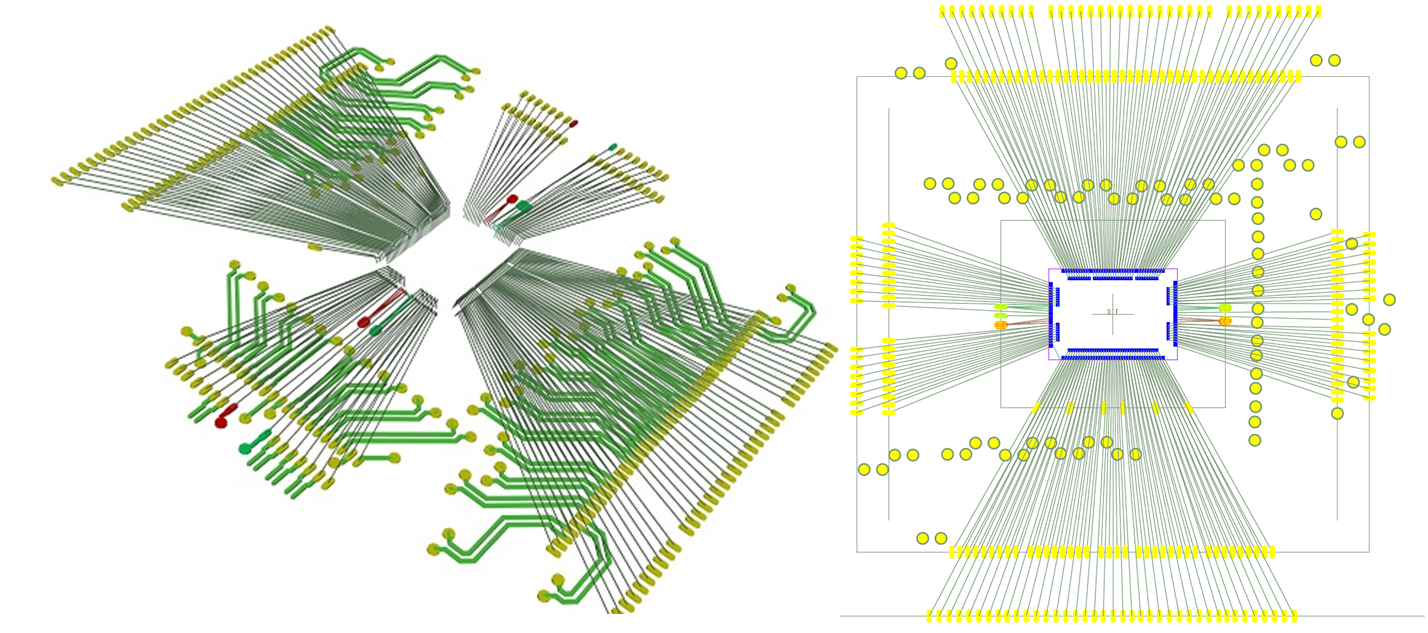


Figure 10. Wire-bonding diagram

1. **Issues to be addressed**

* Implementation of a calibration procedure which needs to be designed at the system level.
* If the output interface uses only 160 or 320Mbps mode, the number of pads may be reduced considerably, possibly removing the need for double pad rows. This choice depends on the measured latency of the GBTx chip in this mode of operation.
* Otherwise, C4 pads may be considered for the next prototype.

# Bibliography

|  |  |
| --- | --- |
| [1] | "New Small Wheel Technical Design Report," [Online]. Available: https://cds.cern.ch/record/1552862/files/ATLAS-TDR-020.pdf. |
| [2] | "GBT-SCA Manual," [Online]. Available: https://espace.cern.ch/GBT-Project/GBT-SCA/Manuals/GBT-SCA\_Manual\_Rev6.2.pdf. |
| [3] | P. Moreira, "GBT Project: Present & Future," [Online]. Available: https://indico.cern.ch/event/331027/session/2/contribution/6/material/slides/1.pdf. |