Comments on VMM Specification Document 23-­‐Sep-­‐15 John Oliver

These comments represent my best understanding of the document. Some may be incorrect due to my mis-­‐reading of the document and some are just minor inconsistencies.

1. Pg 1. “A serial out Address in Real Time at every bunch crossing for the Micromegas Trigger”. My understanding is that the ART serial line is data driven (occurs only on hit channel) and is synced to the 160 MHz ART Clock, not the Bunch Crossing Clock.

Yes, this is correct, synched to the160 MHz clock will rephrase it

1. Pg 7. “Address in Real Time (ART) using in the VMM trigger” should read “in the Micromegas Trigger”

Yes, corrected already

1. Pg 9. In discussion of Micromegas operation and requirements, it would be helpful to develop a spec for front end noise as a function of detector capacitance. Equivalently, a spec could be stated in terms of required dynamic range.

Good point. Next version will include specs for both noise and dyn. range

1. On operation with sTGCs, I understand that a problem was observed in that the positive ion tails were saturating the front end limiting maximum rates. Is this true and has this been resolved?

Yes, there were extensive discussions over several months to redefine

sTGC operating parameters, Gianluigi sent you documentation on this,

I understand.

1. General question on frontend: Is it an integrator or a transimpedance amplifier? The latter would probably be more robust to the possibility of saturation by positive ion tail.

Integrator.

1. Pg 15. On cooling it says “operating temperature range is -­‐55C to +12C”. I assume the latter number is a typo which should read “+120C”.

It is actually +125 deg. Fixed

1. Pg 22. On “NSW specific operation”. There is an issue with “ART dead time” which may be ok but I’m not certain from the document. For MM, there is a requirement that the ART output have a dead time of about 5 BC (125ns) from time of first electron. The ART signal stream takes 9x1/320MHz =

~28ns. What is the total dead time and what limits it?

There is a programmable delay (up to 8x25 ns) in the ART chip, no

dead time imposed in VMM

1. Pg 30. The SEU rate is given as “One tenth of an upset per year per VMM” and later as 3x10-­‐8/s. This latter number would imply an annual rate of about 1 per VMM per yr, not a tenth. Am I misreading this?

Not sure follow how you get 3x10^-8. The last paragraph only contains

the measurement of the upset cross section per bit in VMM1. Perhaps I

am missing something?

1. Pg. 31 “No prior knowledge (on expected reliability” exists”. One resource I have found useful comes from Analog Devices which lists reliability (and “activation energy”) for almost all of its devices. If you can find reference to a similar technology, and scale by die size, you may be able to get a first estimate of expected failure rates. Just a suggestion.

We can try, not sure how reliable estimates can one get this way. Come to

think of it perhaps the IBM design manual has reliability estimates.