**Ancillary functions for the NSW Trigger Processor**

15 March 2015

In addition to implementing the trigger algorithms for the MM and sTGC systems, the NSW Trigger Processor has to perform several ancillary functions. These include time synchronization, configuration, monitoring and debugging mode, among others. Several functions are common to both MM and sTGC and their firmware can be shared as well-defined packages. These functions are:

**Interface for algorithm and other configuration parameters**

Parameters for the algorithms must be stored at runtime. Examples are the Δθ and other cuts, the BCID offset, alignment parameters, the parts of the detector to be considered as disabled, road size, etc. Configuration can be done via Ethernet and the carrier board or via an E-link from FELIX that is available on the link that brings the TTC information. Read back of the parameters must also be provided.

Note: if there are a large number of configuration parameters it may be advisable to use serial bus to set them locally to where they are used.

**TTC interface**

FELIX provides the following TTC information on an E-link from the 8-bit TTC broadcast packet and the raw B-channel (for the Trigger Type):

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| L1A | BCR | ECR | Brcst[2] | Brcst[3] | Brcst[4] | Brcst[5] | B-chan |

The E-link provides the 40 MHz BC clock which is used to synchronize the output to the Sector Logic. This also includes the logic to synchronize a local bunch-crossing ID to the Sector Logic by means of a configurable BC offset loaded on BCR into a local BCID register. Note that the various input links will not have the same phase and may not even be matched to the same BC clock. Input processors must ensure that all sources are aligned to the same BC clock. Both technologies include a BCID or its low bits in the packet sent on every bunch-crossing. Should the offset of this BCID from the local BCID differ from what is expected, an exception message (see below) must be sent. The firmware to do this alignment is not shared.

Clocks for the serial links and the 320MHz algorithm clock must be generated from the 40MHz BC E-link clock.

**Level-1 output buffer**

For bunch-crossings in which at least one segment is found, the input data and the output segment data that is sent to the Sector Logic is stored, along with its BCID for later matching to the BCID of a Level-1 Accept. Those bunch-crossings that have Level-1 Accepts (and possibly those preceding and following) are transferred to the Level-1 output buffer (aka derandomizer). The data must be stored for the duration of the Level-1 latency. The output bandwidth should be sufficient for the rather small fixed input and output data lengths at the full Level-1 rate of 400 kHz. If not, this logic could provide a BUSY output to the RODBUSY system when its output buffer becomes close to full.

**Monitored event buffer**

A random sample of complete events is collected for sending to a monitoring process. Example criteria are: any event, event with at least one segment found, events with segments outside the Δθ cut, …) The data buffered as one event includes all the input data and the output segment data that is sent to the Sector Logic for a given BC.

**Statistics buffer**

Statistics are continuously collected and periodically transferred to the Statistics buffer. Statistics includes the number of bunch-crossings that have candidates that are not accepted by Level-1, their distribution in R, the multiplicity of segments per bunch-crossing, etc.

**Exception buffer**

In the course of processing, exceptional conditions may be found, usually due to corrupted data. A convenient way to handle these is to store an exception code and some context data into a buffer which will be passed to the monitoring PC via FELIX.

**Playback mode to fake input links**

For development and testing we require that simulated data can be injected in place of the data received by the links to the Front End. One way to do this is via an E-link from FELIX that is available on the link that brings the TTC information. Play back can be at full speed, i.e. 40MHz.

**Segment output to Sector Logic and to the ‘other’ detector**

Segments are sent out either to the Sector Logic via the FPGA serializer or to the ‘other’ detector via a parallel LVDS bus. The candidate packet to be sent to the Sector Logic must be prepared from the segments found. Clones must be made and the output links to the Sector logic must be driven. If the segments found are to be sent to the ‘other’ detector's Trigger Processor, the segment data must be sequenced out onto the parallel LVDS bus.

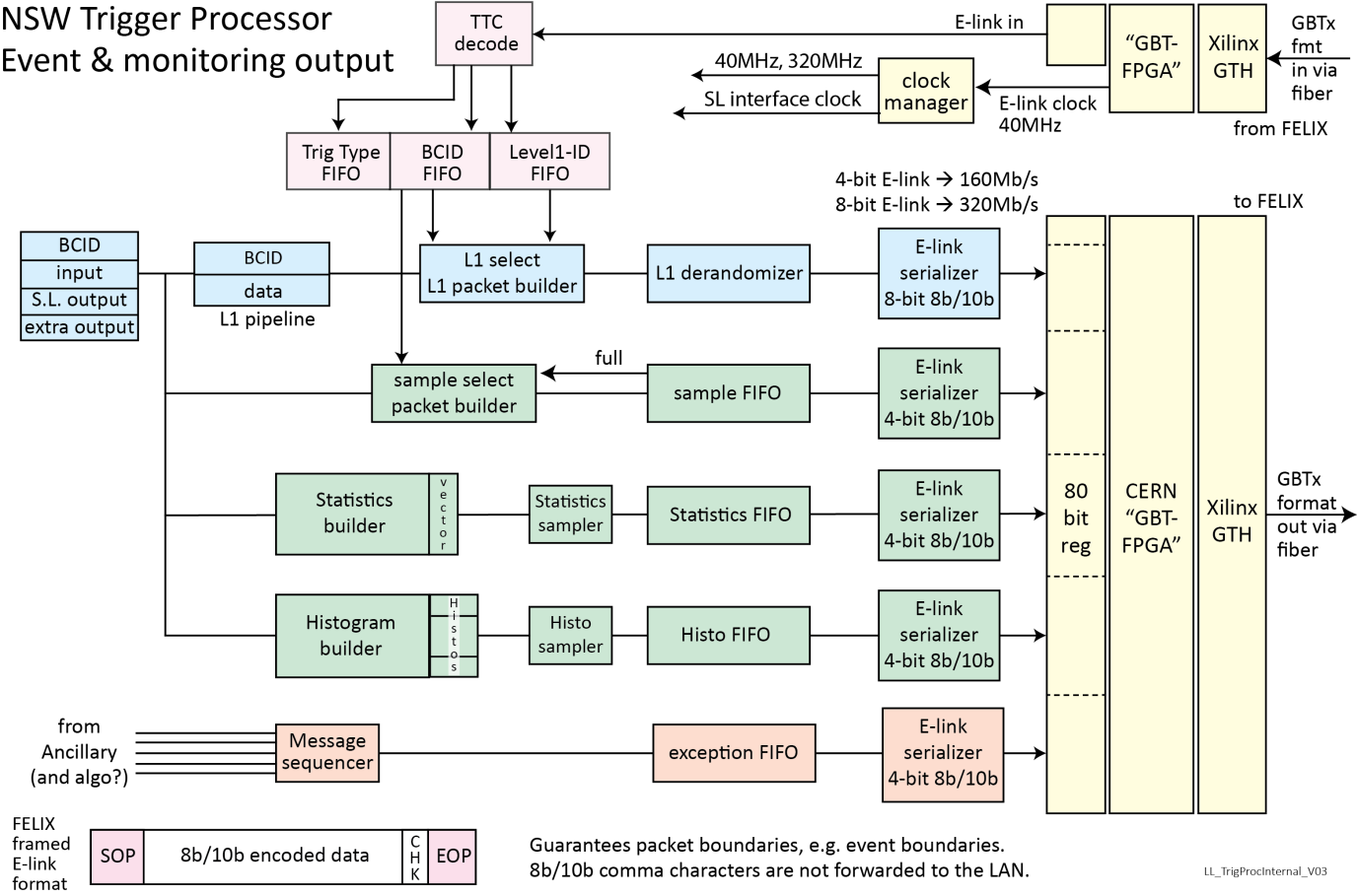
**Merge buffers into the output GBT link to FELIX**

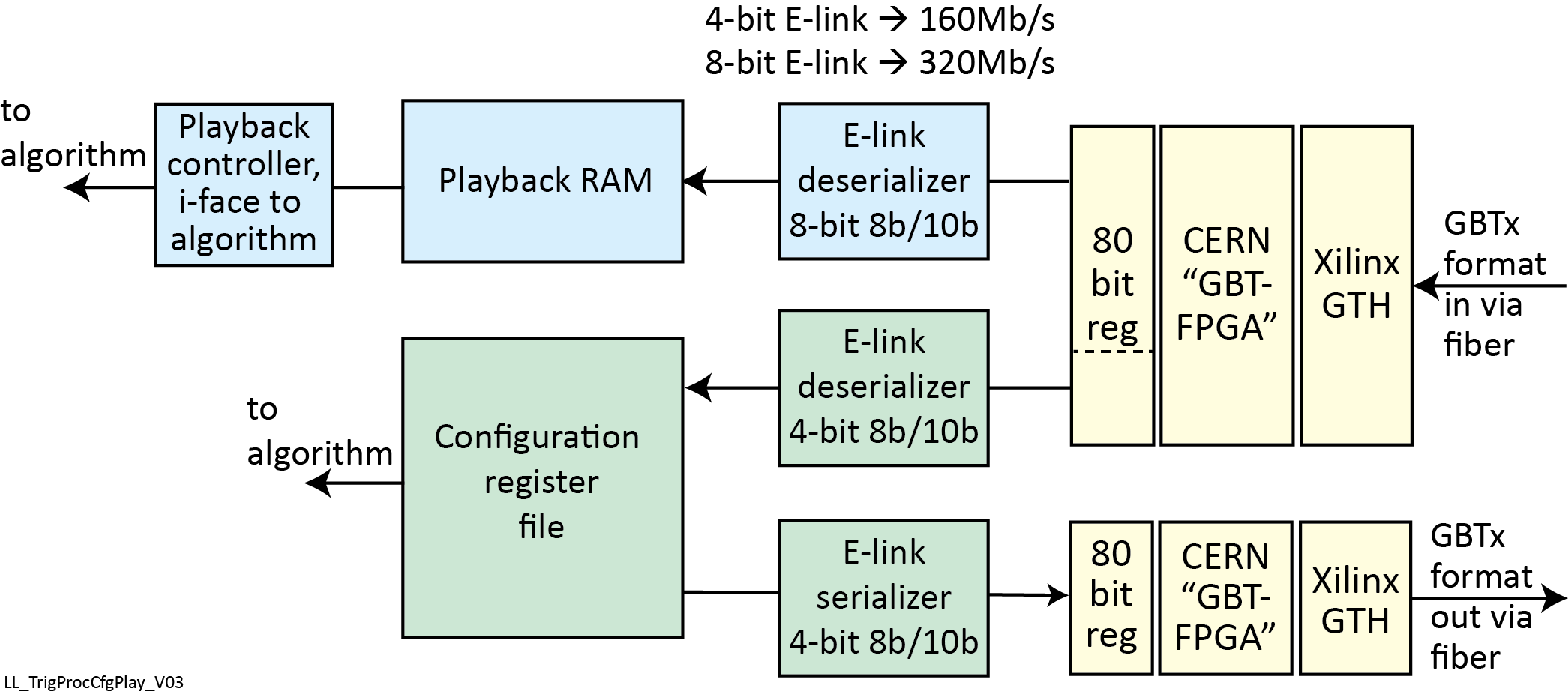
The Level-1, Monitoring, Statistics and Exception buffers are merged, using different E-links onto a fiber link to FELIX. FELIX then routes them to the ROD and Monitoring PCs.

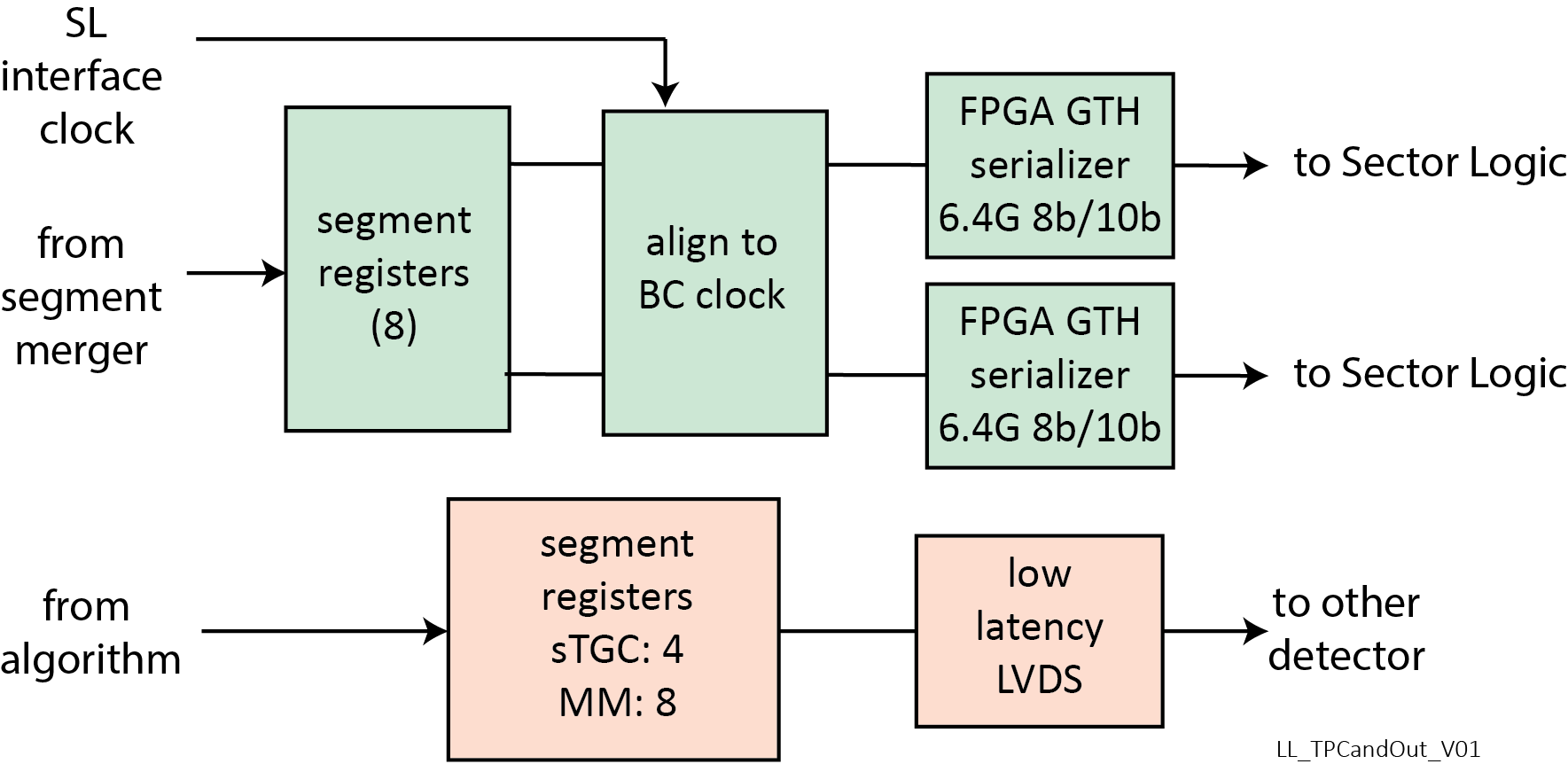
**Front End input links**

Since the MM uses the GBTx to transmit the data from the Front End and the sTGC uses native FPGA serializers, the link interface firmware cannot be shared.

Note that the monitoring of board temperatures and voltages is done by the ATCA Shelf Manager using IPMI.

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**Work packages**

The first step is to define the data formats for both detector types:

* Input from FE
* Output to Sector Logic
* Extra per BC output
* Level-1 event output format

The following functions are the same for the two technologies:

1. TTC FIFOs and the clock managers
2. E-link serializers and interface to the GBT-FPGA package
3. Level-1 selector
4. Message sequencer and exception FIFO
5. Candidate output to the Sector Logic and to the ‘other’ trigger processor
6. FPGA configuration via the ATCA and Ethernet
7. GBT-over-USB for development (uses USB modem on HTG-710 and VC709 boards)

The following functions are slightly different for the two technologies. None-the-less a single person should develop both versions:

1. Level-1 packet builder and derandomizer
2. Sample select packet builder and sample FIFO
3. Statistics builder and statistics FIFO
4. Histogram builder and histogram FIFO
5. Playback controller and RAM. Difference is the data width per FE link.
6. Configuration register file. Params for the algorithms are different; params for the ancillary functions are the same. There are issues regarding the number of copies of algorithm parameters and if some could be in RAM LUTs as opposed to registers,

The following functions are significantly different for the two technologies and so may be developed by different people:

1. Input from the Front Ends and their timing alignment