**LAr Optical Test Card Description**

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In this document we describe the AMC-format Optical Test Card (OTC) hardware features. Section 1 provides an overview of the OTC functionality, and descriptions of each major functional block follow in the remaining sections. These remaining sections include the required AMC MMC functions and JTAG and I2C access (Sec. 2), the clocks provided on the OTC and clocks expected to be available through the AMC interface (Sec. 3), the gigabit Ethernet interface (Sec. 4), the multichannel high speed interface (XAUI; Sec. 5), the GBT interfaces (Sec. 6), the 48 channel optical receiver and 48 channel optical transmitter interfaces (Pod; Sec. 7) and the LVDS connectivity (Sec. 8). In each section control and data signals are described. The full connectivity of the onboard FPGA is listed in Appendix A. Other than the brief outline of the MMC functionality in Sec. 2, no description is made of the AMC standard or functions required by the standard.

**1. Overview**

The main purpose of the OTC is to provide up to 48 channels of optical input to be processed by an onboard FPGA with the results of the processing transmitted on up to 48 channels of optical output. The electro-optical I/O is provided by Avago micropods capable of data rates up to 12.5 Gbps[[1]](#footnote-1). The micropod electronic data inputs and outputs are connected to a Xilinx Virtex-7 XC7VX485TFFG1927-2 FPGA[[2]](#footnote-2) GTX transceivers. The FPGA provides the processing capacity and the micropod control interface. The optical connections to the micropods are made through two 48 channel MTP connectors on the OTC front panel. The OTC is designed to the AMC full height standard. Thus, in addition to the 48 channels of optical I/O, the OTC provides serial transceiver, generic I/O and clock connectivity through the AMC interface as shown in Table 1 as well as the required AMC management interface.

The serial transceivers for the AMC interface are Xilinx GTX blocks so their configuration is flexible, but the expected OTC primary AMC configuration is one GbE interface, one XAUI interface and up to three ATLAS GBT interfaces. The transceivers signals are 100 Ohm differential pairs. The receive channels are AC coupled on the OTC, and the transmit channels are DC coupled on the OTC with AC coupling expected on the receiving end of the differential pair.

The generic I/O connections are provided via Xilinx Select I/O channels, with the primary configuration expected to be 1.8V LVDS signaling. The Select I/O pins also provide a flexible internal termination scheme. Two clocks are available on the AMC interface, one of which is intended to be derived from the LHC clock. The OTC itself provides three additional clocks including one whose frequency is related to the LHC clock.

The OTC has 512 MB of DDR3 memory (128M x 32 bits) connected to the FPGA. The memory uses two Micron MT41J128M16-125 chips rated at 1600 transfers per second. This chip type is known to the Xilinx Memory Interface Generator (MIG) IP core, and the pin connectivity can be found in Appendix A.

|  |  |  |
| --- | --- | --- |
| **AMC Port(s)** | **Type** | **Default Use** |
| 0 | Serial Transceiver (GTX) | Gigabit Ethernet (GbE) |
| 8 – 11 | Serial Transceiver (GTX) | XAUI 10 Gbps Ethernet |
| 12, 13, 20 | Serial Transceiver (GTX) | ATLAS GBT |
| 18, 19 | Generic I/O (Xilinx Select I/O) | 1.8V LVDS, user defined |
| FCLKA | Synthesized clock | Optical I/O reference |
| TCLKA | 156.25 MHz Oscillator | XAUI reference clock |

Table : The OTC ports accessible through the AMC interface

**2. MMC and I2C and JTAG access**

The OTC adheres to the PICMG® AMC.0 R2.0 standard. It includes the mandatory IPMB (I2C), JTAG, hot-swap, LED, MMC and e-keying functionality.

The OTC MMC uses the CERN hardware design[1] implemented directly on the OTC. This gives a more compact design than using the CERN daughter card would. The MMC software is based on the corresponding CERN software, and e-keying descriptors are provided as part of the software customization. Sensor (temperature and voltage) monitoring functionality must be provided through the MMC using data retrieved by the MMC from the FPGA.

In addition to the AMC mandated IPMB I2C functioning, there are two I2C buses on the OTC. One bus connects the MMC to the FPGA and is primarily intended to be used by the MMC to collect sensor data through the FPGA. The second bus connects the FPGA to the clock synthesizer (Sec. 3) and to the micropod receivers and transmitters (Sec. 7). The I2C addresses of the clock synthesizer and micropods are shown in Table 2. The I2C addresses of the FPGA master are defined by firmware.

|  |  |
| --- | --- |
| **I2C Address** | **Device** |
| 0x54 | Clock Synthesizer (Sec. 3) |
| 0x30 | Micropod Rx, U5 (Sec. ) |
| 0x31 | Micropod Rx, U6 |
| 0x32 | Micropod Rx, U7 |
| 0x33 | Micropod Rx, U8 |
| 0x28 | Micropod Tx, U16 |
| 0x29 | Micropod Tx, U17 |
| 0x2A | Micropod Tx, U18 |
| 0x2B | Micropod Tx, U19 |

Table : Addresses of I2C devices on the OTC. The FPGA I2C addresses are defined by whatever firmware is in used.

The MMC also generates an FPGA\_RESET signal usable by firmware, a FPGA\_PROG signal which forces the FPGA firmware to be reloaded from the flash. There are three general purpose pins driven from the MMC to the FPGA (FPGA\_IN0 – FPGA\_IN2), and two in the other direction (FPGA\_OUT0 and FPGA\_OUT1). Finally, there is an FPGA\_DONE signal from the FGPA to the MMC which indicates FPGA firmware loading is complete.

**MMC programming:** The MMC is programmed through a dedicated JTAG connector (J1). No ability to reprogram the MMC in situ is provided because of potential problems disrupting the IPMB communication between the ATCA carrier and the OTC during MMC programming and inadvertently power cycling the OTC leaving it in an unusable state.

**FPGA programming:** A second JTAG chain is driven by either the JTAG signal on the AMC interface or by a header (J2) on the OTC and provides the mechanism used to program the FPGA and its flash memory. If the OTC is inserted into an AMC slot, there must be no cable connected to J2, and the FPGA JTAG access can only be made through the AMC JTAG port.

**3. Clock Signals**

The OTC has five clock sources, three generated on the OTC itself: (1) a 125 MHz oscillator used for the system clock and a GbE clock, (2) a 156.25 MHz oscillator used for a XAUI reference clock, and (3) a 40.079 MHz oscillator used to generate the optical I/O reference clock, and two clocks supplied via the ATCA carrier (4) TCLKA and (5) FCLKA clock ports. When used with the ATCA carrier for the LAr system, the TCLKA signal is a 156.25 MHz signal, and FCLKA is the output of a low jitter clock synthesizer derived from the LHC 40.079 MHz clock which itself is recovered from the GBT signal. TCLKA is intended to provide a common generic data transfer clock (e.g. for XAUI) and FCLKA provides a reference clock for the micropod optical I/O.

The onboard 40.079 MHz oscillator and the FCLKA port drive the two independent clock inputs of a CDCM6208RGZT clock synthesizer. FCLKA is the “primary” channel input, and the onboard oscillator is the “secondary” channel input. The synthesizer has two groups of four outputs[[3]](#footnote-3) which are used to provide the reference clocks for four transceiver quads on the FPGA. Each of the four quads gets a reference clock connection from each of the two groups (i.e. two potentially different reference clocks per quad to allow different transmit and receive speeds for the micropods).

The input select signal REFSEL and the I2C controls of the clock synthesizer are sourced from the FPGA. The synthesizer SYNCHn, RSTn, STATUS0, and STATUS1 synthesizer signals are also connected to the FPGA. The FPGA firmware must ensure that the FPGA pins CLK\_SYNCHn (=SYNCHn) and CLK\_RSTn (=RSTn) are driven HI for the synthesizer to function, and the appropriate value of CLKSEL (=REFCLK) must be chosen. The onboard 40.079 MHz oscillator input is chosen if CLKSEL=0, otherwise the FCLKA input is used. The default firmware provided in the OTC flash memory configures all outputs of the synthesizer to 5 x 40.079 MHz = 200.395 MHz and uses the onboard oscillator as the source.

The output of the synthesizer, the 125 MHz oscillator, the onboard 156.25 MHz oscillator and the AMC TCLKA signal are connected to the FPGA. The 125 MHz oscillator is used as the system clock. Tables 3 and 4 list the connections between the various clock signals and the FPGA system clock and transceiver reference clocks.

|  |  |
| --- | --- |
| **Clock Source** | **FPGA Connection** |
| 125 Mhz Oscillator | System clock, Quad 119 MgtRefClk0 (for GbE) |
| 156.25 MHz Oscillator | Quad 213 MgtRefClk0 (XAUI) |
| AMC TCLKA (156.25 MHz) | Quad 213 MgtRefClk1 (XAUI) |
| CDCM6208RGZT Synthesizer Outputs  (40.079 Osc; AMC FCLKA) | Quads 114, 117, 215, and 218 MgtRefClk0 and MgtRefClk1 (micropod); Quad 119 MgtRefClk1 (for GBT) |

Table : The correspondence between clock source and FPGA resources

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Quad** | 113 | 114 | 115 | 116 | 117 | 118 | 119 | 213 | 214 | 215 | 216 | 217 | 218 | 219 |
| **REFCLK0** | - | S0 | - | - | S1 | - | GbE | XAUI | - | S2 | - | - | S3 | - |
| **REFCLK1** | - | S4 | - | - | S5 | - | S7 | TCLKA | - | S6 | - | - | S7 | - |

Table : Reference clocks provided to the GTX transceivers. The “Sn” notation means the n-th output of the clock synthesizer. The “GbE” notation means the onboard 125 MHz clock, and the “XAUI” notation means the onboard 156.25 MHz clock. A “-“ means no direct clock connection, so the reference clock must come from an adjacent quad using the Xilinx “north” and “south” reference clock choice. “S7” appears twice because that output is fanned out to two quads.

**4. Gigabit Ethernet Interface**

A de facto standard for AMC has a gigabyte Ethernet (GbE) interface available on AMC port 0. This is implemented on the OTC by connecting port 0 to an FPGA serial transceiver. The Xilinx X1\_Y24 transceiver in quad 119 is used for this, and the 125 MHz onboard clock required by GbE is connected to the REFCLK0 input for this quad. Ethernet functionality on the port must be provided by the FPGA firmware. An example design is available[2] which uses the Xilinx GbE IP core with software support provided by the LWIP implementation in the Xilinx SDK.

**5. Multichannel High Speed Interface (XAUI)**

AMC ports 8 – 11 are connected to the four FPGA serial transceivers in quad 213. The onboard 156.25 MHz oscillator is connected to the REFCLK0 input of this quad, and the TCLKA signal on the AMC interface is connected to the REFCLK1 input. Either clock can be selected by firmware as the transceiver reference clock. By default, these ports are intended to be used as a XAUI interface between the OTC and its carrier. However, the transceivers are not XAUI specific, so other protocols (e.g. PCI-e) could be implemented in the FPGA instead of XAUI provided the ATCA carrier uses the same protocol.

**6. GBT Interface**

AMC ports 12, 13 and 20 are connected to three serial transceivers in quad 119[[4]](#footnote-4). The 125 MHz oscillator output is connected to REFCLK0, and the output of the clock synthesizer driven by the recovered LHC clock or onboard 40.079 MHz is connected to REFCLK1. Like the XAUI and GbE interfaces, these transceivers are general purpose. The main intent is the use of REFCK1 to provide at least one (and up to three) GBT connection(s) to the ATCA carrier for the interface to the ATLAS TDAQ system.

**7. Optical I/O: 48 Channel High Density Transmitter and Receiver (micropod) Interface**

The main purpose of the OTC is to receive up to 48 input channels of raw data, process the data in the FPGA, and transmit the results on up to 48 output channels. The input and output are each provided through 4 micropod 12-channel optical receivers (AFBR-78D1SZ) and 4 micropod 12-channel optical transmitters (AFBR-77D1SZ) all of which are in sockets on the OTC and which use a custom heat sink. These I/O channels are connected to 48 transceivers (12 quads) of the FPGA. Each transceiver handles one micropod input and one micropod output channel. The correspondence between the micropod channels and transceivers is shown in Table 5.

The reference clocks for the transceivers come from the outputs of the clock synthesizer. To reduce the fan out demand, only one third of the transceiver quads have their reference clock input pins directly connected to the synthesizer outputs. The other quads must take their reference clock from an adjacent quad using the Xilinx “north clock” and “south clock” reference clock input choice. The clock connections are shown as the “S0” through “S7” entries in Table 4.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micropod Channel | | Xilinx Transceiver | Micropod Channel | | Xilinx Transceiver | Micropod Channel | | Xilinx Transceiver | Micropod Part/Chan | | Xilinx Transceiver |
| Tx | Rx | Tx | Rx | Tx | Rx | Tx | Rx |
| U16/0 | U5/0 | X1\_Y0 | U17/0 | U6/0 | X1\_Y12 | U18/0 | U7/0 | X0\_Y24 | U19/0 | U8/0 | X0\_Y12 |
| 1 | 1 | X1\_Y1 | 1 | 1 | X1\_Y13 | 1 | 1 | X0\_Y25 | 1 | 1 | X0\_Y13 |
| 2 | 2 | X1\_Y2 | 2 | 2 | X1\_Y14 | 2 | 2 | X0\_Y26 | 2 | 2 | X0\_Y14 |
| 3 | 3 | X1\_Y3 | 3 | 3 | X1\_Y15 | 3 | 3 | X0\_Y27 | 3 | 3 | X0\_Y15 |
| 4 | 4 | X1\_Y4 | 4 | 4 | X1\_Y16 | 4 | 4 | X0\_Y20 | 4 | 4 | X0\_Y8 |
| 5 | 5 | X1\_Y5 | 5 | 5 | X1\_Y17 | 5 | 5 | X0\_Y21 | 5 | 5 | X0\_Y9 |
| 6 | 6 | X1\_Y6 | 6 | 6 | X1\_Y18 | 6 | 6 | X0\_Y22 | 6 | 6 | X0\_Y10 |
| 7 | 7 | X1\_Y7 | 7 | 7 | X1\_Y19 | 7 | 7 | X0\_Y23 | 7 | 7 | X0\_Y11 |
| 8 | 8 | X1\_Y8 | 8 | 8 | X1\_Y20 | 8 | 8 | X0\_Y16 | 8 | 8 | X0\_Y4 |
| 9 | 9 | X1\_Y9 | 9 | 9 | X1\_Y21 | 9 | 9 | X0\_Y17 | 9 | 9 | X0\_Y5 |
| 10 | 10 | X1\_Y10 | 10 | 10 | X1\_Y22 | 10 | 10 | X0\_Y18 | 10 | 10 | X0\_Y6 |
| 11 | 11 | X1\_Y11 | 11 | 11 | X1\_Y23 | 11 | 11 | X0\_Y19 | 11 | 11 | X0\_Y7 |

Table : The micropod receiver and transmitter channel to Xilinx transceiver connections

**8. Generic I/O (LVDS) Interface**

AMC ports 18 and 19 are connected to Xilinx Select I/O pins. These can be configured as 1.8V compatible LVDS signals to form standard AMC ports, or they can be user defined for any configuration allowed by Select I/O pins. The signals on port 18 are connected to Xilinx “clock compatible” Select I/O pins. The connections between the ports and the Xilinx FPGA are shown in Table 6.

|  |  |  |  |
| --- | --- | --- | --- |
| **AMC Port** | **AMC Signal** | **Xilinx Pin Name** | **Xilinx Pin** |
| 18 | TXP | IO\_L12P\_T1\_MRCC\_19 | H28 |
|  | TXN | IO\_L12N\_T1\_MRCC\_19 | H29 |
|  | RXP | IO\_L13P\_T2\_MRCC\_19 | K27 |
|  | RXN | IO\_L13N\_T2\_MRCC\_19 | J27 |
| 19 | TXP | IO\_L4P\_T0\_19 | C28 |
|  | TXN | IO\_L4N\_T0\_19 | B28 |
|  | RXP | IO\_L5P\_T0\_19 | B26 |
|  | RXN | IO\_L5N\_T0\_19 | A26 |

Table : The OTC generic I/O connections provided through the AMC connector

References

[1] CERN MMC design document NEED TO FIND

[2] <http://sbhep-nt.physics.sunysb.edu/~hobbs/FPGAStuff/OpticalTestCard-f301-s300.zip> The xaxiemacif.c file in the Xilinx SDK distribution has to be edited. The version in this zip file has the two edits which involve adding #ifdef statements testing on *XPAR\_AXIETHERNET\_0\_CONNECTED\_TYPE*.

Appendix A: FPGA Connections

| **Pin** | **Pin Name** | **Bank** | **Signal Name** | **Description** |
| --- | --- | --- | --- | --- |
| AY31 | IO\_L9P\_T1\_DQS\_14 | 14 | FPGA\_CLK\_SYNCn | Synchronize CDCM6208 Clock IC |
| BA31 | IO\_L9N\_T1\_DQS\_D13\_14 | 14 | FPGA\_CLK\_RSTn | Reset CDCM6208 Clock IC |
| AY28 | IO\_L10P\_T1\_D14\_14 | 14 | FPGA\_CLKSEL | 0 = local Osc., 1 = AMC\_FCLKA |
| AV29 | IO\_L14N\_T2\_SRCC\_14 | 14 | FPGA\_SCL0 | I2C for uPODs and CDCM6208 |
| AN27 | IO\_L15P\_T2\_DQS\_RDWR\_B\_14 | 14 | FPGA\_SDA0 | I2C for uPODs and CDCM6208 |
| AP27 | IO\_L15N\_T2\_DQS\_DOUT\_CSO\_B | 14 | FPGA\_SCL1 | I2C connection to MMC |
| AT28 | IO\_L16P\_T2\_CSI\_B\_14 | 14 | FPGA\_SDA1 | I2C connection to MMC |
| AT29 | IO\_L16N\_T2\_A15\_D31\_14 | 14 | FPGA\_uPOD\_RSTn | reset all uPODs (active low) |
| AP29 | IO\_L17P\_T2\_A14\_D30\_14 | 14 | FPGA\_OUT1 | GP output to MMC |
| AP30 | IO\_L17N\_T2\_A13\_D29\_14 | 14 | uPOD\_INT0 | uPOD interrupt signal |
| AR28 | IO\_L18P\_T2\_A12\_D28\_14 | 14 | uPOD\_INT1 | uPOD interrupt signal |
| AR29 | IO\_L18N\_T2\_A11\_D27\_14 | 14 | uPOD\_INT2 | uPOD interrupt signal |
| AN28 | IO\_L19P\_T3\_A10\_D26\_14 | 14 | uPOD\_INT3 | uPOD interrupt signal |
| AN29 | IO\_L19N\_T3\_A09\_D25\_VREF\_1 | 14 | uPOD\_INT4 | uPOD interrupt signal |
| AM30 | IO\_L20P\_T3\_A08\_D24\_14 | 14 | uPOD\_INT5 | uPOD interrupt signal |
| AN30 | IO\_L20N\_T3\_A07\_D23\_14 | 14 | uPOD\_INT6 | uPOD interrupt signal |
| AK27 | IO\_L21P\_T3\_DQS\_14 | 14 | uPOD\_INT7 | uPOD interrupt signal |
| AK28 | IO\_L21N\_T3\_DQS\_A06\_D22\_14 | 14 | FPGA\_CLK\_STATUS0 | CDCM6208 status |
| AM27 | IO\_L22P\_T3\_A05\_D21\_14 | 14 | FPGA\_CLK\_STATUS1 | CDCM6208 status |
| AM28 | IO\_L22N\_T3\_A04\_D20\_14 | 14 | FPGA\_RESET | input from MMC |
| AJ29 | IO\_L23P\_T3\_A03\_D19\_14 | 14 | FPGA\_OUT0 | GP output to MMC |
| AK29 | IO\_L23N\_T3\_A02\_D18\_14 | 14 | FPGA\_IN0 | GP input from MMC |
| AL28 | IO\_L24P\_T3\_A01\_D17\_14 | 14 | FPGA\_IN1 | GP input from MMC |
| AL29 | IO\_L24N\_T3\_A00\_D16\_14 | 14 | FPGA\_IN2 | GP input from MMC |
| C28 | IO\_L4P\_T0\_19 | 19 | LVDS\_Tx2p | LVDS connected to AMC Port[19] |
| B28 | IO\_L4N\_T0\_19 | 19 | LVDS\_Tx2n | LVDS connected to AMC Port[19] |
| B26 | IO\_L5P\_T0\_19 | 19 | LVDS\_Rx2p | LVDS connected to AMC Port[19] |
| A26 | IO\_L5N\_T0\_19 | 19 | LVDS\_Rx2n | LVDS connected to AMC Port[19] |
| H28 | IO\_L12P\_T1\_MRCC\_19 | 19 | LVDS\_Tx1p | LVDS connected to AMC Port[18] |
| H29 | IO\_L12N\_T1\_MRCC\_19 | 19 | LVDS\_Tx1n | LVDS connected to AMC Port[18] |
| K27 | IO\_L13P\_T2\_MRCC\_19 | 19 | LVDS\_Rx1p | LVDS connected to AMC Port[18] |
| J27 | IO\_L13N\_T2\_MRCC\_19 | 19 | LVDS\_Rx1n | LVDS connected to AMC Port[18] |
| BA18 | IO\_L1P\_T0\_34 | 34 | DDRdm0 | DDR Memory Interface |
| BB18 | IO\_L1N\_T0\_34 | 34 | DDRdata0 | DDR Memory Interface |
| BC19 | IO\_L2P\_T0\_34 | 34 | DDRdata1 | DDR Memory Interface |
| BC18 | IO\_L2N\_T0\_34 | 34 | DDRdata2 | DDR Memory Interface |
| BB17 | IO\_L3P\_T0\_DQS\_34 | 34 | DDRdqs0 | DDR Memory Interface |
| BC17 | IO\_L3N\_T0\_DQS\_34 | 34 | DDRdqs0n | DDR Memory Interface |
| BD17 | IO\_L4P\_T0\_34 | 34 | DDRdata3 | DDR Memory Interface |
| BD16 | IO\_L4N\_T0\_34 | 34 | DDRdata4 | DDR Memory Interface |
| BC15 | IO\_L5P\_T0\_34 | 34 | DDRdata5 | DDR Memory Interface |
| BD15 | IO\_L5N\_T0\_34 | 34 | DDRdata6 | DDR Memory Interface |
| BB16 | IO\_L6P\_T0\_34 | 34 | DDRdata7 | DDR Memory Interface |
| AW17 | IO\_L7P\_T1\_34 | 34 | DDRdm1 | DDR Memory Interface |
| AY16 | IO\_L7N\_T1\_34 | 34 | DDRdata8 | DDR Memory Interface |
| AY18 | IO\_L8P\_T1\_34 | 34 | DDRdata9 | DDR Memory Interface |
| AY17 | IO\_L8N\_T1\_34 | 34 | DDRdata10 | DDR Memory Interface |
| AW16 | IO\_L9P\_T1\_DQS\_34 | 34 | DDRdqs1 | DDR Memory Interface |
| AW15 | IO\_L9N\_T1\_DQS\_34 | 34 | DDRdqs1n | DDR Memory Interface |
| BA16 | IO\_L10P\_T1\_34 | 34 | DDRdata11 | DDR Memory Interface |
| BA15 | IO\_L10N\_T1\_34 | 34 | DDRdata12 | DDR Memory Interface |
| AV18 | IO\_L11P\_T1\_SRCC\_34 | 34 | DDRdata13 | DDR Memory Interface |
| AV17 | IO\_L11N\_T1\_SRCC\_34 | 34 | DDRdata14 | DDR Memory Interface |
| AU15 | IO\_L12P\_T1\_MRCC\_34 | 34 | DDRdata15 | DDR Memory Interface |
| BB22 | IO\_L1P\_T0\_AD4P\_35 | 35 | DDRadr13 | DDR Memory Interface |
| BB21 | IO\_L1N\_T0\_AD4N\_35 | 35 | DDRadr12 | DDR Memory Interface |
| BC22 | IO\_L2P\_T0\_AD12P\_35 | 35 | DDRadr11 | DDR Memory Interface |
| BD22 | IO\_L2N\_T0\_AD12N\_35 | 35 | DDRadr10 | DDR Memory Interface |
| BC20 | IO\_L3P\_T0\_DQS\_AD5P\_35 | 35 | DDRCLKp | DDR Memory Interface |
| BD19 | IO\_L3N\_T0\_DQS\_AD5N\_35 | 35 | DDRCLKn | DDR Memory Interface |
| BD21 | IO\_L4P\_T0\_35 | 35 | DDRadr9 | DDR Memory Interface |
| BD20 | IO\_L4N\_T0\_35 | 35 | DDRadr8 | DDR Memory Interface |
| BA21 | IO\_L5P\_T0\_AD13P\_35 | 35 | DDRadr7 | DDR Memory Interface |
| BB20 | IO\_L5N\_T0\_AD13N\_35 | 35 | DDRadr6 | DDR Memory Interface |
| BA20 | IO\_L6P\_T0\_35 | 35 | DDRadr5 | DDR Memory Interface |
| BA19 | IO\_L6N\_T0\_VREF\_35 | 35 | DDRadr4 | DDR Memory Interface |
| AW22 | IO\_L7P\_T1\_AD6P\_35 | 35 | DDRadr3 | DDR Memory Interface |
| AY22 | IO\_L7N\_T1\_AD6N\_35 | 35 | DDRadr2 | DDR Memory Interface |
| AV20 | IO\_L8P\_T1\_AD14P\_35 | 35 | DDRadr1 | DDR Memory Interface |
| AW20 | IO\_L8N\_T1\_AD14N\_35 | 35 | DDRadr0 | DDR Memory Interface |
| AW21 | IO\_L9P\_T1\_DQS\_AD7P\_35 | 35 | DDRba2 | DDR Memory Interface |
| AY21 | IO\_L9N\_T1\_DQS\_AD7N\_35 | 35 | DDRba1 | DDR Memory Interface |
| AW19 | IO\_L10P\_T1\_AD15P\_35 | 35 | DDRba0 | DDR Memory Interface |
| AY19 | IO\_L10N\_T1\_AD15N\_35 | 35 | DDRrasn | DDR Memory Interface |
| AU22 | IO\_L11P\_T1\_SRCC\_35 | 35 | DDRcasn | DDR Memory Interface |
| AV22 | IO\_L11N\_T1\_SRCC\_35 | 35 | DDRwen | DDR Memory Interface |
| AU20 | IO\_L12P\_T1\_MRCC\_35 | 35 | DDRcsn | DDR Memory Interface |
| AT21 | IO\_L13P\_T2\_MRCC\_35 | 35 | SYSCLKp | DDR Memory Interface |
| AU21 | IO\_L13N\_T2\_MRCC\_35 | 35 | SYSCLKn | DDR Memory Interface |
| AP21 | IO\_L15P\_T2\_DQS\_35 | 35 | DDRcke | DDR Memory Interface |
| AP20 | IO\_L15N\_T2\_DQS\_35 | 35 | DDRodt | DDR Memory Interface |
| AV14 | IO\_L13P\_T2\_MRCC\_36 | 36 | DDRdata24 | DDR Memory Interface |
| AW14 | IO\_L13N\_T2\_MRCC\_36 | 36 | DDRdata25 | DDR Memory Interface |
| AW11 | IO\_L14P\_T2\_SRCC\_36 | 36 | DDRdata26 | DDR Memory Interface |
| AW10 | IO\_L14N\_T2\_SRCC\_36 | 36 | DDRdata27 | DDR Memory Interface |
| AY13 | IO\_L15P\_T2\_DQS\_36 | 36 | DDRdqs3 | DDR Memory Interface |
| BA13 | IO\_L15N\_T2\_DQS\_36 | 36 | DDRdqs3n | DDR Memory Interface |
| AY12 | IO\_L16P\_T2\_36 | 36 | DDRdm3 | DDR Memory Interface |
| AY11 | IO\_L16N\_T2\_36 | 36 | DDRdata28 | DDR Memory Interface |
| BA11 | IO\_L17P\_T2\_36 | 36 | DDRdata29 | DDR Memory Interface |
| BA10 | IO\_L17N\_T2\_36 | 36 | DDRdata30 | DDR Memory Interface |
| AY14 | IO\_L18P\_T2\_36 | 36 | DDRdata31 | DDR Memory Interface |
| BA14 | IO\_L18N\_T2\_36 | 36 | DDRrstn | DDR Memory Interface |
| BB11 | IO\_L19P\_T3\_36 | 36 | DDRdm2 | DDR Memory Interface |
| BB12 | IO\_L20P\_T3\_36 | 36 | DDRdata16 | DDR Memory Interface |
| BC12 | IO\_L20N\_T3\_36 | 36 | DDRdata17 | DDR Memory Interface |
| BD12 | IO\_L21P\_T3\_DQS\_36 | 36 | DDRdqs2 | DDR Memory Interface |
| BD11 | IO\_L21N\_T3\_DQS\_36 | 36 | DDRdqs2n | DDR Memory Interface |
| BB13 | IO\_L22P\_T3\_36 | 36 | DDRdata18 | DDR Memory Interface |
| BC13 | IO\_L22N\_T3\_36 | 36 | DDRdata19 | DDR Memory Interface |
| BC14 | IO\_L23P\_T3\_36 | 36 | DDRdata20 | DDR Memory Interface |
| BD14 | IO\_L23N\_T3\_36 | 36 | DDRdata21 | DDR Memory Interface |
| BC10 | IO\_L24P\_T3\_36 | 36 | DDRdata22 | DDR Memory Interface |
| BD10 | IO\_L24N\_T3\_36 | 36 | DDRdata23 | DDR Memory Interface |
| AG2 | MGTXTXP3\_113 | 113 | Tx03p | Connection to uPOD\_Tx U16 |
| AE6 | MGTXRXP3\_113 |  | Rx03p | Connection to uPOD\_Rx U5 |
| AG1 | MGTXTXN3\_113 |  | Tx03n | Connection to uPOD\_Tx U16 |
| AE5 | MGTXRXN3\_113 |  | Rx03n | Connection to uPOD\_Rx U5 |
| AH4 | MGTXTXP2\_113 |  | Tx02p | Connection to uPOD\_Tx U16 |
| AG6 | MGTXRXP2\_113 |  | Rx02p | Connection to uPOD\_Rx U5 |
| AH3 | MGTXTXN2\_113 |  | Tx02n | Connection to uPOD\_Tx U16 |
| AG5 | MGTXRXN2\_113 |  | Rx02n | Connection to uPOD\_Rx U5 |
| AJ2 | MGTXTXP1\_113 |  | Tx01p | Connection to uPOD\_Tx U16 |
| AJ6 | MGTXRXP1\_113 |  | Rx01p | Connection to uPOD\_Rx U5 |
| AJ1 | MGTXTXN1\_113 |  | Tx01n | Connection to uPOD\_Tx U16 |
| AJ5 | MGTXRXN1\_113 |  | Rx01n | Connection to uPOD\_Rx U5 |
| AK4 | MGTXTXP0\_113 |  | Tx00p | Connection to uPOD\_Tx U16 |
| AK8 | MGTXRXP0\_113 |  | Rx00p | Connection to uPOD\_Rx U5 |
| AK3 | MGTXTXN0\_113 |  | Tx00n | Connection to uPOD\_Tx U16 |
| AK7 | MGTXRXN0\_113 |  | Rx00n | Connection to uPOD\_Rx U5 |
| AC2 | MGTXTXP3\_114 | 114 | Tx07p | Connection to uPOD\_Tx U16 |
| Y8 | MGTXRXP3\_114 | 114 | Rx07p | Connection to uPOD\_Rx U5 |
| AC1 | MGTXTXN3\_114 | 114 | Tx07n | Connection to uPOD\_Tx U16 |
| Y7 | MGTXRXN3\_114 | 114 | Rx07n | Connection to uPOD\_Rx U5 |
| AD4 | MGTXTXP2\_114 | 114 | Tx06p | Connection to uPOD\_Tx U16 |
| AA6 | MGTXRXP2\_114 | 114 | Rx06p | Connection to uPOD\_Rx U5 |
| AD3 | MGTXTXN2\_114 | 114 | Tx06n | Connection to uPOD\_Tx U16 |
| AA10 | MGTREFCLK0P\_114 | 114 | REFCLK\_0p | Ref. Clock for Quads 113, 114, 115 |
| AA5 | MGTXRXN2\_114 | 114 | Rx06n | Connection to uPOD\_Rx U5 |
| AA9 | MGTREFCLK0N\_114 | 114 | REFCLK\_0n | Ref. Clock for Quads 113, 114, 115 |
| AB7 | MGTREFCLK1N\_114 | 114 | REFCLK\_4n | Ref. Clock for Quads 113, 114, 115 |
| AB8 | MGTREFCLK1P\_114 | 114 | REFCLK\_4p | Ref. Clock for Quads 113, 114, 115 |
| AE2 | MGTXTXP1\_114 | 114 | Tx05p | Connection to uPOD\_Tx U16 |
| AC6 | MGTXRXP1\_114 | 114 | Rx05p | Connection to uPOD\_Rx U5 |
| AE1 | MGTXTXN1\_114 | 114 | Tx05n | Connection to uPOD\_Tx U16 |
| AC5 | MGTXRXN1\_114 | 114 | Rx05n | Connection to uPOD\_Rx U5 |
| AF4 | MGTXTXP0\_114 | 114 | Tx04p | Connection to uPOD\_Tx U16 |
| AD8 | MGTXRXP0\_114 | 114 | Rx04p | Connection to uPOD\_Rx U5 |
| AF3 | MGTXTXN0\_114 | 114 | Tx04n | Connection to uPOD\_Tx U16 |
| AD7 | MGTXRXN0\_114 | 114 | Rx04n | Connection to uPOD\_Rx U5 |
| W2 | MGTXTXP3\_115 | 115 | Tx11p | Connection to uPOD\_Tx U16 |
| T8 | MGTXRXP3\_115 | 115 | Rx11p | Connection to uPOD\_Rx U5 |
| W1 | MGTXTXN3\_115 | 115 | Tx11n | Connection to uPOD\_Tx U16 |
| T7 | MGTXRXN3\_115 | 115 | Rx11n | Connection to uPOD\_Rx U5 |
| Y4 | MGTXTXP2\_115 | 115 | Tx10p | Connection to uPOD\_Tx U16 |
| U6 | MGTXRXP2\_115 | 115 | Rx10p | Connection to uPOD\_Rx U5 |
| Y3 | MGTXTXN2\_115 | 115 | Tx10n | Connection to uPOD\_Tx U16 |
| U5 | MGTXRXN2\_115 | 115 | Rx10n | Connection to uPOD\_Rx U5 |
| AA2 | MGTXTXP1\_115 | 115 | Tx09p | Connection to uPOD\_Tx U16 |
| V8 | MGTXRXP1\_115 | 115 | Rx09p | Connection to uPOD\_Rx U5 |
| AA1 | MGTXTXN1\_115 | 115 | Tx09n | Connection to uPOD\_Tx U16 |
| V7 | MGTXRXN1\_115 | 115 | Rx09n | Connection to uPOD\_Rx U5 |
| AB4 | MGTXTXP0\_115 | 115 | Tx08p | Connection to uPOD\_Tx U16 |
| W6 | MGTXRXP0\_115 | 115 | Rx08p | Connection to uPOD\_Rx U5 |
| AB3 | MGTXTXN0\_115 | 115 | Tx08n | Connection to uPOD\_Tx U16 |
| W5 | MGTXRXN0\_115 | 115 | Rx08n | Connection to uPOD\_Rx U5 |
| R2 | MGTXTXP3\_116 | 116 | Tx15p | Connection to uPOD\_Tx U17 |
| M8 | MGTXRXP3\_116 | 116 | Rx15p | Connection to uPOD\_Rx U6 |
| R1 | MGTXTXN3\_116 | 116 | Tx15n | Connection to uPOD\_Tx U17 |
| M7 | MGTXRXN3\_116 | 116 | Rx15n | Connection to uPOD\_Rx U6 |
| T4 | MGTXTXP2\_116 | 116 | Tx14p | Connection to uPOD\_Tx U17 |
| N6 | MGTXRXP2\_116 | 116 | Rx14p | Connection to uPOD\_Rx U6 |
| T3 | MGTXTXN2\_116 | 116 | Tx14n | Connection to uPOD\_Tx U17 |
| N5 | MGTXRXN2\_116 | 116 | Rx14n | Connection to uPOD\_Rx U6 |
| U2 | MGTXTXP1\_116 | 116 | Tx13p | Connection to uPOD\_Tx U17 |
| P8 | MGTXRXP1\_116 | 116 | Rx13p | Connection to uPOD\_Rx U6 |
| U1 | MGTXTXN1\_116 | 116 | Tx13n | Connection to uPOD\_Tx U17 |
| P7 | MGTXRXN1\_116 | 116 | Rx13n | Connection to uPOD\_Rx U6 |
| V4 | MGTXTXP0\_116 | 116 | Tx12p | Connection to uPOD\_Tx U17 |
| R6 | MGTXRXP0\_116 | 116 | Rx12p | Connection to uPOD\_Rx U6 |
| V3 | MGTXTXN0\_116 | 116 | Tx12n | Connection to uPOD\_Tx U17 |
| R5 | MGTXRXN0\_116 | 116 | Rx12n | Connection to uPOD\_Rx U6 |
| L2 | MGTXTXP3\_117 | 117 | Tx19p | Connection to uPOD\_Tx U17 |
| H8 | MGTXRXP3\_117 | 117 | Rx19p | Connection to uPOD\_Rx U6 |
| L1 | MGTXTXN3\_117 | 117 | Tx19n | Connection to uPOD\_Tx U17 |
| H7 | MGTXRXN3\_117 | 117 | Rx19n | Connection to uPOD\_Rx U6 |
| M4 | MGTXTXP2\_117 | 117 | Tx18p | Connection to uPOD\_Tx U17 |
| J6 | MGTXRXP2\_117 | 117 | Rx18p | Connection to uPOD\_Rx U6 |
| M3 | MGTXTXN2\_117 | 117 | Tx18n | Connection to uPOD\_Tx U17 |
| J10 | MGTREFCLK0P\_117 | 117 | REFCLK\_1p | Ref. Clock for Quads 116, 117, 118 |
| J5 | MGTXRXN2\_117 | 117 | Rx18n | Connection to uPOD\_Rx U6 |
| J9 | MGTREFCLK0N\_117 | 117 | REFCLK\_1n | Ref. Clock for Quads 116, 117, 118 |
| L9 | MGTREFCLK1N\_117 | 117 | REFCLK\_5n | Ref. Clock for Quads 116, 117, 118 |
| L10 | MGTREFCLK1P\_117 | 117 | REFCLK\_5p | Ref. Clock for Quads 116, 117, 118 |
| N2 | MGTXTXP1\_117 | 117 | Tx17p | Connection to uPOD\_Tx U17 |
| K8 | MGTXRXP1\_117 | 117 | Rx17p | Connection to uPOD\_Rx U6 |
| N1 | MGTXTXN1\_117 | 117 | Tx17n | Connection to uPOD\_Tx U17 |
| K7 | MGTXRXN1\_117 | 117 | Rx17n | Connection to uPOD\_Rx U6 |
| P4 | MGTXTXP0\_117 | 117 | Tx16p | Connection to uPOD\_Tx U17 |
| L6 | MGTXRXP0\_117 | 117 | Rx16p | Connection to uPOD\_Rx U6 |
| P3 | MGTXTXN0\_117 | 117 | Tx16n | Connection to uPOD\_Tx U17 |
| L5 | MGTXRXN0\_117 | 117 | Rx16n | Connection to uPOD\_Rx U6 |
| G2 | MGTXTXP3\_118 | 118 | Tx23p | Connection to uPOD\_Tx U17 |
| D8 | MGTXRXP3\_118 | 118 | Rx23p | Connection to uPOD\_Rx U6 |
| G1 | MGTXTXN3\_118 | 118 | Tx23n | Connection to uPOD\_Tx U17 |
| D7 | MGTXRXN3\_118 | 118 | Rx23n | Connection to uPOD\_Rx U6 |
| H4 | MGTXTXP2\_118 | 118 | Tx22p | Connection to uPOD\_Tx U17 |
| E6 | MGTXRXP2\_118 | 118 | Rx22p | Connection to uPOD\_Rx U6 |
| H3 | MGTXTXN2\_118 | 118 | Tx22n | Connection to uPOD\_Tx U17 |
| E5 | MGTXRXN2\_118 | 118 | Rx22n | Connection to uPOD\_Rx U6 |
| J2 | MGTXTXP1\_118 | 118 | Tx21p | Connection to uPOD\_Tx U17 |
| F8 | MGTXRXP1\_118 | 118 | Rx21p | Connection to uPOD\_Rx U6 |
| J1 | MGTXTXN1\_118 | 118 | Tx21n | Connection to uPOD\_Tx U17 |
| F7 | MGTXRXN1\_118 | 118 | Rx21n | Connection to uPOD\_Rx U6 |
| K4 | MGTXTXP0\_118 | 118 | Tx20p | Connection to uPOD\_Tx U17 |
| G6 | MGTXRXP0\_118 | 118 | Rx20p | Connection to uPOD\_Rx U6 |
| K3 | MGTXTXN0\_118 | 118 | Tx20n | Connection to uPOD\_Tx U17 |
| G5 | MGTXRXN0\_118 | 118 | Rx20n | Connection to uPOD\_Rx U6 |
| B4 | MGTXTXP3\_119 | 119 | GbE\_Tx3p | connected to AMC\_Port[20] |
| A6 | MGTXRXP3\_119 | 119 | GbE\_Rx3p | connected to AMC\_Port[20] |
| B3 | MGTXTXN3\_119 | 119 | GbE\_Tx3n | connected to AMC\_Port[20] |
| A5 | MGTXRXN3\_119 | 119 | GbE\_Rx3n | connected to AMC\_Port[20] |
| C2 | MGTXTXP2\_119 | 119 | GbE\_Tx2p | connected to AMC\_Port[13] |
| B8 | MGTXRXP2\_119 | 119 | GbE\_Rx2p | connected to AMC\_Port[13] |
| C1 | MGTXTXN2\_119 | 119 | GbE\_Tx2n | connected to AMC\_Port[13] |
| A10 | MGTREFCLK0P\_119 | 119 | GbECLKp | Ref. Clock for GbE Channels |
| B7 | MGTXRXN2\_119 | 119 | GbE\_Rx2n | connected to AMC\_Port[13] |
| A9 | MGTREFCLK0N\_119 | 119 | GbECLKn | Ref. Clock for GbE Channels |
| C9 | MGTREFCLK1N\_119 | 119 | REFCLK\_8n | Ref. Clock for GbE Channels |
| C10 | MGTREFCLK1P\_119 | 119 | REFCLK\_8p | Ref. Clock for GbE Channels |
| E2 | MGTXTXP1\_119 | 119 | GbE\_Tx1p | connected to AMC\_Port[12] |
| C6 | MGTXRXP1\_119 | 119 | GbE\_Rx1p | connected to AMC\_Port[12] |
| E1 | MGTXTXN1\_119 | 119 | GbE\_Tx1n | connected to AMC\_Port[12] |
| C5 | MGTXRXN1\_119 | 119 | GbE\_Rx1n | connected to AMC\_Port[12] |
| F4 | MGTXTXP0\_119 | 119 | GbE\_Tx0p | connected to AMC\_Port[0] |
| D4 | MGTXRXP0\_119 | 119 | GbE\_Rx0p | connected to AMC\_Port[0] |
| F3 | MGTXTXN0\_119 | 119 | GbE\_Tx0n | connected to AMC\_Port[0] |
| D3 | MGTXRXN0\_119 | 119 | GbE\_Rx0n | connected to AMC\_Port[0] |
| AG43 | MGTXTXP3\_213 | 213 | XAUI\_Tx3p | connected to AMC\_Port[11] |
| AE39 | MGTXRXP3\_213 | 213 | XAUI\_Rx3p | connected to AMC\_Port[11] |
| AG44 | MGTXTXN3\_213 | 213 | XAUI\_Tx3n | connected to AMC\_Port[11] |
| AE40 | MGTXRXN3\_213 | 213 | XAUI\_Rx3n | connected to AMC\_Port[11] |
| AH41 | MGTXTXP2\_213 | 213 | XAUI\_Tx2p | connected to AMC\_Port[10] |
| AG39 | MGTXRXP2\_213 | 213 | XAUI\_Rx2p | connected to AMC\_Port[10] |
| AH42 | MGTXTXN2\_213 | 213 | XAUI\_Tx2n | connected to AMC\_Port[10] |
| AF37 | MGTREFCLK0P\_213 | 213 | XAUICLKp | Ref. Clock for XAUI Channels |
| AG40 | MGTXRXN2\_213 | 213 | XAUI\_Rx2n | connected to AMC\_Port[10] |
| AF38 | MGTREFCLK0N\_213 | 213 | XAUICLKn | Ref. Clock for XAUI Channels |
| AH38 | MGTREFCLK1N\_213 | 213 | AMC\_TCLKAn | Ref. Clock for XAUI Channels |
| AH37 | MGTREFCLK1P\_213 | 213 | AMC\_TCLKAp | Ref. Clock for XAUI Channels |
| AJ43 | MGTXTXP1\_213 | 213 | XAUI\_Tx1p | connected to AMC\_Port[9] |
| AJ39 | MGTXRXP1\_213 | 213 | XAUI\_Rx1p | connected to AMC\_Port[9] |
| AJ44 | MGTXTXN1\_213 | 213 | XAUI\_Tx1n | connected to AMC\_Port[9] |
| AJ40 | MGTXRXN1\_213 | 213 | XAUI\_Rx1n | connected to AMC\_Port[9] |
| AK41 | MGTXTXP0\_213 | 213 | XAUI\_Tx0p | connected to AMC\_Port[8] |
| AK37 | MGTXRXP0\_213 | 213 | XAUI\_Rx0p | connected to AMC\_Port[8] |
| AK42 | MGTXTXN0\_213 | 213 | XAUI\_Tx0n | connected to AMC\_Port[8] |
| AK38 | MGTXRXN0\_213 | 213 | XAUI\_Rx0n | connected to AMC\_Port[8] |
| AC43 | MGTXTXP3\_214 | 214 | Tx47p | Connection to uPOD\_Tx U19 |
| Y37 | MGTXRXP3\_214 | 214 | Rx47p | Connection to uPOD\_Rx U8 |
| AC44 | MGTXTXN3\_214 | 214 | Tx47n | Connection to uPOD\_Tx U19 |
| Y38 | MGTXRXN3\_214 | 214 | Rx47n | Connection to uPOD\_Rx U8 |
| AD41 | MGTXTXP2\_214 | 214 | Tx46p | Connection to uPOD\_Tx U19 |
| AA39 | MGTXRXP2\_214 | 214 | Rx46p | Connection to uPOD\_Rx U8 |
| AD42 | MGTXTXN2\_214 | 214 | Tx46n | Connection to uPOD\_Tx U19 |
| AA40 | MGTXRXN2\_214 | 214 | Rx46n | Connection to uPOD\_Rx U8 |
| AE43 | MGTXTXP1\_214 | 214 | Tx45p | Connection to uPOD\_Tx U19 |
| AC39 | MGTXRXP1\_214 | 214 | Rx45p | Connection to uPOD\_Rx U8 |
| AE44 | MGTXTXN1\_214 | 214 | Tx45n | Connection to uPOD\_Tx U19 |
| AC40 | MGTXRXN1\_214 | 214 | Rx45n | Connection to uPOD\_Rx U8 |
| AF41 | MGTXTXP0\_214 | 214 | Tx44p | Connection to uPOD\_Tx U19 |
| AD37 | MGTXRXP0\_214 | 214 | Rx44p | Connection to uPOD\_Rx U8 |
| AF42 | MGTXTXN0\_214 | 214 | Tx44n | Connection to uPOD\_Tx U19 |
| AD38 | MGTXRXN0\_214 | 214 | Rx44n | Connection to uPOD\_Rx U8 |
| W43 | MGTXTXP3\_215 | 215 | Tx43p | Connection to uPOD\_Tx U19 |
| T37 | MGTXRXP3\_215 | 215 | Rx43p | Connection to uPOD\_Rx U8 |
| W44 | MGTXTXN3\_215 | 215 | Tx43n | Connection to uPOD\_Tx U19 |
| T38 | MGTXRXN3\_215 | 215 | Rx43n | Connection to uPOD\_Rx U8 |
| Y41 | MGTXTXP2\_215 | 215 | Tx42p | Connection to uPOD\_Tx U19 |
| U39 | MGTXRXP2\_215 | 215 | Rx42p | Connection to uPOD\_Rx U8 |
| Y42 | MGTXTXN2\_215 | 215 | Tx42n | Connection to uPOD\_Tx U19 |
| U35 | MGTREFCLK0P\_215 | 215 | REFCLK\_2p | Ref. Clock for Quads 214, 215, 216 |
| U40 | MGTXRXN2\_215 | 215 | Rx42n | Connection to uPOD\_Rx U8 |
| U36 | MGTREFCLK0N\_215 | 215 | REFCLK\_2n | Ref. Clock for Quads 214, 215, 216 |
| W36 | MGTREFCLK1N\_215 | 215 | REFCLK\_6n | Ref. Clock for Quads 214, 215, 216 |
| W35 | MGTREFCLK1P\_215 | 215 | REFCLK\_6p | Ref. Clock for Quads 214, 215, 216 |
| AA43 | MGTXTXP1\_215 | 215 | Tx41p | Connection to uPOD\_Tx U19 |
| V37 | MGTXRXP1\_215 | 215 | Rx41p | Connection to uPOD\_Rx U8 |
| AA44 | MGTXTXN1\_215 | 215 | Tx41n | Connection to uPOD\_Tx U19 |
| V38 | MGTXRXN1\_215 | 215 | Rx41n | Connection to uPOD\_Rx U8 |
| AB41 | MGTXTXP0\_215 | 215 | Tx40p | Connection to uPOD\_Tx U19 |
| W39 | MGTXRXP0\_215 | 215 | Rx40p | Connection to uPOD\_Rx U8 |
| AB42 | MGTXTXN0\_215 | 215 | Tx40n | Connection to uPOD\_Tx U19 |
| W40 | MGTXRXN0\_215 | 215 | Rx40n | Connection to uPOD\_Rx U8 |
| R43 | MGTXTXP3\_216 | 216 | Tx39p | Connection to uPOD\_Tx U19 |
| M37 | MGTXRXP3\_216 | 216 | Rx39p | Connection to uPOD\_Rx U8 |
| R44 | MGTXTXN3\_216 | 216 | Tx39n | Connection to uPOD\_Tx U19 |
| M38 | MGTXRXN3\_216 | 216 | Rx39n | Connection to uPOD\_Rx U8 |
| T41 | MGTXTXP2\_216 | 216 | Tx38p | Connection to uPOD\_Tx U19 |
| N39 | MGTXRXP2\_216 | 216 | Rx38p | Connection to uPOD\_Rx U8 |
| T42 | MGTXTXN2\_216 | 216 | Tx38n | Connection to uPOD\_Tx U19 |
| N40 | MGTXRXN2\_216 | 216 | Rx38n | Connection to uPOD\_Rx U8 |
| U43 | MGTXTXP1\_216 | 216 | Tx37p | Connection to uPOD\_Tx U19 |
| P37 | MGTXRXP1\_216 | 216 | Rx37p | Connection to uPOD\_Rx U8 |
| U44 | MGTXTXN1\_216 | 216 | Tx37n | Connection to uPOD\_Tx U19 |
| P38 | MGTXRXN1\_216 | 216 | Rx37n | Connection to uPOD\_Rx U8 |
| V41 | MGTXTXP0\_216 | 216 | Tx36p | Connection to uPOD\_Tx U19 |
| R39 | MGTXRXP0\_216 | 216 | Rx36p | Connection to uPOD\_Rx U8 |
| V42 | MGTXTXN0\_216 | 216 | Tx36n | Connection to uPOD\_Tx U19 |
| R40 | MGTXRXN0\_216 | 216 | Rx36n | Connection to uPOD\_Rx U8 |
| L43 | MGTXTXP3\_217 | 217 | Tx35p | Connection to uPOD\_Tx U18 |
| H37 | MGTXRXP3\_217 | 217 | Rx35p | Connection to uPOD\_Rx U7 |
| L44 | MGTXTXN3\_217 | 217 | Tx35n | Connection to uPOD\_Tx U18 |
| H38 | MGTXRXN3\_217 | 217 | Rx35n | Connection to uPOD\_Rx U7 |
| M41 | MGTXTXP2\_217 | 217 | Tx34p | Connection to uPOD\_Tx U18 |
| J39 | MGTXRXP2\_217 | 217 | Rx34p | Connection to uPOD\_Rx U7 |
| M42 | MGTXTXN2\_217 | 217 | Tx34n | Connection to uPOD\_Tx U18 |
| J40 | MGTXRXN2\_217 | 217 | Rx34n | Connection to uPOD\_Rx U7 |
| N43 | MGTXTXP1\_217 | 217 | Tx33p | Connection to uPOD\_Tx U18 |
| K37 | MGTXRXP1\_217 | 217 | Rx33p | Connection to uPOD\_Rx U7 |
| N44 | MGTXTXN1\_217 | 217 | Tx33n | Connection to uPOD\_Tx U18 |
| K38 | MGTXRXN1\_217 | 217 | Rx33n | Connection to uPOD\_Rx U7 |
| P41 | MGTXTXP0\_217 | 217 | Tx32p | Connection to uPOD\_Tx U18 |
| L39 | MGTXRXP0\_217 | 217 | Rx32p | Connection to uPOD\_Rx U7 |
| P42 | MGTXTXN0\_217 | 217 | Tx32n | Connection to uPOD\_Tx U18 |
| L40 | MGTXRXN0\_217 | 217 | Rx32n | Connection to uPOD\_Rx U7 |
| G43 | MGTXTXP3\_218 | 218 | Tx31p | Connection to uPOD\_Tx U18 |
| D37 | MGTXRXP3\_218 | 218 | Rx31p | Connection to uPOD\_Rx U7 |
| G44 | MGTXTXN3\_218 | 218 | Tx31n | Connection to uPOD\_Tx U18 |
| D38 | MGTXRXN3\_218 | 218 | Rx31n | Connection to uPOD\_Rx U7 |
| H41 | MGTXTXP2\_218 | 218 | Tx30p | Connection to uPOD\_Tx U18 |
| E39 | MGTXRXP2\_218 | 218 | Rx30p | Connection to uPOD\_Rx U7 |
| H42 | MGTXTXN2\_218 | 218 | Tx30n | Connection to uPOD\_Tx U18 |
| E35 | MGTREFCLK0P\_218 | 218 | REFCLK\_3p | Ref. Clock for Quads 217, 218, 219 |
| E40 | MGTXRXN2\_218 | 218 | Rx30n | Connection to uPOD\_Rx U7 |
| E36 | MGTREFCLK0N\_218 | 218 | REFCLK\_3n | Ref. Clock for Quads 217, 218, 219 |
| G36 | MGTREFCLK1N\_218 | 218 | REFCLK\_7n | Ref. Clock for Quads 217, 218, 219 |
| G35 | MGTREFCLK1P\_218 | 218 | REFCLK\_7p | Ref. Clock for Quads 217, 218, 219 |
| J43 | MGTXTXP1\_218 | 218 | Tx29p | Connection to uPOD\_Tx U18 |
| F37 | MGTXRXP1\_218 | 218 | Rx29p | Connection to uPOD\_Rx U7 |
| J44 | MGTXTXN1\_218 | 218 | Tx29n | Connection to uPOD\_Tx U18 |
| F38 | MGTXRXN1\_218 | 218 | Rx29n | Connection to uPOD\_Rx U7 |
| K41 | MGTXTXP0\_218 | 218 | Tx28p | Connection to uPOD\_Tx U18 |
| G39 | MGTXRXP0\_218 | 218 | Rx28p | Connection to uPOD\_Rx U7 |
| K42 | MGTXTXN0\_218 | 218 | Tx28n | Connection to uPOD\_Tx U18 |
| G40 | MGTXRXN0\_218 | 218 | Rx28n | Connection to uPOD\_Rx U7 |
| B41 | MGTXTXP3\_219 | 219 | Tx27p | Connection to uPOD\_Tx U18 |
| A39 | MGTXRXP3\_219 | 219 | Rx27p | Connection to uPOD\_Rx U7 |
| B42 | MGTXTXN3\_219 | 219 | Tx27n | Connection to uPOD\_Tx U18 |
| A40 | MGTXRXN3\_219 | 219 | Rx27n | Connection to uPOD\_Rx U7 |
| C43 | MGTXTXP2\_219 | 219 | Tx26p | Connection to uPOD\_Tx U18 |
| B37 | MGTXRXP2\_219 | 219 | Rx26p | Connection to uPOD\_Rx U7 |
| C44 | MGTXTXN2\_219 | 219 | Tx26n | Connection to uPOD\_Tx U18 |
| B38 | MGTXRXN2\_219 | 219 | Rx26n | Connection to uPOD\_Rx U7 |
| E43 | MGTXTXP1\_219 | 219 | Tx25p | Connection to uPOD\_Tx U18 |
| C39 | MGTXRXP1\_219 | 219 | Rx25p | Connection to uPOD\_Rx U7 |
| E44 | MGTXTXN1\_219 | 219 | Tx25n | Connection to uPOD\_Tx U18 |
| C40 | MGTXRXN1\_219 | 219 | Rx25n | Connection to uPOD\_Rx U7 |
| F41 | MGTXTXP0\_219 | 219 | Tx24p | Connection to uPOD\_Tx U18 |
| D41 | MGTXRXP0\_219 | 219 | Rx24p | Connection to uPOD\_Rx U7 |
| F42 | MGTXTXN0\_219 | 219 | Tx24n | Connection to uPOD\_Tx U18 |
| D42 | MGTXRXN0\_219 | 219 | Rx24n | Connection to uPOD\_Rx U7 |

1. There are two speed grades of micropods, one rated to 10.3 Gbps and one to 12.5 Gbps. Tests thus far have used only the slower speed grade micropods. Tests will be made with the higher speed micropods in the coming month. [↑](#footnote-ref-1)
2. Pin compatible higher capacity XC7VX550TFFG1927 and XC7VX690TFFG1927 FPGAs with GTH transceivers can be used in place of the XC7VX485TFFG1927. The default speed grade is -2, but -3 parts have also been tested for the 485 series. [↑](#footnote-ref-2)
3. The eight outputs are actually quasi-independent, but for the OTC the natural use is two groups of four with one group used for the input frequency and the second for the output frequency if the two frequencies differ. [↑](#footnote-ref-3)
4. The fourth transceiver in the quad is used for the GbE interface on port 0 and is described in Sec. 3. [↑](#footnote-ref-4)