ALAIN LOU

ECE, UNIVERSITY OF WATERLOO

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SKILLS

LANGUAGES: Bash, C, C#, C++, Java, JavaScript, Perl, Python, RISC-V, Rust, Verilog/SystemVerilog, VHDL
FRAMEWORKS: cocotb, CppUTest, Litex, oneAPI, OpenCL, SYCL
TOOLS: AWS, Azure, CMake, GDB, Git, Linux, Logic Analyzer, Perforce, Quartus, Soldering, Vivado

EMPLOYMENT

Intel Sept. 2021 - Dec. 2021
IP Design Intern, External Memory Interfaces Remote
• Features for platform designer (Quartus) and next-gen memory

University of Waterloo May 2021 - Current
Research Assistant (part-time), Configurable Arch. Lab Remote
• Investigating area and performance characteristics of Efinix FPGA architecture
• Python and Tcl scripting, OpenCV to extract metrics not available in tool reporting
• Paper planned for FPGA 2022

Intel Jan. 2021 - May 2021
FPGA Software Engineering Intern, High Level Design Remote
• Improving performance, usability and code quality of OpenCL and SYCL products for Intel FPGAs
• Implemented USM host allocation use-after-free detection and warning, reset FPGA kernels on host program exit
• Ground-up rewrite of build system for FPGA runtime, using modern CMake, deleting 2.5k lines of Make code
• Addressed release gating issues: error in compiler, installation script shell compatibility and functional errors in SYCL designs
• Used GDB, OpenCL Intercept Layer and VS Debugger; gained knowledge about GCC, LD, MSVC and Quartus
• Group-wide triager for regression test failures in HLD products

Microsoft May 2020 - Aug. 2020
Explore Intern, OneDrive + SharePoint Remote
• PM and SWE in feature development lifecycle of datetime formatting and boolean rendering features in Microsoft Lists
• Collaborated cross-team to create design (Figma) and PM specs, iterating through user feedback, design critiques, spec reviews
• Implemented new web components using React, Fluent UI and the JavaScript Date API
• Wrote library functions to deal with localization, internationalization and timezone conversions

University of Waterloo Jan. 2020 - Apr. 2020
Research Assistant (part-time), Intelligent Connectivity Lab Waterloo, Canada
• Developed platform for distributed RFID readers, using Raspberry Pi running Windows 10 IoT and .NET framework
• Used Octane SDK for Impinj RAIN RFID reader and Azure services to build batch data pipeline
• Webapp GUI using d3.js frontend and Azure VM running nginx, gunicorn, flask, cronjobs for batch processing

PROJECTS

Litex Aug. 2021
• Booting and running RISC-V code on my FPGA board
• Learned about external memory interfacing, using ILAs, electrical effects of board connections
• Contributed to litex-boards open-source repo

Synth Apr. 2021
• All-digital monophonic square wave synthesizer, using a single clock domain
• 115 200-baud UART TX/RX

Pong Feb. 2021 - Mar. 2021
• Pure hardware implementation of Pong on an FPGA board
• 480x640 1-bit VGA controller, 7-segment scoreboard, ALTPLL

AWARDS

2nd Overall & Best Use of Azure, *Hack the 6ix* Aug. 2019

Best Use of StdLib, *EngHack* June 2019

Top 10 Overall, *Hack Lassonde* Mar. 2019

EDUCATION

University of Waterloo Sept. 2018 - Apr. 2023
Candidate for BASc Computer Engineering
• Dean's Honours List x2
• President's Research Award x2
• Mentor in Tech+, ECE Society; UW Engineering Ambassador