



# Bangladesh University of Engineering and Technology

Electrical and Electronic Engineering Department

## EEE 318 : Control System I Laboratory

### Experiment No. 5: PID Controller Design Using Root Locus Method

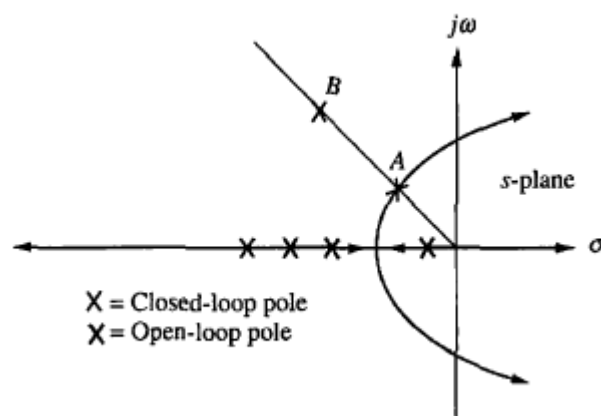
#### Objective:

To successfully design the P, I, PD, PI and PID Controllers to meet closed loop performance specifications including transient performance and steady-error.

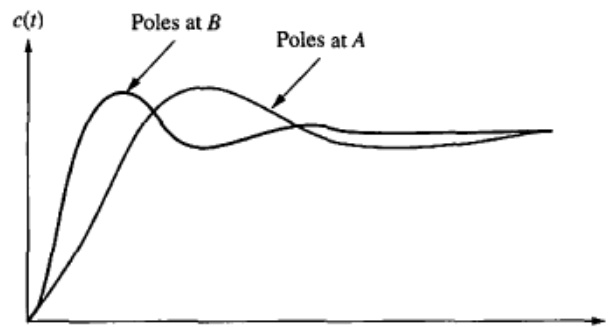
**Minimum required software packages:** MATLAB, Simulink, and the Control System Toolbox.

#### Theory:

The root locus indicates the achievable closed-loop pole locations of a system as a parameter (usually the controller gain) varies from zero to infinity. For a given plant it may or may not be possible to implement a simple proportional control (i.e., select a gain that specifies closed-loop locations along the root locus) to achieve the specified performance constraints. In fact, in most cases it will not be possible.



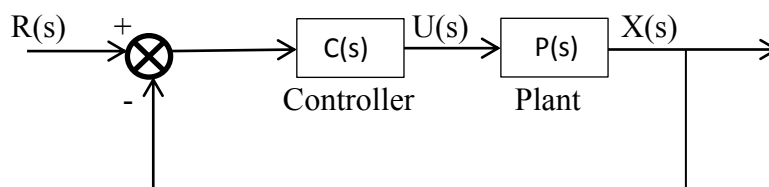
**Figure1:** Sample root locus, showing possible design point via gain adjustment(A) and desired design point that can not be met via simple gain adjustment(B)



**Figure 2: Responses from poles at A and B**

Figure 1 illustrates the concept. Assume that the desired transient response, defined by percent overshoot and settling time, is represented by point B. Unfortunately, on the current root locus at the specified percent overshoot, we only can obtain the settling time represented by point A after a simple gain adjustment. Thus, our goal is to speed up the response at A to that of B, without affecting the percent overshoot. This increase in speed cannot be accomplished by a simple gain adjustment, since point B does not lie on the root locus. Figure 2 illustrates the improvement in the transient response we seek. The faster response has the same percent overshoot as the slower response.

When such kind of problem occurs, it is the controller engineer's job to select a controller structure (a gain and a number of poles and zeros of a controller transfer function) and the respective controller parameters (values for the gain poles and zeros) to change the shape of the root locus so that for some values of the controller gain, the dominant second order closed-loop poles lie within the performance region.



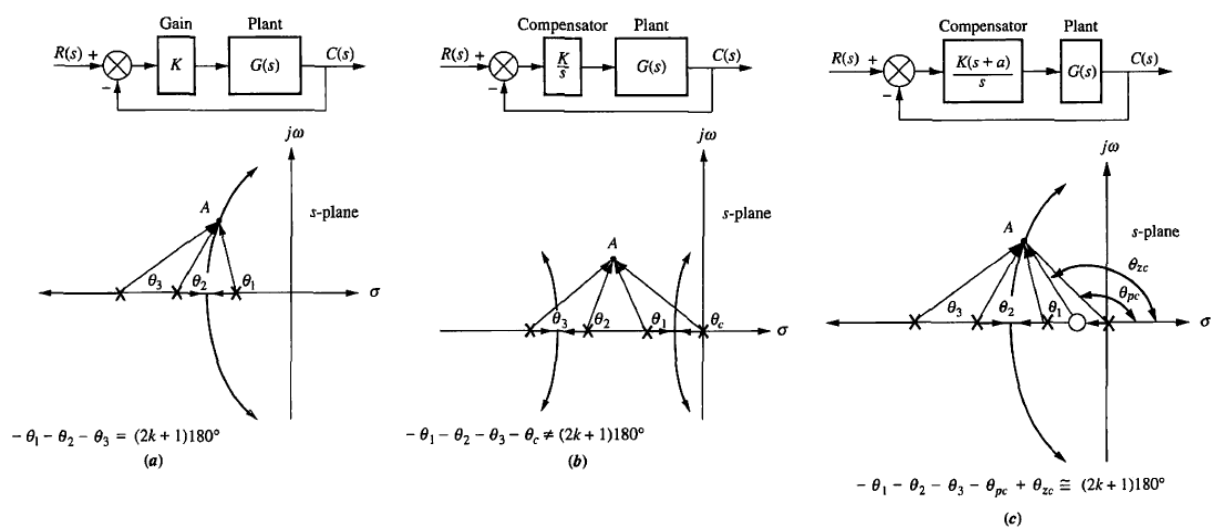
**Figure 3: Generic Unity Feedback Control System**

In controller design there are multiple solutions, some better than others. It is possible to have multiple designs that satisfy the given performance constraints, but practical implementation issues and cost could be prohibitive for some designs. As a general rule, it is good idea to keep controller as simple as possible while meeting the prescribed performance criteria. Some common controller structures that will be used in this lab is listed in the Table along with the respective transfer function.

Compensator	Transfer function	Functions
PI	$K \frac{S+Z_c}{S}$	Improve steady state error
Lag	$K \frac{S+Z_c}{S+P_c}$	Improve steady state error
PD	$K(S + Z_c)$	Improve transient response
Lead	$K \frac{S+Z_c}{S+P_c}$	Improve transient response
PID	$K \frac{(S + Z_{lag})(S + Z_{lead})}{S}$	Improve steady state error and transient response
Lag-lead	$K \frac{(S + Z_{lag})(S + Z_{lead})}{(S + P_{lag})(S + P_{lead})}$	Improve steady state error and transient response

### PI Compensator:

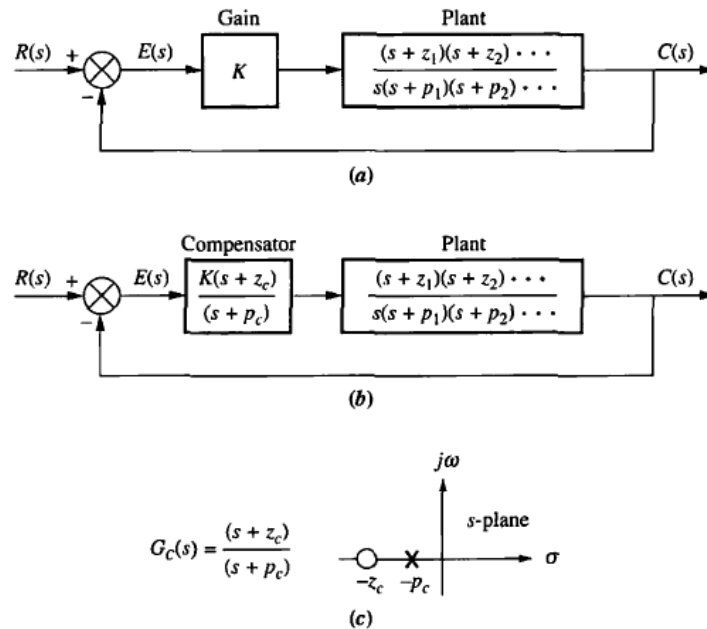
Steady-state error can be improved by placing an open-loop pole at the origin. For example, a Type 0 system responding to a step input responds with zero error if the system type is increased to one. However, the angular contribution of the open-loop poles will no longer be  $180^\circ$  as illustrated in Figure 4(b). To solve this, a zero is added close to the pole at the origin, for example at  $s = -0.1$  (Figure 4c).



**Figure 4: Demonstrating how PI compensator increases system type to reduce steady state error without affecting transient response**

## Lag Compensator:

PI compensation requires active integrator and demands the use of external power supply. In lag compensation, passive networks are used which moves the pole and zero to the left, but close to the origin as shown in Figure 5(c). Although it does not increase the system type, but yields an improvement in the static error constant over an uncompensated system.



**Figure 5: (a) Type I uncompensated system. (b) Type I lag-compensated system. (c) compensator pole-zero plot**

## PD Compensator:

As previously described in Figure 1, if the transient performance requirement of a system is not achieved by simple gain adjustment, then we need to reshape the root locus so that the compensated (new) root locus goes through the selected closed-loop pole location. This task is accomplished by the PD controller, where a single zero is placed 'judiciously' on the forward path to force the root locus go through the desired pole location.

## Lead Compensator:

Lead compensation employs passive elements, hence a single zero cannot be produced; rather a compensator zero and pole results. However, if the pole is farther from the imaginary axis than the zero, the angular contribution of the compensator is still positive and thus approximates an equivalent single zero.

For design, we arbitrarily select either a lead compensator pole or zero and find the angular contribution at the design point of this pole or zero along with the system's open-loop poles and zeros. The difference between this angle and  $180^\circ$  is the required contribution of the remaining compensator pole or zero. This is illustrated in Figure 6, where if we place the compensator zero  $z_c$  first, then the location of the compensator pole  $p_c$  is calculated using trigonometry.

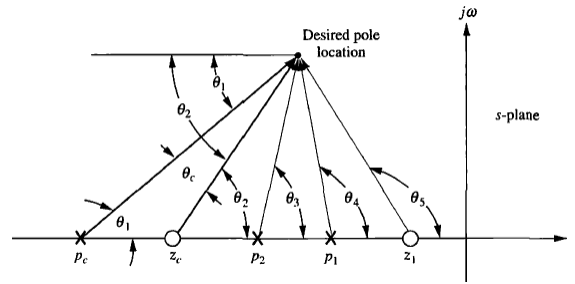


Figure 6: Geometry of lead compensation

### PID compensator:

This type of compensation employs using both PI and PD compensation schemes. Basically, transient response is first improved by designing a PD controller which involves placing a zero  $z_c$  such that the root locus meets the transient response specification. Then the PI controller is designed by simply placing a pole at the origin and a zero close to the pole at the origin.

### Lag-lead compensator:

In lag-lead compensation both the transient response and the steady-state error is improved. We first design the lead compensator to improve the transient response. Next we evaluate the improvement in steady-state error still required. Finally, we design the lag compensator to meet the steady-state error requirement.

Suppose we want to design a lag-lead compensator for the system in Figure 7 so that the system will operate with 20% overshoot and a twofold reduction in settling time. Further, the compensated system will exhibit a tenfold reduction in steady-state error for a ramp input.

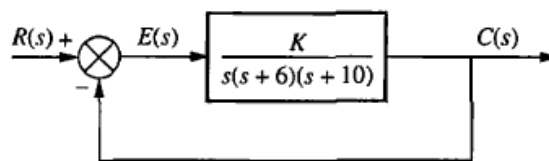


Figure 7

First we plot the root locus of the uncompensated system and use *rlocfind()* to identify the closed-loop pole for an overshoot of 20% ( $\zeta = 0.456$ ) as shown in Figure 8.

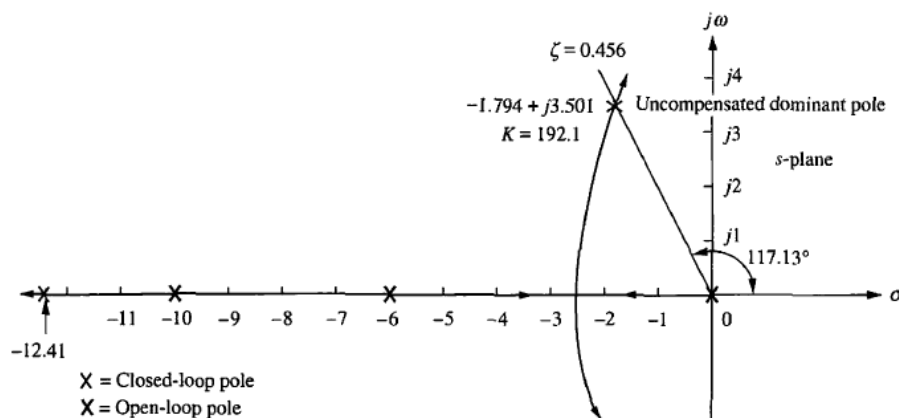


Figure 8: Root locus for uncompensated system

We find the dominant poles at  $-1.794 \pm j3.501$  with a gain of 192.1. Next we begin the lead compensator design by selecting the location of the compensated system's dominant poles. In

order to realize a twofold reduction in settling time, the real part of the dominant pole must be increased by a factor of 2, since the settling time is inversely proportional to the real part. Thus,

$$-\zeta\omega_n = -2(1.794) = -3.588$$

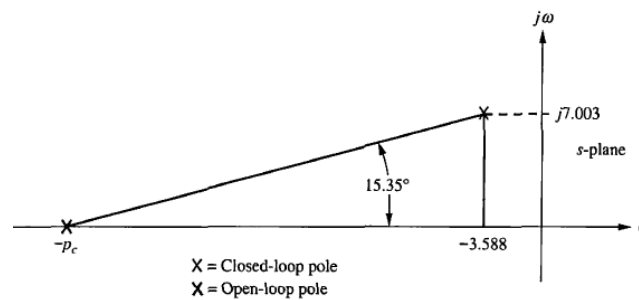
The imaginary part of the closed-loop pole should also be doubled in order to keep overshoot constant.

$$\omega_d = 2(3.501) = 7.003$$

Next we select a location for the lead compensator zero  $z_c$  arbitrarily. For this example, we select the location of the compensator zero coincident with the open-loop pole at -6. This choice will eliminate a zero and leave the lead-compensated system with three poles, the same number that the uncompensated system has. The sum the angles to the design point from the uncompensated system's poles and zeros and the compensator zero is found to be  $-164.65^\circ$ .

$$\theta_c - \theta_1 - \theta_2 - \theta_3 = 70.99 - 70.99 - 47.52 - 117.13 = -164.65^\circ$$

The difference between  $-180^\circ$  and this quantity is the angular contribution required from the compensator pole i.e  $15.35^\circ$ . Using trigonometry, the location of the compensator pole is found to be -29.1 as shown in Figure 9.



**Figure 9: Evaluating the compensator pole**

$$\frac{7.003}{p_c - 3.588} = \tan(15.35)$$

$$p_c = 29.1$$

This concludes the lead compensator design. The lead compensated system root locus is drawn which gives a gain of 1977 for an overshoot of 20%.

$$G_{LC}(s) = \frac{1977}{s(s + 10)(s + 29.1)}$$

To begin lag compensator design, we must first compute the improvement in static error due to Lead compensator. The uncompensated system's open-loop transfer function is

$$G(s) = \frac{192.1}{s(s + 6)(s + 10)}$$

For the uncompensated system static error constant  $K_v$ , which is inversely proportional to steady-state error, is 3.201 for ramp input. The static error  $K_v$  for the lead-compensated system is 6.794. Thus, the addition of lead compensation has improved the steady-state error by a factor of 2.122. For a tenfold improvement, the lag compensator must be designed to improve the steady-state error by a factor of 4.713 ( $10/2.122 = 4.713$ ) over the lead-compensated system.

$$\frac{z_c}{p_c} = 4.713$$

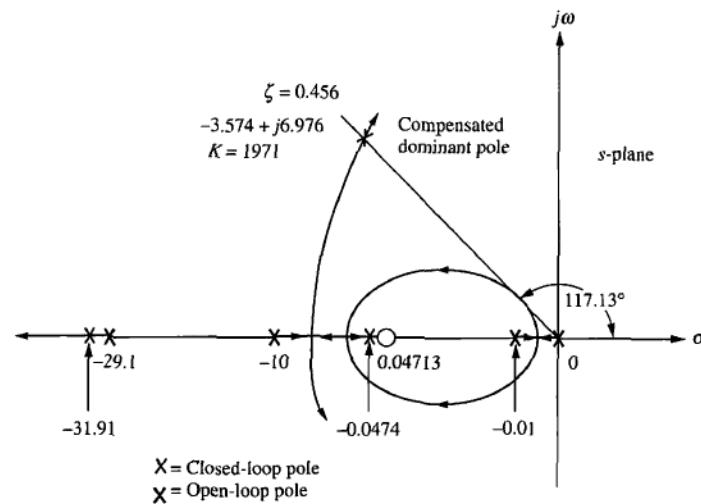
We arbitrarily choose the lag compensator pole at -0.01, which then places the lag compensator zero at -0.04713, yielding

$$G_{lag}(s) = \frac{s + 0.04713}{s + 0.01}$$

as the lag compensator. The lag-lead-compensated system's open-loop transfer function is

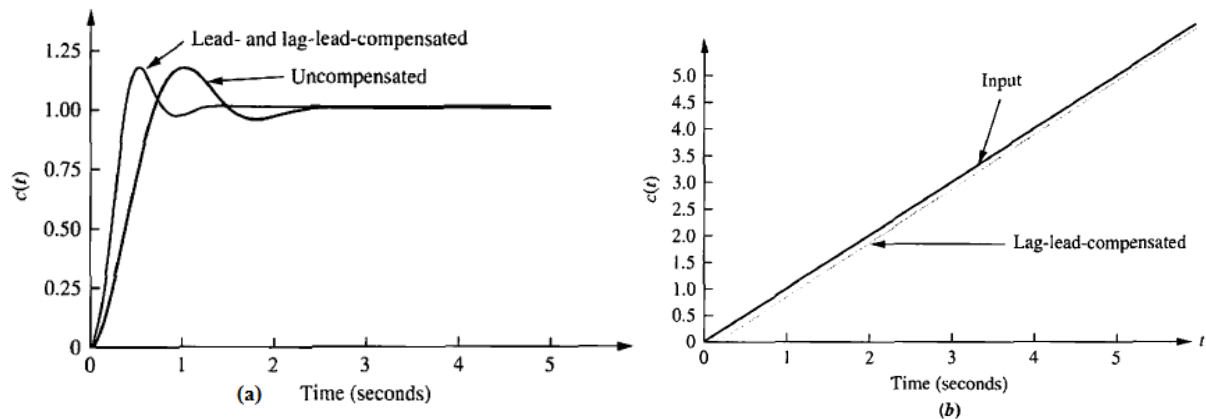
$$G_{LLC}(s) = \frac{K(s + 0.04713)}{s(s + 10)(s + 29.1)(s + 0.01)}$$

The root locus for the lag-lead compensated system is shown in Figure 10.



**Figure 10: Root locus for the lag-lead compensated system**

The step response and ramp response of the lag-lead compensated system is shown in Figure 11, which reflects the improvement in both steady state and transient response.



**Figure 11: Improvement in step response and ramp response error for the lag-lead compensated system**

For further detail, you can go through the sections 9.1-9.4 of “CONTROL SYSTEMS ENGINEERING” by Norman S. Nise.

## PRELAB:

1. Read the theory discussed in the previous section.
2. How many lead compensator designs will meet the transient response specifications of a system?
3. What differences do the lead compensators of Prelab2 make?
4. Design a lead compensator for a unity negative feedback system with a forward transfer function of  $G(s) = \frac{K}{s(s+3)(s+6)}$  to meet the following specifications: percent overshoot = 20%; settling time = 2 seconds. Specify the required gain,  $K$ . Estimate the validity of the second-order approximation.
5. What is the total angular contribution of the lead compensator of Prelab 4?
6. Determine the pole and zero of two more lead compensators that will meet the requirements of Prelab 4.
7. What is the expected steady-state error for a step input for each of the lead compensated systems?
8. What is the expected steady-state error for a ramp input for each of the lead compensated systems?
9. Select one of the lead compensator designs and specify a PI controller that can be cascaded with the lead compensator that will produce a system with zero steady state error for both step and ramp inputs.

## LAB WORK:

1. Using MATLAB, draw the step response for the system shown in Figure 12 for a particular gain that operates with a damping ratio of  $\zeta = 0.174$ . Note down the steady-state error and the gain  $K$  of your selected point. Now use PI compensator to reduce steady-state error to zero and draw the step response of the overall configuration. [Hint: Use *rlocfind()* to find gain corresponding to  $\zeta = 0.174$ ]

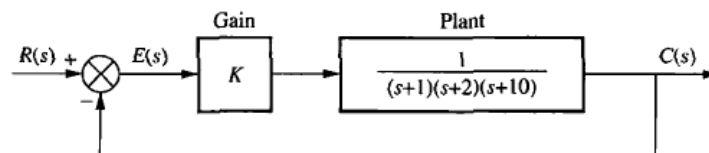
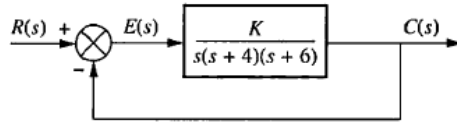


Figure 12

2. Use lag compensation to reduce the steady state error of the system in Figure 12 by a factor of 10 if the system is operating with a damping ratio of 0.174. Place the compensator pole  $p_c$  at -0.01 and compensator zero  $z_c$  accordingly. Plot the step response of both the compensated and uncompensated system in the same window.
3. For the system in Figure 13, draw the step response of the uncompensated system with 16% overshoot. Design a PD compensator with a three-fold reduction in settling time, keeping overshoot constant. Plot the step response of both the compensated and uncompensated system in the same window.





**Figure 13**

4. Design a lead compensator for the system in Figure 13 that will reduce the settling time by a factor of 2 while maintaining 30% overshoot. Plot the step response of both the compensated and uncompensated system in the same window.
5. Using MATLAB, create the design in Prelab 4 and plot the root locus, step response, and ramp response. Take data to determine the percent overshoot, settling time, and step and ramp steady-state errors. Record the gain,  $K$ .
6. Repeat Lab 5 for each of the designs in Prelab 6.
7. For the design selected in Prelab 9, insert the PI controller. Plot the step response and measure the percent overshoot, settling time, and steady-state error. Also, plot the ramp response for the design and measure the steady-state error.
8. Plot the step and ramp responses for two more values of the PI controller zero.

### **REPORT:**

1. Make a table showing calculated and actual values for percent overshoot, settling time, gain,  $K$ , steady-state error for step inputs, and steady-state error for ramp inputs. Use the three systems without the PI controller and the single system with the PI controller from Lab 3.
2. Itemize the benefits of each system without the PI controller.
3. Choose a final design and discuss the reasons for your choice.

### **Prepared By:**

I.K.M. Reaz Rahman, Ajanta Saha

### **Supervised By:**

Dr. Pran Kanai Saha

Professor, Department of Electrical and Electronic Engineering  
Bangladesh University of Engineering and Technology

Dr. Mohammad Ariful Haque

Professor, Department of Electrical and Electronic Engineering  
Bangladesh University of Engineering and Technology

Dr. Md. Zahurul Islam

Associate professor, Department of Electrical and Electronic Engineering  
Bangladesh University of Engineering and Technology