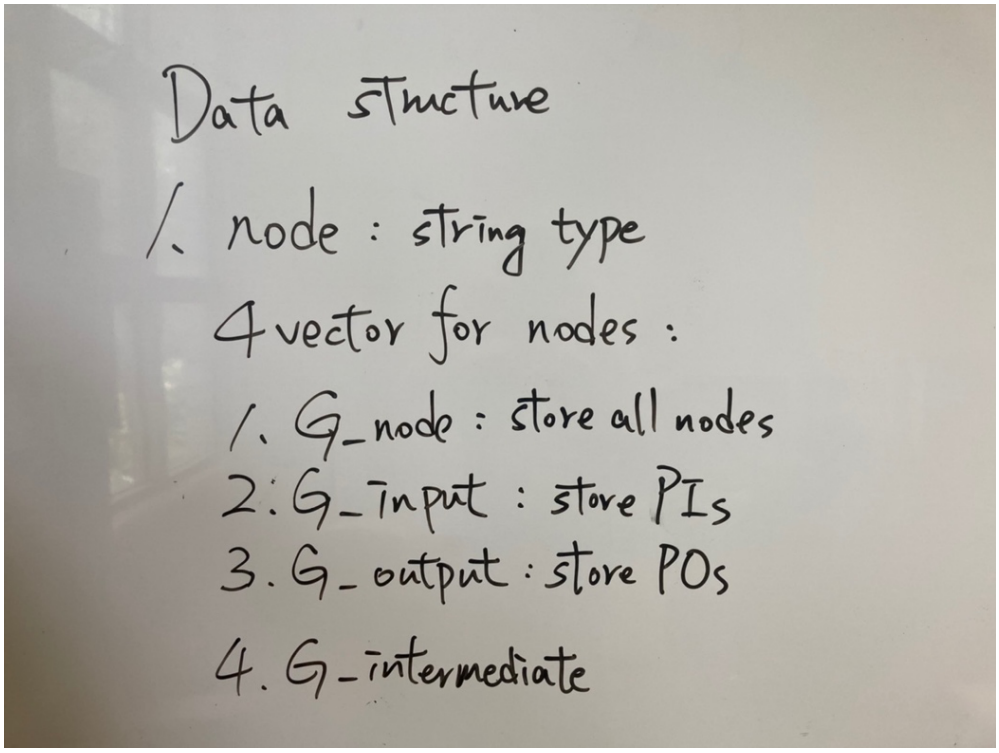
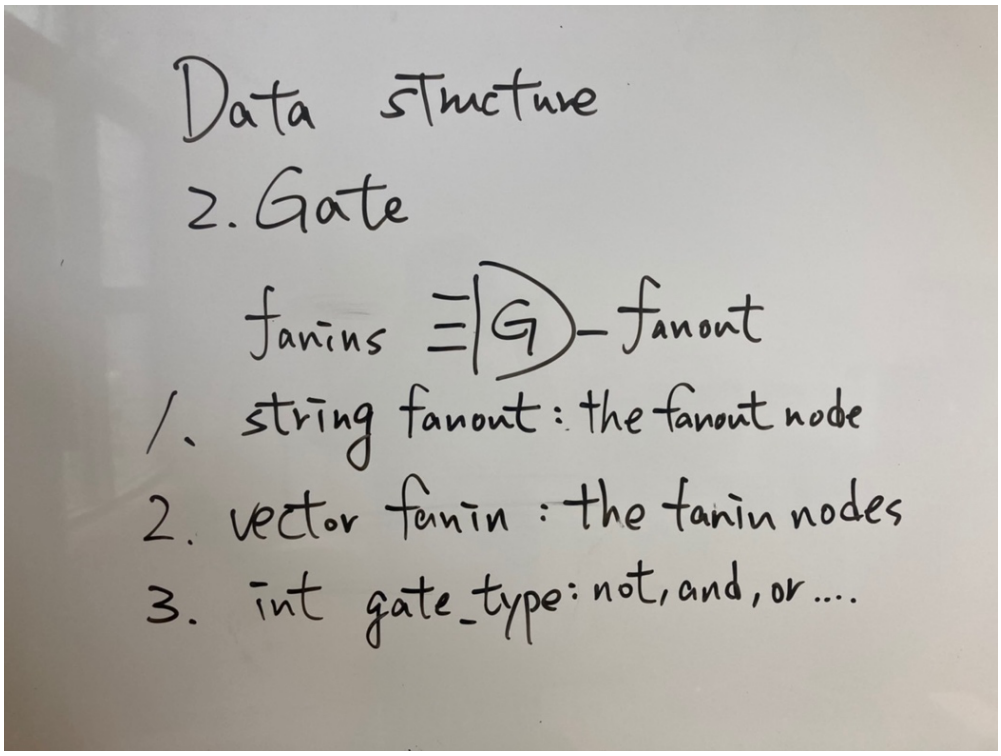
Final Project Report

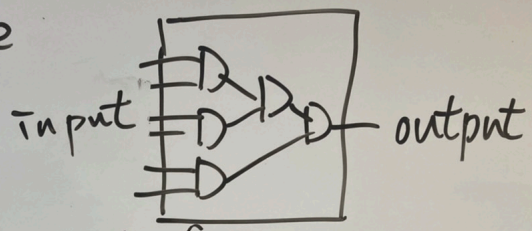
1. Data structure





Data structure

3. LUT

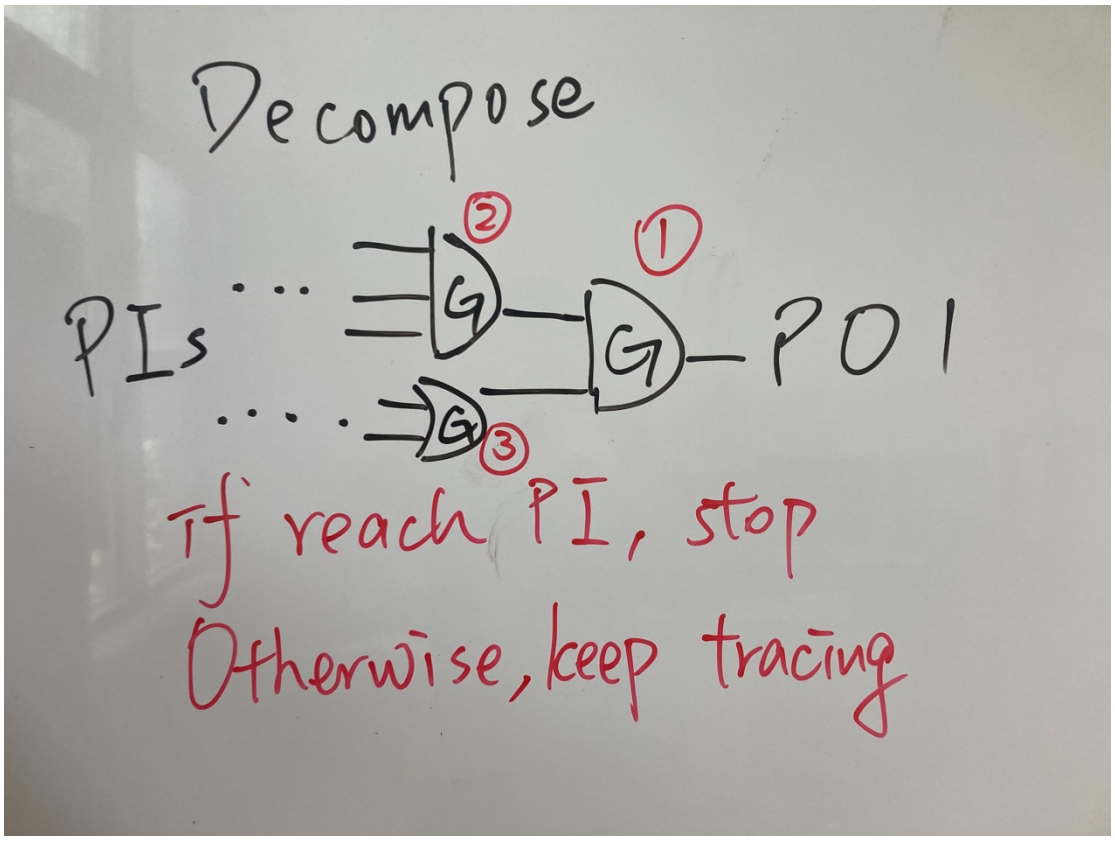


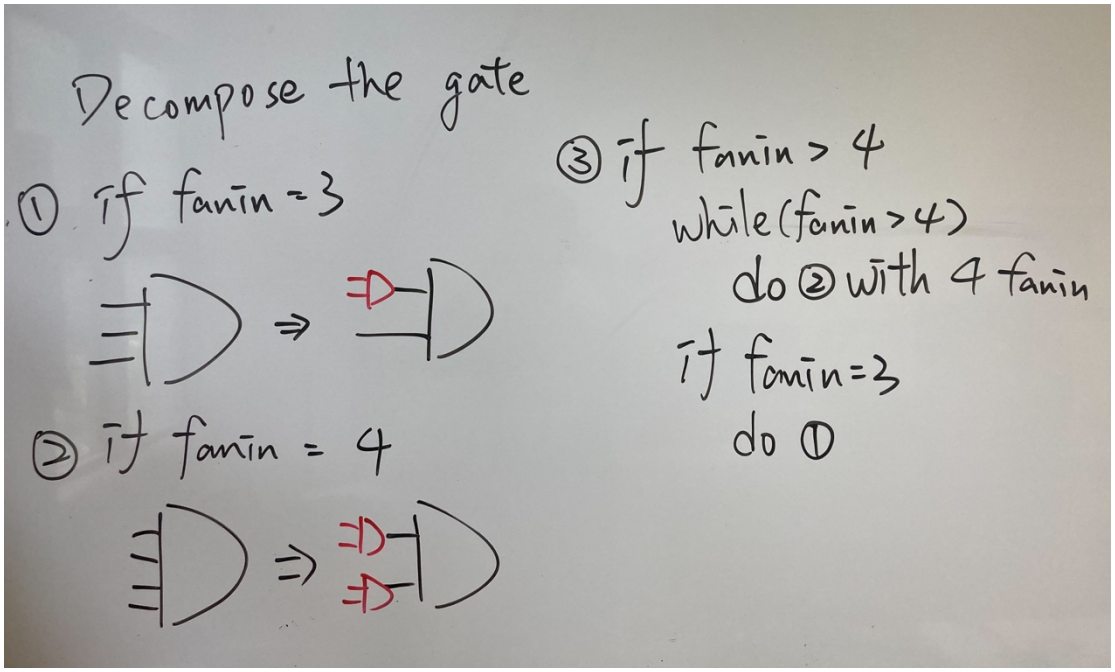
String output : the output of LUT

vector input : the input set of LUT

vector gate : the gates inside the LUT

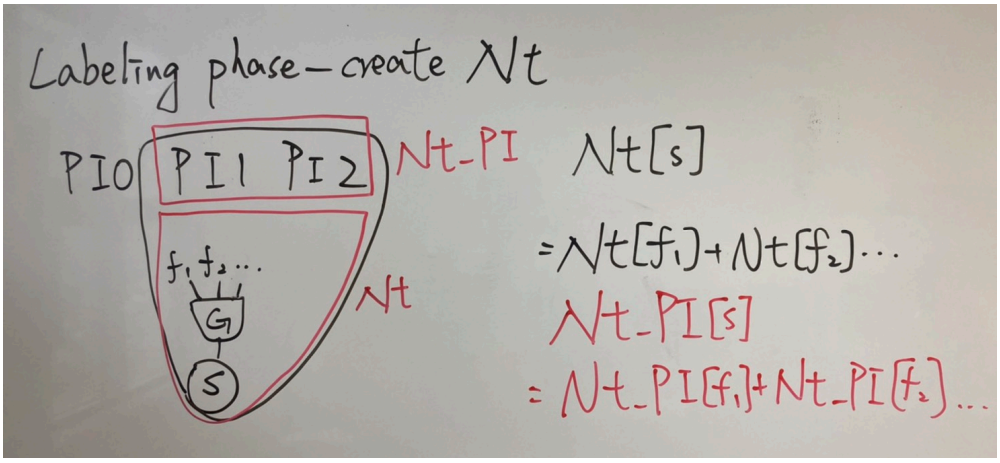
2. Decompose

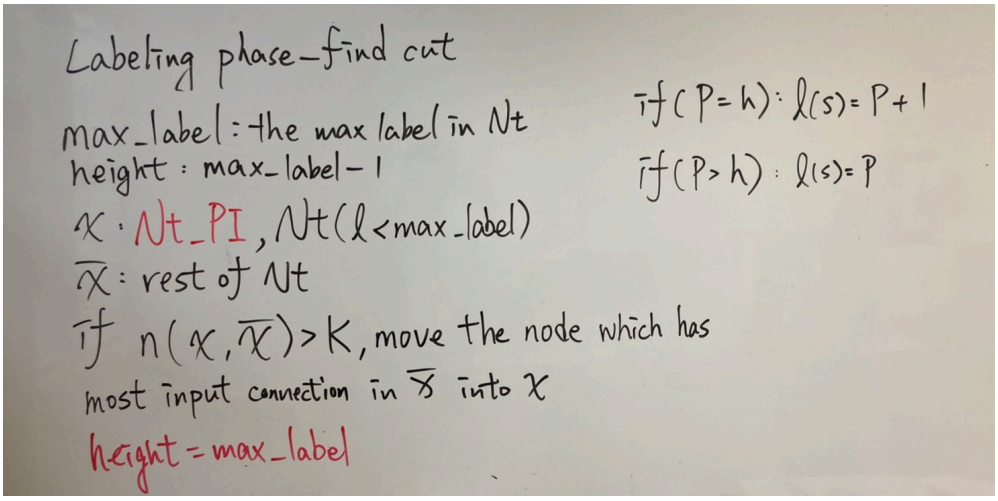

Decompose
PIs
PO1
if reach PI, stop
Otherwise, keep tracing


Decompose the gate
① if fanin = 3
② if fanin = 4
③ if fanin > 4
while (fanin > 4)
do ② with 4 fanin
if fanin = 3
do ①

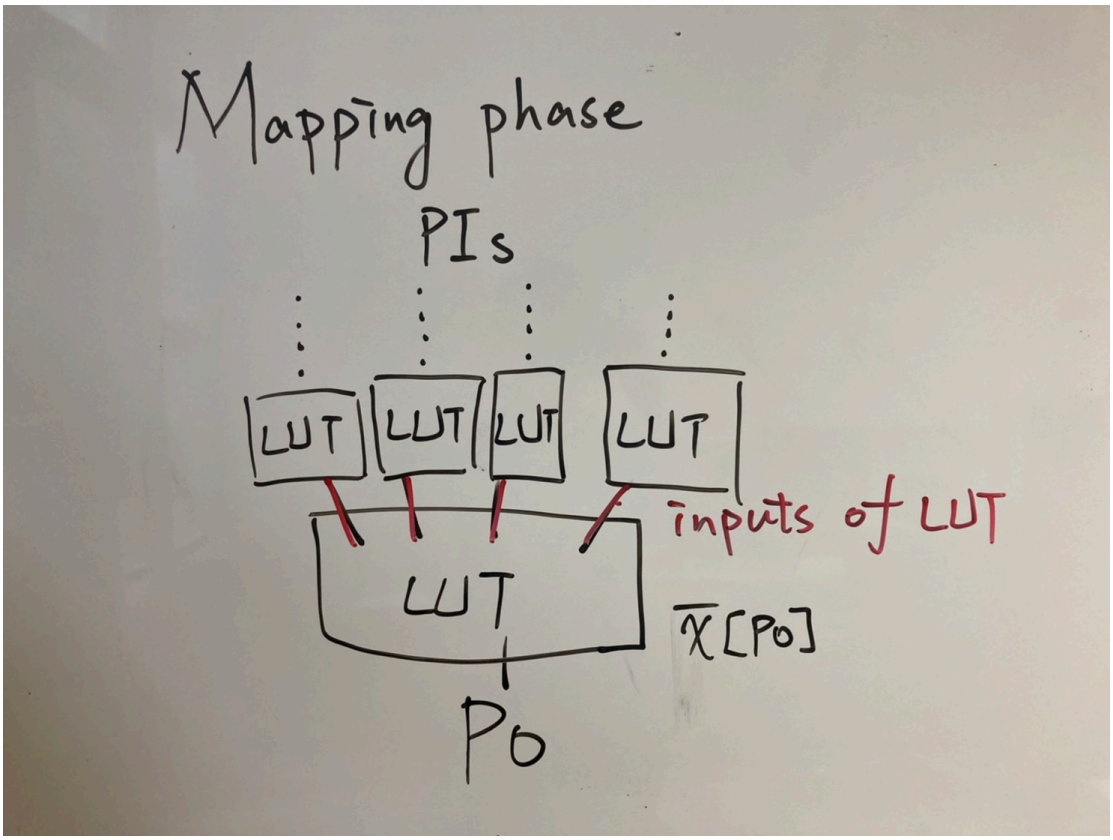
3. Technology mapping

- Labeling

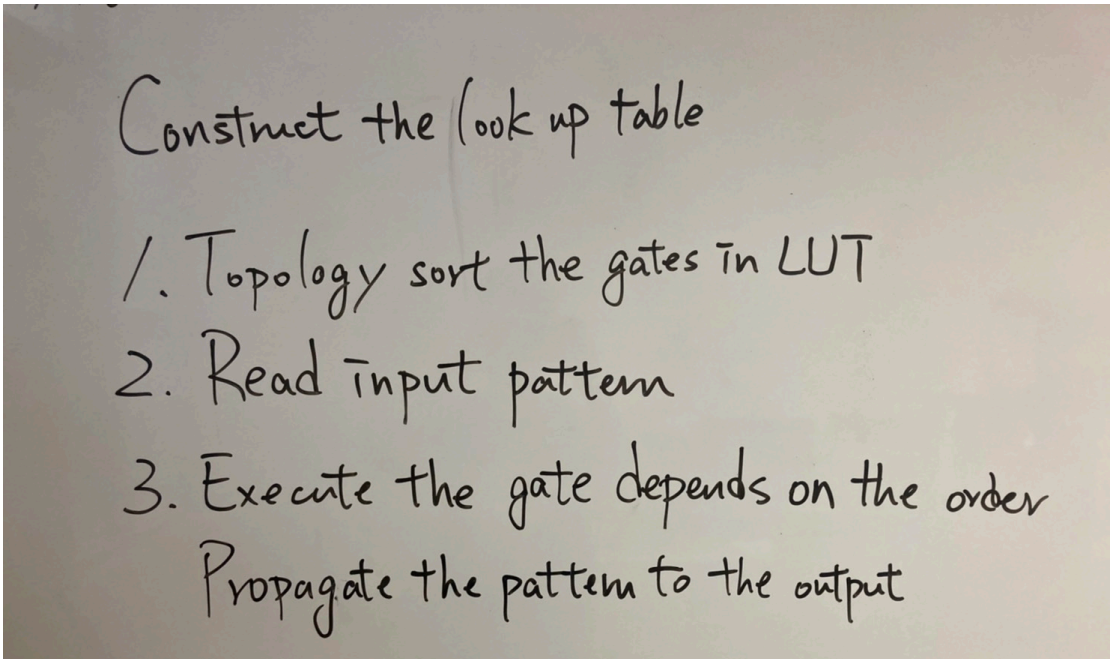




- Mapping



- Construct LUT



4. Experience result

	alu4	big2	C1355	C6288	des	k2
Decompose time	0.03	1.5	0.01	0.32	1.17	0.18
K = 4 Mapping time	3.41	34.01	2.84	40.96	29.73	3.92
K = 6 Mapping time	5.21	45.59	6.66	79.49	43.43	4.83
K = 8 Mapping time	7.61	63.01	9.07	92.07	78.93	9.93
K = 4 node/level with min_label	767/15	5437/16	220/7	2017/39	4265/9	1797/10
K =6 node/level with min_label	616/10	5109/10	197/5	1302/21	3630/6	1426/7
K = 8 node/level with min_label	413/8	3668/8	147/4	1060/17	2713/5	939/5
K = 4 node/level with max_label	784/15	5354/16	229/7	2035/39	4241/9	1496/10
K =6 node/level with max_label	621/10	5098/10	207/5	1300/21	3630/6	1250/7
K = 8 node/level with max_label	413/8	3658/8	160/4	1155/17	2696/5	892/5