國立清華大學 電機工程學系

110 學年度第一學期

EE-6250 超大型積體電路測試 VLSI Testing

Homework #1 (佔學期總成績 10 分)

Due on Nov. 7, 2021

Late Homeworks will NOT be accepted !

Submit to https://eeclass.nthu.edu.tw/ 作業區

1. (100%) Consider the testing of a complex CMOS logic cell.
   (a) (20%) Draw the transistor schematic for a logic cell with the following functionality:
   Y = (A + CD + EFG)'
   (b) (20%) **Write a C or C++ program to generate the truth table of this logic cell**. Your program should print out the response of each of the 2^6 = 64 input combinations. Also, report the **cardinalities of the ON-SET and the OFF-SET**, respectively.
   (c) (20%) A transistor could have unexpected **short fault** (meaning that the source and drain are connected at all times independent of the value of its gate). Consider one such type of logic cell with E-controlled nMOS having a short fault. **Modify your program to show the truth table for this faulty cell**. (Note that the output signal may not be perfectly logical under some input combinations due to the fighting of paths to VDD and ground. Use logic symbol 'X' to represent an ambiguous output value. The input combinations that cause an 'X' at the output can be considered as potential test vector for the short fault).
   (d) (20%) A transistor could have unexpected **open fault** as well (meaning that the source and drain are disconnected at all times independent of the value of its gate). Consider one such type of logic cell with E-controlled pMOS having an open fault. **Modify your program to show the truth table for this faulty cell**. (Note that the output signal could be floating under some input combinations. Use logic symbol 'Z' to represent it when it occurs.)
   (e) (20%) An open fault is more deterministically testable than the short fault but requires two-pattern tests. Modify your program to **list all 2-pattern tests** for the faulty cell described in part (d). Report the **total number of tests** you derived.

Note: 繳交資料: Combine all of the following items into a single PDF file for the submission to the iLMS system. On top of the combined PDF file there should be a cover page with your 系所，中英文姓名，學號等資訊.

- In addition to the answers to the above questions, you should include all the source codes of your C or C++ programs for sub-problems (b) to (d) as appendices.