國立清華大學 電機工程學系

110 學年度第一學期

EE-6250 超大型積體電路測試 VLSI Testing

Homework #3 (佔學期總成績 10 分)

Due on Jan. 6 (Thursday), 2022

Late Homeworks will NOT be accepted !

Submit to https://eeclass.nthu.edu.tw/ 作業區

1. (10%) Derive the logic circuit of a 16-bit adder. (You can use Design Compiler if you know how to use it). Report the netlist of your adder.
2. (40%) **Insert BIST circuit into your adder**, by using a 7-stage **Linear Feedback Shift-Register (LFSR)**, as the automatic pattern generator of 127 pseudo random patterns, and a **Multi-Input Shift-Register (MISR)** as the signature analyzer. Report the netlist of your BISTed circuit, and its golden signature when the circuit is fault free.
3. (10%) Set up the simulation environment to verify if your adder can operate at the speed of 1GHz? Report the execution trace.
4. (40%) Find a procedure to approximate the **maximum operating speed** of your BISTed adder design. During the procedure, use 100ps as the time resolution when you tune the clock cycle time for the simulation. Report your execution trace and the final conclusion. (Note: The procedure could be either manual or automated by a script. You are advised to write a brief paragraph describing how you solve this problem).

Note: 繳交資料: (1) Combine the results of the above sub-problems into a single PDF file. (2) Attach a cover page with your 系所，中英文姓名，學號等資訊 before submitting your PDF file to our **https://eeclass.nthu.edu.tw/ 作業區**.