Computer Organization, Spring 2022

LAB 4 : Single-Cycle CPU

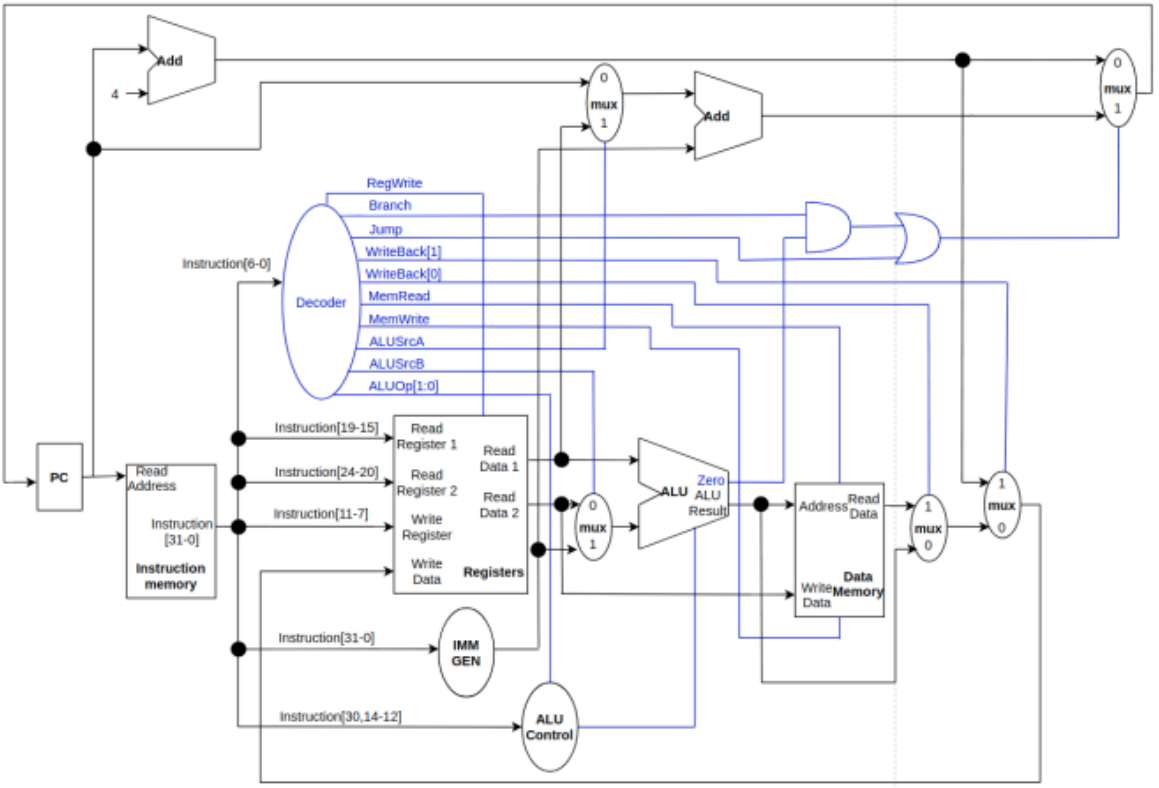
Due : 2022/5/11 23:59

1. Goal

- To realize how to set the control signal in different instruction type.(Decoder & ALU Controller)
- To clarify how sign-extend work.
- Connect all datapath to form a single cycle CPU

2. HW Requirement

-

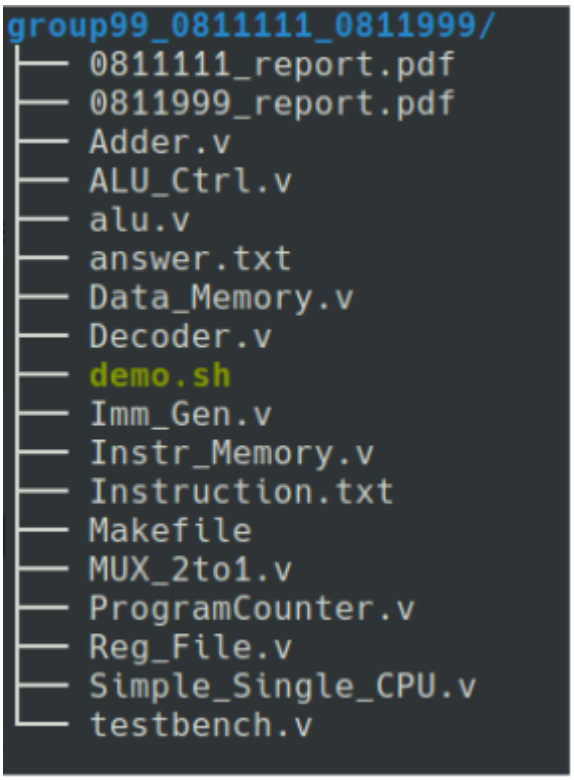


- **Implement bellow instruction for testing data(80%)**
    - **add**
    - **slt**
    - **addi**
    - **lw**
    - **sw**
    - **jal**
    - **jalr**
    - **You world not get any score for this part if you program can’t pass the test by script.**
- **Report(20%)**

3. Hand in

- $(groupN)_$(studentid1)_$(studentid2).zip
    - $(groupN)_$(studentid1)_$(studentid2)
        - $(studientid1)_report.pdf
        - $(studientid2)_report.pdf

- {*.v}



- Your report should be in PDF format.

4. Grade

Single Cycle CPU (80%)
Report (20%)

- Detailed description of the implementation
- Implementation results
- Problems encountered and solutions

❖ Late submission: 10% penalty per day
❖ No plagiarism, or you will get 0 points

5. Q&A

- Feel free to ask on HackMD if you need.
  - Lab4 討論區

- We will not debug for you

6. Reference

- RISC V(https://riscv.org/technical/specifications/)