Application Note # 2438

Galil SSI Encoder Interface

This application note will discuss the special SSI firmware created by Galil for interfacing to SSI encoders. Galil has created two distinct versions of the SSI firmware, and this note will cover the version created after the second quarter of 2006. For literature on the prior version of SSI firmware please consult the factory.

The following topics will be covered in this application note:

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General SSI Information

Synchronous Serial Interface (SSI) allows for serial transmission of absolute position data (either binary or Gray code) from the encoder based on a timed clock pulse train from the controller. Connection between the controller and encoder is based on two signal lines, clock and data, which are usually differential for increased noise immunity. For each sequential clock pulse of the controller, the encoder transmits one data bit from shift registers on the encoder. Figure 1 shows a typical SSI timing diagram, which shows the sequential clock pulse train from the controller and the corresponding data bits.

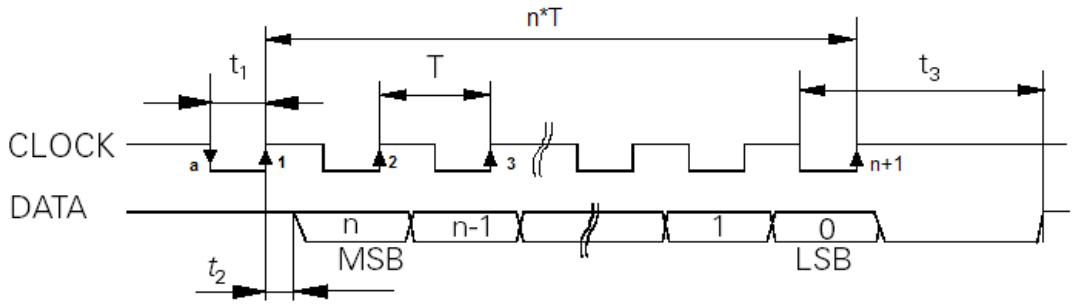

Figure 1 – Typical SSI Timing Diagram

n = total # of data bits
T = clock period (sec)
1/T = clock frequency ~500kHz to ~2.5 MHz (set by sign of p argument of SI command*)
t_1 = minimum time required for encoder to freeze data and prepare shift registers before receiving the first rising edge to prompt the MSB
t_2 = data transmission delay (increases with cable length)
t_3 = required delay to refresh position data between subsequent position reads.

The transfer of data from the encoder to the controller is initiated when the first "falling" edge (a) of the clock pulse train prompts the encoder to freeze the current absolute position data into the encoder shift registers and prepare for the coming clock pulse train from the controller. Typical SSI encoders trigger on the rising edges (as shown in Figure 1) where the first rising edge on the clock (1) prompts the encoder to set the first data bit (MSB) on the data line. The controller then latches and stores the data bit at the next "rising" edge (2) while also sending the next request for the subsequent bit. The process continues until all data bits (down to the LSB) have been clocked and stored on the Galil, after which, the clock signal remains high until the next position read cycle occurs. This cycle occurs every sample period of the controller (i.e. 1 kHz at TM1000).
The Galil controller is configurable for a specific SSI encoder using the following **SI** command. Extended I/O and custom hardware/firmware modification are both necessary for any Galil controller to interface with SSI encoder data (contact Galil for an NRE quote).

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Galil Controller Hardware Options with SSI

There are two items required when connecting an SSI encoder to the Galil controller; special SSI firmware and an extended I/O option. The custom firmware is discussed in later sections. For the extended I/O, there are a few interface options to gain access to the SSI Signals. The specific options depend on the model of the controller:

- **DMC-40x0/41x3**. The SSI inputs go through the auxiliary encoder inputs found on the Encoder D-subs. There is one D-sub for each axis. Note that the standard 4xxx must be ordered with the –SSI option to have SSI I/O points at the Aux encoder locations. If using Dual Loop, "See Considerations for DMC-4000 with SSI and DV" at the end of this document.

- **DMC-17x0 /18x0/18x2 /34x5 /14x5/12x0**. Using the DB-14064-SSI the signals are accessed via two 50-pin IDC headers (at J6 & J8).

- **DMC-21x2/x3/ 18x6**. Using the DB-28040-SSI signals are accessed via two 20-pin IDC headers (at J4 & J5).

- **DMC-2x00-SSI**. The signals are accessed via the 80-pin SCSI type extended I/O connector. The standard extended I/O must be modified at the factory to support SSI I/O points. Using the CABLE-80-1m cable to a CB-50-80 converter will allow signal access using two 50-pin IDC headers labeled J6 & J8.
  -The Phoenix Contact MD/80 module offers screw terminals, which directly connects to the CABLE-80. Note: this option can also be used with the CB-50-80 installed on the DB-14064-SSI.

For specific pin outs please see Table 1 located below.

Galil SSI firmware limitations

There are two limitations placed on the controller when using SSI; I/O limitations and serial communication limitations.

I/O Limitations

These limitations only depend on hardware and are not affected by firmware version

- DB-28040-SSI Revision D: Only 32 I/O points are available and at least one bank of eight must be inputs
- DB-28040-SSI Revision E: With 1-4 axis all 40 I/O are available. With 5-8 axis only 32 I/O are available

Serial Communication Limitations

Affected controllers:21x2/3,22x0,20x0 with SSI firmware. The maximum baud rate that can be used to communicate to the controller is limited with certain configurations of SSI. This is a result of the data transmission time based on number of axes sampled and the chosen SSI clock frequency. The tables below show first a common SSI configuration and then an extreme configuration. This limitation is seen in all revisions of the DB-28040 ***Note**: These restrictions will only affect serial communication. If you intend to communicate over Ethernet then there are no limitations. Please consult Galil with any questions.

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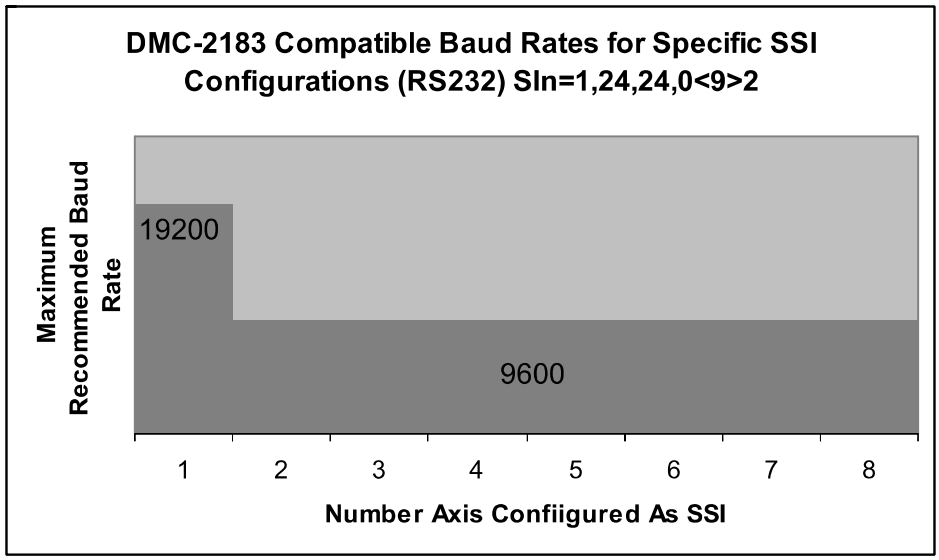

Figure 2 - A common configuration which uses 24 bits and 1Mhz clock frequency

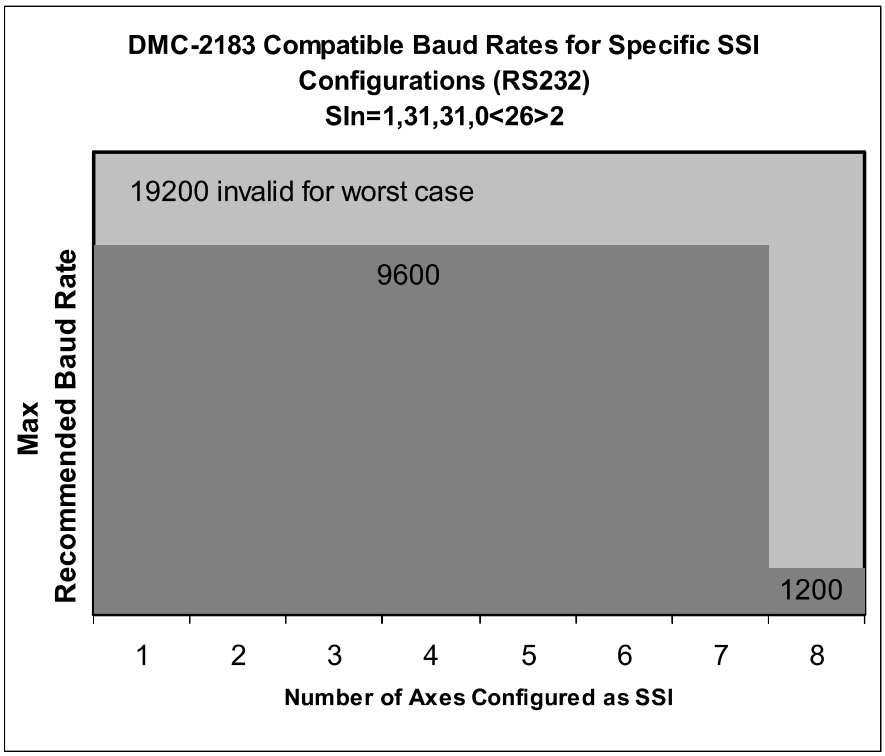

Figure 3 -The worst case scenario with 31 bits and 370kHz clock frequency

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SSI Command Specifications
Command Reference

ARGUMENTS: **SIn = si0, si1, si2, si3 <p >q** where

n = The axis designator (XYZW or ABCDEFGH). Each axis must be set individually

si0 = **0** is for NO SSI
1 is for SSI to replace MAIN encoder data
2 is for SSI to replace AUX encoder data

si1 = Total # of Bits of SSI. A positive number designates No Rollover. A negative number will cause the controller to act as an incremental encoder, allowing the encoder to count past the max value of the encoder. (Note: when the controller is powered down, the rollover values are lost)

si2 = # of Single Turn Bits

si3 = # of Status Bits (ie: Error Bits)
Positive # designates status bits as trailing the SSI data
Negative # designates status bits as leading the SSI data

The number of Multi-turn bits of the encoder is internally calculated by the following equation:
Multi-turn Bits = (Total Bits) - (Single-Turn) - (Status Bits)

P is an integer in the range of 4-26.

P Designator for SSI Firmware
-A positive value of p reads data on the rising clock edge; a negative value reads data on the falling clock edge for all versions

$$\textbf{SSI Freq} = \frac{ClockSpeed}{2 \cdot (p+1)}$$

Clock Speed: 20 Mhz*
-DMC 40x0
-DMC 21x3/18x6+DB-28040 (RevE)

P	SSI Frequency(kHz)
4	2000
8	1111
10	909
12	769
13	714
24	400
26	370

Clock Speed: 25 Mhz
-DMC 18x0 + DB-14064
-DMC 14x5/34x5 + DB-14064
-DMC 17x0 + DB-14064
-DMC 21x3 + DB-28040(RevA-D)
-DMC 2xx0
-DMC 16x0
-DMC 12x0 + DB-12064

P	SSI Frequency(kHz)
4	2500
8	1389
10	1136
12	962
13	892
24	500
26	463

*Actual 20Mhz frequency ranges from 18Mhz to 26Mhz.
Contact Galil if tolerances must be tighter for a particular application (this is rare).

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q = **1** for Binary Code
2 for Gray Code

SIn=? Returns the configuration parameters (where n is the axis)

Examples for DB-14064
BEI (H25D-SS-12GC) 12-bit Single Turn Gray Code Encoder on X axis Main
SIX=1,12,12,0<-11>2
Codechamp S.A. (COA 11018A) 23-bit Single Turn Binary with 2 Error Bits on X axis Main
SIX=1,25,23,2<10>1
Heidenhain (ROQ 425) 25-bit (13-bit Single, 12-bit Multi) Binary on X axis Main
SIX=1,25,13,0<-11>1
Kubler by Turck (T8.5862) Gray Code 25-bit (13-bit Single, 12-bit Multi) on D Axis Main
SID=1,25,13,0<-11>2
SICK SSI Laser Measuring Device 24-bit Binary on Y axis Auxiliary
SIY=2,24,24,0<-11>1
Stegmann (AG626) 24-bit Binary Multi-turn Encoder on X axis Main
SIX=1,24,12,0<-11>1
Stegmann (CA6S -CoreTech) 13-bit Single-turn Gray Code Encoder on X axis Main
SIX=1,13,13,0<-11>2
Temposonics (RH) 24-bit Binary Linear Encoder on X axis Main
SIX=1,24,24,0<-10>1
Stegmann/SICK (ATM60-A4AO-K17) 12 bit Single, 12bit Multi, Accelera with DB-28040
SIX=1,24,12,0<13>1 (Binary with a clock frequency of 964kHz)

SSI Pinouts

The following pinouts are used to connect an SSI encoder to the corresponding Galil hardware. Each encoder requires 4 signal wires: Data+, Data-, Clock+, and Clock-. Pinout locations in Table-1 are noted as <connector> - <pinout>. The pin number assignment of the IDC header alternates, with the odd numbers along one side of the two row header and the even along the other. Pin #1 is noted with either an arrow on the IDC housing or a "1" on the board silkscreen. The SSI pinouts in Table-1 do not apply to the DMC-2100 (obsolete); contact Galil for a correct pinout.

2X 50 pin IDC	2X 20 pin IDC	Phoenix MD80	15 pin D-sub	80 pin SCSI
DMC-2xx0+CB-50-80 DMC-1640+CB-50-80 DMC-18x2,0+DB-14064 DMC-17x0+DB-14064 DMC-14x5+DB-14064 DMC-12x0+DB-12064	DMC-21x3 + DB-28040 DMC-18x6 + DB-28040	DMC-2xx0 DMC-1640	DMC-40x0 **26pin D-sub** DMC-41x3 DMC-40x0-I200	DMC-2xx0 DMC-1640

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Clock +	Cn+	**Data +**	Dn+
Clock -	Cn-	**Data -**	Dn-

**Note: some encoders may require that Data+ and Data- be reversed.*

SSI signal	2X 50 pin IDC (J6 & J8)	2X 20 pin IDC (J4 & J5)	Phoenix MD/80	4000 15 pin Dsub	80 pin SCSI	41X3 26 pin Dsub
D0-	J6-4	J4-4	34	A axis - 12	44	Axis A - 23
D0+	J6-2	J4-5	33	A axis - 4	42	Axis A - 15
D1-	J6-8	J4-9	36	B axis - 12	48	Axis B - 23
D1+	J6-6	J4-10	35	B axis - 4	46	Axis B - 15
D2-	J6-12	J4-14	38	C axis - 12	52	Axis C - 23
D2+	J6-10	J4-15	37	C axis - 4	50	Axis C - 15
D3-	J6-16	J4-19	40	D axis - 12	56	Axis D - 23
D3+	J6-14	J4-20	39	D axis - 4	54	Axis D - 15
D4-	J8-4	J5-4	74	E axis - 12	4	Axis E - 23
D4+	J8-2	J5-5	73	E axis - 4	2	Axis E - 15
D5-	J8-8	J5-9	76	F axis - 12	8	Axis F - 23
D5+	J8-6	J5-10	75	F axis - 4	6	Axis F - 15
D6-	J8-12	J5-14	78	G axis - 12	12	Axis G - 23
D6+	J8-10	J5-15	77	G axis - 4	10	Axis G - 15
D7-	J8-16	J5-19	80	H axis - 12	16	Axis H - 23
D7+	J8-14	J5-20	79	H axis - 4	14	Axis H - 15
C0-	J6-31	J4-3	11	A axis - 9	71	Axis A - 6
C0+	J6-29	J4-2	12	A axis - 11	69	Axis A -24
C1-	J6-27	J4-8	13	B axis - 9	67	Axis B - 6
C1+	J6-25	J4-7	14	B axis - 11	65	Axis B -24
C2-	J6-23	J4-13	15	C axis - 9	63	Axis C - 6
C2+	J6-21	J4-12	16	C axis - 11	61	Axis C -24
C3-	J6-19	J4-18	17	D axis - 9	59	Axis D - 6
C3+	J6-17	J4-17	18	D axis - 11	57	Axis D -24
C4-	J8-31	J5-3	51	E axis - 9	31	Axis E - 6
C4+	J8-29	J5-2	52	E axis - 11	29	Axis E -24
C5-	J8-27	J5-8	53	F axis - 9	27	Axis F - 6
C5+	J8-25	J5-7	54	F axis - 11	25	Axis F -24
C6-	J8-23	J5-13	55	G axis - 9	23	Axis G - 6
C6+	J8-21	J5-12	56	G axis - 11	21	Axis G -24
C7-	J8-19	J5-18	57	H axis - 9	19	Axis H - 6
C7+	J8-17	J5-17	58	H axis - 11	17	Axis H -24
Vcc (+5V)	J6-49 J8-49	J4-1 J5-1	9, 19, 21, 31, 49, 59, 61, 71	15	40,80	9
GND	J6-18>50 (even) J8-18>50 (even)	J4-6,11,16 J5-6,11,16	10, 20, 22, 32, 50, 60, 62, 72	5	18,20,22,24,26,28,30,58,60,62,64,66,68,7	18

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Considerations for DMC-4000 with SSI and DV

For users wishing to operate in Dual Loop mode, the DF command can be used to configure a load-based SSI encoder and a motor-based incremental encoder with DV1. Wire the motor's incremental encoder per normal to the 4000's main encoder inputs. The load SSI encoder should be wired to the axis aux encoder lines following the table above. Issue an SSI configuration command to setup the SSI decoding for the axis aux encoder (e.g. SIn = **2**, si1, si2, si3 <p >q). Verify proper SSI operation by moving the motor in non-dual loop mode and checking TDn. Disable the motor with MO and issue DFn=1 and DVn=1. The axis control law will now fragment the PID loop. P and I will be closed around the SSI encoder. D will be closed around the motor encoder. Using DF allows this nonstandard mapping to apply to DV. See DV in the standard 4000 command reference for more details.

DF
Function: *Dual Feedback (DV feedback swap)*
Description:
Used in conjunction with DV to invert the normal PID fragmentation. Instead of PI calculating on the Main encoder register, and D on the Aux, DF enabled will close the PI loop on the Aux and the D loop on the Main.

This is used for applications where the load employs SSI feedback and the motor has standard incremental feedback.

Arguments: DF n,n,n,n,n,n,n,n where
n represents a Boolean ("on" or "off") and is either 1 or 0.

Usage:
While Moving: No
In a program: Yes
Command Line: Yes
Controller: DMC40x0 Rev 1.0a-SI or later
Default Value: 0

Operand Usage:
_DFn contains the value (1 or 0) of the specified axis.

Related Commands
DV
SI

Example:

```
MOX                          ;'Disable motor on X
SIX=2,25,15,0<13>2           ;'Setup SSI encoder to fill the Aux
                             ;'encoder register
DF1                          ;'Enable Dual Feedback Swap
DV1                          ;'Enable Dual Loop mode
SHX                          ;'Enable servo with new configuration
```


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