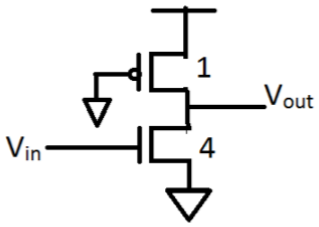
ECE 165 – Homework #4

Due: Never!
(but it is recommended to do the problems before the midterm)

Problem 1.

a) Calculate V_{out} for the pseudo-NMOS inverter when:
   i. V_{in} =0V
   ii. $V_{in} = V_{DD}$



Assume $\mu_n C_{ox} = 2\ \mu_p C_{ox}$, $V_{DSAT,\{n,p\}} = 0.2V$, $V_{tn} = |V_{tp}| =$ 0.4V, and V_{DD}, = 1.0 V. Ignore DIBL and channel-length modulation.

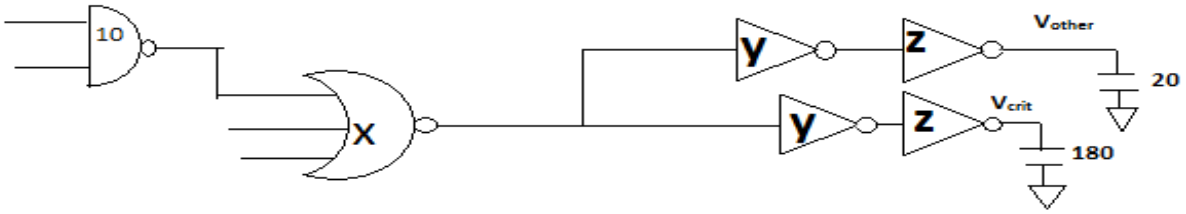
b) Ignoring leakage, does this gate consume static power?

c) Calculate the logical effort (i.e. g) of the gate. Remember that to calculate g, we compare to an inverter with the same current capability for a particular transition. Please use the class convention when sizing (i.e., keep the inverter P/N ratio 2/1).

d) Would you ever use a gate like this? A brief explanation discussing the pros and cons is fine.

Problem 2.

a) Calculate the input capacitance x, y, z that minimize the delay through the following circuit to V_{crit}. Note that in this problem, the input capacitance of each gate is proportional to the capacitance of a single NMOS transistor.



a) What is the delay to V_{crit} and V_{other} in units of τ_{inv}?

b) Now resize the circuit for minimum delay to V_{other} and recalculate both delays

Problem 3.

a) Design a single stage gate representing the function $F = \overline{(A + B)CD}$ using complementary static CMOS. Size the transistors for equal (worst case) rise/fall times.

b) Draw a stick diagram layout, using shared and merged contacts as much as possible. Annotate your schematic with all parasitic diffusion capacitance. Please use colored pens/pencils (or at least clearly label all lines).

c) Calculate the worst case pull up Elmore delay.