CDA 4213 001/CIS 6930 012
Fall 2017
CMOS VLSI Design

Lab 1 Report

Canvas Submission
Due: 11:59 PM, 8th Sept. 2017

Note: Upload PDF version of this report. Only PDF format is accepted.

Today's Date:	9/20/17
Your Name:	Alan Rodriguez
Your U Number:	U86831061
No. of Hours Spent:	6
Exercise Difficulty: (Easy, Average, Hard)	Average
Any Other Feedback:	

Question 1: Inverter

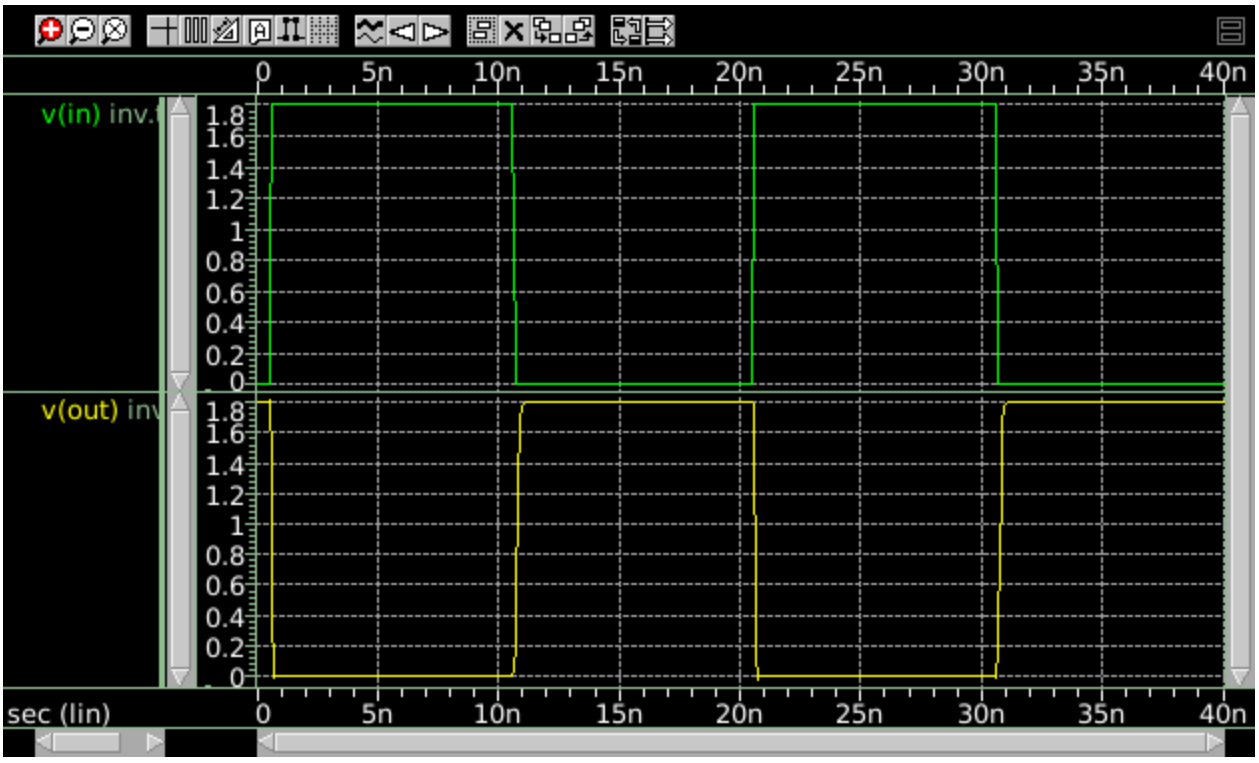
a) Complete the following table with values estimated in your simulations

Cload	tr	tf	tpdr	tpdf
0.01 pF	126.1036p	75.9393p	109.7278p	75.0610p
0.05pF	619.5977p	428.1802p	439.4759p	311.2846p
0.1pF	1.2380n	796.8495p	895.2210p	565.1435p

b) For each Cload, show your spice netlist (.sp file contents) and the waveform results. Use as many pages as needed.

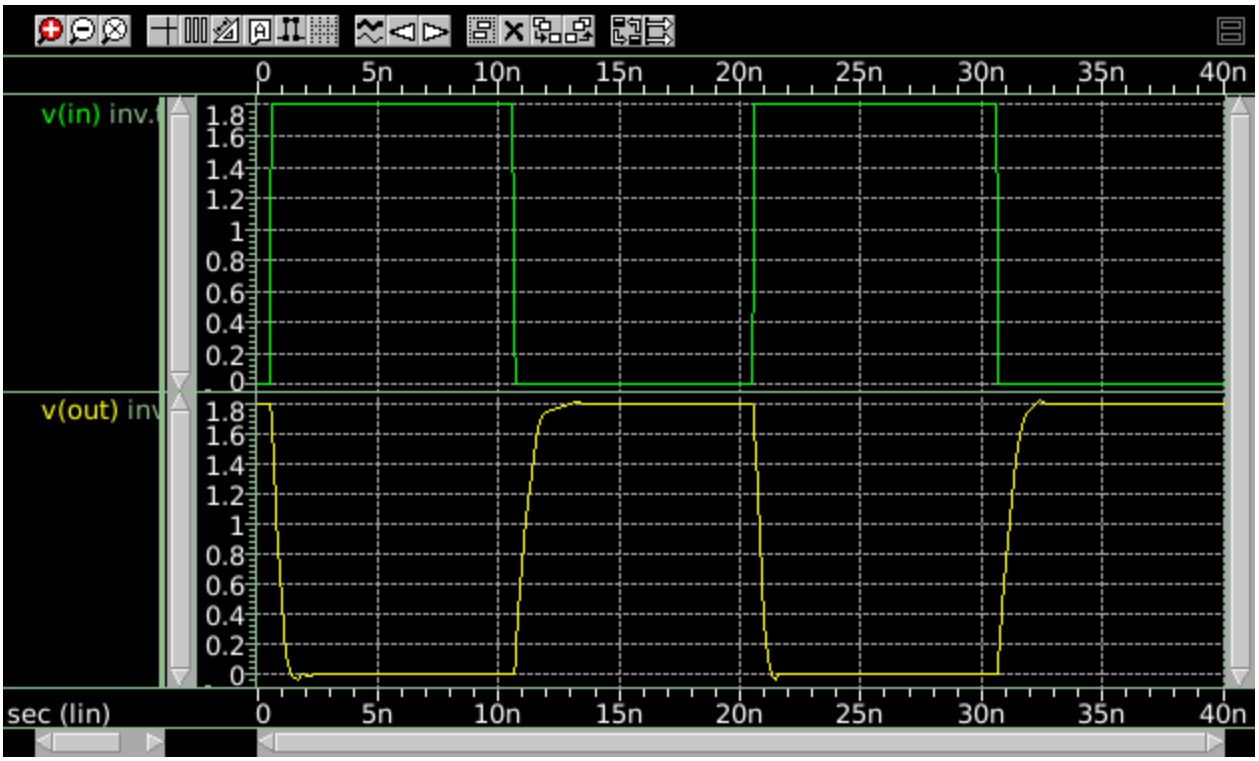
Cload 0.01pF:

```
**-------------------------------------------------------------
* Inverter SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m0 out in Vdd Vdd PMOS W=360 L=180
m1 out in  0   0  NMOS W=180 L=180

Cload out 0 0.01pF

.tran 1ns 40ns


.measure tran tr TRIG v(out) val=.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=.36 FALL=1
.measure tran tpdr TRIG v(in) val=.9 FALL=1 TARG v(out) val=.9 RISE=1
.measure tran tpdf TRIG v(in) val=.9 RISE=1 TARG v(out) val=.9 FALL=1
.plot V(in) V(out)
.end
```



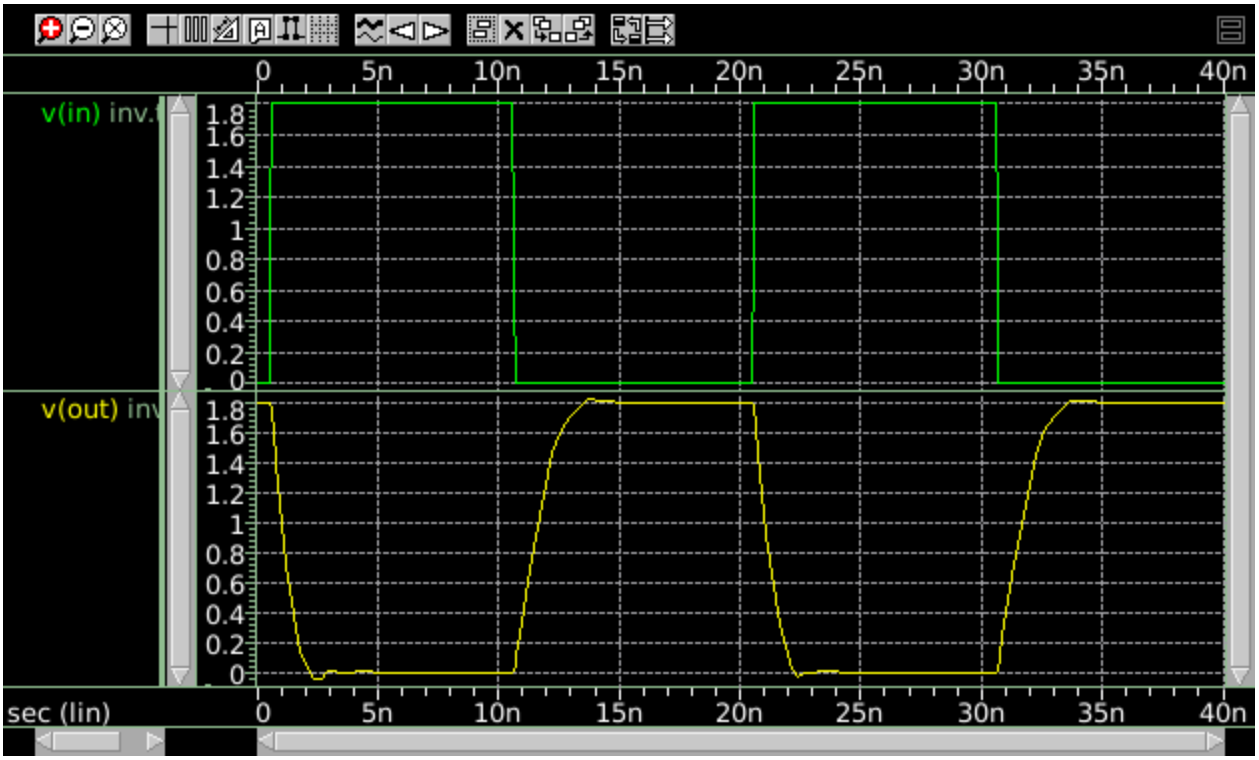
Cload 0.05pF:

```
**-------------------------------------------------------------
* Inverter SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m0 out in Vdd Vdd PMOS W=360 L=180
m1 out in  0   0  NMOS W=180 L=180

Cload out 0 0.05pF

.tran 1ns 40ns


.measure tran tr TRIG v(out) val=.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=.36 FALL=1
.measure tran tpdr TRIG v(in) val=.9 FALL=1 TARG v(out) val=.9 RISE=1
.measure tran tpdf TRIG v(in) val=.9 RISE=1 TARG v(out) val=.9 FALL=1
.plot V(in) V(out)
.end
```



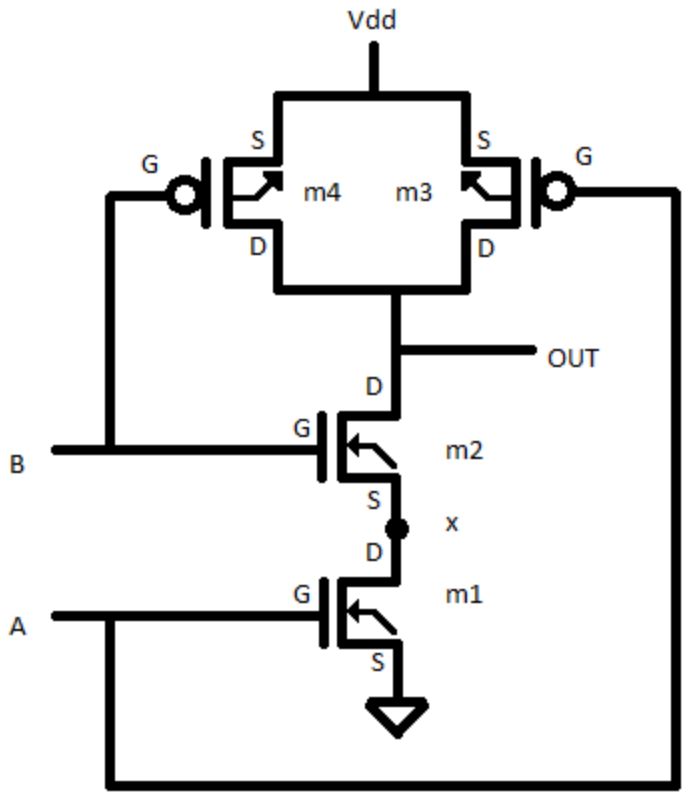
Cload 0.1pF

```
**-------------------------------------------------------------
* Inverter SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m0 out in Vdd Vdd PMOS W=360 L=180
m1 out in  0   0  NMOS W=180 L=180

Cload out 0 0.1pF

.tran 1ns 40ns

.measure tran tr TRIG v(out) val=.36 RISE=1 TARG v(out) val=1.44 RISE=1
.measure tran tf TRIG v(out) val=1.44 FALL=1 TARG v(out) val=.36 FALL=1
.measure tran tpdr TRIG v(in) val=.9 FALL=1 TARG v(out) val=.9 RISE=1
.measure tran tpdf TRIG v(in) val=.9 RISE=1 TARG v(out) val=.9 FALL=1
.plot V(in) V(out)
.end
```

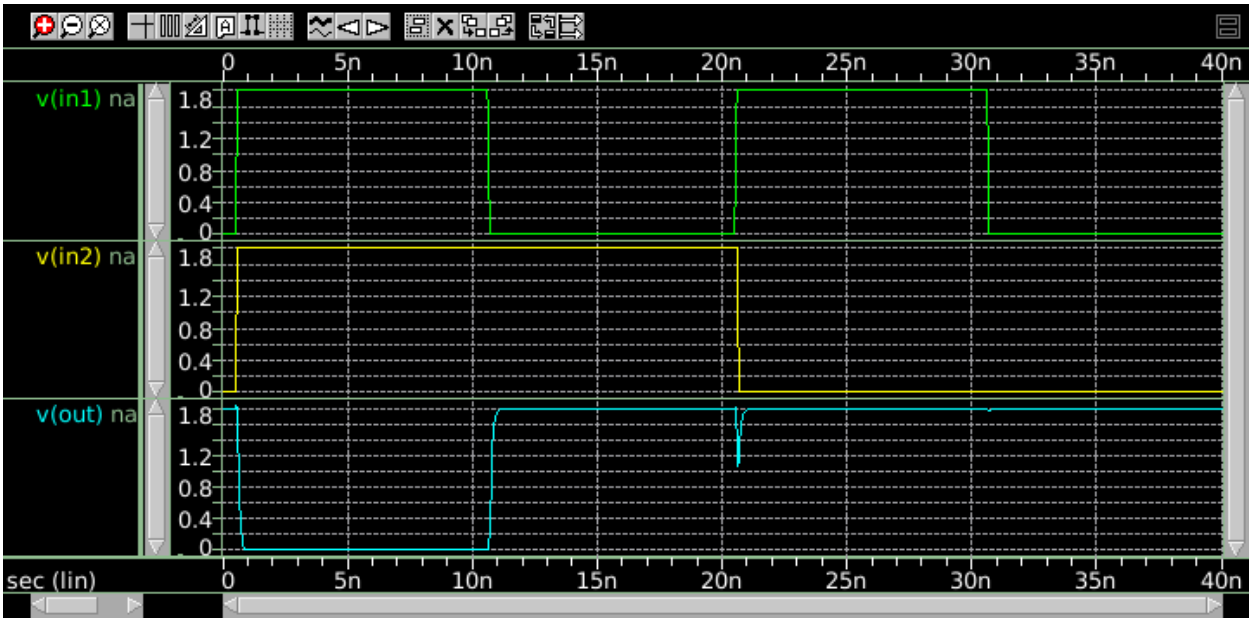


Question 2: 2-input NAND Gate

Include the following
a) Transistor level diagram
b) Spice netlist (.sp file contents)
c) Waveform results



```
**-------------------------------------------------------------

* Nand 2input SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin1 in1 0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns
Vin2 in2 0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 20ns 40ns

m1 X in1 0 0 NMOS W=180 L=180
m2 out in2 X X NMOS W=180 L=180
m3 out in1 Vdd Vdd PMOS W=360 L=180
m4 out in2 Vdd Vdd PMOS W=360 L=180

Cload out 0 0.01pF

.tran 1ns 40ns

.plot V(in) V(out)
.end
```



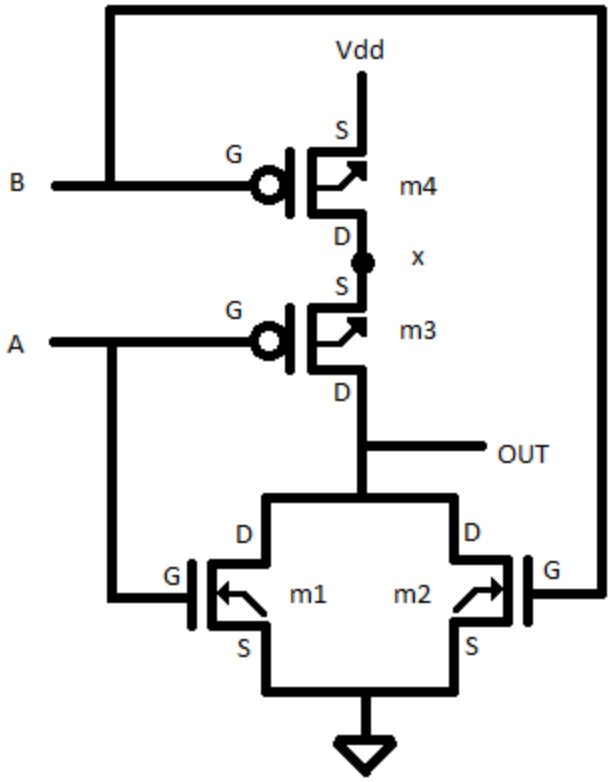
Question 2: 2-input NOR Gate

Include the following

a) Transistor level diagram

b) Spice netlist (.sp file contents)

c) Waveform results



```
**-------------------------------------------------------------
* 2-INPUT NOR SPICE deck
**-------------------------------------------------------------
* Parameters and models
**-------------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------------
Vdd Vdd 0 1.8V
Vin1 in1 0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns
Vin2 in2 0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 20ns 40ns

m1 out in1 0 0 NMOS W=180 L=180
m2 out in2 0 0 NMOS W=180 L=180
m3 out in1 X X PMOS W=360 L=180
m4 X in2 Vdd Vdd PMOS W=360 L=180

Cload out 0 0.01pF

.tran 1ns 40ns

.plot V(in) V(out)
.end
```