CDA 4213 001/CIS 6930 012
Fall 2017
CMOS VLSI Design

Lab 2 Report

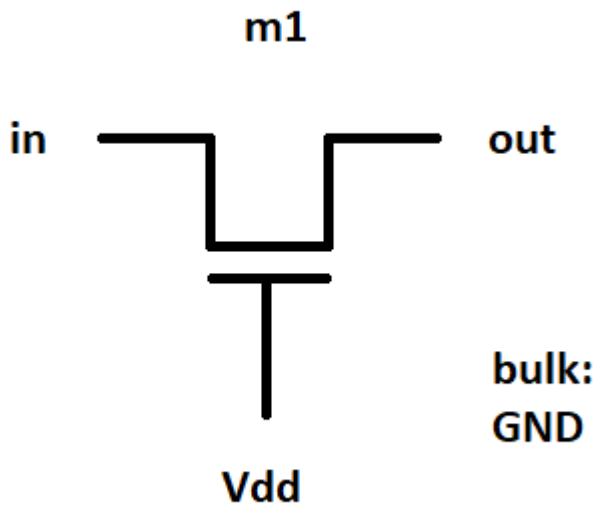
Canvas Submission
Due: 11:59 PM, 1st Oct. 2017

Note: Upload PDF version of this report. Only PDF format is accepted.

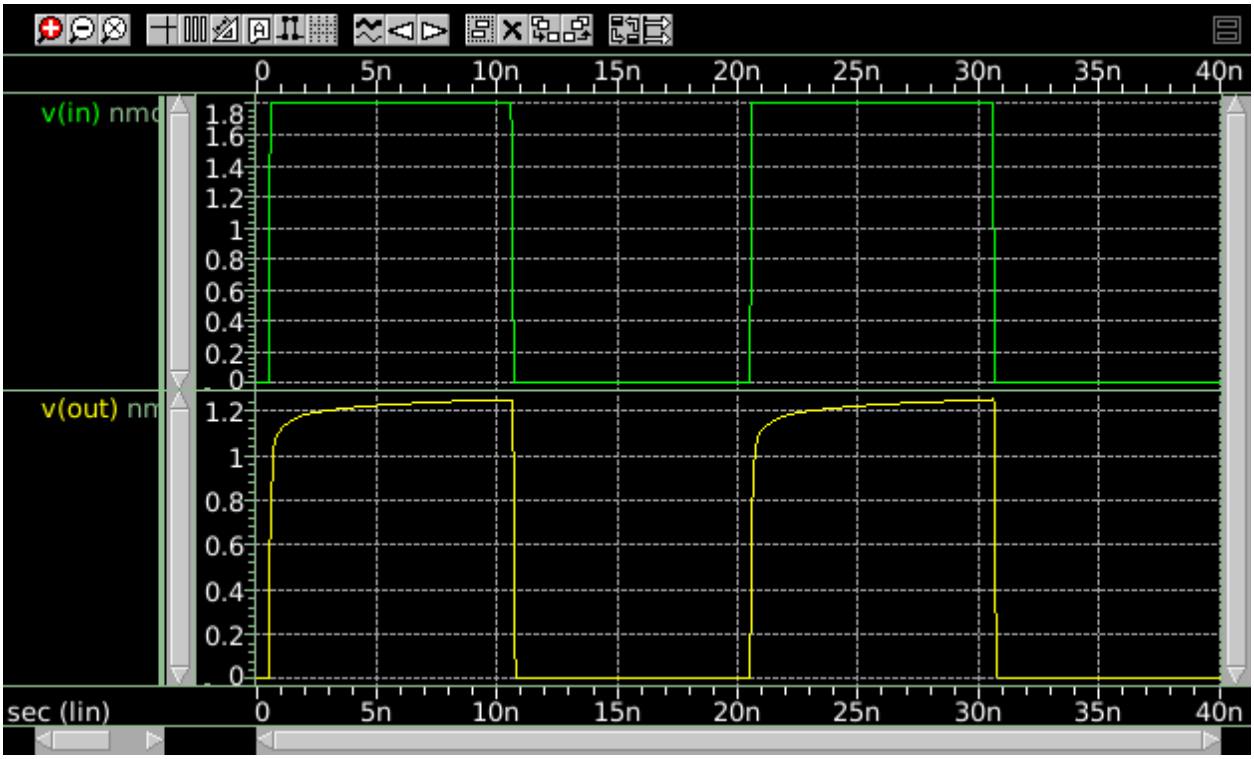
Today's Date:	10/1/17
Your Name:	Alan Rodriguez
Your U Number:	86831061
No. of Hours Spent:	3
Exercise Difficulty: (Easy, Average, Hard)	Average
Any Other Feedback:	

Question 1 (5 pts): NMOS Transistor

Include the following
a) Transistor level diagram
b) Spice netlist (.sp file contents)
c) Waveform results
d) Explain how you demonstrate that NMOS transistor is good (poor) conductor of 0 (1).



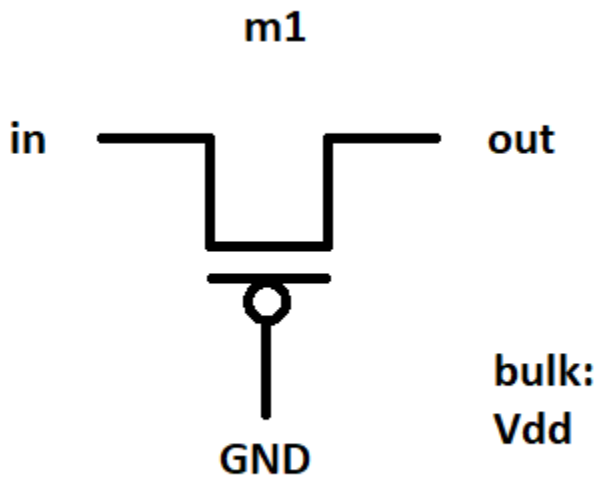

```
**-------------------------------------------------------
* NMOS SPICE deck
**-------------------------------------------------------
* Parameters and models
**-------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m1 out Vdd  in  0  NMOS W=180 L=180

Cload out 0 0.01pF

.tran 1ns 40ns
.plot V(in) V(out)
.end
```



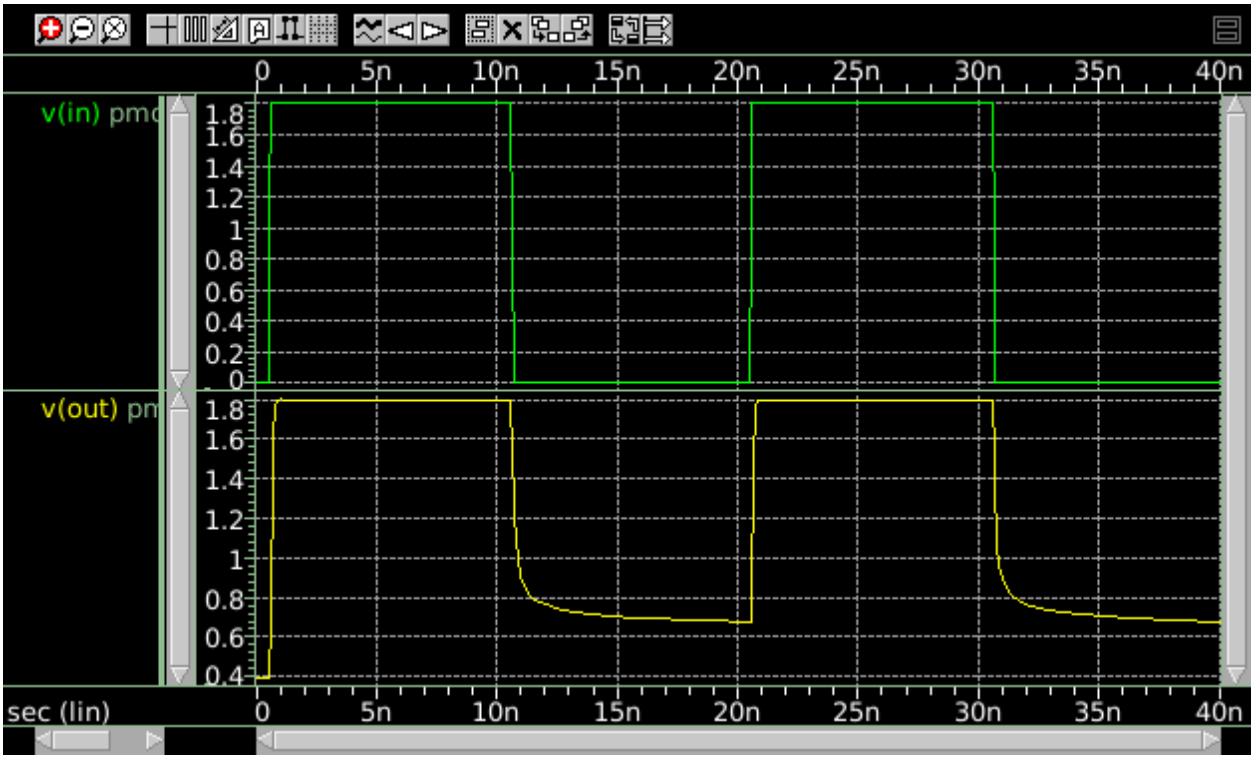
By passing the VDD into the gate for the NMOS transistor, it is shown that the value is only “strong” for 0 and degrades for logic of 1.

Question 2 (5 pts): PMOS Transistor

Include the following
a) Transistor level diagram
b) Spice netlist (.sp file contents)
c) Waveform results
d) Explain how you demonstrate that NMOS transistor is good (poor) conductor of 1 (0).



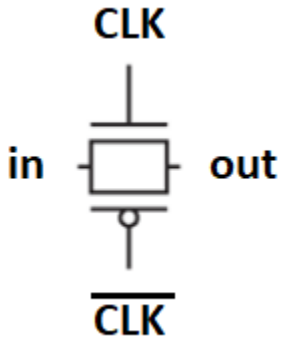

```
**-------------------------------------------------------
* PMOS SPICE deck
**-------------------------------------------------------
* Parameters and models
**-------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns

m1 out 0  in  Vdd  PMOS W=360 L=180

Cload out 0 0.01pF

.tran 1ns 40ns
.plot V(in) V(out)
.end
```



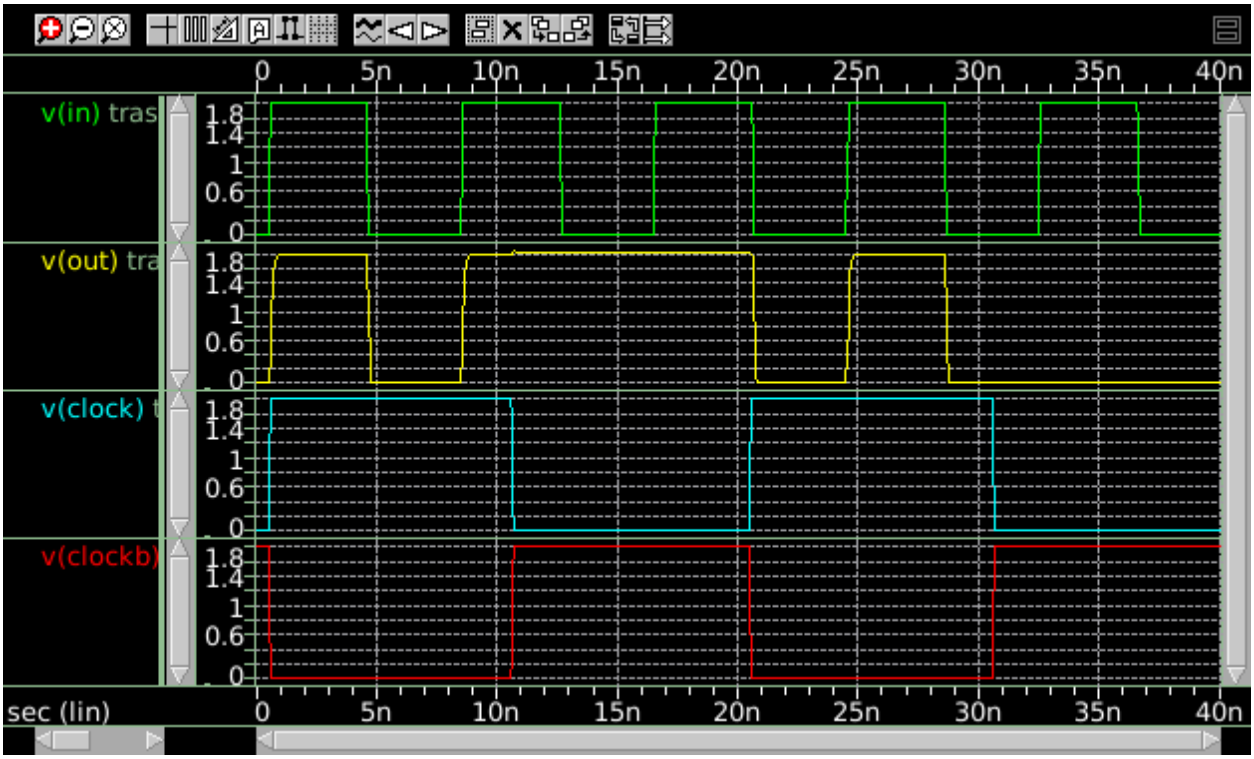
By passing the GND (0) into the gate for the PMOS transistor, it is shown that the value is only “strong” for 1 and degrades for logic of 0.

Question 3 (10 pts): Transmission Gate

Include the following
a) Transistor level diagram
b) Spice netlist (.sp file contents)
c) Waveform results




```
**-------------------------------------------------------
* Transmission Gate SPICE deck
**-------------------------------------------------------
* Parameters and models
**-------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------
Vdd Vdd 0 1.8V
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 4ns 8ns
Vin2 Clock  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns
Vin3 Clockb 0 PULSE 1.8V 0 0.5ns 0.1ns 0.1ns 10ns 20ns

m1 out ClockB  in  Vdd  PMOS W=360 L=180
m2 out Clock   in  0    NMOS W=180 L=180
Cload out 0 0.01pF

.tran 1ns 40ns
.plot V(in) V(out)
.end
```


0
5n
10n
15n
20n
25n
30n
35n
40n
v(in) tras
v(out) tra
v(clock) t
v(clockb)
1.8
1.4
1
0.6
0
sec (lin)

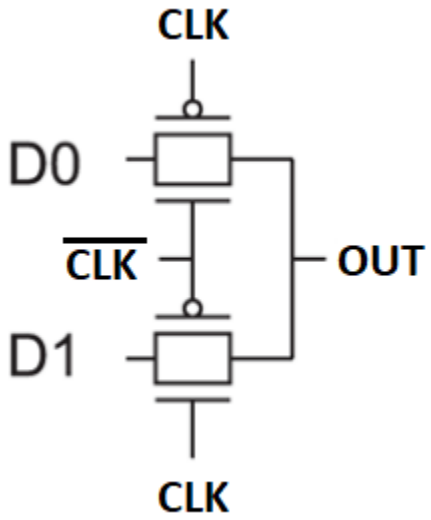
Question 4 (10 pts): 2-input Multiplexor

Include the following

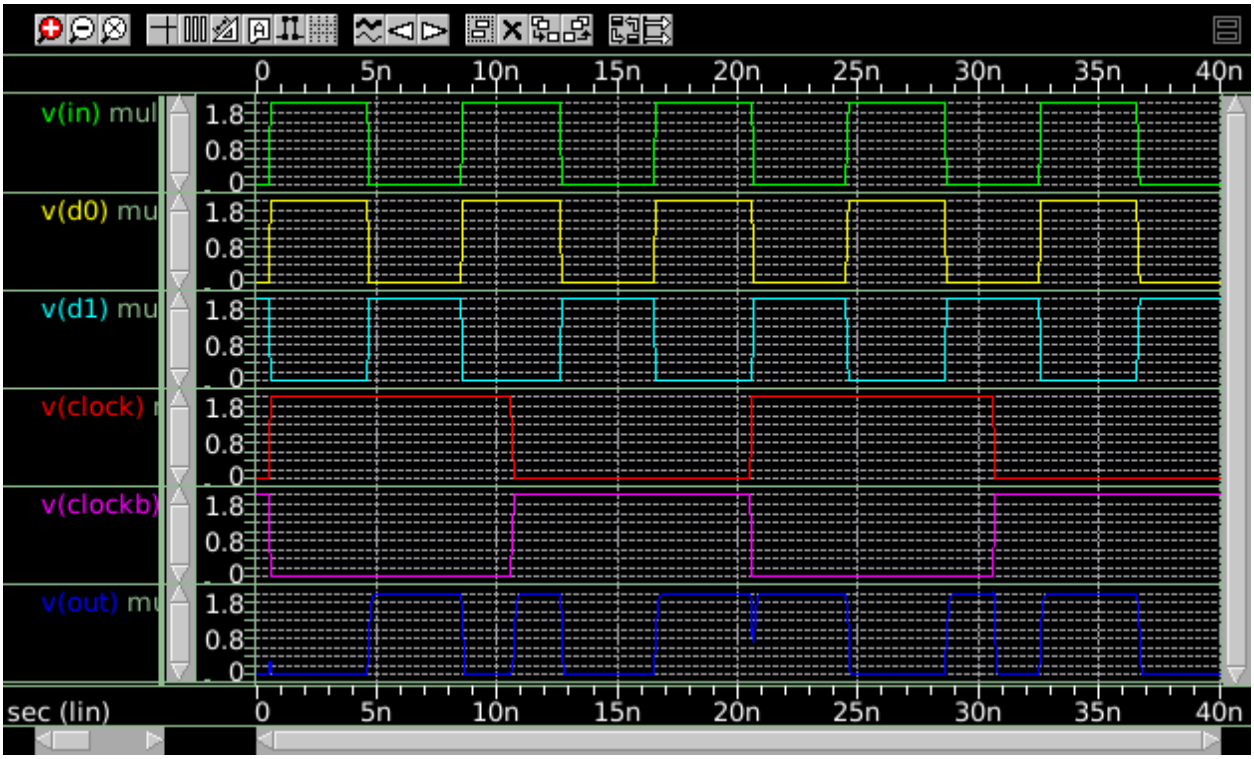
a) Transistor level diagram

b) Spice netlist (.sp file contents)

c) Waveform results




```
**-------------------------------------------------------
* 2-input Multiplexer Gate SPICE deck
**-------------------------------------------------------
* Parameters and models
**-------------------------------------------------------
.include mosistsmc180.sp.txt
.options post list scale=1n

**-------------------------------------------------------
* Simulation netlist
**-------------------------------------------------------
Vdd Vdd 0 1.8V
Vd0 d0  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 4ns 8ns
vd1 d1  0 PULSE 1.8V 0 0.5ns 0.1ns 0.1ns 4ns 8ns
Vin in  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 4ns 8ns
Vin2 Clock  0 PULSE 0 1.8V 0.5ns 0.1ns 0.1ns 10ns 20ns
Vin3 Clockb 0 PULSE 1.8V 0 0.5ns 0.1ns 0.1ns 10ns 20ns

m1 out Clock   d0  Vdd  PMOS W=360 L=180
m2 out Clockb  d0  0    NMOS W=180 L=180
m3 out Clockb  d1  Vdd  PMOS W=360 L=180
m4 out Clock   d1  0    NMOS W=180 L=180


Cload out 0 0.01pF
.tran 1ns 40ns
.plot V(in) V(out)
.end
```


0
5n
10n
15n
20n
25n
30n
35n
40n
v(in) mul
v(d0) mu
v(d1) mu
v(clock)
v(clockb)
v(out) mu
1.8
0.8
0
sec (lin)