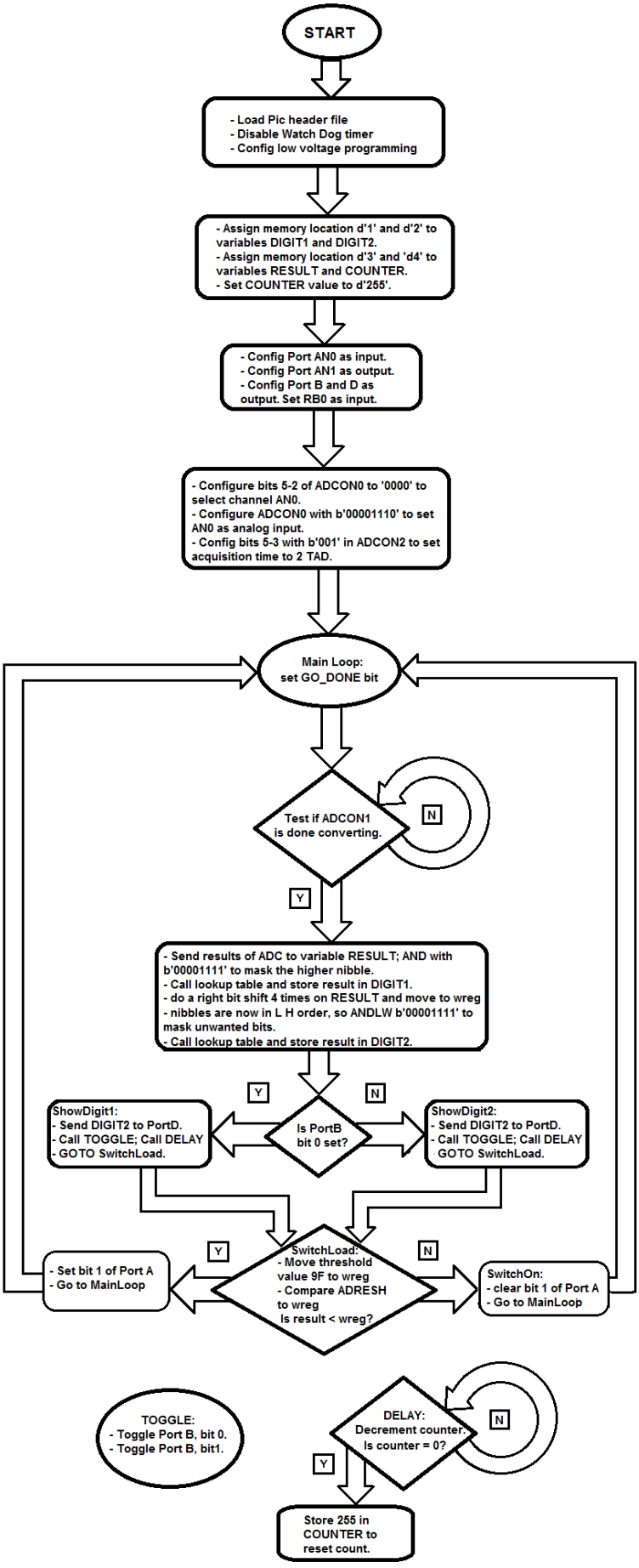
Problem Description:

In this assignment, we built an embedded system that read the ADC (analog to digital converter) and displayed the readings onto two 7-segment LEDs. The input value to the ADC was supplied by a potentiometer; when the potentiometer exceeded a threshold digital voltage of 9F (hex), the system turned on a servos motor powered fan. An optocoupler connected to a relay was used to enable the servos motor and power it on.

Pseudocode:

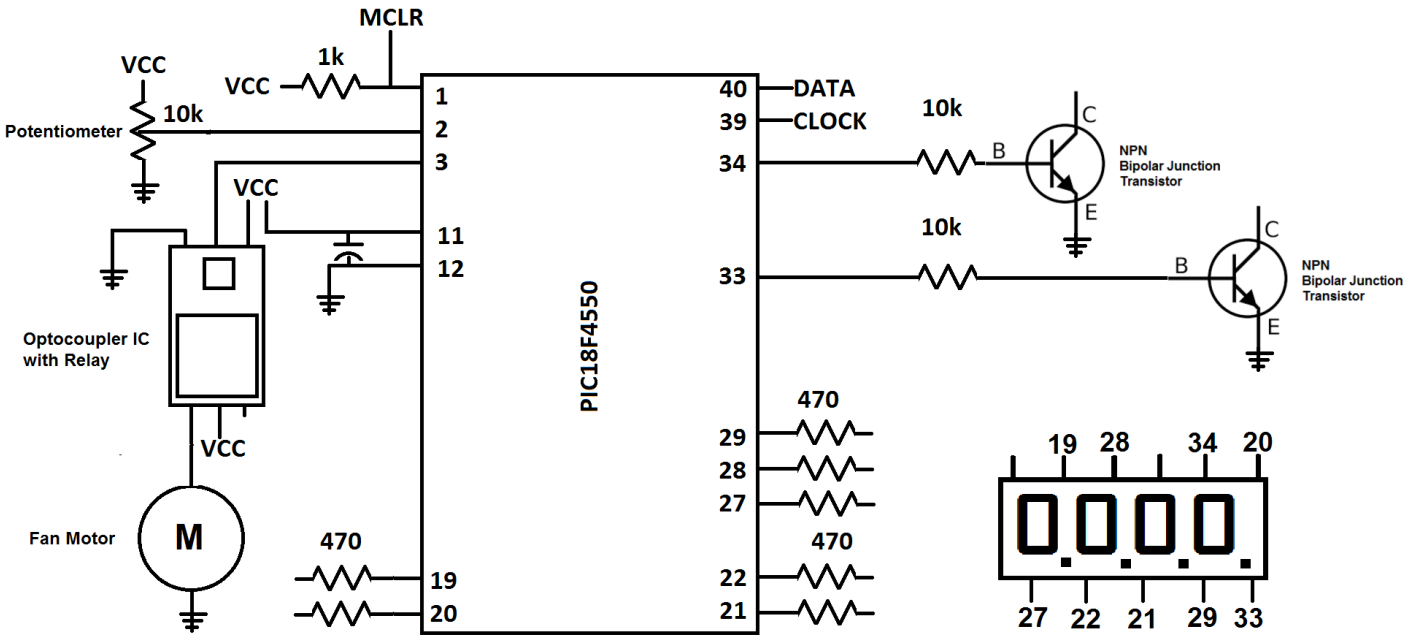

START
- Load Pic header file
- Disable Watch Dog timer
- Config low voltage programming
- Assign memory location d'1' and d'2' to variables DIGIT1 and DIGIT2.
- Assign memory location d'3' and 'd4' to variables RESULT and COUNTER.
- Set COUNTER value to d'255'.
- Config Port AN0 as input.
- Config Port AN1 as output.
- Config Port B and D as output. Set RB0 as input.
- Configure bits 5-2 of ADCON0 to '0000' to select channel AN0.
- Configure ADCON0 with b'00001110' to set AN0 as analog input.
- Config bits 5-3 with b'001' in ADCON2 to set acquisition time to 2 TAD.
Main Loop: set GO_DONE bit
Test if ADCON1 is done converting.
N
Y
- Send results of ADC to variable RESULT; AND with b'00001111' to mask the higher nibble.
- Call lookup table and store result in DIGIT1.
- do a right bit shift 4 times on RESULT and move to wreg
- nibbles are now in L H order, so ANDLW b'00001111' to mask unwanted bits.
- Call lookup table and store result in DIGIT2.
Y
N
ShowDigit1:
- Send DIGIT2 to PortD.
- Call TOGGLE; Call DELAY
- GOTO SwitchLoad.
Is PortB bit 0 set?
ShowDigit2:
- Send DIGIT2 to PortD.
- Call TOGGLE; Call DELAY
GOTO SwitchLoad.
Y
N
- Set bit 1 of Port A
- Go to MainLoop
SwitchLoad:
- Move threshold value 9F to wreg
- Compare ADRESH to wreg
Is result < wreg?
SwitchOn:
- clear bit 1 of Port A
- Go to MainLoop
TOGGLE:
- Toggle Port B, bit 0.
- Toggle Port B, bit1.
DELAY:
Decrement counter.
Is counter = 0?
N
Y
Store 255 in COUNTER to reset count.

Assembly Code:

```
#include <p18f4550.inc>
 CONFIG WDT=OFF              ; disable watchdog timer
 CONFIG MCLRE = ON           ; MCLEAR Pin on
 CONFIG DEBUG = OFF          ; disable Debug Mode
 CONFIG LVP = OFF    ; Low-Voltage programming disabled (necessary for debugging)
 CONFIG FOSC = INTOSCIO_EC   ;External oscillator, port function on RA6
 org 0                ;

DIGIT1 EQU D'1'              ;variables to store digit values
DIGIT2 EQU D'2'
RESULT EQU D'3'
COUNTER EQU D'4'             ;counter variable

   MOVLW D'255'              ;Move decimal value of 255 to Working register
   MOVWF COUNTER ;Move value of working register to counter address
   BSF PORTA, 1              ;set portA pin 1 to 1
   BCF TRISA, 1              ;set portA pin 1 for output
   CLRF PORTD                ;clear port D bits
   CLRF TRISD          ;setup port D as output
   CLRF TRISB          ;set port B as output pins
   MOVLW B'00000001'         ;set all bits to 0 but RB0
   MOVWF PORTB
   MOVLW B'00000000'         ;bits 5-2 select channel AN0
   MOVWF ADCON0
   MOVLW B'00001110'         ;set pin AN0 for analog input
   MOVWF ADCON1
   MOVLW B'00001000'         ;bits 5-3 16 TAD aquisition time, bits 2-0 Fosc/2 conversion clock select bits
   MOVWF ADCON2
   BSF ADCON0, ADON          ;set bit 0 to enable analog digital conversion to be on

MainLoop:
   BSF ADCON0, GO_DONE

TEST:
   BTFSC ADCON0, 1   ;bit test go/notdone, skip if clear
   BRA TEST          ;branch to test

   MOVF ADRESH, 0    ;send high byte of result to wreg
   MOVFF ADRESH, RESULT

   ANDLW B'00001111';AND low nibble of byte to wreg

   CALL LookUp
   MOVWF DIGIT1

   RRNCF RESULT, 1
   RRNCF RESULT, 1
   RRNCF RESULT, 1
   RRNCF RESULT, 1
   MOVF RESULT, 0

   ANDLW B'00001111'
   CALL LookUp
   MOVWF DIGIT2

   BTFSS PORTB, 0
   BRA ShowDigit2
```

```
ShowDigit1:
   MOVFF DIGIT2, PORTD
   CALL TOGGLE
   CALL DELAY
   GOTO SwitchLoad

ShowDigit2:
   MOVFF DIGIT1, PORTD
   CALL TOGGLE
   CALL DELAY

SwitchLoad:
   MOVLW 0x9F
   MOVFF ADRESH, RESULT
   CPFSLT RESULT
   BRA SwitchOn
   BSF PORTA, 1
   GOTO MainLoop

SwitchOn:
   BCF PORTA, 1
   GOTO MainLoop

TOGGLE:
   BTG PORTB, 0
   BTG PORTB, 1
   RETURN

DELAY:
   DECFSZ COUNTER
   BRA DELAY

   MOVLW D'255'        ;resets counter to 255
   MOVWF COUNTER
   RETURN

LookUp:
   MULLW 2
   MOVF PRODL, 0       ;Move low byte of product of mult to wreg
   ADDWF PCL, 1        ;Add low byte of program counter to wreg
   RETLW B'00111111'   ;0
   RETLW B'00000110'   ;1
   RETLW B'01011011'   ;2
   RETLW B'01001111'   ;3
   RETLW B'01100110'   ;4
   RETLW B'01101101'   ;5
   RETLW B'01111101'   ;6
   RETLW B'00000111'   ;7
   RETLW B'01111111'   ;8
   RETLW B'01100111'   ;9
   RETLW B'01110111'   ;A
   RETLW B'01111100'   ;B
   RETLW B'00111001'   ;C
   RETLW B'01011110'   ;D
   RETLW B'01111001'   ;E
   RETLW B'01110001'   ;F
 end
```

Circuit Diagram:



Actual Implementation:

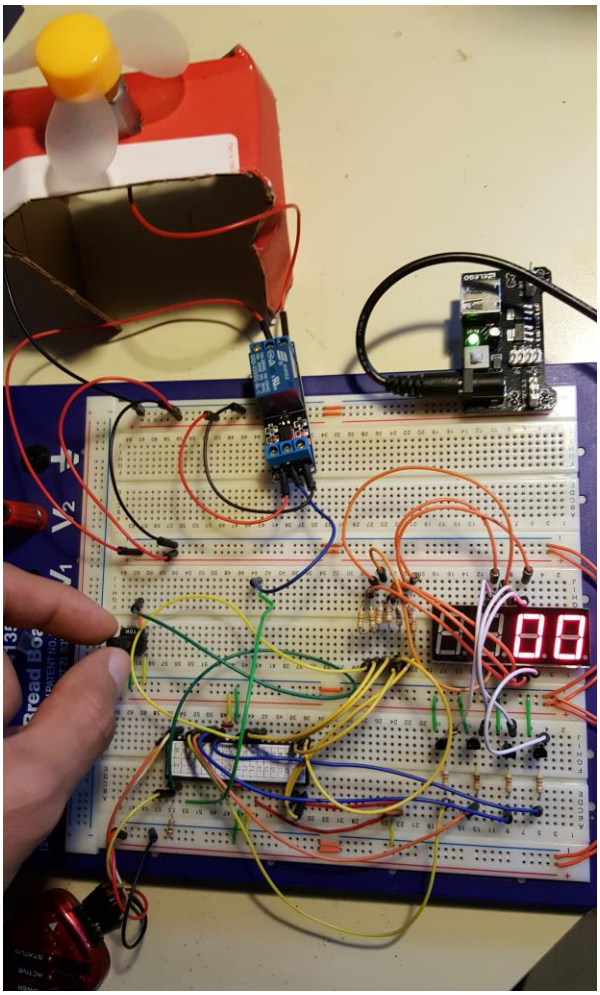


Figure 1- Potentiometer is set to lowest analog input, fan motor is off.

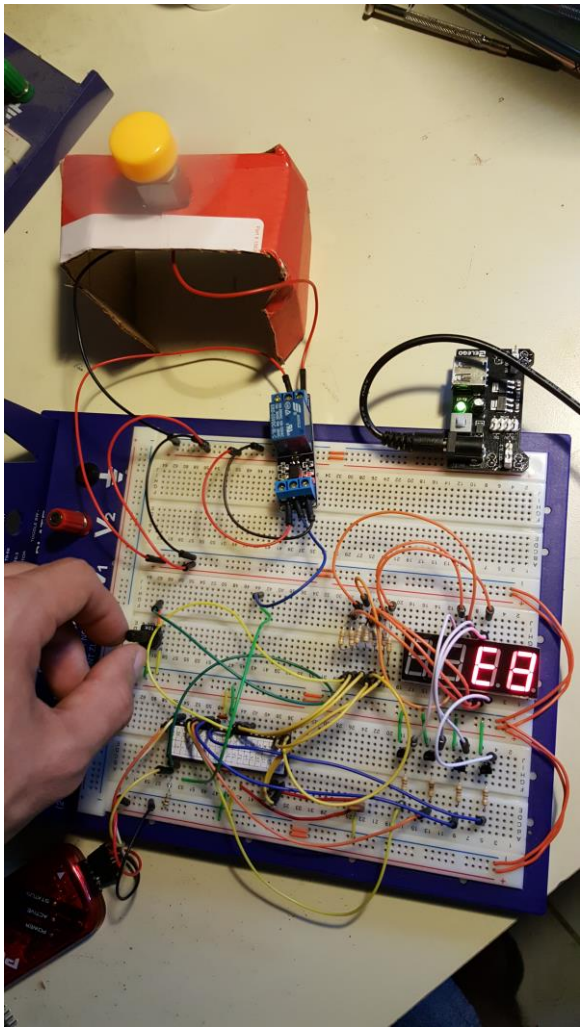


Figure 2- ADRESH is larger than threshold value of 9F, fan motor is on.

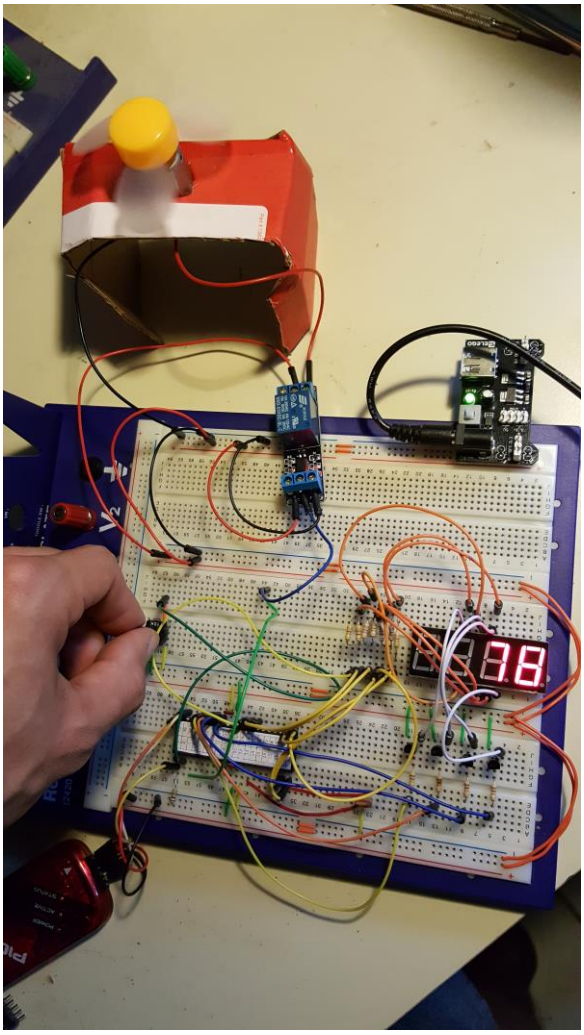


Figure 3- The analog input is lowered below the threshold. Fan motor turns off and fan slows to a stop.