B.1 Friendly ESD Integration of 3rd Party IP in SoCs?

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More and more 3rd party IP are used to accelerate large SoCs creation, therefore ESD-robust SoCs implementation can't be controlled anymore by only one ESD specialist and obviously becomes a joint effort and responsibility for the SoC-level designer and the IP providers. Indeed, the success in this IP integration task strongly relies on passing all the required information and aligning on some common ESD assumptions between the IP provider and the SoC designer:

- The key IP design targets and assumptions for ESD & LU
- Some IP ESD protection network details
- The IP integration rules at SoC level
- Some IP silicon validation details
- ESD EDA checks enabled for the IP verification on SoC

A few EDA-ESD tools may come into the loop to help, but no mainstream EDA solution enforces a full comprehensive solution. Come to share your expectations and your experience (good or bad) about SoC implementation with 3rd party IP and ESD-EDA tools. This would be of great value to improve methodology and support for ESD-robust IP integration.