Charged device ESD threats with high speed RF interfaces

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Abstract - High speed RF interfaces operating in tens Gbit/s range have limited ESD immunity. These interfaces are accessible when electro-mechanics are assembled on a printed circuit board. Charged device ESD threats due to charged assemblies with less than 1 pF source capacitances are discussed in this paper.

I. Introduction

An increasing amount of data transmitted in communication networks has pushed electronic systems to operate in tens of Gbits/s range. At the same time, analogic signal frequencies are above 10 GHz which requires system designers to meet strict signal integrity targets. Here any additional capacitive load along the signal path would worsen signal quality. Unfortunately, on-chip electrostatic discharge (ESD) protection structures or on-board protection devices would increase the capacitive load and are implemented in most cases only at limited level. These high-speed signal I/Os on an IC level have typically human body model (HBM) or charged device model (CDM) withstand voltages in the range of <500 V and <250 V, respectively.

In this paper, we show how a small size charged metal object, such as a single connector pin, can inject a high amplitude short current pulse through a printed circuit board (PCB) trace, bypass on-chip CDM protection designs, and damage the RF input gate. The study bases on real life failures observed on high-speed RF silicon after electromechanical components assembly. The failure signature on the silicon is identical to damages caused by current pulses in CDM qualification, but the current waveform has a faster rise time. Therefore, the component-level CDM withstand voltage cannot be used to predict ESD risks during assembly.

The target of the paper is to analyze the main discharge parameters affecting ESD risks. At first, we will present a basic discharge scenario and simulation models to predict discharge waveforms from small charged metal objects. Next, we will introduce the test setup and tools used in laboratory and field measurements, and finally we will present results of the analysis.

We will also discuss challenges and uncertainties related to the analysis where fast ESD events are measured and propose different corrective actions to minimize observed type of ESD risks in the future.

II. Measurement and Simulation Methods

A. Discharge Scenario

Most on-board connectors have a plastic encapsulation and signal pins are thin metal wires inside the plastic. With high speed connectors, the plastic material is purely selected based on the electrical conductivity, permeability and permittivity targets. In addition, the plastic material has rigid requirements for manufacturability and physical tolerances to maintain the signal integrity through the component.

The plastic material is a good insulator and gets static surface charges when the surface is touched. These surface charges can induce >100 kV/m electrostatic fields (*E-field*) inside the connector and polarize kV level potentials on signal pins inside the connector. The amount of stored charge depends on the capacitance of the pins, but typically pins are only a few centimeters long with a capacitance between 0.5 pF – 2 pF just before assembly. In this case, 1 kV charging potential

would give a total discharge energy of about 0.25 µJ – 1 µJ.

On top of the surface charges, internal plastic parts can have additional surface charges. Connectors can be built of small separate subparts with varying material properties. These subparts can have small gaps between each other and can get static charges when vibrating during handling. All charged surfaces may not be visible, and for example, ionization cannot remove charges.

Figure 1 shows an example discharge scenario where a charged through-hole connector is pressed on the surface of the PCB. There can be several discharges from individual metal pins through the PCB trace and via the RF component soldered on the PCB. Through-hole connectors are typically assembled after reflow.

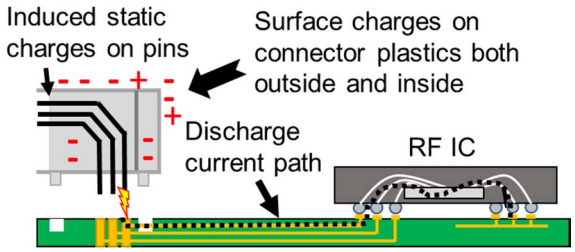

Figure 1: Growth for Technique Alpha.

B. Simulations

CDM type of discharges from charged metal objects are simulated with LTspice software by using an equivalent circuit shown in Figure 2. In this case the DUT is a charged metal wire. In a real ESD event the RF I/O receiving the stress pulse is in a high impedance state, but here the discharge current is measured with the one-ohm shunt resistor *R_meas*.

The metal wire is modelled with a simplified source circuit with two parallel capacitors *C_dut* and *C_wire* with an initial charge. In addition, there is a delay line *T1* providing a rectangular few hundred picoseconds long pulse with a decaying amplitude. Capacitance and inductance values are variables and are selected based on the used measurement setup and type of the discharge source.

Simulating discharge current through the PCB board requires to add trace parasitics into the equivalent circuit. Here the PCB traces between the connector input and RF I/O are modelled with S-parameters by using SIwave software and data is exported to Simplorer co-simulator tool for system-level simulations. The discharge equivalent circuit in Figure 3 is a modified version of the circuit in Figure 2 and includes trace S-parameters in the imported two-port module.

The high-speed signal is built with a 50 Ω differential signal pair inside the PCB. However, the discharge current is going through one trace at the time. Therefore, S-parameters are also extracted for one trace at the time when the trace is terminated with 50 Ω ports. In parallel, another differential pair is terminated at the IC side with a 50 Ω port and the other end is left electrically floating.

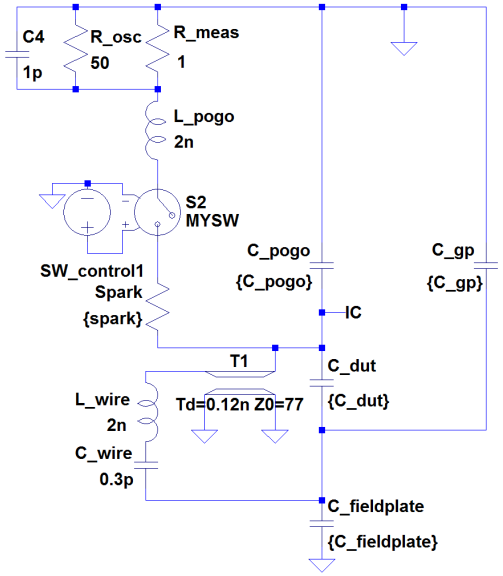

Figure 2: CDM discharge event equivalent circuit.

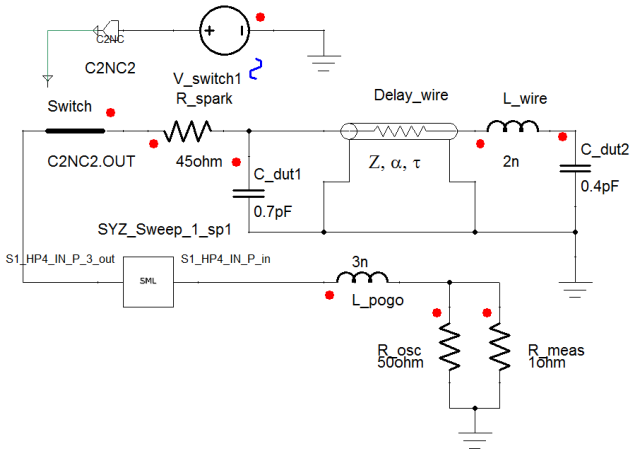

Figure 3: Equivalent circuit for system level discharge simulations.

C. Measurement Methods

Discharge currents in a laboratory environment are measured by using a CDM head model 4106 from Barth Electronics with 36 cm^2 size ground plate. Measurements in process areas are made with a self-made one-ohm shunt resistor current probe shown in Figure 4 [1]–[3]. Both discharge heads have 1 dB bandwidth limit at 10 GHz. The self-made discharge head has a 4.8 cm^2 or 17.6 cm^2 optional ground

reference plate. This probe produces lower peak current amplitudes due to smaller capacitance *C_gp* than the model 4106 when the total capacitance of the discharge source *C_dut* + *C_wire* is above 3 pF.

The main reason for the self-made current probe was to have a small size tool that could be used manually in the manufacturing process area during ESD risk analysis. It is challenging to contact small objects in the process area even when the size of the discharge head ground plate is just about 2 x 2 cm. In addition, manual testing brings extra uncertainties due to varying contact speed and positioning of the pogo pin. Therefore, each measurement need to be repeated multiple times to detect the worst-case discharge scenario.

Connectors are charged by field induction or by direct contact with a high voltage source. Here the main challenge in the process area was the relative humidity that was above 50 %. Therefore, high ohmic contact charging was used when the leakage was higher than a few volts/second. Voltages were controlled with Prostat and TREK contact voltage meters, TREK 520 and Trek 542 non-contact voltage meters.

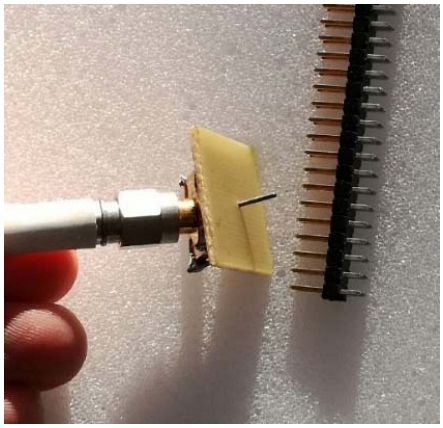

Figure 4: A discharge current probe with one ohm shunt resistor and 4.8 cm^2 ground plate.

Discharges are measured by touching charged pins directly with the current probe, and secondly, when a charged pin touches the PCB through-hole pad area and the discharge current travels through the PCB trace. In this latter case, the current is captured from the IC pad area with the current probe shown in Figure 4.

Discharge current measurements were made at first with an 8 GHz oscilloscope, but when the source capacitance is well below 1 pF the required current measurement bandwidth can be around 11 GHz. Therefore, measurements are made with a 12.5 GHz oscilloscope having 100 GSa/s speed. Therefore, the current probes limit the measurement bandwidth to 10 GHz with the 1 dB bandwidth limit.

An additional measurement error comes from the coaxial cables between the current probe and oscilloscope. A typical insertion loss at 10 GHz was about 1 dB with the 1 m long flexible cables, depending on the bending of the cable. This attenuation is not compensated from measurement results. The measurement setup also induced high frequency ringing on the current waveforms. Therefore, an estimated error with the current amplitude measurements can be in the range of ±30 % when the discharge bandwidth is close to the 10 GHz range [2]. Uncertainties related to the rise time measurements are mainly depending on the measurement-setup bandwidth, the current waveform oscillations, and are estimated to be below ±20 %.

III. Results

A. Simulation Results

Charged device ESD type of simulations are made for the through-hole connector design with pins in four rows as shown in Figure 5. This connector has several differential signal pairs and ground pins in a matrix format, but only one column is shown to simplify the design. The length of the metal pins is; 1st row 39 mm, 2nd row 33.5 mm, 3rd row 19.5 mm, and 4th row is the shortest 14.3 mm.

Figure 6 presents the measured and simulated discharge current waveforms for the 39 mm long corner pin no.1. The metal pin is charged up to 500 V and discharged with the hand-held current probe. Source capacitances *C_dut* and *C_wire* are calculated based on the measured dynamic charge and the charging voltage. Transmission line *T1* parameters are set based on vector network analyzer (VNA) measurements. In addition, the delay parameter depends on the size and position of the charged metal pin inside the plastic material.

The simulated waveform matches the measured waveform when the spark resistance is adjusted up to 45 ohms and the total capacitance is set based on the calculated source capacitance 0.9 pF. With the shortest 14.3 mm long wire the simulation source can be simplified and a single capacitance *C_dut* alone can model the charged pin with reasonable accuracy.

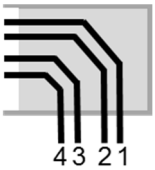

Figure 5: A side view of the through-hole connector.

Figure 7 shows the simulated S21 parameters for the two signal traces with 35 mm and 85 mm length. S-parameters were also measured with the VNA, but the measurement setup available had challenges with impedance matching when the frequency was over 5 GHz and simulations were estimated to be more accurate. As expected, the traces have a higher attenuation when the frequency approaches 11 GHz.

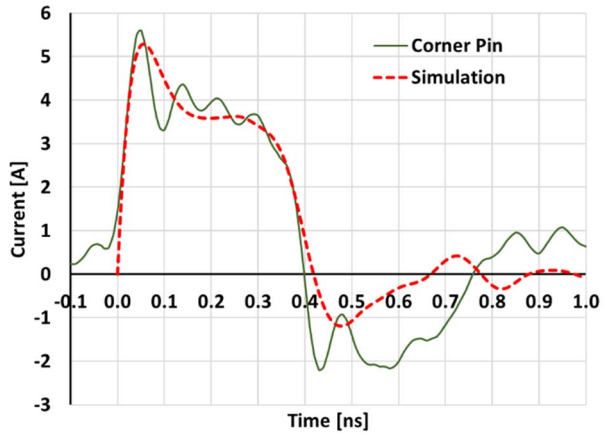

Figure 6: Measured and simulated discharge current waveforms from the 39 mm long pin with 500 V initial charging voltage.

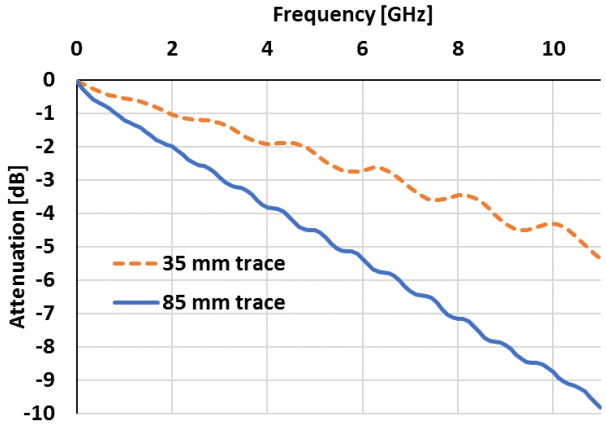

Figure 7: Simulated S21 parameters for the two traces between connector input and RF I/O pad.

Figure 8 and Figure 9 show the simulated discharge waveforms for the 39 mm long and 14.3 mm long pins with 100 V initial charge. Based on simulations the peak current has about 15 % attenuation, and the pulse rise time is about 1.5 – 2 times longer depending on the trace length if compared to the direct discharge from the charged pin. The trace will also attenuate high frequency oscillations, but adds additional low frequency current bouncing along the discharge path as shown in Figure 10. These reflections exist also in measurement results.

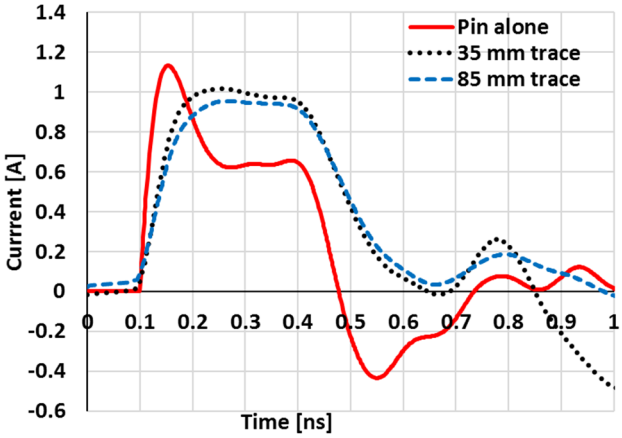

Figure 8: Simulated 39 mm long pin discharges via two different lengths of PCB traces and a direct discharge from the charged pin.

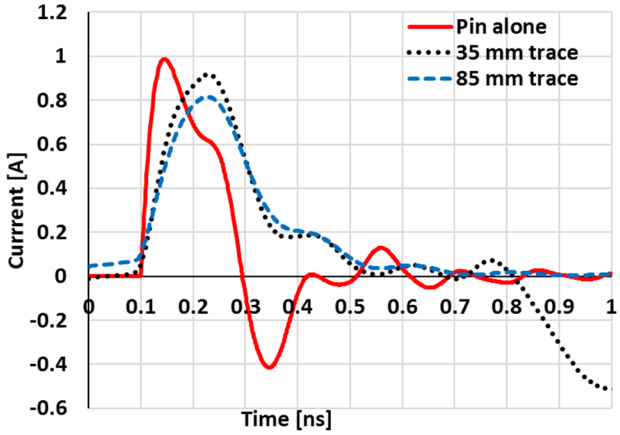

Figure 9: Simulated 14.3 mm long pin discharges via two different length of PCB traces and a direct discharge from the charged pin.

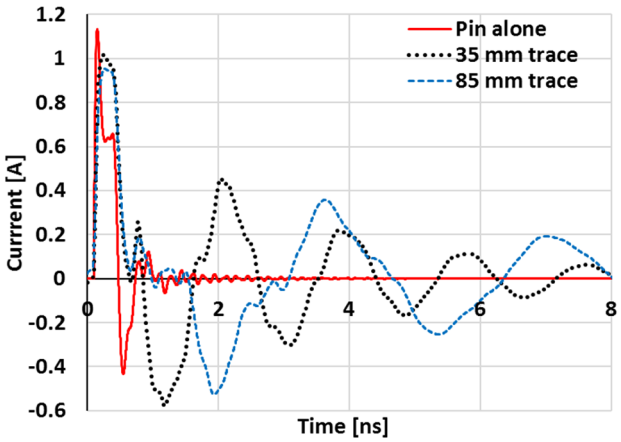

Figure 10: The same data as in Figure 9 with longer simulation time showing the waveform bouncing due to the trace parasitics.

B. Measurement Results

1. IC and pin discharges

Figure 11 shows measured CDM qualification discharge current waveforms with 110 V for two BGA components. These BGAs have high speed RF I/Os in connection with the through-hole connector on the PCB. Discharges from the RF pins have a lower peak current than the CDM current waveforms measured from the ground pins. A detailed design of the BGAs is not known and the difference in discharge waveforms can be due to the isolation of the RF pins from the power domains of the silicon. The measured current rise time is always more than 140 ps and the maximum *di/dt* is <17 A/s with 110 V.

CDM waveforms are compared to the current waveforms shown in Figure 12 and Figure 13, which are measured direct discharges from the charged metal pins. Table 1 has a summary of the typically observed discharge waveforms. The most interesting parameters are the pulse rise time, peak current, total energy content, and the maximum derivative of the current.

Based on simulation and measurements with short metal pins, the shorter a pin is the faster is the rise time and the shorter is the pulse. At the same time, the peak current and total discharge energy decreases with the same charging voltage. However, here a charge distribution on the charged object can affect results and the maximum ESD current derivative and rise time depends, for example, on the initial voltage, total inductance, and discharge current waveform reflections along the discharge path. This is visible in Table 1 where the discharge current ringing affects the results. It is out of the scope of this paper to analyze what shape of charged object would provide the fastest ESD pulses.

These pins are designed to be 50 Ω transmission lines, and with a 39 mm long pin it is possible to see similar current waveforms as found in a TLP testing [3]. So, the pin is acting like a charged 50 Ω transmission line and gives rectangular discharge pulses, but now lasting about 400 picoseconds.

Figure 13 shows also that measurement uncertainties with the shortest 14.3 mm long pin are higher due to the ringing in the current measurements and bandwidth limitations of the measurement setup. In addition, it was challenging to repeat the ESD event with 100 V charge level. A varying air spark channel resistance increases measurement variation with above 500 V test level.

Table 1: Typical measured discharge current parameters for the two signal pins with two charging voltages.

	di/dt [A/s]	$di/dt/V_{charge}$ [A/s]	Rise time [ps]	Peak [A]
100 V, 14.3 mm	27	0.27	32	1.0
100 V, 39 mm	18	0.18	34	0.76
500 V, 14.3 mm	114	0.23	33	4.6
500 V, 39 mm	170	0.35	32	7.0

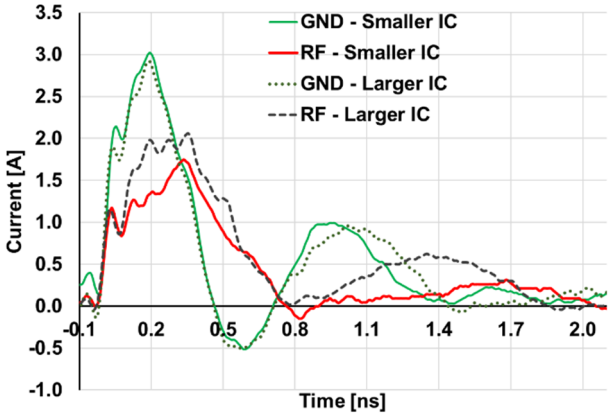

Figure 11: RF BGA CDM discharges with 110 V.

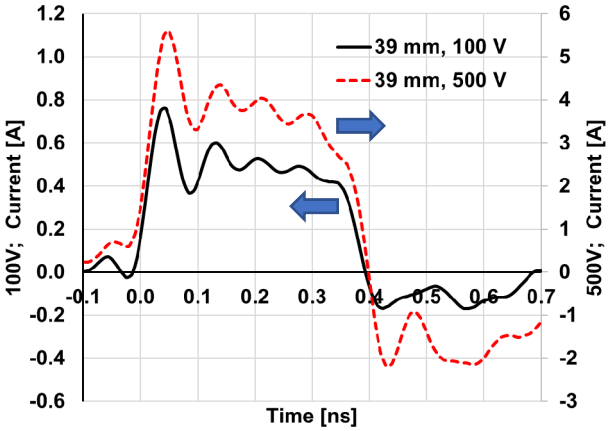

Figure 12: Measured discharges from a 39 mm long signal pin.

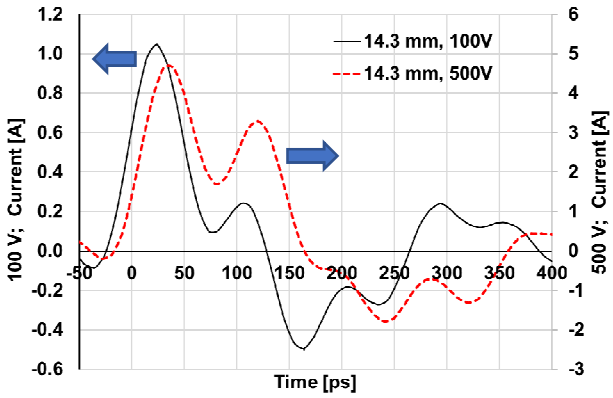

Figure 13: Measured discharges from a 14.3 mm long signal pin.

2. PCB trace effect

PCB traces increase electrical signal losses for higher frequencies, and therefore, high speed signal traces inside a PCB are typically kept as short as possible. In addition, the signal, or more commonly, a signal pair may have a good impedance matching only around the designed operation frequency range. This affects the transient signal coupling through the PCB, and transients with similar main oscillation frequency may have minimal attenuation and reflections.

Trace attenuation is studied in Figure 14 which presents measured discharge current waveforms from a charged 33.5 mm long metal pin. The RF pin alone is the original discharge from a standalone pin and the two additional waveforms show pulses visible at the RF pin input after it has travelled through the PCB trace. In this case, about half of the energy of the original ESD pulse is available at the RF pin input. As predicted based on simulations, the 85 mm long trace attenuates the pulse more than the shorter 35 mm long trace. Similarly, a well-matched trace has relatively small effect on the pulse rise time, thus, it is possible to get fast rise time ESD pulses through the PCB traces. The rise time can be even below 30 ps with small discharge source capacitances and can be several times faster than the measured values on ICs in a CDM qualification.

The maximum current derivative per the set charging voltage decreases with the decreasing trace length. However, the current derivative can be just about 25 % smaller with the trace than when measuring discharges from a charged pin directly. Therefore, a charged small size metal pin can be a serious ESD risk for sensitive RF I/Os even there is a trace between the IC and discharge point. Observed discharge parameters are summarized in Table 2.

Measurements results show slightly faster pulse rise time values than estimated based on the simulations when the current waveform travels through the PCB trace. Here one unknown parameter is the higher initial voltage level with ESD events. VNA S-parameter measurements and theoretical simulations base on small-signals and may underestimate high frequency and high voltage signal propagation through a PCB board. This topic is left for further research.

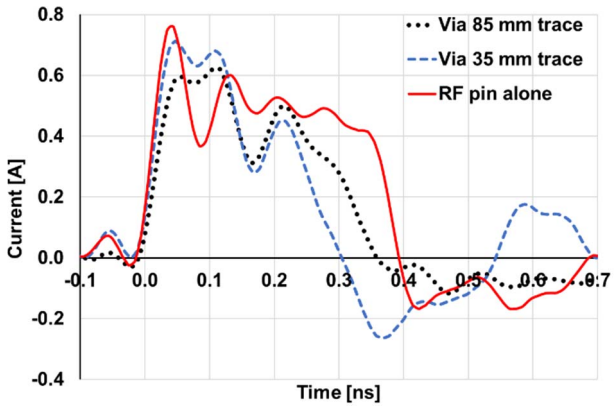

Figure 14: Pin discharges via two different length of PCB traces and a direct discharge from the charged pin.

Table 2: Discharge current parameters from a 100 V charged pin via two different trace lengths and a direct pin discharge.

	di/dt [A/s]	$di/dt/V_{charge}$ [A/s]	Rise time [ps]	Peak [A]
Pin alone	18	0.18	34	0.76
Via 35 mm trace	17	0.17	38	0.70
Via 85 mm trace	15	0.15	36	0.63

IV. Corrective Actions

A. Measurements in Process Area

It is challenging to control connector charges in manufacturing. Non-contact E-field or voltage meters cannot measure accurate potential values of single connector metal pins due to a large E-field averaging window. Contact voltage meters can measure potentials accurately, but the measured voltage may not be the same when the charged pin is placed on the PCB and the ESD event occurs. Here a capacitive coupling between the connector pin and PCB changes the voltage value before the pin touches the PCB surface.

The charge of the pin can be measured accurately with a contact charge meter, but once again, the charge value depends on the E-field and the level of polarization at the pin position. The measured charge value is accurate only when the pin has a static charge and an external E-field has been removed.

A metal pin with around 1 pF source capacitance and a less than 1 kV initial potential emits only a weak electromagnetic pulse when it discharges during assembly. Based on electromagnetic interference (EMI) measurements in manufacturing, the measured EMI pulse amplitudes are typically below or in the same range as the background electromagnetic noise from process equipment. EMI measurements can be used to detect ESD events when the sensor is placed next to the discharge point, but the EMI pulse must be synchronized to the ESD event by the user.

It is also possible to measure connector charges with discharge current measurements as shown in this paper. However, these require trained personnel, fast oscilloscopes and calibrated high frequency current probes. Therefore, the current measurement method is best suited for research purposes and failure threshold analysis.

The best way to try to control connector charging is to combine all available measurement methods. Here the contact voltage and charge measurement methods give the most accurate information for control purposes. Discharge current measurements can give more accurate information if the measured voltage and charge levels indicate increased ESD risks.

B. Prevention of Connector Charging

ESD risks due to charged connector pins can be prevented, for example, with the following methods:

a) neutralizing connectors with ionization before assembly,
b) shunting all metal pins together with a tool and grounding the tool during assembly,
c) changing the connector plastic material to more conductive with charge dissipation properties,
d) changing assembly order of components, and
e) verifying that package materials don't create excess surface charges on connectors.

These methods have their own limitations and benefits.

- Ionization can only partially neutralize charges of plastic connectors in an assembly phase. In addition, ionization cannot neutralize charges inside the connector assembly and ionization is slow to neutralize small size metal pins. On the other hand, ionization is typically easy to add into the assembly phase.
- Metal pins inside the connector can be shorted together with an additional tool during the assembly. However, this will add more work phases into the process, requires a specific tool for each connector type, and may also cause mechanical damages for fragile metal pins.
- Connectors can be made of dissipative plastic with a resistivity in the range of $10^{11} - 10^{12}$ Ω. This would limit surface charge build up during assembly. However, it is challenging to control resistivity of plastics in this range and high speed signal lines may not allow any conductivity with the plastics.
- Connectors can be assembled on to a second PCB, cable, or assembly at first, but this option may not be possible with most product designs.
- Most connectors are not ESD sensitive and trays and other packaging materials can be made of dielectric plastic. Dissipative packages can help with ESD control during assembly phase.

A high relative humidity is not an option to prevent ESD risks when there is only a few seconds time delay between the connector charging and assembly. For example, the connector can be charged by the operator hand touch just prior the assembly.

V. Conclusions

Electromechanical on-board connectors are made of plastic material and these connectors can get static charges measured in kilovolts during handling and assembly. Connectors have small size metal pins inside which can discharge on the PCB and initiate fast ESD events with current rise time around tens on picoseconds and current peak amplitudes several amperes. In comparison, IC packages have typically a higher source capacitance in CDM qualification, and the resulting rise time of the discharge current pulse is typically more than 100 ps and the peak currents are measured in several amperes. Therefore, due to the different ESD sources, discharges from small size charged metal parts can be much faster than the on-chip CDM protection devices can handle.

A PCB trace between the connector and the IC attenuates RF signals and ESD pulses. The ESD risk level is higher when the length of the PCB trace is kept short, which is typical for high speed on-board RF signal lines. Therefore, a PCB trace alone cannot protect ICs if charged connectors are assembled on the PCB, and specific precautions are required to detect and prevent these ESD risks with the emerging high-speed RF designs.

Contact voltage and charge measurements can detect charged connectors and metal pins, and discharge current measurements can be used for more detailed analysis. Simulations can predict the discharge waveforms and can be used to verify measurement results. However, there is no single easy way to neutralize charged connector components.

Metal pins can have static charges and induced potentials due to surface charges on dielectric plastic material. For example, ionization can only partially limit charge build up and shunting metal pins together during assembly makes the process more complicated. One additional way to limit charges on metal pins could be to use plastic materials with some charge dissipation properties. However, RF signals may require good dielectrics to maintain signal integrity targets.

VI. Acknowledgements

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References

[1] Gärtner R, Stadler W., Niemesheim J., Hilbricht O.,"Do Devices on PCBs Really See a Higher CDM-like ESD Risk? ", Paper 4B.3, EOS/ESD Symposium, 2014.

[2] Tamminen P., Smallwood J., Stadler W.," Charged device discharge measurement methods in electronics manufacturing", Paper 1B.4, EOS/ESD Symposium, 2017.

[3] Tamminen P., Smallwood J., Stadler W.," The main parameters affecting charged device discharge waveforms in a CDM qualification and manufacturing" Paper 4B.2, EOS/ESD Symposium, 2017.

[4] Maloney T., Khurana N., "Transmission Line Pulse Technique for Circuit Modeling and ESD phenomena", Proc. EOS/ESD Symp. 1985.