ESD protection structure enhancement against Latch-Up issue using TCAD Simulation

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Abstract – During IO qualification's LUP tests in CMOS28nm Bulk technology, undesired ESD structure triggering has been found to be the root cause of LUP fails. Deeper test analysis identifies the combination of IOs abutment sequence that generate the fail. The understanding of the phenomenon is investigated through a specific TCAD simulation set-up.

I. Introduction

Silicon Controlled Rectifier (SCR) is the main ESD protection which allows a high current sustainable in small silicon foot print area. This structure is fully compatible with local clamp protection in dedicated fail safe IO as I2C, LVDS or HDMI applications for example. But its low holding voltage makes it very sensitive to unexpected triggering during Latch-Up (LUP). A very compact 3V3 ESD protection for Analog IO has been developed based on SCR power device in CMOS28nm technology. During Latch-up qualification, it appears that SCR ESD protection turns-on during negative current injection on neighboring IOs. In this study, we propose to set-up a TCAD environment in the aim of understanding LUP phenomenon, but also giving some improvement and securing the layout design keeping same area footprint.

II. Protection description & Qualification Results

A. ESD Structure Description

At STMicroelectronics, we have developed a bidirectional device with a PWELL/N+ return diode directly integrated into a P+/NWELL/PWELL/N+ SCR. This device, call SCR Merged Diode, is already published in [1] and a 2D cross section is presented in Figure 1. This square device has the particularity to have further concentric rings which are from center to external:

- N+ Cathode of Diode (K_{Diode})
- P+ Anode of Diode and also P-gate of SCR (A_{Diode})
- N+ Cathode of SCR (K_{SCR})
- P+ Anode of SCR (A_{SCR})
- N+ N-gate of SCR (N-gate)

P-gate is thus shorted to K_{SCR} allowing a PWELL/N+ reverse diode. Furthermore, to reduce the turn-on voltage, this device is triggered thank its N-gate.

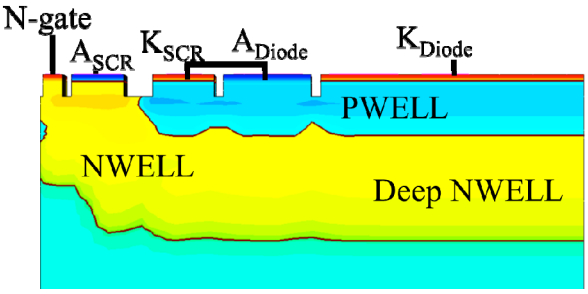


Figure 1: TCAD cross section of SCR merged Diode

To keep as much as possible its compactness, SCR Merged Diode is triggered through its N-gate thanks to two cascaded NMOS, both connected in BIMOS mode [2]. This BIMOS configuration allows a reduction of triggering voltage. The N-gate do not have any pull-up resistor during normal operation range to improve the transient triggering time during an ESD event. Furthermore, for a gain of area, NWELL (NW) isolation of the cascaded MOSFET has been merged with SCR N-gate. Figure 2-a) shows the implementation of the protection inside an IO frame. Figure 2-b) gives the schematic with SCR Merged Diode (SCR + return Diode), trigger circuit (cascaded BIMOS) and two parasitical diodes generated by the NWELL/Deep NWELL (DNW) isolation and both isolated PWELL (PW) from each

BIMOS. For an easiest integration, trigger circuit was localized beside SCR Merged Diode with the consequence of moving the power device from center to aside of IO frame. It is known that this SCR configuration, with its N-gate floating, has a high Latch-Up level sensitiveness. Consequently, the all structure is surrounded with N+/NWELL and P+/PWELL guard ring connected respectively to VDD and GND.

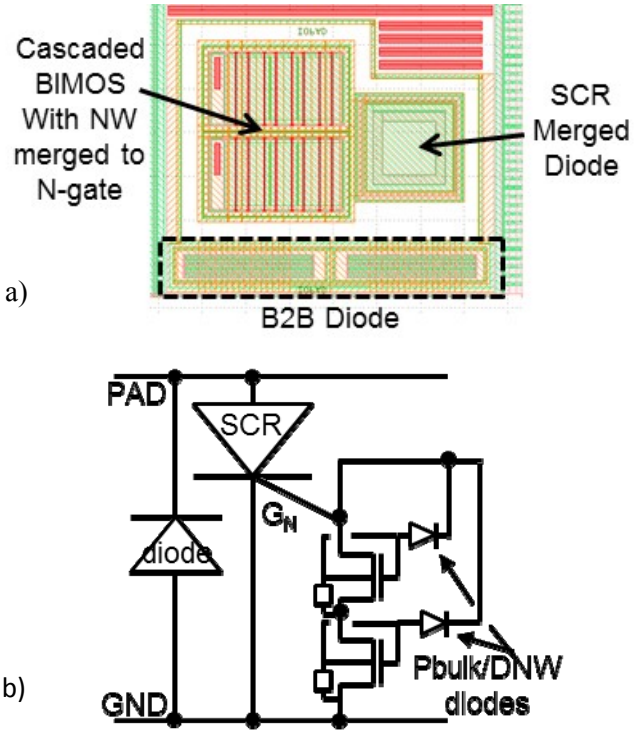


Figure 2: Layout (a) and schematic (b) of the Latching IO

B. ESD Qualification and simulation

This solution has been tested and qualified on silicon and gives a good performances by reaching 2kV HBM and 250V CDM.

Furthermore, other specific ESD TCAD simulations have been performed to show the behavior of the protection during an HBM event and also a TLP to get the characteristic points such as triggering voltage (V_{t1}) and on-resistance (R_{on}). Results are presented in Figure 3.

The HBM waveform (Figure 3-a) shows a double triggering with a first spike at 7.5V which corresponds to the cascaded BIMOS voltage triggering. Then SCR Merged Diode structure turns on and voltage drops until 3V, all current flows from Anode to Cathode.

This double triggering can also be seen on TLP simulation with a first BIMOS activations at around V_{t11}=3V. Then current flows through the Anode/N-gate until it reaches I_{t12}=100mA which is the triggering current of SCR Merged Diode. The voltage is then V_{t12}=5.5V. After, SCR turns on and discharges the ESD event through an on-resistance of R_{on}=0.25Ω. This resistance is particularly low since metallization and self-heating are not taking into account in this simulation.

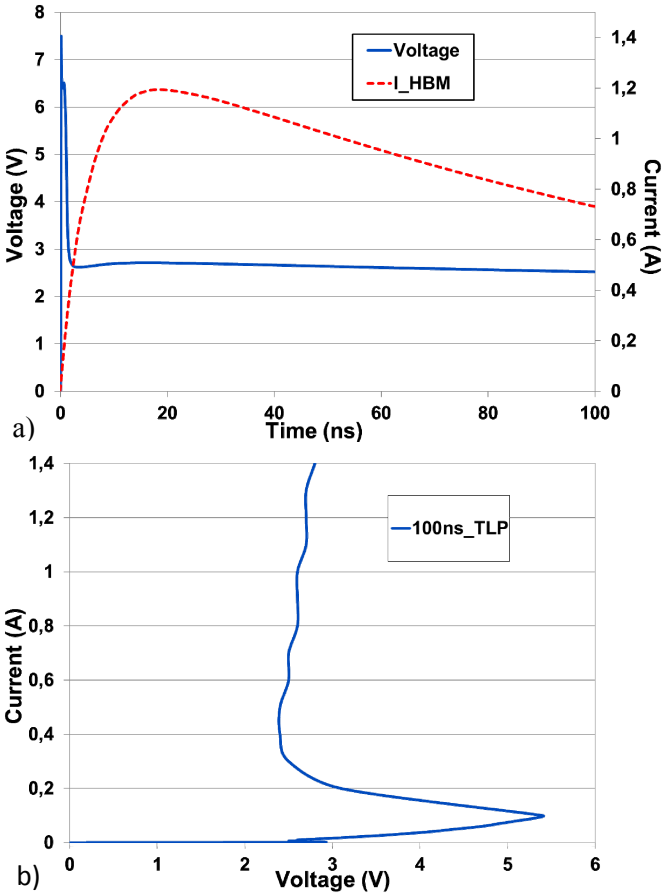


Figure 3: TCAD simulations of the ESD protection behavior during 2kV HBM (a) and 100ns TLP (b)

Good ESD behavior of SCR Merged Diode triggered with cascaded BIMOS has been demonstrated by measurements and TCAD simulations. Next part is dedicated to the understanding of Latch-up phenomenon, from its origin to its holding.

C. Latch-Up Qualification Results

Results of Latch-Up qualifications are given by Table 1. It appears one failing test condition. This particular condition consists of a pre-conditioning of all IOs (victims) in logic-high (3.6V) state while performing negative current injection on IOs (Standard, with classical diodes network or fail-safe IOs, with SCR Merged Diode solution) (aggressors). This LUP fail is reproduced whatever VDD state: powered ON or OFF. Deeper tests analysis isolate the critical configuration where aggressor IO is next by (victim)

3v3 analog IO described earlier. Current is sank from 3v3 IO to GND. Failure Analysis technics shows a high current flowing into SCR Merged Diode proving that it is triggered after LUP injection.

stress type	Preconditioning	Pad type	Trigger stress	result	Localization
Over Voltage	logic high/low	Power Supply	5.4V	No LU	
Current Injection	logic high/low	3V3 IO	+200 mA	No LU	
	logic low	3V3 IO	-200 mA	No LU	
	logic high	3V3 IO	-200 mA	LU < 100mA	IOs aside

Table 1: Table showing Latch-Up qualification results

Whatever the injecting/aggressor IO (standard or fail-safe), a reverse N+/PWELL diode between PAD (IO) and GND is integrated for ESD reason (cf. Figure2). During negative injection, voltage at aggressor's PAD becomes negative and lower than GND. The reverse diode goes in on-state and injects current into the substrate. This test is applied until -200mA or -0.5*VDD (around -1.8V) is reached.

Latch-up phenomenon study is able only if substrate is taken into account [3]. A good mean to simulate it, is to use a TCAD simulator which considers all physical devices available at silicon level [4] [5]. In this work, TCAD simulations were carried out using the same setup than the electrical qualification. The goal was to understand the root cause, to study qualitatively the physical phenomenon and finally to give some way to improve the design robustness of IO against this kind of event without enlarging the protection area.

III. Latch-Up Propagation

A. TCAD Cross Section

In this work, Latch-Up is an undesired consequence of two IOs interaction during the IC operating mode. The consequence is a false triggering of SCR which has a holding voltage much lower than IO supply voltage and leads to a holding phenomenon. Furthermore, the injected current needed for Latch-Up is also strongly linked to the silicon environment around SCR. So, for a better mimic of the phenomenon, the TCAD structure must be as much as possible similar to what it is really implemented on the silicon. Figure 4 represents the physical IOs implementation (a) with its A-B TCAD cross-section (b).

In the TCAD view, injector is an N+/PWELL diode embedded in the ESD structure. Also, the NW isolation of BIMOS is merged to SCR NW isolation which is also its N-gate. The P+/substrate (Psub) and N+/NWELL guard ring are not taking into account at this stage. This simplifies the TCAD structure for an easier and better understanding of Latch-Up propagation phenomenon. This configuration is a worst case in comparison to the failing silicon configuration since substrate is floating. BIMOS topology is also not exactly the same since it has been adapted to have both NMOS on the same 2-D cross-section and avoiding 3-D simulations which are a lot more time consuming.

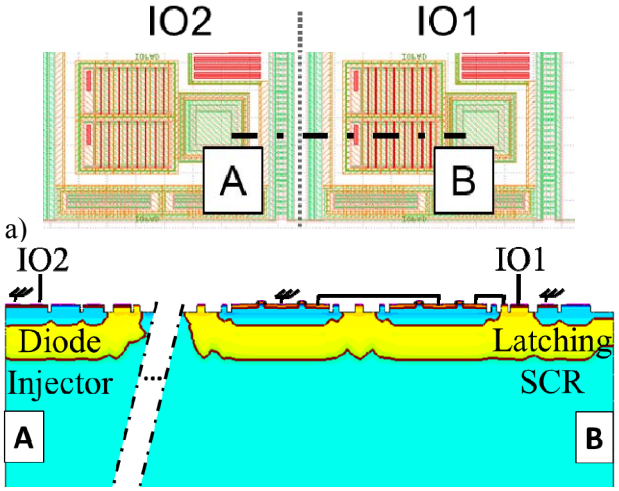


Figure 4 : Physical implementation a) with its simplified TCAD cross-section b)

B. Latch-Up Propagation

During the qualification, the latching configuration is reached by following different electrical steps. First of all, voltage of the victim IO (IO1) beside aggressor IO (IO2) increases until 3.6V with a slow rise time (1us) as shown in blue solid line in Figure 5 (step 1).

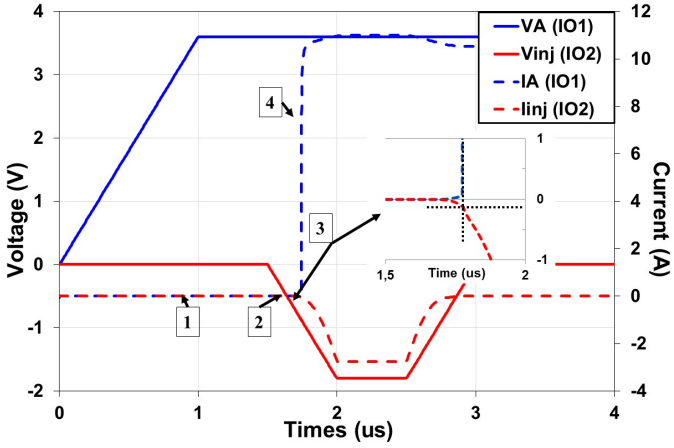


Figure 5 : Electrical simulation reproducing Latch-Up phenomenon in 4 states

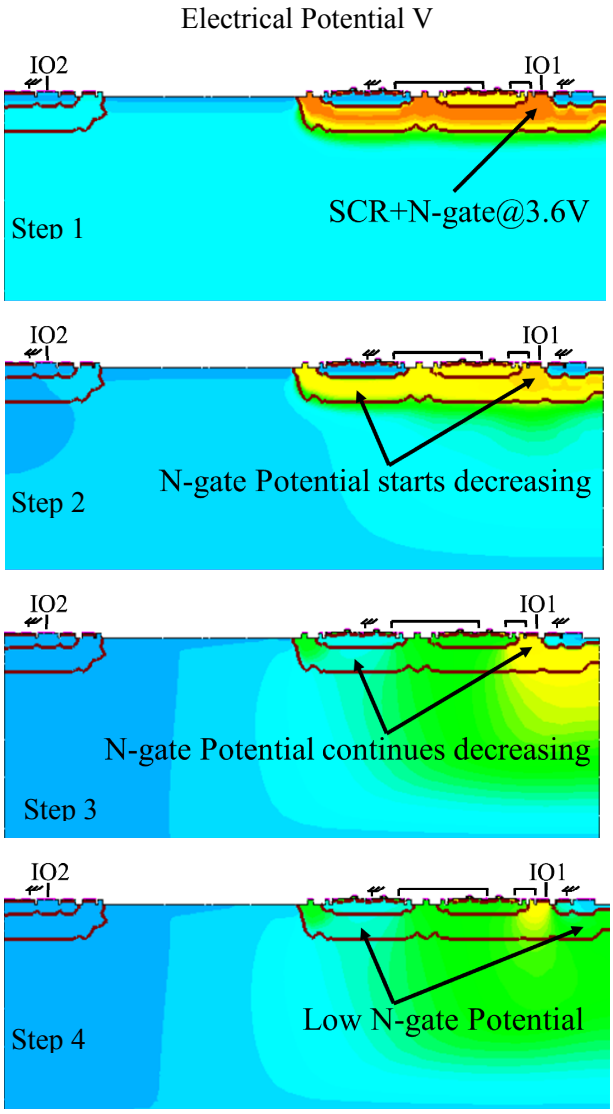


Figure 6 : electrical potential TCAD extraction showing Latch-Up propagation phenomenon

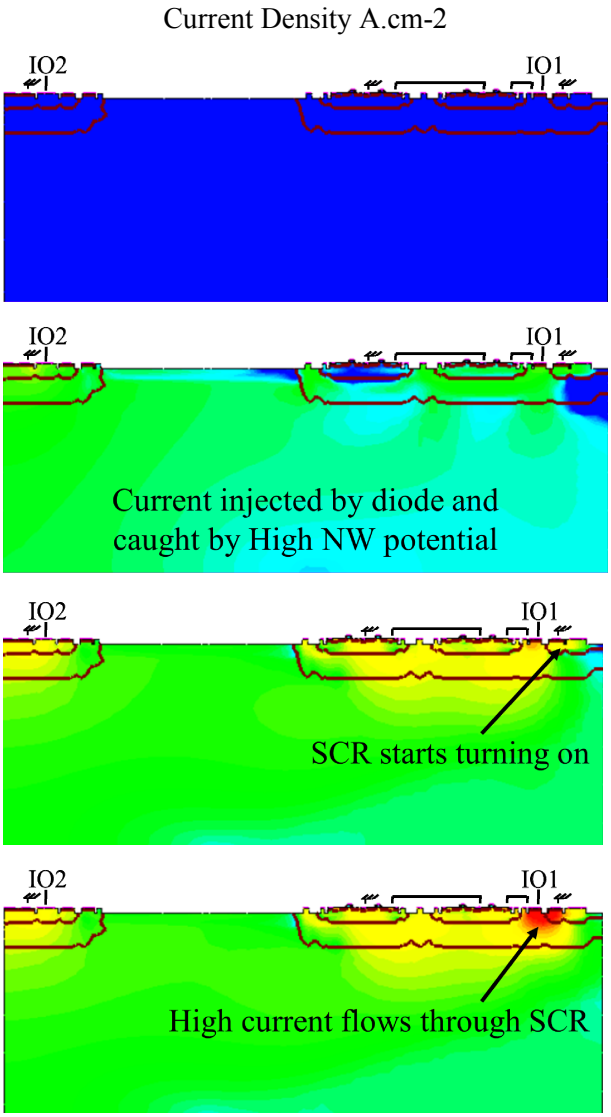


Figure 7 : current density TCAD extraction showing Latch-Up propagation phenomenon

Then a negative voltage injection is applied on IO2 until -1.8V with the same dV/dt (red solid line, step 2). Following the drop voltage, the current inside IO2 decreases (red dot line) with the consequence of generating a current consumption from IO1 (blue dot line). The generated currents are unrealistically high and reach I_{IO2}=-3A and I_{IO1}=11A. The explanation comes from further external parameters such as: the compliance of the tester (around 200mA) or internal parameters as self-heating (which increases the ON resistance) which are not taking into account on purpose. There are two main advantages of keeping the high currents: first of all, self-heating simulation by solving hot carrier temperature of electron and hole is time-consuming. This is not adapted for fast layout optimization compatible with IO roadmap development. Then it allows also an easier analysis of the efficiency of the studied solutions.

In this study, the Latch-Up starting point (step 3) has been defined when current inside the IO1 (blue dot line) breaks the continuity with a jump of several amps (step 4). The maximum current injection before Latching is carried over the IO2 current (red dot line) at the Latch-Up starting point time. The value is around 30mA and is below the measurement value (between 70mA and 100mA). This difference is due to the fact that the guard rings have been removed for the simulation and substrate is floating.

Figures 6 and 7 present the electrical potential and the current density TCAD extractions at four different steps (from 1-4 in Figure 5) of Latch-Up propagation. They are described below:

Step 1: First, the voltage of IO1 increases slowly until 3.6V, Anode and N-gate of SCR is quite at the

same potential, all silicon and junctions are well polarized. There is not injection of current.

Step 2: Then, the voltage of IO2 starts decreasing, and generates some current through reverse diode (left device). A part of this current is injected into the substrate and collected by high NW potential which is also SCR N-gate. It leads to a drop voltage of NW.

Step 3: IO2 voltage continues decreasing, generating more and more current inside the substrate which is caught by SCR N-gate. Then, NWELL potential decreases and PNP bipolar of SCR starts to conduct.

Step 4: SCR turns on and a high current flows from its Anode to its Cathode. SCR is in latching mode.

IV. Design Improvement Investigation

The Latch-up phenomenon has been demonstrated and understood in the previous part, the goal now is to improve design to avoid this false triggering.

A. Trigger Circuit Isolation

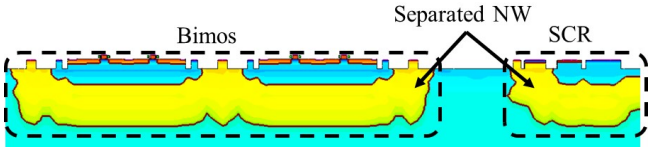


Figure 8 : Cross section of SCR with unmerged trigger BIMOS

The first investigation is focused on the triggering circuit (BIMOS) which is directly merged with SCR N-gate. This merged has for consequence to enlarge the collector N-gate area. To reduce this area, trigger circuit isolation (NW) is unmerged from N-gate as seen in Figure 8.

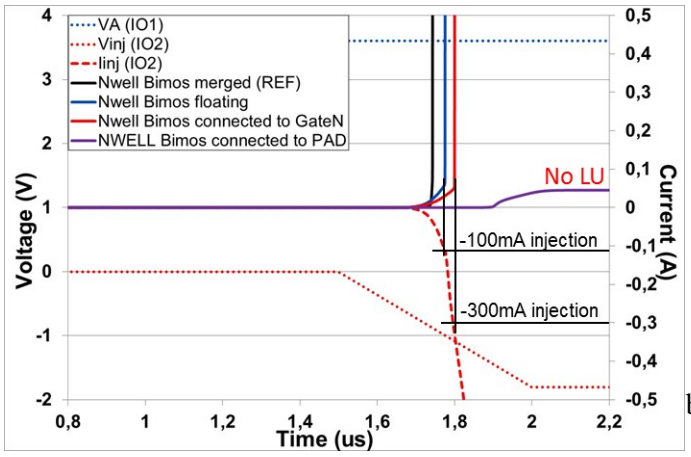


Figure 9 : Latch-up simulation with different NWELL trigger circuit (BIMOS) connections

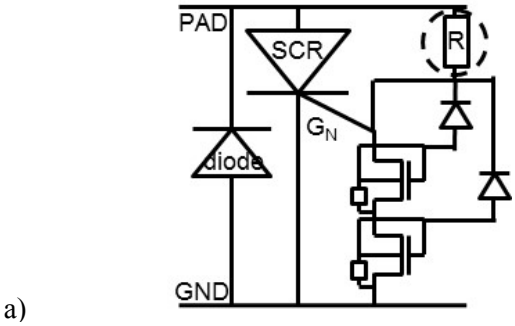
Figures 9 and table 2 present different NW surrounding BIMOS connections and their efficiencies.

In each case, the injecting current needed for Latch-up triggering is higher than the reference (SCR with merged trigger BIMOS). Furthermore, when NW is connected to PAD (IO1), Latch-up disappears. This connection makes NW to be a very good collector when structure is a victim. But in opposite it becomes a very good aggressor with high current injection into substrate. This trade-off can be mitigated by adding a resistor R between NW and PAD.

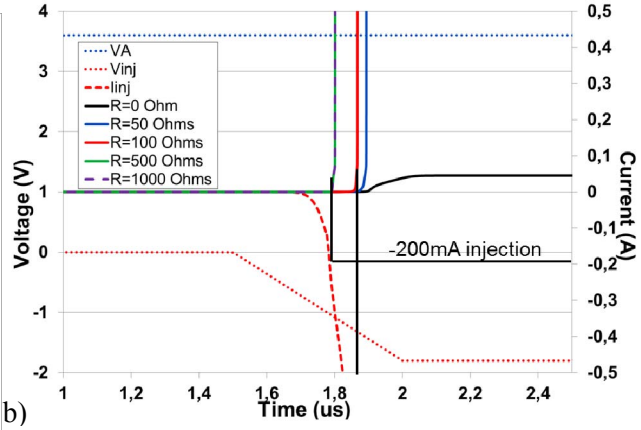
Nwell Bimos merged (ref)	≈ 30mA
Nwell Bimos floating	≈ 100mA
Nwell Bimos connected to N-gate	≈ 300mA
Nwell Bimos connected to IO1	No LU

Table2 : Table showing the efficiency of NWELL connection

Further Latch-Up simulations have been performed by adding a resistor from 0 to 1000Ω. The schematic is represented in Figure 10-a). The impact analysis of the resistance on the capability of BIMOS NWELL isolation to catch the carrier injected into the substrate is given by Figure 10-b).



a)



b)

Figure 10 : Schematic showing the resistance in series with the isolated NWELL of the BIMOS in a) and the result of simulation with different values in b)

Connecting the NWELL to the PAD is always better than letting it floating. Indeed, even if for 1kΩ the

injecting current needed is around 200mA before latching whereas it is only 100mA when NWELL is floating. At 500Ω, the resistance is not enough efficient. The value has to drop until 100Ω and 50Ω to see a huge impact (respectively equal to 700mA and 1A current injection).

At STMicroelectronics, the maximal current injection allowed through IO is 200mA. Also, the selected resistance can be 50Ω and 100Ω. For a gain of area in the new integration of the protection, we will add 50Ω resistance in series with the isolated NWELL of the BIMOS trigger circuit. This isolation will play the same role as classical NW guard ring.

The following part is dedicated of the study of the localization of specific substrate and NWELL guard ring to have the best efficiency.

B. Substrate and NWELL Guard Ring Connection

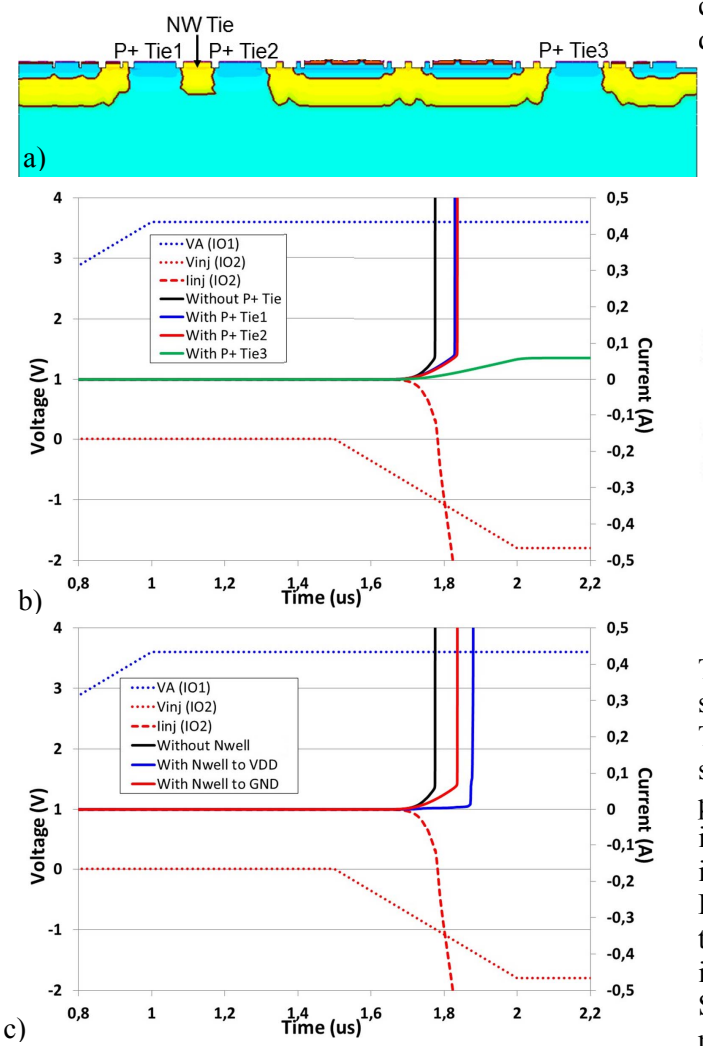


Figure 11 : New design implementation (a) showing the efficiency of P+ substrate connections (b) and NW Guard ring (c)

To enhance a design against Latch-up, different guard ring are implemented. The goal is to define the main guidelines. Figure 11-a) presents an updated layout of ESD protection with different P+/substrate (P+ Tie) and NWELL (NW Tie) guard ring connection. Simulation in Figure 11-b) is a TCAD comparison of different P+ Tie efficiency. It clearly shows that a well-grounded connection around SCR is strongly recommended to avoid an electrical potential increase. Furthermore, adding P+ tie everywhere is still better than keeping floating substrate since Latch-up occurs after 500mA instead of 100mA current injection.

The same study has been done for NWELL ring which is designed to be compliant with design rules manufacturing. This NW is always connected to VDD during normal operation mode. But sometime, for fail safe mode application, this NWELL can be grounded. In both case, simulations show in Figure 11-c) that adding a connected NW guard ring decreases the current injection sensitivity and allow a safer SCR design.

V. New Implementation & Experimental Results

A. Layout Implementation

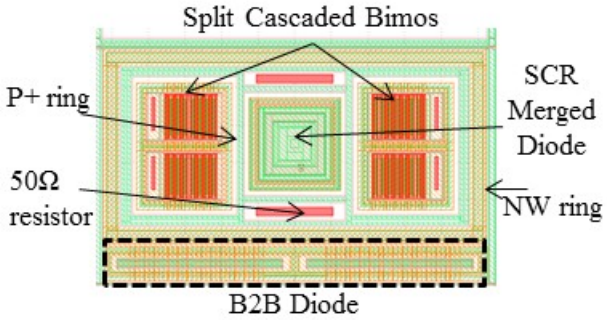


Figure 12 : New layout optimization keeping same silicon footprint

Taking into account of the different rules given in this study, layout of ESD protection has been redesigned. The goal is to keep the same silicon area footprint to stay with the same IO width. To reach the Latch-up performances, BIMOS trigger circuit is now separated in two parts at both side of SCR. Its isolated NWELL is unmerged to N-gate. This NWELL is connected to PAD through a 50Ω resistor. It plays the same role than guard ring and collects the injected carrier. The impact Psub strap is better as closer as possible to SCR in order to have a very good substrate polarization. Finally, NW ring is added all around the protection and connected to VDD. To stay inside the dedicated area, the BIMOS trigger circuit is adapted

by decreasing the un-silicide width of each MOS and the number of fingers. The new layout is presented in Figure 12

B. Impact on ESD performances

Before sending this new solution on silicon, some simulations have been performed to de-risk the ESD IO qualification. Figure 13 presents the behavior during HBM and TLP stresses. Both responses are compare to the old integration for an easier analysis. It is clearly demonstrated that the impact on HBM event is minim at 2kV. For TLP, V_{t12} increases slightly around 0.5V. It can easily be explained by the fact that between first V_{t11} and the second triggering V_{t12}, the driving path is Anode/N-gate of SCR (which is the same before and after) and the cascaded BIMOS which has a reduced finger number. So the total BIMOS width is lower in the fixed layout, the on-resistance increases. As SCR triggering current I_{t12}=100mA is the same the V_{t12} increases. This overvoltage is not enough significant to reduce the global ESD performances. Then both curves match perfectly meaning that SCR drives all the current.

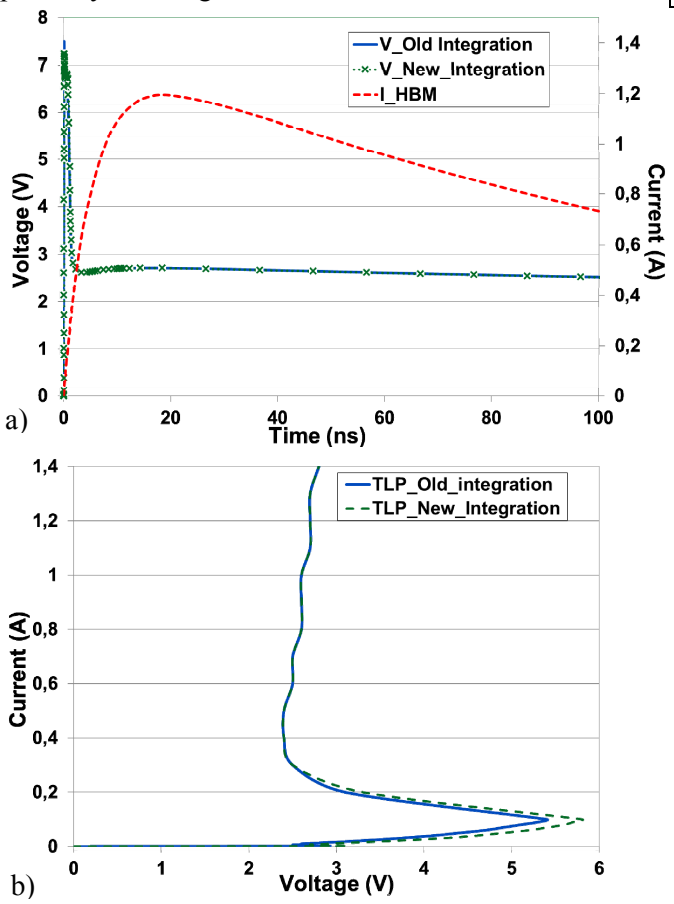


Figure 13: TCAD simulations comparison of the ESD protection behavior during 2kV HBM (a) and 100ns TLP (b) before and after layout optimization

This new layout implementation gives satisfaction on ESD and Latch-Up and has been embedded on silicon for qualification.

This solution has been tested and qualified on silicon and gives a good performances by reaching 2kV HBM and 250V CDM.

ESD tests have been performed and show the same robustness before and after modification which are 2kV HBM and 250V CDM.

C. Latch-Up validation

The final latch-up qualification, including Overvoltage and Current injection checks for logic high and low, passes successfully. Results are reported in Table 3.

Kind of stress	Preconditioning	Pad type	Trigger stress	result	Localization
Over Voltage	logic high/low	Power Supply	5.4V	No LU	
Current Injection	logic high/low	3V3 IO	+200 mA	No LU	
	logic high/low	3V3 IO	-200 mA	No LU	

Table 3 : New Latch-up qualification of fixed IO

VI. Prospective solution

Thanks to earlier proposed TCAD LUP study methodology, it is possible to deeply study various LUP immunity improvements. The so called van Zanten guard ring [6] can be an elegant solution since no additional implant would be necessary with the actual design. Indeed, van Zanten guard ring consists in two opposite type guard rings shorted together. (Figure 14). A simple metal fix would allow to reconfigure the original guard ring design in van Zanten guard rings. Would such low cost redesign would be efficient?

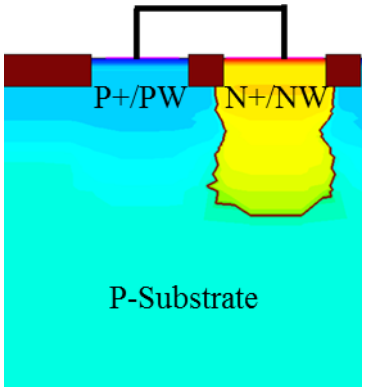


Figure 14 : Van Zanten guard ring 2D cross section

Similar TCAD simulations, as described earlier in this article, have been performed with classical guard ring solution or with van Zanten guard ring configuration In Classical Guard ring (GR) configuration, NWELL and Psub are connected to GND as in a Fail Safe pre-conditioning. As already shown in Figure 14, van Zanten GR are shorted together and let floating (NWELL and Psub shorted). Using exactly the same biasing sequence, allows to benchmark both strategies. We clearly observe a significant improvement of the LUP immunity with van Zanten GR, as presented on Figure 15. Nevertheless, LUP is still occurring but for a higher injected current. With classical GR configuration the SCR structure is triggered for an injected current of around 40mA since for van Zanten GR configuration 70mA is necessary to trigger it. It is then possible to have a deeper understanding of this improvement since TCAD tools allow a visualization of physical parameters inside the structure. As shown in the Figure 16, before LUP occurs, electric field and current conduction is different in both cases. Due to van Zanten GR connection, the current collected by NWELL is re-injected into substrate modifying local electric field (below the NWELL) preventing electron substrate conduction. As shown in Figure 15, N-gate of SCR (NWBIMOS) is pull down later than for classical GR delaying LUP.

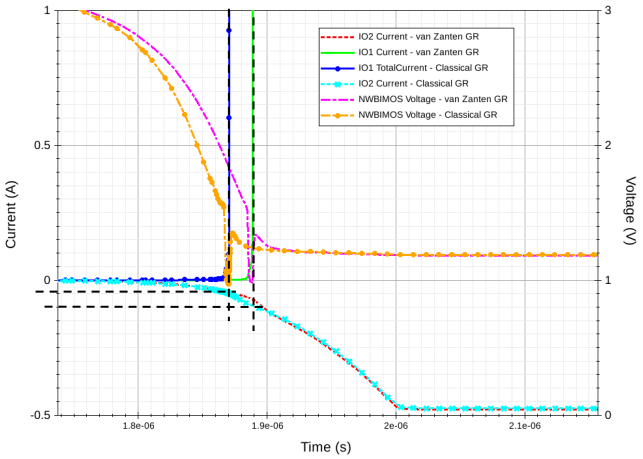


Figure 15: Impact of Van Zanten guard ring configuration on LUP immunity

Thanks to the proposed TCAD LUP methodology, we clearly shown that with a simple metal fix, LUP immunity can be improved by doubling negative injection necessary to generate LUP of the ESD structure. Other configuration using DNW for N type Van Zanten GR can be imagine in order to improve even further the LUP immunity and tuned with TCAD simulations.

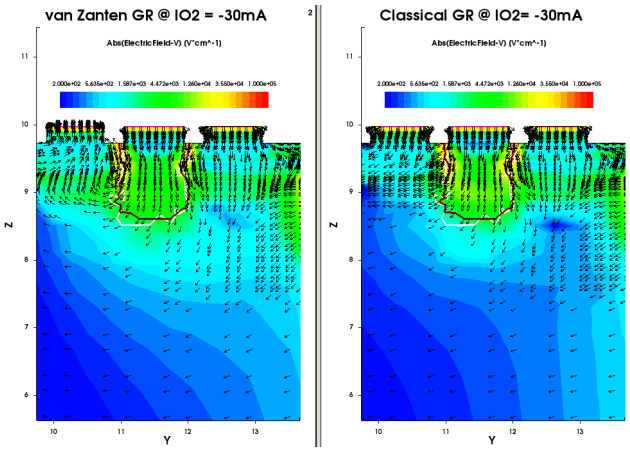


Figure 16: Current and electric field for both configuration: van Zanten GR (left) or classical grounded GR (right) @ IO2 = -30mA

VII. Conclusion

After discovering an undesired latch-up inside compact 3V3 IO due to false SCR triggering, a dedicated TCAD methodology has been put in place. This paper explores various ways to optimize and enhance a layout using TCAD simulation in 28nm CMOS technology. After a clear understanding of the phenomenon, showing the drop voltage of SCR N-gate due to carrier collection, simulations show a real benefit to unmerged the trigger circuit from SCR. It is proven that the NWELL isolation of cascaded BIMOS can be a very efficient collector when it is connected to PAD. But at the opposite, it can be a dangerous aggressor for the other contribution. A tradeoff has been studied with the addition of 50Ω resistance in series. Then substrate connection simulations have been proposed and highlight that it is not necessary to have a good potential control everywhere but only in strategic area such as SCR Merged Diode structure's surrounding. All those results are implemented with the same silicon footprint to enhance the 3V3 IO against Latch-up and keep it compact. Before manufacturing the fixed layout on silicon, TCAD simulations de-risking have been performed to mimic HBM and TLP stresses. The result shows a slightly impact on ESD behavior and can be considered as negligible.

As anticipated, the final qualification shows the same ESD robustness of 2kV HBM and 250V CDM without any latch-up risk.

Acknowledgements

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