A novel, SCR-based, distributed power supply ESD network for advanced CMOS technologies

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Abstract - In this work, a novel, Dual-Diode ESD cell with Embedded Lateral SCR between power supplies is presented (DDELSCR). The triggering voltage of the DDELSCR is remotely modulated through the triggering circuit of the Power Supply ESD cell. A highly area-efficient distributed SCR ESD Network is demonstrated.

I. Introduction

In advanced bulk CMOS technologies, traditional snapback-based nMOS protections progressively drifted out of mainstream ESD networks since the inception of 65nm technology node, where the combination of newly introduced low-power requirements together with the increased leakage of nMOS (caused by both gate and drain/body tunneling currents) rendered them unable to fulfill basic ESD transparency requirements to normal operating conditions [1]. On I/O-based designs, Dual-Diode I/O ESD cells in combination with Active FET-based Power Supply ESD cells gained more popularity [2]. To mitigate one of the fundamental limitations of such approach (bus resistance, rendering the approach less and less effective, as the Power Supply ESD cell is placed further from the Dual-Diode I/O ESD cell), a power-supply distributed approach was introduced [3], whereby smaller versions of the Power Supply ESD cells were embedded into each Dual-Diode I/O ESD cell (and triggered by the same triggering circuit).

To mitigate the other intrinsic limitation of the approach (the fairly limited maximum current capability of MOS devices), architectural schemes to disconnect Drain and Gate terminals of the clamping devices to over-drive the gates of the MOS embedded into the Dual-Diode ESD I/O cell, were devised [4]. Still, the effectiveness of MOS conduction mode in dissipating ESD energy is fairly limited, compared to the intrinsic limit of Silicon.

On the other side of the spectrum, relatively small Silicon Controlled Rectifiers (SCRs) for local ESD protection, without the need to rely upon a discharge on the power supply line, were introduced. The utilization of an external triggering network setting the triggering voltage (V_{T1}) of the SCR, obsoleted the need to rely upon any internal breakdown mechanism (see, for instance, the Diode-Triggered SCR, [5]) to trigger the device.

The primary goal of this work is to devise a novel structure and a related integration scheme that would take advantage of the best features that two aforementioned approaches have to offer: current distribution, lowest possible triggering voltage, minimum theoretical ESD network area, and fail-safe compatibility. This should lead to minimum impact in terms of buffer protection, both under HBM and CDM conditions (i.e. ballasting resistance, secondary ESD clamps).

II. Novel Structure Description (DDELSCR)

It is well known that the Lateral SCR (LSCR) triggering voltage (V_{T1}) can be easily modulated by the injection of either holes into the substrate (LNPN triggering) or electrons into the Nwell (PNPN triggering). When the injection of either carrier's type equals or exceeds the amount of carriers generated by impact ionization of the Nwell-Pwell breakdown at the triggering point, junction breakdown is no longer needed to trigger either parasitic bipolar and, hence, the LSCR.

Besides the LSCR's V_{T1} reduction, another significant advantage of injecting current in either parasitic bipolar base, consists in the LSCR turn-on time reduction. This method was specifically exploited in [6]. In this work we take further the notion of SCR external triggering injection, by creating a novel structure, amenable to be easily embedded into a standard Dual-Diode ESD I/O

cell, as well as being triggered by remote triggering circuits, to form a very effective distributed network. The work presented in this manuscript is performed in a standard dual-well, 65nm CMOS bulk technology (1.1V-1.8V). However, the concept can be straightforwardly applied to any technology with dual or triple well, with similar characteristics. The new structure devised, called Dual-Diode with Embedded Lateral SCR (DDELSCR), is depicted in Figure 1.

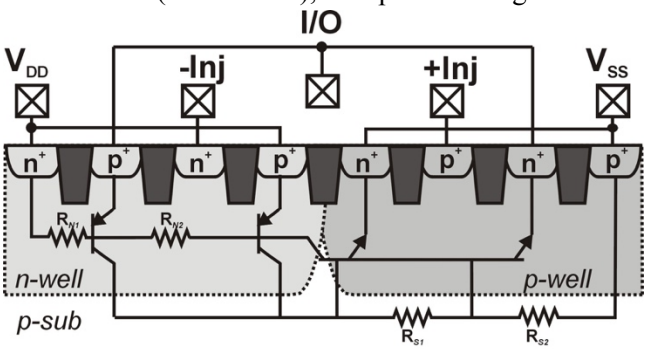

Figure 1: Cross-section of the novel SCR structure embedded into a standard Dual-Diode design (DDELSCR). Note that there are actually two parasitic SCR's, one from V_{DD} to V_{SS}, and one from I/O to V_{SS}. The former is what is being relied on in the proposed approach, whereas the latter is never active, in that Anode and Cathode are at the same potential (I/O).

As one can see, the starting point is the standard Dual-Diode ESD I/O cell (P+ in Nwell diode connected between I/O and V_{DD}, N+ in Pwell diode connected between V_{SS} and I/O). An additional Anode (P+) in Nwell (connected to V_{DD}) and an additional Cathode (N+) in Pwell (connected to V_{SS}) are introduced, thereby forming:

1. A LSCR between V_{DD} and V_{SS}, whose triggering voltage is set by the Nwell-Pwell breakdown
2. An additional SCR between I/O and V_{SS}. Since Anode (P+) and Cathode (N+) are shorted, this SCR is not active, in that an extremely high current would be needed to reverse NPN base-emitter polarity

Furthermore, additional majority carrier injectors (P+ in Pwell, N+ in Nwell) are introduced to modulate triggering voltage.

The equivalent DDELSCR schematic is shown in Figure 2. The negative injector is removed, as it will not be used in this work. As shown in [6], it is worth highlighting that negative injection for triggering can be used as well.

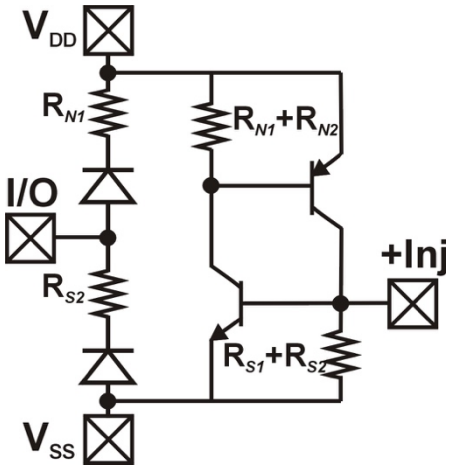

Figure 2: Equivalent schematic of DDELSCR embedded in the structure depicted in Figure 1. The diodes on the left are the standard diodes from a signal Dual-Diode cell. The parasitic resistance associated to these diodes (R_{N1}, R_{S2}) is reported in that it does contribute to the overall R_{SUB} and R_{NWELL} of the LSCR that is being relied on with this approach.

The base layers layout implementation of the DDELSCR with W=40µm is fairly trivial and it is reported in Figure 3. Please note that the device as shown is non-optimized from a form-factor perspective. Optimization of the DDELSCR from both performance and form-factor perspective will be presented ahead.

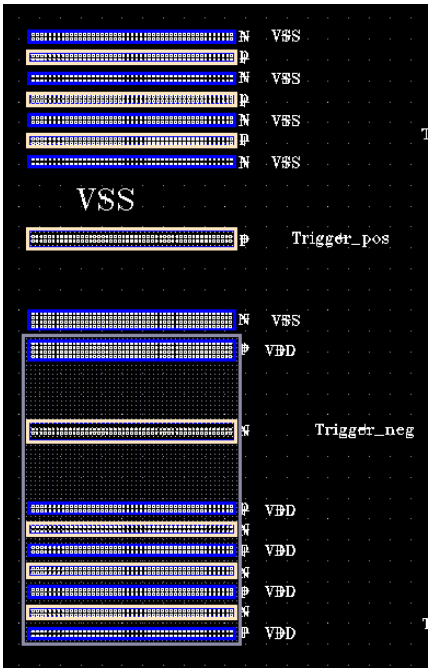

Figure 3: Layout implementation of the DDELSCR. The structure investigated is not optimized from a form-factor perspective, but it is meant to provide a proof of concept of the approach.

III. DDELSCR Characterization

High-current TLP (100ns) characteristic of DDELSCR between V_{DD} and V_{SS} is shown in Figure 4. The typical LSCR behavior is observed, with Nwell-Pwell breakdown setting triggering voltage (V_{T1}~11.5V) and holding voltage of around 2V. As it can be seen, LSCR scales as expected with respect to width, with an I_{T2}=50mA/µm. These figures are pretty much in line with what reported in literature and are to be expected.

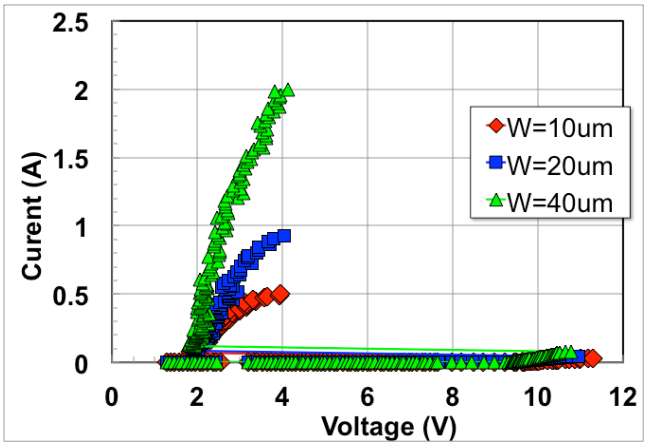

Figure 4: High-current TLP (100ns) characteristic of **VDD vs VSS**. Behavior is typical for an LSCR, with Nwell-Pwell breakdown setting triggering voltage (V_{T1}~11.5V).

Next, we focus on the TLP characteristic of the DDELSCR between I/O and V_{SS}. As shown in Figure 5, the triggering voltage V_{T1} is increase by 1V and the failure voltage V_{T2} is increase by about 2V. Therefore, high-current behavior is consistent with LSCR (Figure 4) plus high-side diode, thereby confirming the correctness of the schematic shown in Figure 2. Note that a 40µm-wide structure is able to clamp the voltage at the I/O at ~4V for 2KV HBM stress.

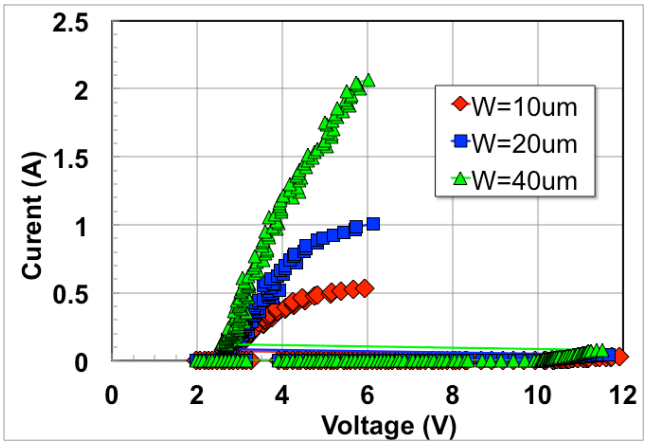

Figure 5: High-current TLP (100ns) characteristic of I/O vs VSS. Behavior is typical for an LSCR + High-side diode, thereby confirming the correctness of the schematic shown in Figure 2.

It has to be noted that the high-side diode failure current is about 30mA/µm, making it the limiting factor in the overall ESD robustness (i.e. its perimeter needs to be increased through multi-fingers).

The LSCR high-current characteristics vs injected current into the base of the LNPN are investigated next. Both DC and transient current injection (Figure 6) are considered. For transient injection, we used a simple RC-triggering circuit, similar to that used to turn on typical RC-triggered Power Supply ESD cell [6].

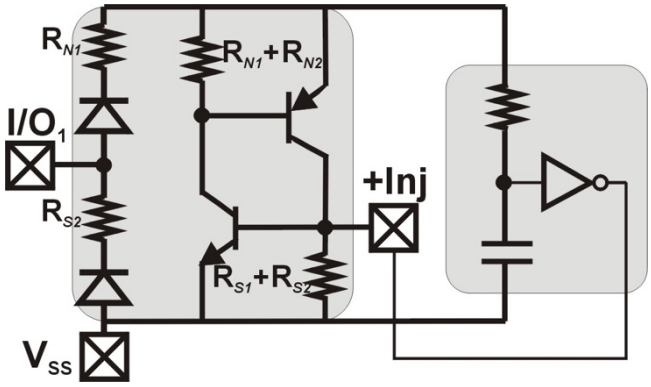

Figure 6: Simple RC triggering circuit used to transiently inject current into the base of the DDELSCR [6].

Figure 7 depicts the results of the aforementioned characterization. At 800µA/µm of DC current, the device goes immediately into SCR mode, without the need for Nwell-Pwell breakdown to generate majority carriers to trigger the LSCR. Same results can be obtained through RC triggering: the critical current to trigger the SCR needs to be provided for the turn-on time of the SCR itself, which is roughly 500-700ps for the structure investigated (more on this ahead).

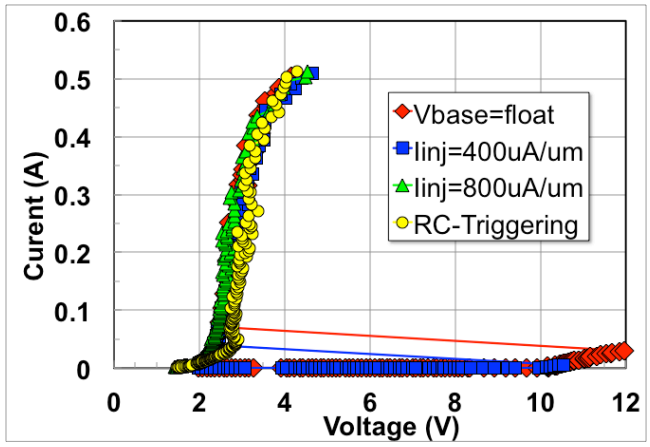

Figure 7: High-current TLP (100ns) characteristic of **V_{DD} vs V_{SS} vs Iinj** for W=10µm structure. With an injected current of Iinj=800µA/µm, the device goes smoothly into SCR conduction mode, without the need for Nwell-Pwell breakdown.

As long as the RC time constant of the RC trigger exceeds DDELSCR turn-on time and the minimum

triggering current provided, the device goes directly into SCR conduction mode, without the need for Nwell-Pwell breakdown. The 4V clamping voltage at 2KV HBM of the 40µm-wide structure, combined with RC-triggering, make the DDELSCR suitable to protect the most fragile devices in the technology (1.1V nMOS, which feature V_{T1}=4.8V and BV_{OX_100ns}=4.5V). VF-TLP characteristics (pulse width: 5nsec) for the RC-triggered DDELSCR are shown in Figure 8. It can be seen that the DDELSCR follows the expected Power scaling [7, 8] by exhibiting a factor 4 increase in failure current vs 100ns TLP, for the same on-resistance.

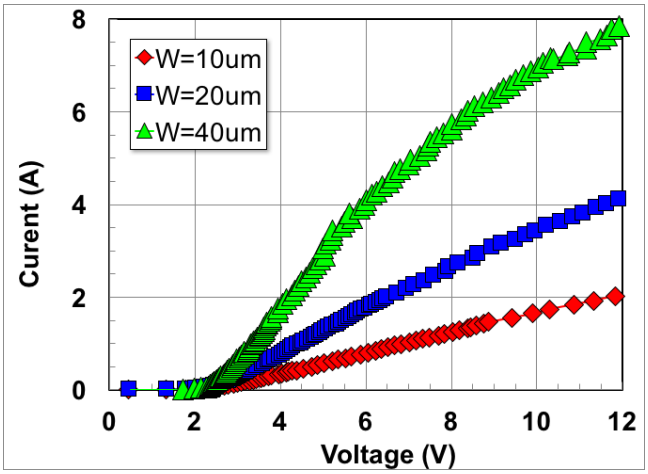

Figure 8: VF-TLP characteristics (pulse width: 5nsec) for the RC-triggered DDELSCR showing a factor 4 increase vs 100ns TLP) in failure current, for the same on-resistance

Transient voltage plots for an injected current of 1.5A for the same VF-TLP characterization as shown in Figure 8 are reported in Figure 9.

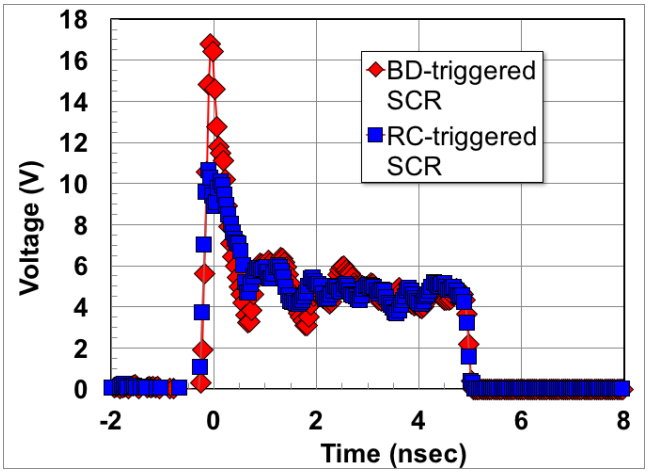

Figure 9: 5nsec VF-TLP BD-DDELSCR vs RC triggered DDELSCR

It can be seen that:

1. The amount of voltage overshoot is significantly reduced with RC-triggering scheme vs Breakdown-based approach (10V vs 17V). The voltage overshoot is a combination of both Nwell diode and LSCR overshoot. Neither structure is optimized the achieve the fastest turn-on time (more on this ahead).
2. Nevertheless, in terms of ability to protect thin gate oxides (BV_{OX_1ns}=11V) the critical voltage overshoot measured with RC-triggered DDELSCR is very close (10.5V). With an active power supply clamp implemented, the scenario will be identical to that occurring with any Dual-Diode ESD cell. It likely that a small, secondary CDM clamp (Dual-Diode + isolation resistor) may be needed.
3. It is well known that the amount of voltage overshoot is function of the square root of the current density [9]. Hence halving the current density (from 1.5A to 0.75A in the example shown), reduced the overshoot by roughly 30%, from 6V (delta between peak voltage and holding voltage) to 4V. It is then inferred that a distributed network of DDELSCR's, each one exercised at current densities well below their current failure, will also prove very advantageous in terms of overall voltage overshoot.

IV. DDELSCR Compact Modeling

In order to fully simulate the structure in Figure 1, a VerilogA model with the ability to modulate triggering voltage (V_{T1}) as function of injected substrate current was implemented. Figure 10 depicts a high-level representation of the model as well the triggering voltage of the DDELSCR vs the injected substrate current.

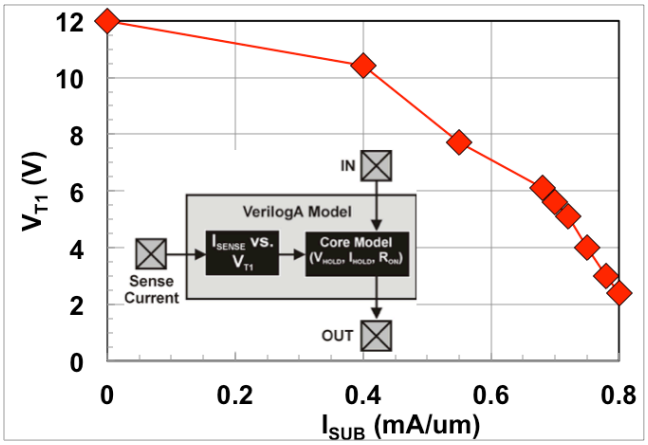

Figure 10: Modulation of SCR triggering voltage (V_{T1}) vs injected substrate current. In the inset, a high-level implementation scheme of the VerilogA model

In Figure 11, the current and voltage response of the aforementioned model for HBM=2KV vs triggering current is shown. The triggering voltage modulation (not inclusive of overshoot) vs external triggering

current is apparent. It can be seen that the external triggering current also modulates the time it takes to turn-on the SCR. In particular, for no injected current (i.e. purely breakdown-driven triggering), V_{T1} is reached at about 600ps, which is in good agreement with the characterization in Figure 9.

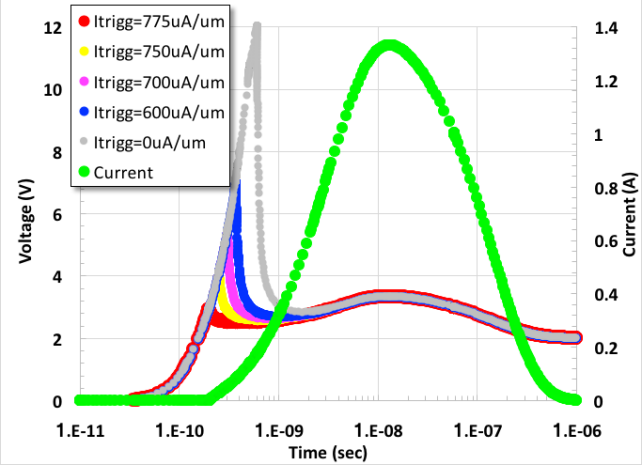

Figure 11: Current and voltage response of the developed VA model for HBM=2KV vs triggering current

V. DDELSCR Layout Considerations

1. R_{SUB}/R_{NWELL}

As mentioned in the Paragraph II, the layout shown in Figure 3 is not optimized from an area/performance standpoint. In particular, this specific implementation leads to a triggering current of 800µA/µm, which translates to 32mA of injection current needed to reduce the triggering voltage to the minimum holding voltage. The easiest way to modulate the triggering current is the modulation of parasitic substrate (R_{SUB}) and Nwell resistance (R_{NWELL}), by virtue of the inverse relationship between triggering current and R_{SUB} or R_{NWELL}. The caveat is that there must not be an impact on R_{S2} and R_{N1} (Dual-diodes series resistance), as this would obviously have a detrimental impact on the overall approach effectiveness. This can be achieved through partial Pwell blocking [10]: in this way, R_{S1} can be significantly increased with a small P_{SUB} area. Figure 12 shows a pictorial description of this option, which is "free" from a process cost standpoint. Analogously, R_{N2} can be increased with selected Nwell counter-doping, achieving similar results to the case of Pwell blocking.

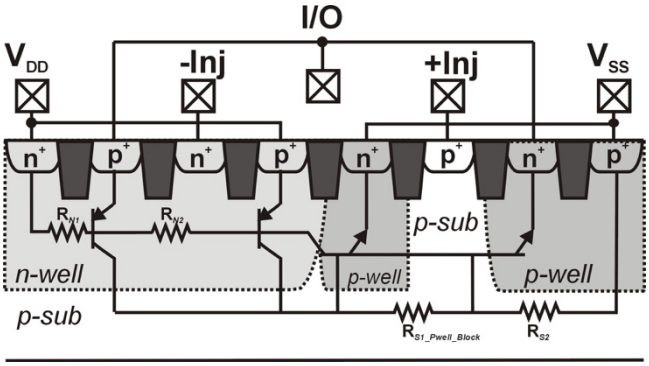

Figure 12: Pictorial representation of Pwell-block concept to increase effective substrate resistance of the lateral NPN in the DDELSCR

By applying the techniques above, a reduction up to a factor 20 is to be expected (leading to the need of the external triggering current of about 40µA/µm). This leads to a significant reduction overall of the buffer strength (and, hence, area) needed to drive the base(s) of the DDELSCR.

2. Turn-on time improvement

The DDELSCR construction shown in this work is fundamentally based on a combination of Lateral SCR and Nwell/Pwell diodes. While this construction is adequate to explain the concept, it is certainly not optimized to provide the fastest turn-on time. Modifications to both LSCR and Nwell/Pwell diodes can be easily made to achieve the aforementioned goal. For instance, Nwell/Pwell diodes can be replaced by Poly-defined diodes. LSCR Anode-Cathode isolation (STI) can be blocked to achieve similar results to Poly-defined diodes. The analysis of this modified structure is beyond the scope of the work. However, based on the large amount of literature at this regard, it should be a pretty straightforward implementation.

VI. Circuit Implementation

A DDELSCR network has been implemented in a bank of 16 I/O's, each with W=40µm, 100mΩ of resistance on both V_{DD} and V_{SS} rails between I/O's (Figure 13, Top). External triggering current has been chosen as 8mA (i.e. 200µA/µm) per I/O bank, as intermediate value between the non-optimized layout in Figure 3 and full-optimized layout after applying the R_{SUB}/R_{NWELL} increase techniques detailed in the previous Paragraph. Due to the high current capability of each I/O instance, the Power Supply ESD cell has been reduced to the sole triggering circuit (i.e. no active clamp is present, in that the total SCR network is 640µm). The triggering line from the Power Supply cell is very similar to that used for the standard Dual-

Diode distributed approach. For the sake of comparison, similar configuration but with traditional embedded MOS in Dual-Diode cells was created (Figure 13, Bottom). Embedded MOS width is 150µm (i.e. total distributed MOS width of 2,400µm). MOS are "over-driven", so the failure current would be around 1mA/µm, leading to an overall network capable of withstanding in excess of 2KV ESD stress. Triggering circuits are placed on either side of the I/O bank.

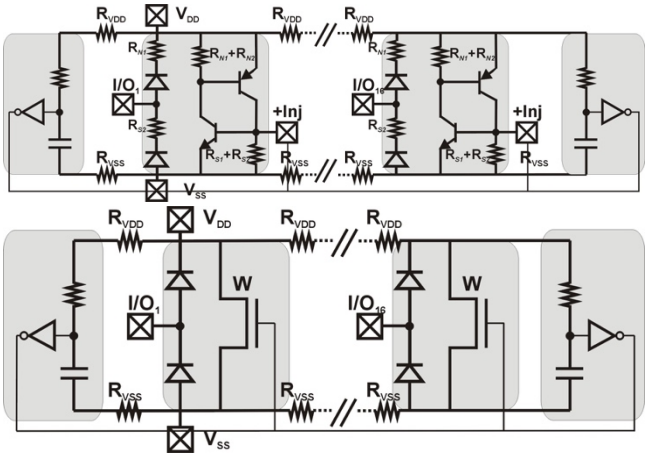

Figure 13: Test benches for the circuit verification. Top: 16 DDELSCR I/O ESD cells. Bottom: 16 Dual-Diodes I/O ESD cells with embedded a remotely triggered FET, with W=150um. No supply clamp is present, only triggering circuit.

In Figure 14, as reference point, the response to 2KV HBM stress between V_{DD} and V_{SS} on traditional Dual-Diodes with embedded remotely triggered FETs is shown. It can be seen that all FETs do contribute to sharing ESD current, from a minimum of 65mA to a maximum of 115mA. Peak voltage is limited to 2.3V.

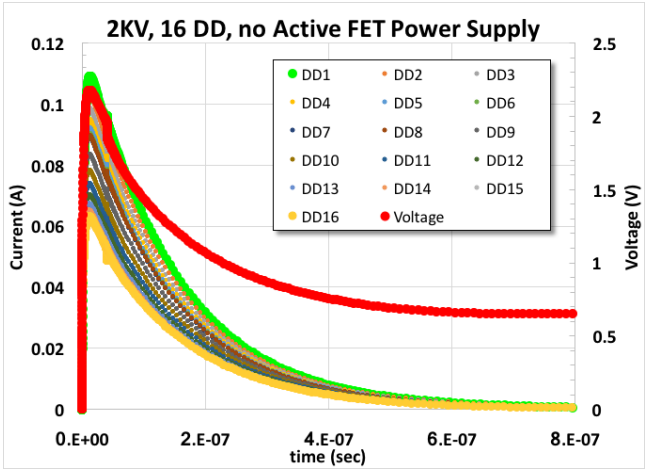

Figure 14: Transient response to 2KV HBM stress between V_{DD} and V_{SS} on the traditional Dual-Diodes with embedded remotely triggered FETs.

In Figure 15, the same 2KV HBM stress is applied to the DDELSCR network. It can be seen that only three DDELSCR's contribute to dissipate the entire ESD energy. This is caused by the fact that the simple triggering circuit chosen in this work (RC + Inverter), is not an ideal current source. The current actually delivered to the DDELSCR's is a function of the inverter output voltage, as well as of the parasitic V_{SS} bus resistance path of each DDELSCR to the ground pad. This resistance is simply a function of where the return path (i.e. the V_{SS} pad, in this case) is located. In summary, the DDELSCRs triggered first are those closest to the selected V_{SS} pad. Yet, due the significant efficiency in currently handling and voltage of each DDELSCR, the peak voltage is around 2.8V. Note that the triggering circuit generates around 130mA of current for about 40nsec. In reality, there is no need for the triggering circuit to generate this current for such long time: as previously mentioned, about 700psec is what is needed to trigger the DDELSCR directly into holding mode. This is the primary difference with a MOS-based approach, whereby the active FETs gates need to be held high for the entire duration of the HBM event (1-2µsec). More considerations at this regard will be discussed in the next Paragraph. Finally, the DDELSCR clamping voltage is set at the LSCR holding voltage, until the stress current reaches the LSCR triggering current, at which point the DDELSCR will shut off.

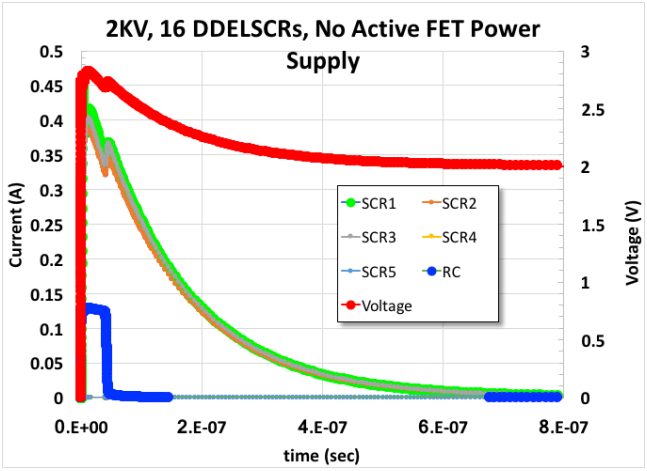

Figure 15: Transient response to 2KV HBM stress between V_{DD} and V_{SS} on the DDELSCR network.

In Figure 16, the transient response to 4KV HBM stress between V_{DD} and V_{SS} is applied to the DDELSCR network. The peak voltage is now 3.1V and still only six out of sixteen DDELSCRs are engaged to dissipate the ESD Energy (higher inverter output voltage vs 2KV HBM case). The DDELSCR that takes the most current carries about 560mA, which is much below the intrinsic limit of the structure (roughly 2A). Based on

the previous considerations, such current density will not yield any meaningful voltage overshoot.

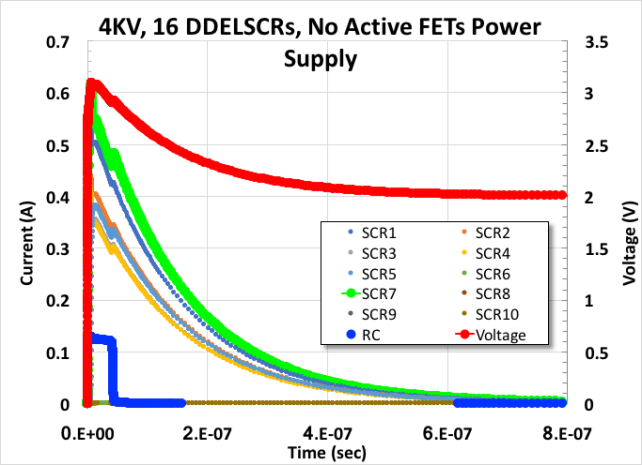

Figure 16: Transient response to 4KV HBM stress between VDD and VSS on the DDELSCR network.

Finally, in Figure 17, the transient response to 8KV HBM stress between V_{DD} and V_{SS} is applied to the DDELSCR network. The peak voltage is now 3.8V and still only eight out of sixteen DDELSCRs are engaged to dissipate the ESD energy. It is pretty obvious that the DDELSCR network is able to sustain a very significant amount of current, which can be conservatively estimated in 22A (35mA/µm in average for each I/O bank). This level of performance, together with the very limited footprint makes it very desirable for on-chip system-level protection.

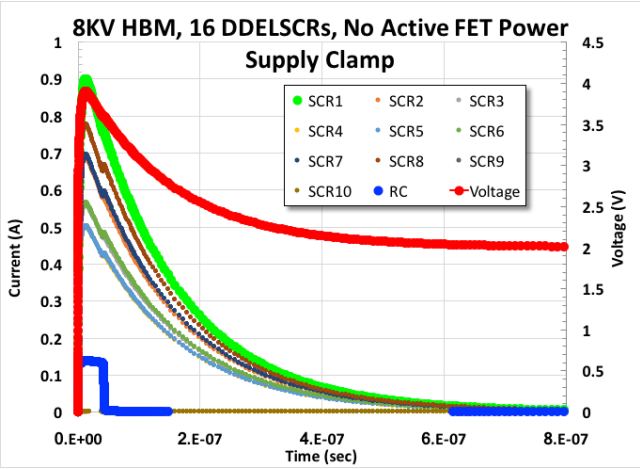

Figure 17: Transient response to 8KV HBM stress between VDD and VSS on the DDELSCR network.

VII. DDELSCR Network Optimization

1. Fail-Safe applications

Applications where no low-impedance path between I/O and Power Supply are allowed are quite problematic with Dual-Diode ESD cells. Using Dual-Diode with a simple dummy rail to an active FET is very penalizing in terms of area. With DDELSCR, this is not the case, due to the extremely limited footprint of this solution. As a matter of fact, the implementation shown in Figure 6 is already Fail-Safe by construction.

2. "False-triggering" considerations

There is no denying that having an SCR-based power supply network requires careful evaluation of the latchup risks under powered on conditions. At the same time, two considerations hold true:

1. It is very likely that there is some parasitic SCR between Power Supply at any given time
2. The DDELSCR's are OFF during most conditions. The only way to turn them on is through the injection of a current in excess of the triggering current.

For example, Figure 18 shows the response of the circuit in Figure 13-bottom to a voltage ramp from 0V to 2.5V, 2.75V and 3V under variable rise-times. For ramps from 0V to 2.5V, irrespectively of the rise-times, the DDELSCR will never trigger (current in the nA range), even if the power supply far exceeds the holding voltage of the DDELSCR (2V). This is simply caused by the fact that, irrespectively of the rise-time, the output voltage of the inverter in the triggering circuit never reaches a voltage high enough to generate a sufficient triggering current in the closest (i.e. with smallest V_{SS} parasitic resistance, leading to largest triggering current) DDELSCR. Notice also that 2.5V is well above the maximum operating voltage of this technology (2V), yielding a virtually latch-up free ESD network. If we further increase the voltage ramp from 0V to 2.75V, the scenario changes significantly.

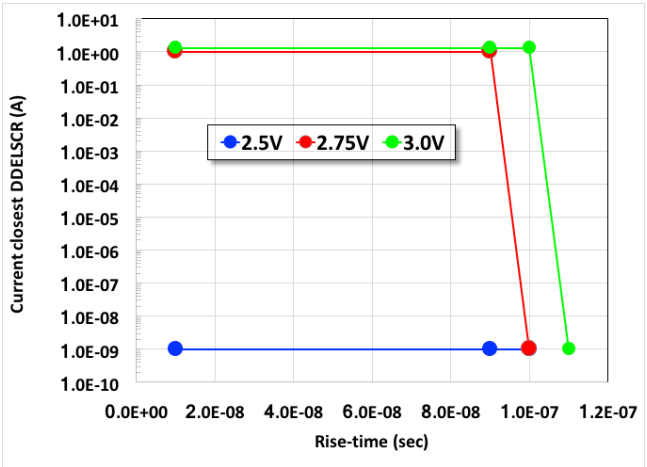

Figure 18: DDELSCR "false-triggering" sensitivity to rise-time as function of maximum ramp voltage. Note how the DDELSCR do not trigger for ramps from 0V to 2.5V, irrespectively of the rise-time.

As can be seen from Figure 18, closest DDELSCR triggers for any rise-time smaller than 90ns, yielding a current of ~1A, corresponding to a holding voltage of 2.75V. If, by exercise, we continue to increase the maximum ramp voltage, the "false-trigger" occurs at lower and lower rise-time (for instance, from Figure 18, 100ns for 3V ramp). The data presented is shown for nominal silicon at RT. However, similar analysis can be performed for all PVT corners needed.

In general, it is pretty clear that "false-triggering" characteristics of this approach can be modulated by either engineering DDELSCR's triggering current and/or triggering circuit strength.

3. Performance vs Area

From the analysis discussed above, it is clear that all critical design parameters can be accounted and the overall network optimized for performance vs area.

In particular, a low-current density in each DDELSCR is desirable for the minimization of triggering voltage overshoot. Furthermore, a relatively high triggering current is extremely desirable to minimize any risk of power-on "false-triggering". It is clear that both goals can be achieved with DDELSCR in multi-finger (2) configuration, and minimum Body-Cathode and Body-Anode spacing. This would yield a much more compact LSCR structure, compared to that shown in Figure 3: a good estimate would be around 40µmx30µm, leading to an overall DDELSCR I/O cell of about 40µmx90µm.

VIII. Conclusions

In this work, a novel, Dual-Diode ESD cell with Embedded Lateral SCR between power supplies was presented (DDELSCR). The triggering voltage of the DDELSCR is remotely modulated through the triggering circuit of the Power Supply ESD cell. A highly area-efficient distributed SCR ESD Network was demonstrated.

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