On-Chip Sensors to Measure Level of Transient Events

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Abstract – On-die circuits were developed to measure the size of transient electrical events experienced at I/O pads. The circuits allow an integrated circuit (IC) to determine the peak voltages across the electrostatic discharge diodes during the event. Experiments and simulations with a 90 nm test chip show the sensor can determine the peak magnitude of the transient event within 1 A for events larger than 0.7 A and duration longer than 1 ns.

I. Introduction

Developing and validating electronic systems that are robust against electrostatic discharge (ESD) is a major challenge, particularly given the shrinking size and growing complexity of electronic devices. Knowing the voltages or currents at IC pins during system-level ESD tests could dramatically reduce the time to test and debug these systems, but adding the instrumentation to measure these quantities is often infeasible. Furthermore, adding probes and cables may change the discharge path and other characteristics of the event. Better methods are needed to determine when, where, and with what magnitude transient distortions like ESD are affecting ICs.

On-die circuits have previously been proposed to determine the magnitude of transient events influencing an IC, primarily by measuring the fluctuation in the on-die power supply voltage. In [1], transients in the on-die power supply are coupled to the input of a static latch. The sample-and-hold circuit in [2] provides a similar measurement of power supply noise. While not explicitly designed to detect the magnitude of transient events, it is a possibility. A similar circuit in [3] determines the magnitude of power supply voltage over- or under-shoot. A major limitation of these circuits is that one cannot determine the size of the event at the I/O pad nor on which pad the event occurred. While circuits have been designed to determine the peak voltage at the pad [4-5], these circuits require careful measurement of the levels after the event using external equipment and may realistically only be used in the lab. The presence of an event can be detected using on-die fuses, as in [6], but the fact the fuse can only be used once limits its utility.

This paper introduces circuits that measure voltages across the ESD protection diodes during transient electrical events. A measure of the peak voltage is stored on a capacitor where it can be read by an on-die A/D converter after the event has passed. A look-up table can be used to convert this voltage to a measure of the peak event current through the protection diode. The level of the event is thus made available to the user or microprocessor. The proposed circuits were implemented in a 90 nm microcontroller test chip. Simulations and measurements demonstrate the ability of the circuits to accurately measure the peak transient current *in situ* for a variety of transient events and across process and temperature variations.

II. Level Sensors

The on-die transient level sensors were designed to be small, inexpensive, accurate over a wide range of transient events and process or temperature variations, to minimize leakage current, and to have minimal impact on normal operation of the I/O. Figs. 1 and 2 show conceptual schematics of the proposed level sensors. Fig. 1 shows the circuit for a positive level sensor, which senses the level of events where the pad voltage rises above VDD, and Fig. 2 shows the circuit for a negative level sensor, for when the pad voltage falls below VSS.

For the positive level sensor, an overstress voltage causing the pad to rise above VDD will cause current to flow through ESD protection diode A1. The gate-source voltage of M1 is equal to the voltage across the ESD protection diode. When the diode voltage is

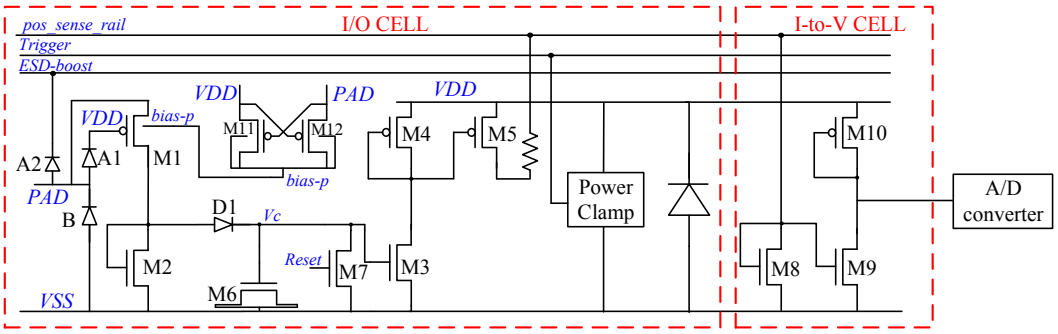

Figure 1. ESD protection network and positive level sensor circuitry

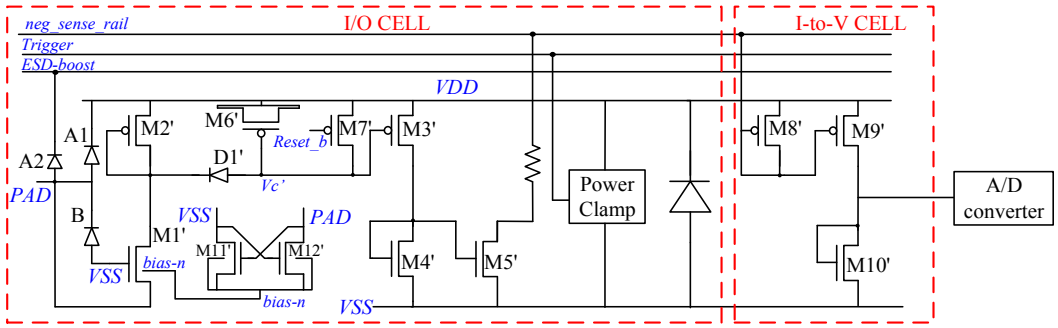

Figure 2. ESD protection network and negative level sensor circuitry

greater than the PMOS threshold voltage, M1 drives a current through M2 which is directly related to the diode voltage. This current produces a voltage drop across M2, which is stored on capacitor M6, minus a diode (D1) voltage drop. The diode D1 and capacitor M6 form a peak detector stage. The voltage on M6 drives current via M3 through a current mirror (M4, M5) and onto a sense rail ("pos_sense_rail") that is routed throughout the I/O ring, as will be shown later. The current on this rail returns to VSS through M8 at the IC's A/D converter and is mirrored to M9, where it is then converted to a voltage by M10. The output of the I-to-V converter (M8, M9, M10) is a voltage which can be mapped directly back to the voltage across diode A1 by accounting for the gain of the circuit through SPICE circuit simulations. A small series resistance is placed in series with the drain of M5 to prevent damage to MOSFETs M5 and M8 if they go into snapback during a transient disturbance of the power supply. This resistance is kept small to minimize its impact on the A/D converter reading.

The diode D1 allows the peak charge to remain on capacitor M6 for a relatively long time. This level can be read after the event has passed (e.g. many microseconds later, as will be shown later) and when the power supply voltage has fully recovered from potential distortion during a transient event. After reading the capacitor charge, the user can discharge capacitor M6 via M7 using a "Reset" control signal. M7 is a narrow width, long-channel device to minimize leakage off the storage capacitor M6. Diode D1 is made sufficiently large to allow fast charging of M6 and to minimize the impact of parasitic resistance. D1 is an N-type diode and is implemented in an isolated pwell.

An nwell biasing circuit (M11, M12) is required to prevent forward-biasing of the source-body junction of M1 during a stress event. Without this circuit, any resulting collector current from the parasitic lateral PNP of M1 may add to M1's MOSFET channel current and interfere with the intended circuit operation. The bias circuit shown in Fig. 1 switches the body of M1 to the larger of VDD or the pad voltage [7].

The negative level sensor in Fig. 2 works in much the same way as the positive level sensor. The negative level sensor measures the peak current through ESD protection diode B during a negative stress event on the pad. NMOSFETs M1', M11', and M12' are placed in an isolated pwell and biased to the lower of VSS or the pad voltage using the bias circuit formed by M11' and M12'. The peak voltage stored on capacitor M6' is sent to an I-to-V converter at the A/D through a current mirror connected to a negative sense rail ("neg_sense_rail") routed throughout the I/O ring.

To read the level sensors after an event, the IC must know when a transient stress event has occurred. A transient event detector is presented in [7] which

accomplishes this task. The event detector schematics are presented in Fig 3. During normal conditions, the output of the positive detector (Fig. 3a) is high and node A is low. During a positive event, the positive protection diode A1 turns on, applying a voltage across the gate-source of the sense MOSFET M11. For a voltage of sufficient size, M11 turns on, causing the voltage at node A to go high and for the latch circuit to change state so the output is low. Hence the detector circuit triggers and latches the presence of an event when the voltage across the ESD diode exceeds a threshold determined primarily by the sizes of M11 and M15. The negative detector (Fig. 3b) works in a similar manner, triggering when the voltage across the B protection diode exceeds a threshold determined primarily by M11' and M15'.

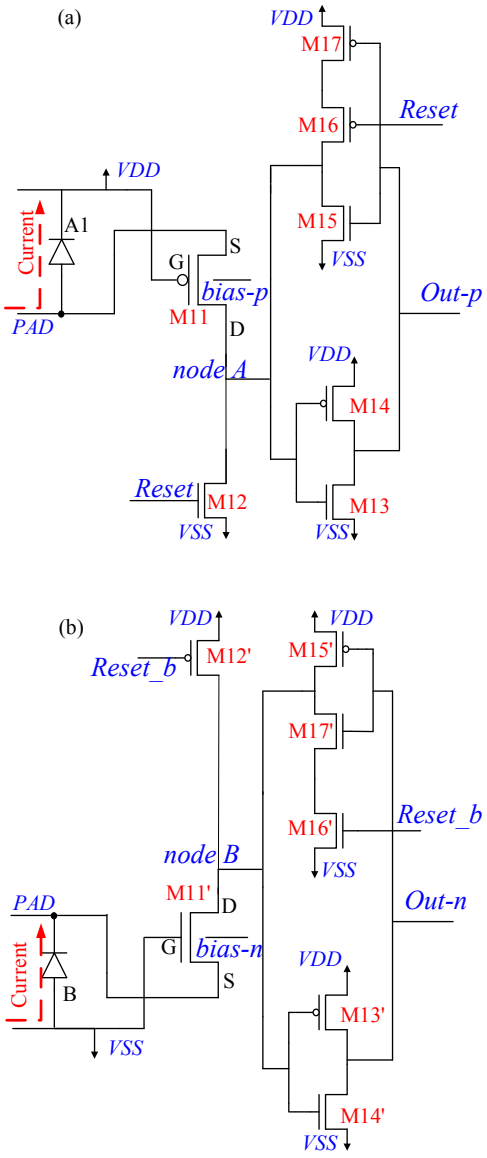

Figure 3. Schematic of (a) positive and (b) negative stress event detectors

The negative and positive event detectors and negative and positive level sensors are implemented in the I/O pads, as shown in Fig. 4. The output of each detector is routed to addressable registers in the IC core. A detected stress event triggers an interrupt, which reads these registers and the A/D converter to determine on which pin(s) the event has occurred and the magnitude of the event.

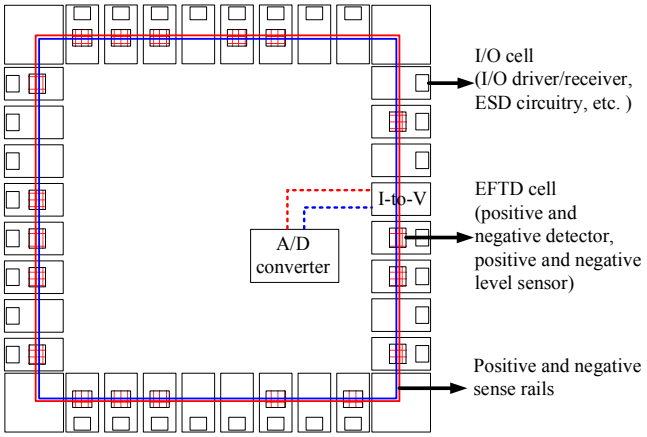

Figure 4. Placement of ESD detectors, level sensors, I-to-V converter, and sense rails

III. Simulations

A block diagram of the simulation setup is shown in Fig. 5. In addition to the ESD detector and level sensor circuits, the simulation included validated models of the on-board power delivery network, Electrically Fast Transient (EFT) source, IC package, and the ESD protection network.

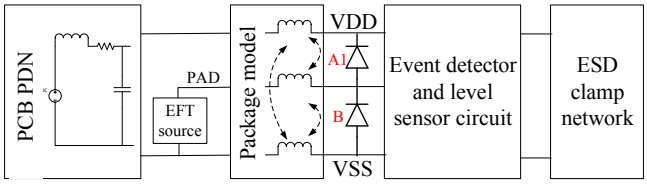

Figure 5. Block diagram of simulation model

The test-board power delivery network impedance was measured looking from a set of the IC power pins into the board and was modeled using lumped capacitors and transmission lines. Fig. 6 shows a comparison of the measured and modeled power delivery network impedance. The modeled impedance matched measurements within a few decibels up to 3 GHz, the upper frequency limit of anticipated transients.

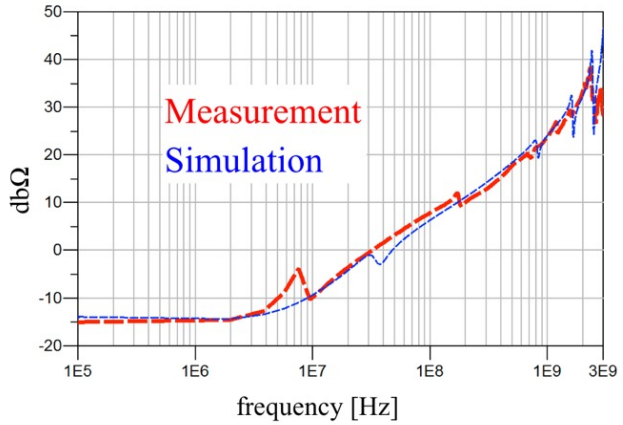

Figure 6. Comparison of measured and modeled PCB power bus impedance

The IC package model was developed using 3D electromagnetic simulations, and includes all parasitic self- and mutual-inductances and capacitances and parasitic resistances associated with the bond-wires and lead-frame.

The model for the ESD protection network includes the ESD diodes, power clamps and trigger cells, and on-die I/O power delivery network. The ESD diodes were characterized through wafer-level transmission line pulse (TLP) testing. SPICE models of the diodes were built to include thermal characteristics, as well as voltage overshoot [8]. Fig. 7 shows a comparison between the measured and modeled overshoot voltage across the A1 diode during a fast-transient event. Fig. 8 shows the simulated and measured transient response of the A1 diode for an 8 A TLP injection. The transient response shows the overshoot peak and the overshoot duration is modelled correctly. The simulated peak overshoot voltage matches the measured overshoot to within 200 mV.

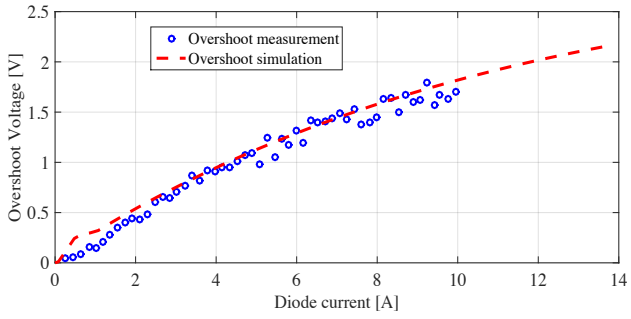

Figure 7. Comparison of measured and simulated ESD diode overshoot

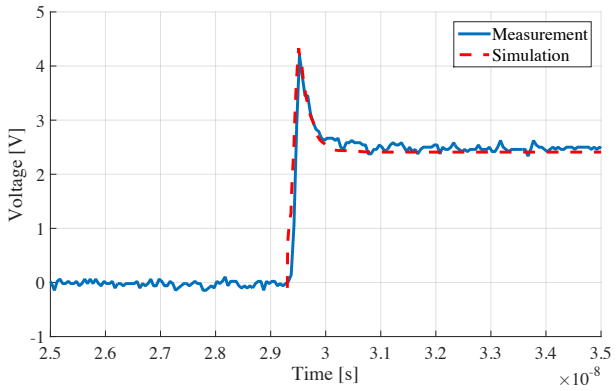

Figure 8. Comparison of measured and simulated transient overshoot voltage across the A1 ESD diode during an 8 A TLP injection

The ESD power clamps and the I/O power supply network determine the VDD/VSS voltage swing during a transient event. The protection network [9-11] includes a boost bus, distributed trigger circuits, and distributed power clamps. The rail clamps are designed for proportional triggering rather than strictly being "on" or "off", so that a collapsing power supply voltage can be prevented during a transient event [9]. The power clamp model also accounts for a snapback mode of the clamp MOSFET during strong events.

Initial simulations were performed using a TLP source. The stress was applied between an I/O pad and the board return plane (VSS), as indicated in Fig. 5. Fig. 9 shows the simulated diode current (injected current) during a 5 A, 20 ns TLP stress applied at time t=50 ns, the voltage stored on capacitor M6 (Vc-VSS), and the resulting impact on the local power supply voltage (VDD-VSS). A reset pulse is applied to M7 at time t=10 ns which removes any charge across the capacitor M6. The falling edge of the reset pulse, however, capacitively pulls additional charge from M6, resulting in a slight negative starting voltage across the capacitor as seen in Fig. 9. This negative voltage has no impact on the measurement. Fig. 10 shows simulated waveforms for a negative TLP stress event. In this figure the voltage across the capacitor is expressed as (VDD–Vc'). The waveforms show that the level sensors successfully retain a measure of the peak level of the transient event during and after the event.

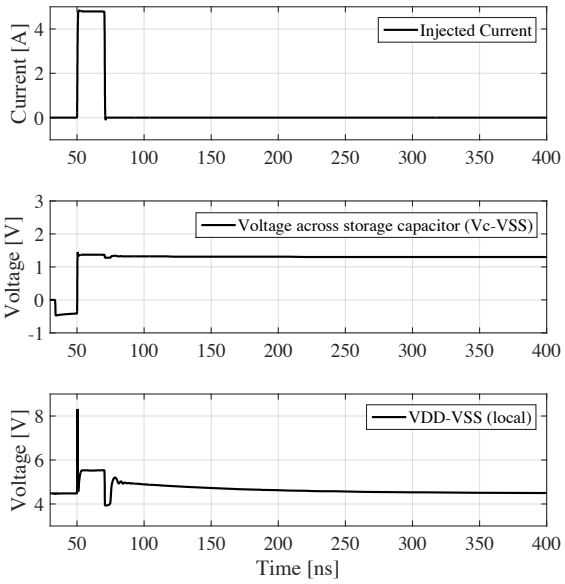

Figure 9. Simulated transient response during a positive 5 A TLP event

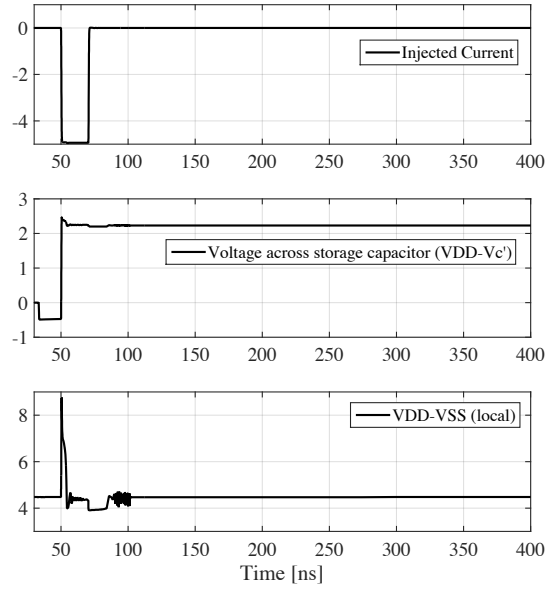

Figure 10. Simulated transient response during a negative 5 A TLP event

Simulations were also performed using a human metal model (HMM) source. The SPICE model generates a waveform as specified in IEC-61000-4-2. The ESD event was injected between the I/O pin and the board return plane (VSS) as indicated in Fig. 5. Fig. 11 and Fig. 12 show the response of the circuit to a positive and negative HMM event respectively. The simulated waveforms show that the capacitor effectively records the peak of the event, which occurs within the first 1-2 ns of the event, as designed.

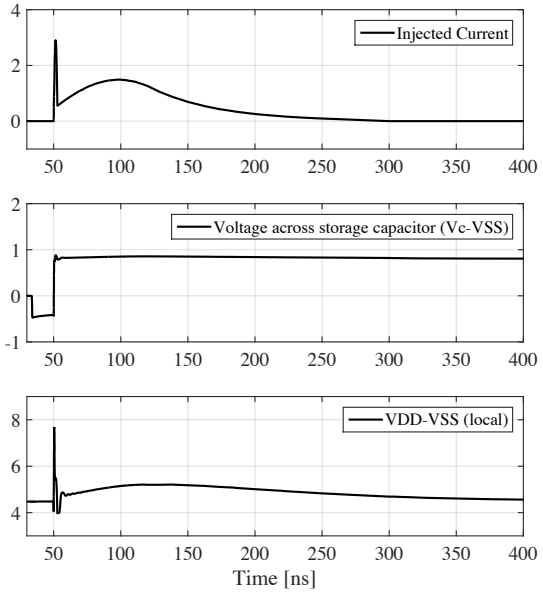

Figure 11. Simulated transient response during a positive 2 kV HMM event

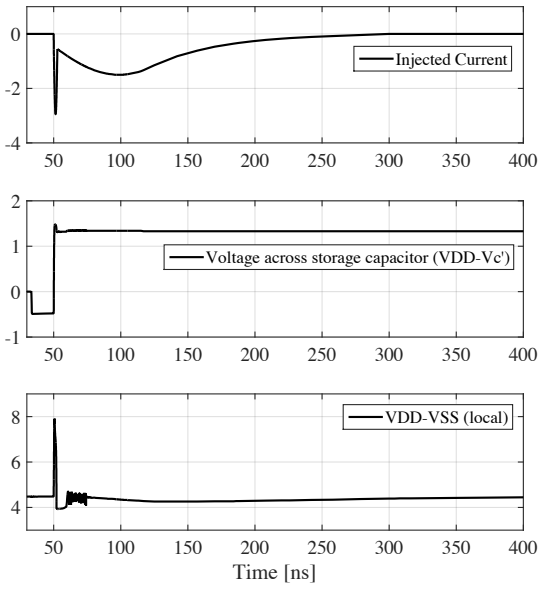

Figure 12. Simulated transient response during a negative 2 kV HMM event

Additional simulations were performed to determine the minimum current level and the minimum pulse width of the injection needed for a reliable reading of the event level. The minimum event current was determined by placing a TLP source between the I/O pin and the board return plane (VSS) and sweeping the peak current in 0.1 A steps in simulation while reading

the voltage at the A/D converter. The simulated A/D converter voltage as a function of the input current is shown in Fig. 13 for the negative level sensor. The minimum detectable current is 0.3 A. This threshold is lower than the threshold of the event detectors, which are set to trigger for events with 0.9 A peak currents or above [7]. This 0.9 A threshold should be sufficient to capture events of concern, but could be adjusted through circuit design to capture smaller events, if needed.

To determine the minimum pulse width required for a reliable reading, TLP pulses with different peak current levels and different pulse widths were injected between the pad and the board return plane (VSS). Fig. 14 shows the simulated voltage at the A/D converter as a function of pulse length for different peak current levels for the negative level sensor. The level sensor is able to reliably detect the level of events with a peak current of 0.7 A and above with pulse widths of 1 ns or greater. Events with current lower than 0.7 A must have a duration of several tens of nanoseconds to generate a reliable reading at the A/D converter.

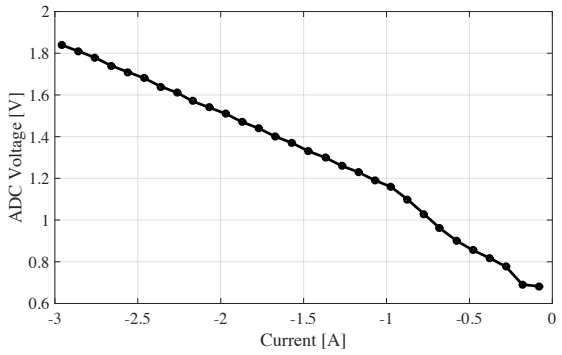

Figure 13. Simulated voltage at A/D converter during a negative event as a function of peak ESD diode current

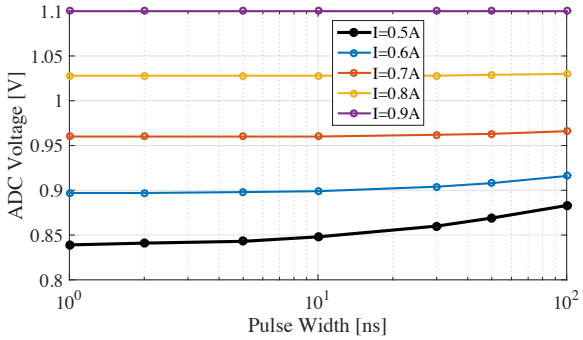

Figure 14. Simulated voltage at A/D converter during a negative event as a function of pulse width for different event current levels

Simulations were also performed to measure the sensor's performance over process variations. Five process corners were tested: typical-typical, fast-fast, slow-slow, fast-slow, and slow-fast, where the first word indicates the process model used for the NMOS and the second word the model for the PMOS. Process variations for the ESD diode were not included in simulations as these corner characterizations were not available. The simulated voltage at the A/D converter for different TLP current levels and different process corners is shown in Fig. 15 for the negative level sensor. The simulation suggests the peak current can be measured within approximately 1 A across process variation.

Better accuracy could be achieved by performing a calibration measurement on each IC to eliminate the impact of process variation. For example, a simple calibration process might consist of injecting a few TLP events of known size and duration (e.g. 10 ns pulses ranging from 1 A to 7 A) to generate a lookup table similar to Fig. 15. This measurement could be used to reliably map ADC readings to peak injected current levels. The number of points required in the calibration and size of the readings might vary depending on the desired accuracy or range. The results in Fig. 14 suggest that, above 0.7 A, testing with different event durations is not required.

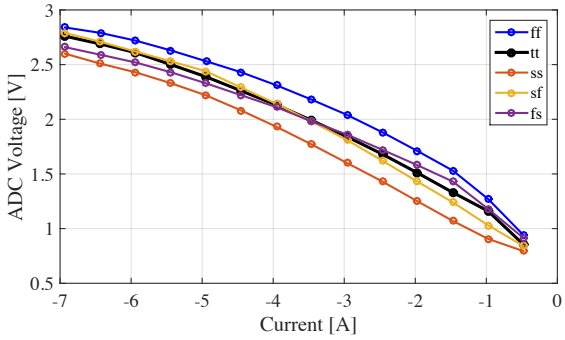

Figure 15. Voltage at A/D converter as a function of the peak ESD diode current for different process corners

Fig. 16 shows the transfer curves for the negative level sensor with different temperatures. Curves were generated at 10º, 25º, and 45º C. The variation in output with temperature is minimal. It appears that process variations have significantly greater impact on the accuracy of the sensor.

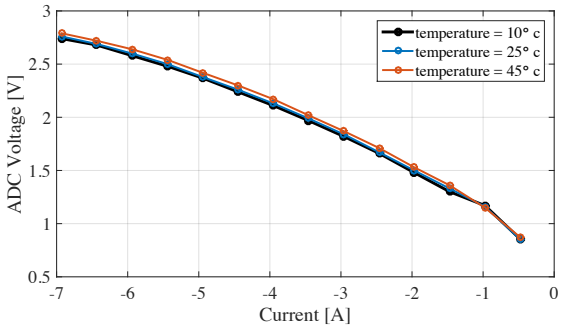

Figure 16. Voltage at A/D converter as a function of the peak ESD diode current for different operating temperatures

IV. Implementation and Testing

The positive and negative level sensors were implemented on a microcontroller test IC manufactured using a 90 nm technology and a 5 V I/O library. The level sensors and event detectors were added to 72 I/O cells of the ~100 pads forming the pad ring. A high-level description of the I/O floorplan is shown in Fig. 17. The EFT detectors and level sensors are abutted to the I/O pad in a spacer cell. This spacer cell includes the positive and negative event detectors and level sensors, along with an ESD clamp. The event detectors and level sensors increase the area of the I/O cell by approximately 27%. For this test chip, no attempt was made to minimize the area of this spacer cell. However, with careful layout optimization a much more compact spacer cell could be achieved.

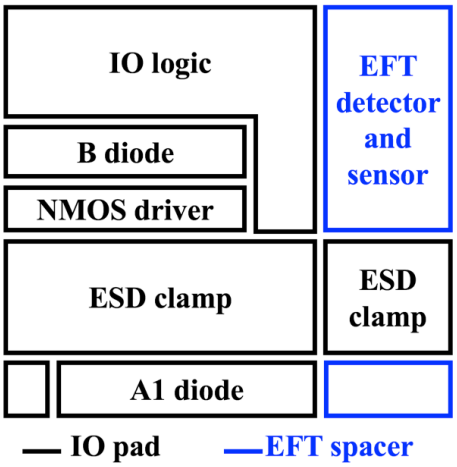

Figure 17. I/O floor plan along with abutted EFT cell

The reset signals for the transient event detectors and level sensors must be handled carefully to avoid an unintentional reset during a high-power transient event. The on-die voltages on VDD and VSS near a pin subject to a positive transient event will rise relative to VDD and VSS on the other side of the IC. Similarly, VDD and VSS will fall near the pin during a negative event. A signficant rise in the local value of VDD and VSS may cause a "high" signal generated on the other side of the IC to be interpreted as a "low", or vice-versa. To avoid this problem, two reset signals are generated by the core and distributed throughout the I/O padring (reset and reset_b – i.e. "reset not"). The positive detectors/sensors are designed to only react to the ("active high") reset signal and the negative detectors/sensors to to the ("active low") reset_b signal (see Figs 1-3). For the positive detectors/sensors, a rise in the local value of VDD and VSS relative to the normally "low" reset signal will not change the interpretation of reset as a "low" signal. Similarly, for the negative detectors/sensors, a fall in the local value of VDD and VSS relative to the normally "high" reset_b signal during a negative event will not cause a change in the interpretation of the reset_b as a "high" signal. While the reset_b signal could be created by inverting reset at the pad, rather than distributing the signal throughout the padring, this inverter could misread the reset signal during a transient event and cause an unintended reset of the negative detectors/sensors.

The process used to measure the test IC is shown in Fig. 18. The event detectors and the level sensors were reset on power-up. A transient event larger than 0.9 A triggers the event detector and an interrupt. The interrupt service routine (ISR) reads the A/D converter after 1 us, to give the on-die power supply voltage time to recover after the event. The values read from the A/D converter are read from the microcontroller through a serial port.

Fig. 19 shows the measurement probe when using a TLP as the transient source. The I/O pad was stressed between the pin and VSS as in the simulation. The TLP voltage was increased in steps for each injection and the A/D converter output was recorded. A resistive PI network was added to the injection probe to measure the injected current. The resistive PI network consists of a series resistor (13.5 Ω) and two voltage pickup resistors (400 Ω) which are connected to two oscilloscope channels. The injected current is determined from the voltage drop across the 13.5 Ω resistor and the probe and oscilloscope resistor values.

Fig. 20 shows the transient voltage measured at the two sides of the 13.5 Ω resistor and the injected current calculated from these transient waveforms. Care must be taken to eliminate skew between the voltage waveform measurements as this may lead to an unreal spike in the calculated current.

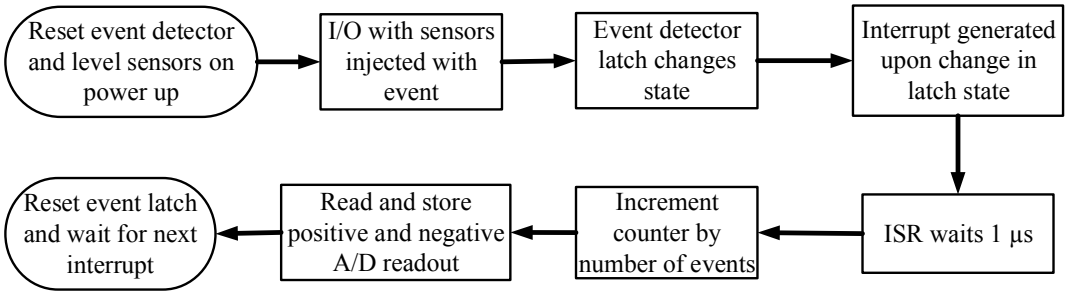

Figure 18. Functional flow diagram of measurement process

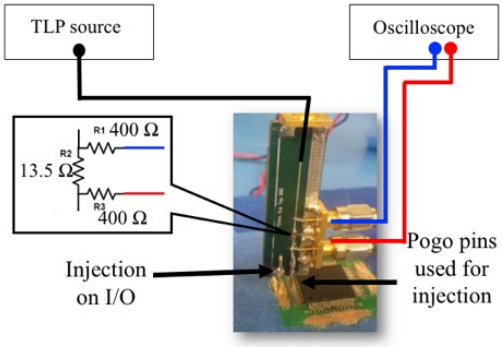

Figure 19. Test setup for characterizing level sensors using TLP injection

Fig. 21 shows a comparison between the measured and simulated voltage at the A/D converter as a function of the peak TLP injection current when injecting into pin 1 of the test chip. Results are shown for the negative level sensor. The simulation was conducted with typical process conditions and at room temperature. The simulated A/D converter voltages predict the measured peak current within about 0.5 A. Fig. 22 shows a similar curve for positive stress events applied between the pin and board return plane (VSS). The simulated A/D converter voltages also predict the measured peak current within about 0.5 A for the positive level sensor, though additional measurements are needed to fully validate performance of this sensor.

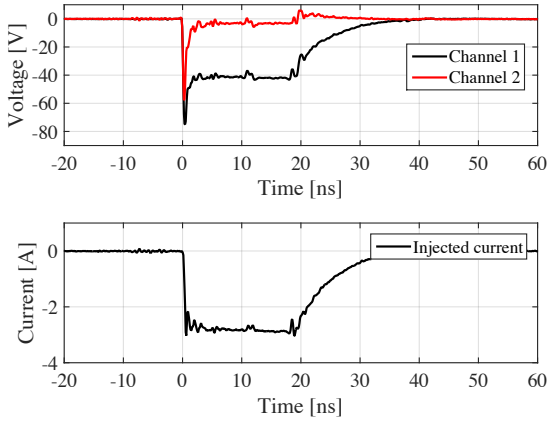

Figure 20. Transient waveforms measured using the voltage probe (top) and the calculated current (bottom)

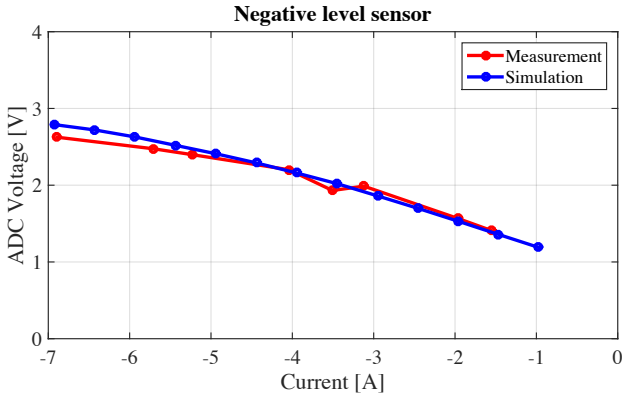

Figure 21. Measured and simulated voltage at the A/D converter for the negative level sensor as a function of the injected current

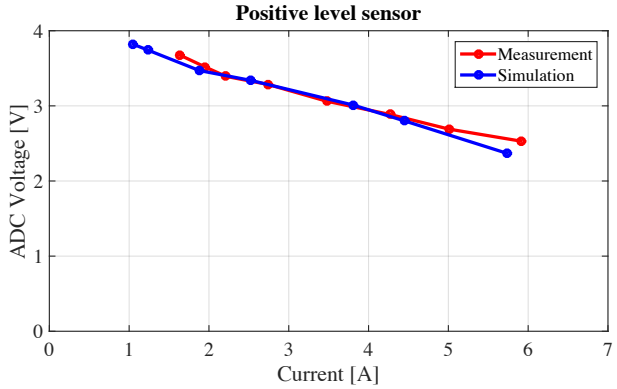

Figure 22. Measured and simulated voltage at the A/D converter for the positive level sensor as a function of the injected current

The test IC was also tested using transient waveforms consistent with a negative HMM event. The transient HMM event was injected between the I/O pin and board return plane (VSS) as before. Fig. 23 shows a comparison between the measured and simulated A/D converter reading as a function of the peak injected current. As with the TLP source, the simulated A/D converter voltages predict the measured peak current in the HMM transient waveform within about 0.5 A.

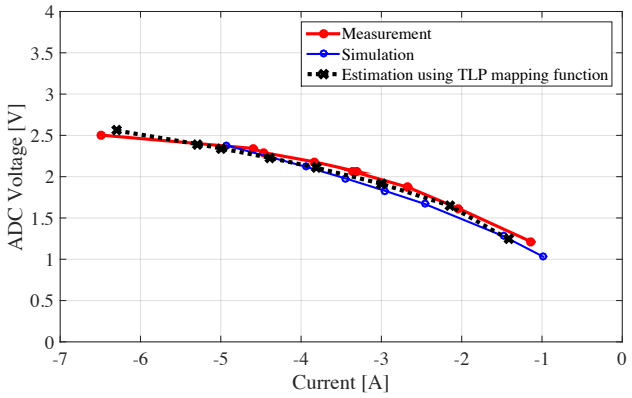

Figure 23. Comparison of measured and simulated A/D converter voltage as a function of injected current for negative HMM events

As mentioned earlier, better results can be obtained through calibration. The TLP measurements in Fig. 21 can serve as a calibration, since the peak current levels and resulting A/D converter readings are known. Using these readings to predict the peak current from the measured A/D converter readings in the HMM tests gives the black curve shown in Fig. 23. After calibration, the measured current is predicted within about 10%, or roughly 0.3 A).

V. Discussion and Conclusions

On-die sensors were developed which allow the user to determine the peak level of a transient stress event applied to an IC. Simulations demonstrate the sensors can determine the peak level within about 1 A when accounting for typical variations in process parameters and temperature. The accuracy of the sensor can be improved significantly through calibration measurements which mitigate the impact of process variations. The sensors were able to detect events with peak currents of 0.7 A or larger with durations of 1 ns or longer. Measurements on a product test chip show good correlation between simulations and measurements and demonstrate the sensor can accurately predict the peak transient current under realistic conditions.

On-die transient event sensors, like those proposed here, can give the ESD test engineer and product developer access to significant information about transient events which are difficult to obtain through other means. With these sensors, the user and the software can know when a transient event occurs, which pins were affected, and how large the event was. This information can make testing and debugging of the immunity of electronic devices substantially easier, since the engineer can know which ICs and which pins are impacted by a test without adding any additional hardware, and can directly observe the impact of any design changes (i.e. to show how much the transient event level seen by an IC is reduced by a system board change). Testing for soft errors using conventional means is notoriously difficult and can be made easier with such on-die sensors, since the test engineer can readily determine if an IC buried within an electronic device undergoes a stress event as a result of a transient immunity test, even if there is no readily-observable effect from the outside. The presence of sensors in the I/O of the final product also gives the software developer the option to program defensive reactions to transient events that occur in the field, for example by restoring the device to a known safe state after an event or by recommending product maintenance after detecting more than a given number of events above a given size.

Acknowledgements

This material is based upon work supported by the National Science Foundation (NSF) under Grants IIP-1440110.

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