Schottky LDNMOS for HV ESD Protection

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50 Words Abstract – A simple and useful scheme to improve the ESD performance of HV LDNMOS is reported. Removing the N+ implant from the drain, the silicide to NDDD junction of HV LDNMOS becomes a Schottky barrier. This modification can incorporate a Schottky pnp bipolar into LDNMOS to form an SCR.

I. Introduction

Metal source/drain (S/D) Schottky-barrier (SB) MOSFET has been proposed for replacing implanted salicided S/D junction, eliminating bipolar action to increase latchup immunity and high-speed RF circuits in CMOS technology since 1966 [1]-[6]. However, most SB MOSFET's used in the early literature are the low-voltage (LV) device and most studies focus on the DC-IV and RF characteristics of transistor. To the best of our knowledge, there are only two studies for the Schottky barrier (SB) effect on the ESD performance of high-voltage (HV) device. First study addressed a diode [7] while the other study focused on an npn bipolar [8] device. For the npn bipolar, the SB is on the cathode to increase the holding voltage and it is well known that any ESD performance improvement would require optimization on anode to drive the majority carrier conduction.

In this paper, the SB HV-LDNMOS is proposed and studied for the first time for ESD performance enhancement without any basic device electrical performance degradation. The concept is simple wherein the ohmic contact is converted into Schottky by removing the highly doped region (the purpose of which is to prevent Schottky diode formation). In the HV-LDMOS, this is achieved by removing the N+ implant of the drain. This simple modification significantly improves the device ESD performance without any I_{DSat} degradation at the high V_G nor increase the junction leakage current of the device, unlike any Schottky diode implementation on CMOS technology. This report explains in a novel way why Schottky contact significantly increase the device ESD performance without suffering the high leakage current problem using device physics fundamentals.

II. Experiment

GLOBALFOUNDRIES 0.18um HV 18V BCD process is used for demonstrating the novel device. Fig. 1-4 shows the layouts, cross-section and equivalent circuits of the HV-poly diode, SB HV-poly diode, HV-LDNMOS and SB HV-LDNMOS used for this study. All these structures are designed with same single finger width (50um) and having a total width of 100um. The only difference for the HV devices and SB HV devices is the drain contact implant. The SB HV devices do not have the N+ implants, unlike the HV-LDNMOS, resulting in the Schottky barrier at the silicide and NDDD of SB HV device.

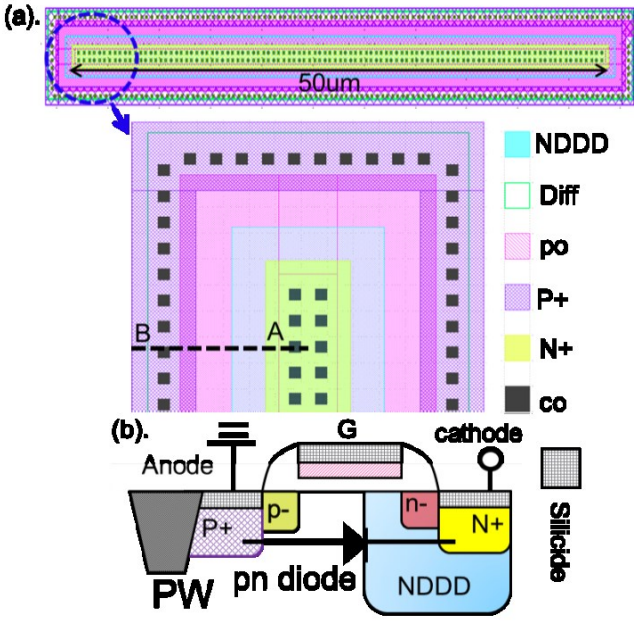

Figure 1: (a) Layout of HV-poly diode: upper –full layout; lower – rotated zoomed layout view, (b). cross-section and equivalent circuit between A-B in Fig. 1a lower.

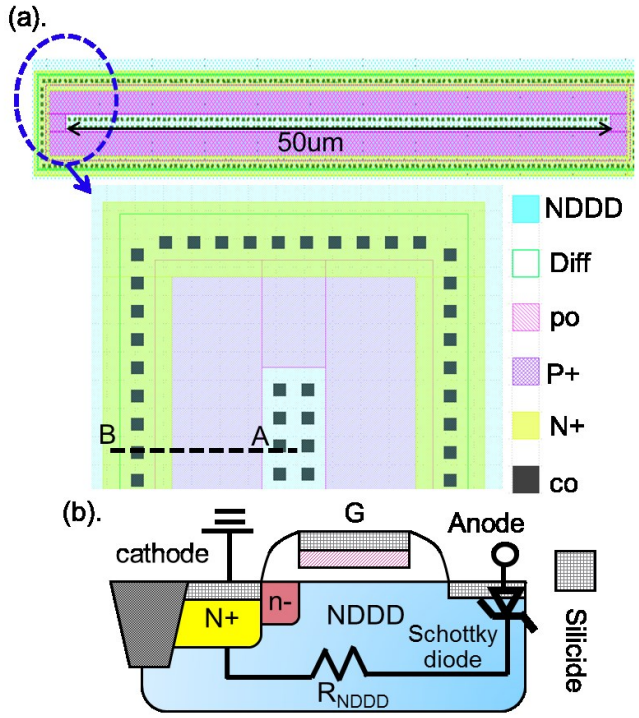

Figure 2: (a) Layout of SB HV-poly diode: upper –full layout; lower – rotated zoomed layout view, (b) cross-section and equivalent circuit between A-B in Fig. 2a lower.

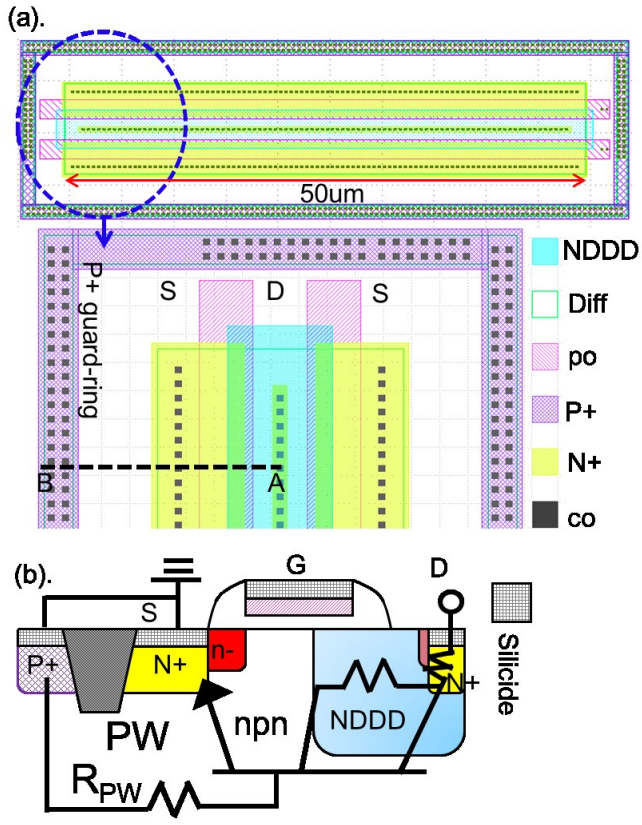

Figure 3: (a) Layout of HV-LDNMOS: upper –full layout; lower – rotated zoomed layout view, (b). cross-section and equivalent circuit between A-B in Fig. 3a lower.

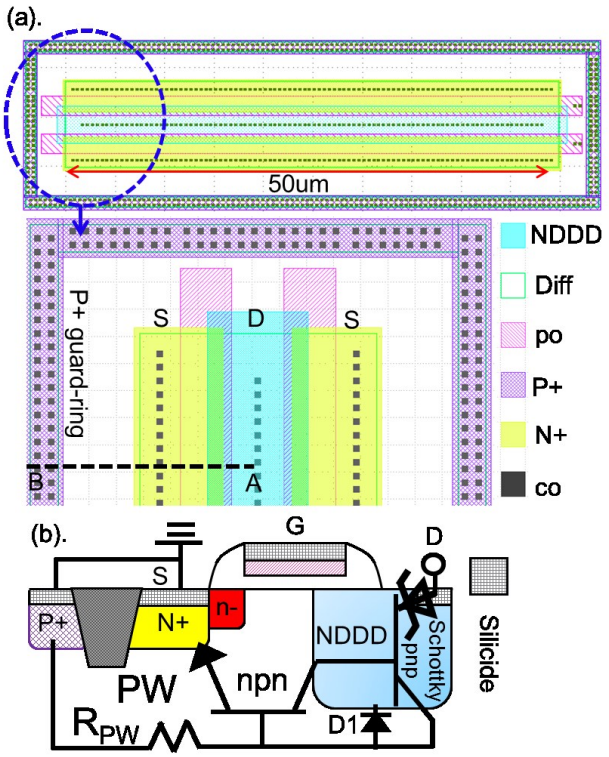

Figure 4: ((a) Layout of SB HV-LDNMOS: upper –full layout; lower – rotated zoomed layout view, (b) cross-section and equivalent circuit between A-B in Fig. 4a lower.

A. HV-Poly Diode and SB HV-Poly Diode

Fig. 5-6 show the DC-IV characteristics of the HV-poly diode and SB HV-poly diode. Under the reverse bias, the HV-poly diode has very low leakage current (<10pA at 30V), while the SB HV-poly diode has high leakage current (~1uA at -1V). Under the forward bias, the HV-poly diode can clamp the voltage since the current increases exponentially with voltage. However, the SB HV-poly diode neither clamp the voltage nor sink the current. Fig. 6b shows that the SB HV-poly diode current linearly increases with voltage beyond the turn-on threshold voltage and jumps to 100mA, latter caused by the thermal runaway beyond 35mA.

Fig. 7 and Fig. 8 show the forward bias TLP IV characteristics of the two diodes. It can be seen that changing the anode contact from the ohmic to Shottky significantly degrade the It2 from 3.6A to 36mA for the HV-poly diode. The TLP current of SB HV-poly diode does not increase exponentially with voltage like its DC-IV characteristic, instead the current linearly increases with voltage until thermal runaway.

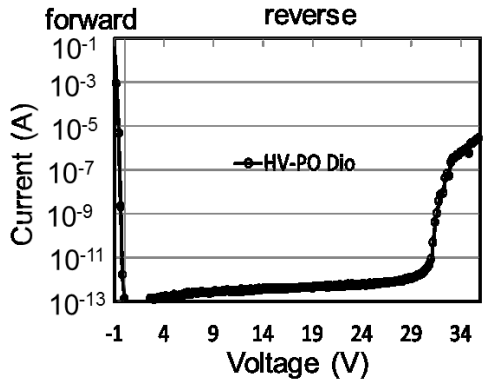

Figure 5: DC-IV Characteristics of HV-poly diode in Fig. 1.

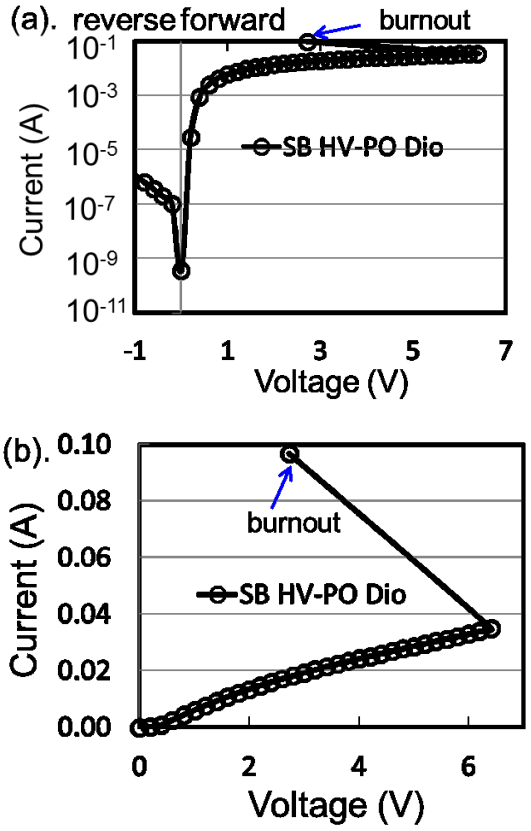

Figure 6: DC-IV Characteristics of SB HV-poly diode in Fig. 2 (a) in log scale, (b) in linear scale.

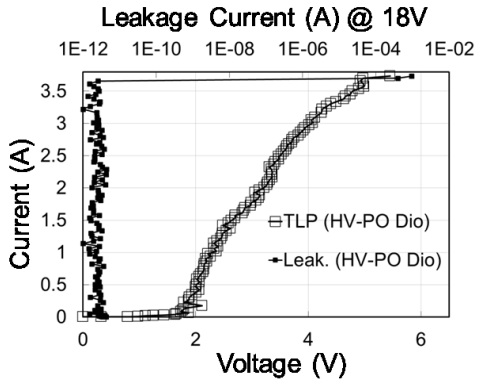

Figure 7: TLP IV Characteristic of HV-poly diode in Fig. 1 in the forward biased mode .

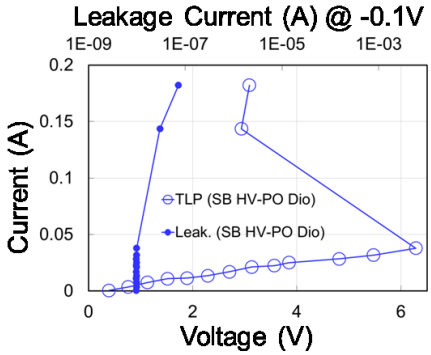

Figure 8: TLP IV Characteristic of SB HV-poly diode in Fig. 2 in the forward biased mode.

B. HV-LDNMOS and SB HV-LDNMOS

Fig. 9 shows the DC-IV characteristics of the grounded-gate HV-LDNMOS and SB HV-LDNMOS. Unlike the SB HV-poly diode (Fig. 6), switching the drain contact from ohmic to Schottky does not increase leakage current since it is clamped by the reverse-bias diode between NDDD and PW (D1 in Fig. 4b). The leakage current of SB HV-LDNMOS is identical with that of HV-LDNMOS as the applied voltage is below the junction breakdown voltage (~30V).

Fig. 10 shows the I_D-V_G curves of the HV-LDNMOS and SB HV-LDNMOS for V_D 0.1V, 0.5V, 1V and 2V. Except V_D 0.1V, the current I_D of SB HV-LDNMOS at the subthreshold region ($V_G \leq 1.5V$) is nearly identical to that of HV-LDNMOS. In series with a SB diode, the current I_D of SB HV-LDNMOS beyond the subthreshold region ($V_G > 1.5V$) is always smaller than that of HV-LDNMOS. However, they are close to each other as V_D increases to 2V or more since the voltage drop across the SB diode becomes smaller compared to that across the channel.

Fig. 11 shows the I_D-V_D of the HV-LDNMOS and SB HV-LDNMOS for V_G 1V-5V. The SB diode results in the decrease of drain current I_D at the linear region. Nevertheless, it does not change the saturation current I_{DSAT} of the SB HV-LDNMOS for high V_G ($\geq 3V$), attributed to the smaller voltage drop across the SB diode compared to that across the channel at large V_D.

Fig. 12 and Fig. 13 show the wafer level TLP and HBM IV characteristics [9-10] of the grounded-gate HV-LDNMOS and SB HV-LDNMOS. Each point of the IV curves in the two figures is based on the average values of the voltage and current waveforms at 40ns-80ns and 54ns-94ns for TLP and HBM, respectively. Due to the SB diode, the trigger voltage

Vt1 of SB HV-LDNMOS (35V) is higher than that of HV-LDNMOS (32V). The HV-LDNMOS is damaged after the 1st snapback, however, the SB HV-LDNMOS is not damaged by the 1st snapback and can sustain the 1.1A TLP current and 2kV HBM stress (average current 0.8A in Fig. 13). Based on the 1uA failure criterion, the HV-LDNMOS only can pass 0.3kV HBM, while the SB HV-LDNMOS with same total width (100um) can pass 2kV HBM.

These demonstrate that SB HV-LDNMOS implementation is both ESD robust and do not impact the device electrical performance unlike the HV-Poly diode and HV-SB Poly diode.

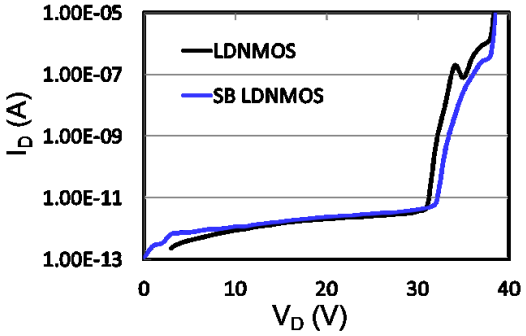

Figure 9: DC-IV characteristics of LDNMOS and SB LDNMOS (V_G=0V).

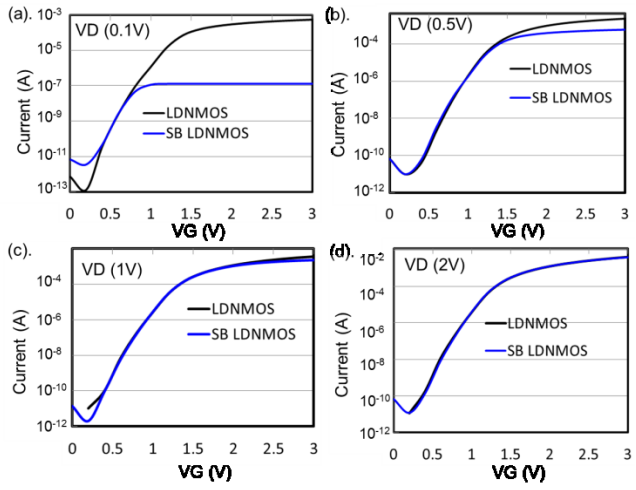

Figure 10: DC I_D-V_G of LDNMOS and SB LDNMOS.

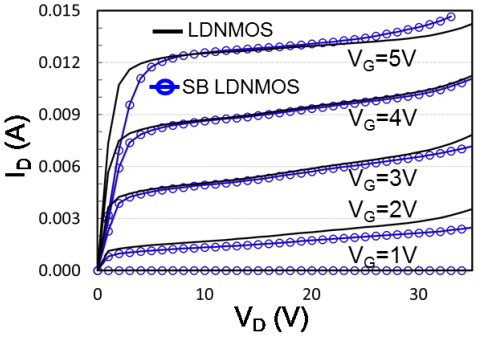

Figure 11: DC I_D-V_D of LDNMOS and SB LDNMOS.

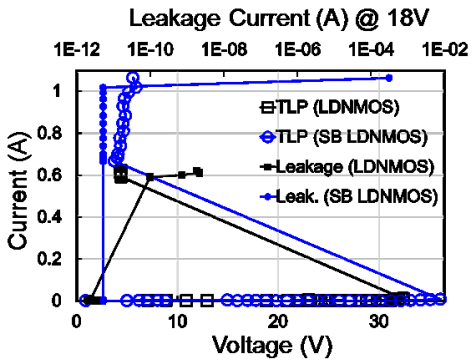

Figure 12: TLP IV characteristics of LDNMOS and SB LDNMOS (V_G=0V).

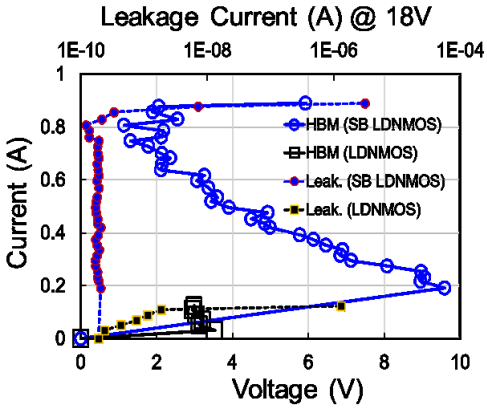

Figure 13: HBM IV characteristics of LDNMOS and SB LDNMOS (V_G=0V).

III Discussion

TLP results shown in Fig. 8 and Fig. 12 clearly indicate that the SB HV-poly diode behavior is contradictory to that of the SB HV-LDNMOS. The SB HV-poly diode is very vulnerable to the TLP stress (It2=37mA), while the SB HV-LDNMOS can sustain the high current stress (It2=1A). Moreover, the SB HV-poly diode is a high-leakage current device (Fig. 6a), while the SB LDNMOS has low leakage current below the avalanche breakdown voltage (Fig. 9). The key question that requires an answer is - Why the deficiency of one structure becomes the virtue of another structure? The physics behind these seemingly similar devices but with strikingly different behavior is primarily the focus of the subsequent section.

A. Comparison of SB HV-Poly Diode and SB HV-LDNMOS

In order to better understand the involved physical mechanisms, several in-depth analysis were carried out such as Transmission Electron Microscope (TEM), TCAD, etc. Fig. 14 shows that TEM images of the interface between silicon and silicide is not a smooth

interface since they are two different materials with different lattices and orientations [11], resulting in high interface-state density [12]. With the fragile interface, it will induce the new defects once there is any current flowing through the interface. Fig. 14b shows that there are two stacking faults generated at the region below the silicide of the SB HV-poly diode after the TLP stress. This creates new interface-state density inside the NDDD junction, which in turn will increase the leakage current (Fig.8). These observations clearly explain the high leakage current of the SB HV-poly diode (Fig. 6a).

In the case of SB HV-LDNMOS, all defects are buried inside the NDDD (Fig. 4). So, the increase in the interface-state density inside the NDDD does not result in the increase of the leakage current of the SB HV-LDNMOS since it is clamped by the reverse-bias diode D1 shown in Fig.4.

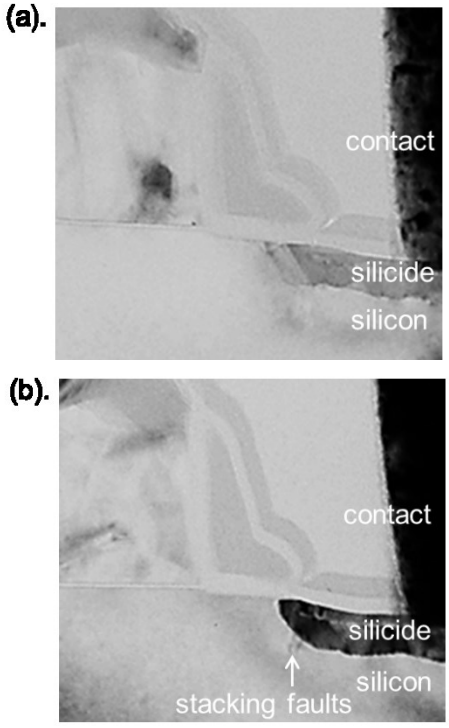

Figure 14: TEM pictures of SB-HV poly diodes (a) unstressed device, (b) after TLP stress.

B. Simulation Result

Fig. 15 and Fig. 16 show the Drain-Source band-diagrams for the HV-LDNMOS (Fig. 3) and SB HV-LDNMOS (Fig. 4). During the positive ESD stress event, the energy-band of the drain will be pulled down. This lowers the energy barrier between source and drain to result in the electrons injecting from the source to the drain. Due to the high drain electric field these electrons results in the generation of the substrate current to raise the substrate-potential. Eventually, the source junction is forward biased to keep injecting the electrons to the high field drain, resulting in the npn bipolar transistors turn-on [13].

TCAD simulations were carried out to validate the physical understanding explained above. The total width of the two devices used for simulation study during the ESD events was identical to that of the test devices (100um). The simulation result shows that the electron current flow from the source to the N+ diffusion of the drain and to the silicide of the drain, through the regions below the gates for the HV-LDNMOS and SB HV-LDNMOS (Fig. 17), respectively.

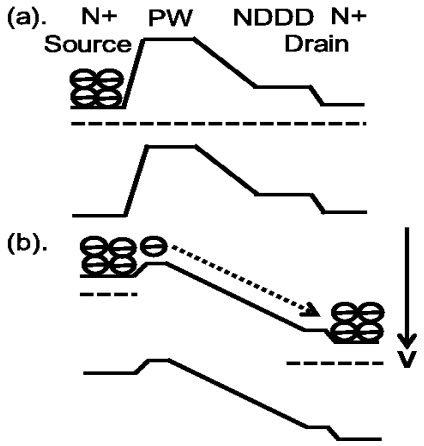

Figure 15: Band diagram of HV-LDNMOS at V_D= (a). 0V, (b) >0V.

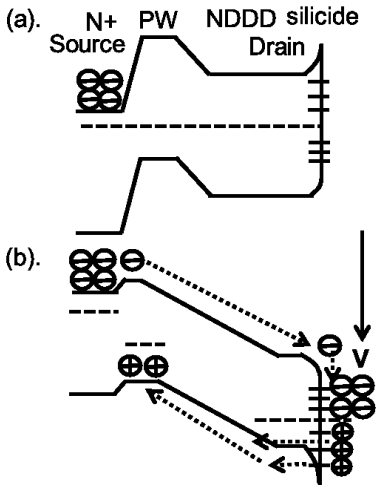

Figure 16: Band diagram of SB HV-LDNMOS at V_D= (c) 0V, (d). >0V.

Fig. 18 shows the simulated hole-current densities of the HV-LDNMOS and SB HV-LDNMOS under 0.6A TLP stress. For the HV-LDNMOS, the hole-current flows from the corner of the N+ junction of the drain. This is attributed to the maximum electron-current density (Fig. 17a) and electrical field (Fig. 19a) to give rise to the high impact-ionization rate for hole

generation. From Fig. 18b, the hole current flows through whole NDDD diffusion of the SB HV-LDNMOS without having the N+ junction to build the high electrical field for hole generation. With significant interface-state density existing at the interlayer between the silicide and NDDD [12], as the energy-band between the drain and source of the SB HV-LDNMOS is pulled down by the drain (Fig. 16b), the interlayer can inject the holes into the PW through the NDDD [14]. This action corresponds to the Schottky pnp bipolar turning on. Thus, with the npn bipolar and pnp bipolar (Fig. 4), the action of SB HV-LDNMOS during the positive ESD stress event is like an SCR [15].

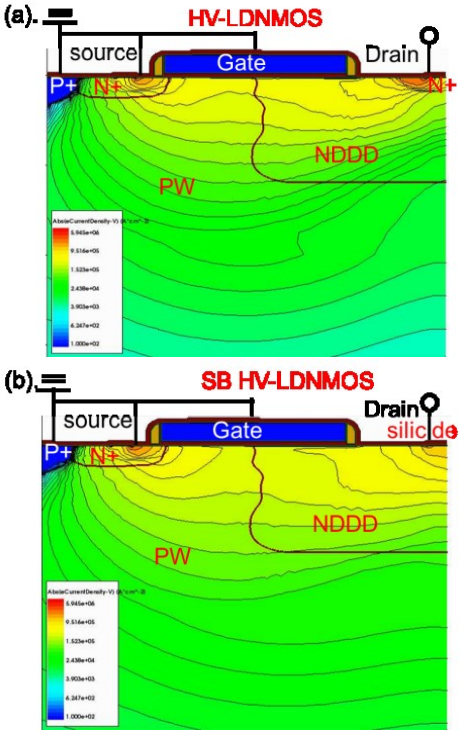

Figure 17: Simulated electron-current densities of (a). HV-LDNMOS, (b). SB HV-LDNMOS at the 100ns TLP stress (0.6A).

Fig. 19 shows the electric field of the HV-LDNMOS and SB HV-LDNMOS under the 0.6A TLP stress from TCAD simulations. Due to the base push-out effect [16], the high electric field of the HV-LDNMOS is pushed to the N+ junction from the NDDD junction once it is driven into the snapback region [10]. Without the N+ junction, the high electric electrical of the SB HV-LDNMOS is pushed to the region below the silicide. Comparison of Fig 19a and Fig. 19b shows that the maximum electrical field of the SB HV-LDNMOS is much smaller than that of the HV-LDNMOS due to the SCR turn-on. Based on P=E×J, the higher electrical field can generate more Joule-heating to give rise to the higher temperature for same current density.

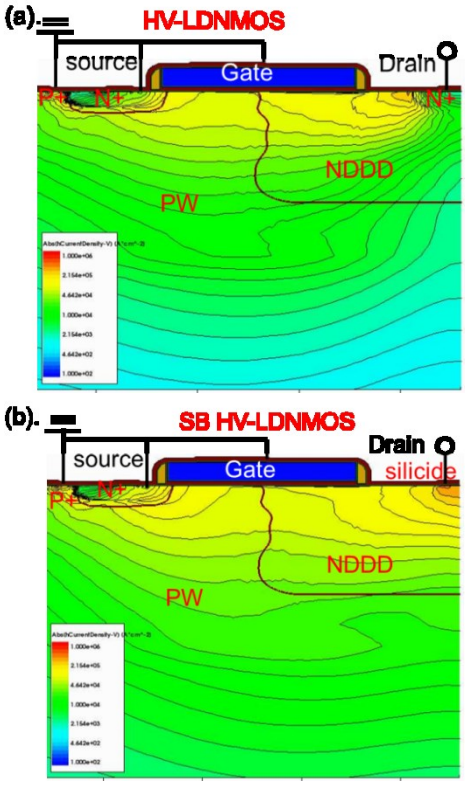

Figure 18: Simulated hole-current densities of (a) HV-LDNMOS, (b). SB HV-LDNMOS at the 100ns TLP stress (0.6A).

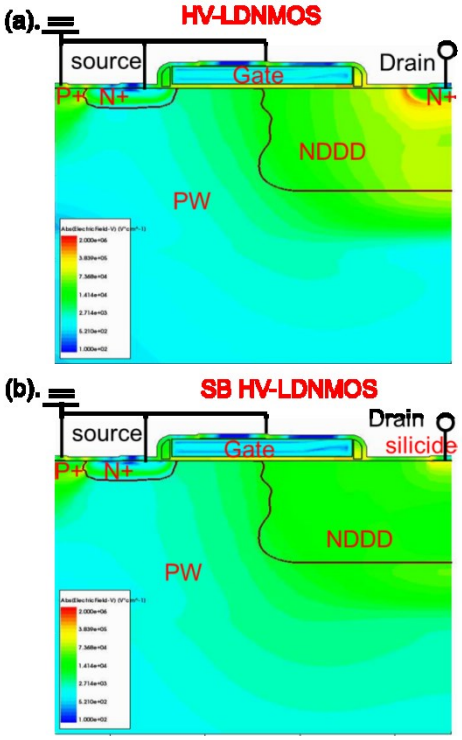

Figure 19: Simulated electrical fields of (a). HV-LDNMOS, (b). SB HV-LDNMOS at the 100ns TLP stress (0.6A).

From the simulation result shown in Fig. 20, the maximum temperature of the HV-LDNMOS under

the 0.6A TLP is reaching the silicon melting point (1414°C), while it is only 800°C for the SB HV-LDNMOS. This is why the SB HV-LDNMOS has much higher It2 compared to the HV-LDNMOS.

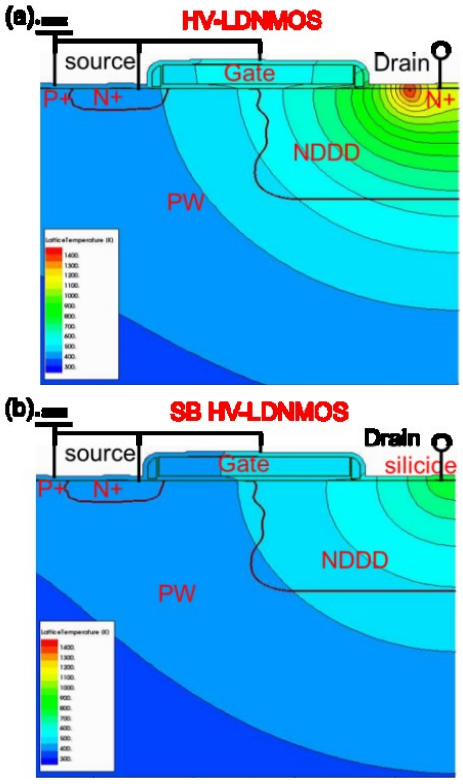

Figure 20: Simulated temperatures of (a). HV-LDNMOS, (b). SB HV-LDNMOS at the 100ns TLP stress (0.6A).

C. Comparison of conventional HV-SCR and SB HV-LDNMOS

Fig. 21 and Fig 22 show two types of HV-LDNMOS SCR's for this study, which are the open-base SCR (SCR1) [17] and embedded-SCR (SCR2) [18]. For the SCR1, it uses the P+ implant as the drain contact implant instead of the N+ implant. During the ESD event, the diode D1 is forward-biased with the current I_{CB} flowing through the junction capacitor C_B and P-Well resistor R_{PW} raising the substrate potential V_{sub}. Once the V_{sub}>0.7V, the source is forward biased to inject the electrons into the NDDD diffusion through the PW, representing the npn bipolar turn-on. Since the diode D1 is forward-biased, the P+ diffusion will inject the holes into the PW through the NDDD diffusion, corresponding to the SCR turning on since the npn and pnp both turn on [15].

Comparison of Fig. 12 and Fig. 23 shows that the It2 of SCR1 is much larger than that of the SB HV-LDNMOS. This is attributed to the higher doping concentration of P+ implant compared to the interface-state density of the interlayer between the silicide and silicon. However, the Schottky pnp bipolar cannot inject as many holes as the pnp bipolar [14], [19] due to the low doping concentration.

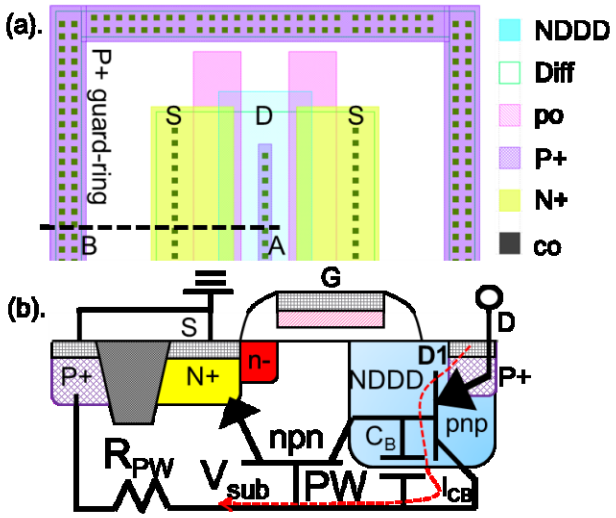

Figure 21: (a) Layout of open-base SCR LDMOS (SCR1), (b). cross-section and equivalent circuit between A-B in Fig. 21(a).

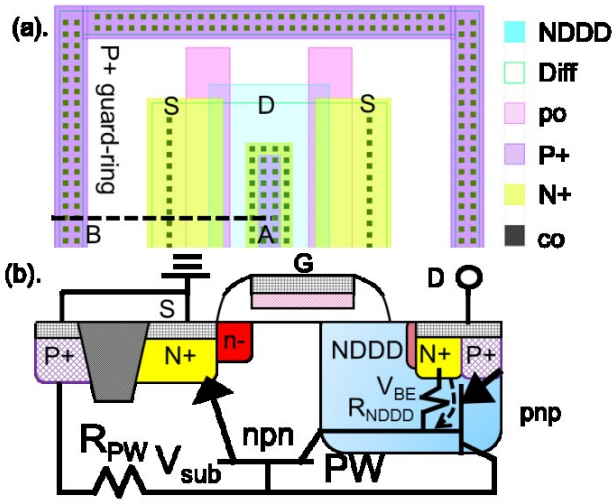

Figure 22: (a) Layout of embedded-SCR LDMOS (SCR2), (b). cross-section and equivalent circuit between A-B in Fig. 22(a).

Fig 22 shows the SCR2, where an additional P+ implant is inserted into the drain along with the N+ implant. TLP IV curve in Fig. 23 shows that it has a larger Vt1, but with a lower It2. This is explained by the fact that the P+ implant that is butted with N+ implant (Fig. 22a). With the very small R_{NLDD} (Fig. 22b), the voltage drop (V_{BE}) across the base and emitter of the pnp bipolar is too small to turn on the pnp for driving the SCR operating at the high current injection during the ESD event.

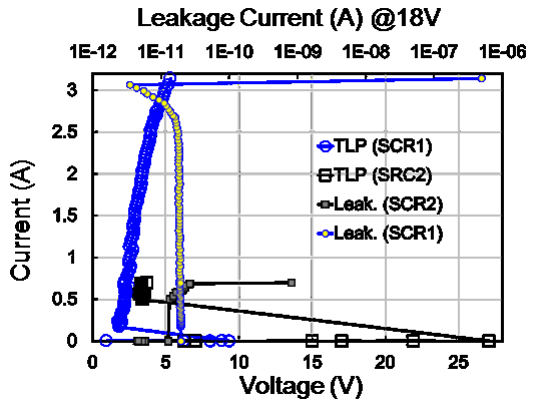

Figure 23: TLP IV characteristics of SCR1 (Fig. 21) and SCR2 (Fig. 22).

D. ESD Protection for HV-LDNMOS

As shown in the previous section, the only layout difference between the two HV-LDNMOS devices is the drain N+ implant and that SB HV-LDNMOS device electrical parameters are almost identical to standard HV-LDNMOS. In this section, influence of SB insertion location into the HV-LDNMOS is presented, which is very important for ESD performance optimization. Fig. 24 shows various SB locations of the output buffer HV-LDNMOS [20]. All the three structures are designed with same finger width (50um) and total width (500um). The structure in Fig. 24a is the reference HV-LDNMOS. The total widths of HV-LDNMOS and SB HV-LDNMOS (Fig. 24b/24c), are 400um and 100um.

Fig. 25 shows the TLP test result of these three structures. Near identical TLP IV characteristics are observed for the two structures in Fig. 24a and Fig. 24b with double snapback phenomenon and are damaged by the first TLP pulse at the 2nd snapback region. This implies that the SB HV-LDNMOS cannot protect the HV-LDNMOS if it is at the edge of the structure. However, the TLP IV characteristic of the structure in Fig. 24c is very different from to other two structures, with only one snapback region and large It2 (~1A), which is very close to the It2 of SB HV-LDNMOS (1.1A in Fig. 12). Based on the 1uA failure criterion, the structure in Fig. 23c can pass 3.5kV HBM, while the SB HV-LDNMOS in Fig. 4 only passes 2.0kV HBM (Fig. 13). Moreover, the structures in Fig. 24a and Fig. 24b only can pass 0.35kV and 0.5kV. This clearly demonstrates that the SB HV-LDNMOS can simultaneously protect the HV-LDNMOS and enhance the ESD performance of the HV-LDNMOS if it is at the center of the structure.

This can be explained as a direct consequence of the higher Vt1 of SB HV-LDNMOS than that of HV-LDNMOS, as well as, the substrate potential V_{SUB} varied with the device location with reference to the P+ guard-ring [21]. With the small Vt1, the parasitic npn bipolar of HV-LDNMOS turns on first to pull up the V_{SUB}. However, the region close to the P+ guard-ring has the small V_{SUB} while the region away from the P+ guard-ring has the large V_{SUB} for the device at the snapback region [20]. As the SB HV-LDNMOS is located at the edge of the structure, it cannot be turned on to protect the HV-LDNMOS from ESD damage due to too low V_{SUB}. On the contrary, the V_{SUB} is large enough to turn on the SB HV-LDNMOS to clamp the ESD voltage for protecting the HV-LDNMOS from ESD damage if it is located at the center of the structure. With the Schottky pnp bipolar, the SB HV-LDNMOS also can provide the hole current into the substrate to enhance the ESD performance of HV-LDNMOS once it is triggered on.

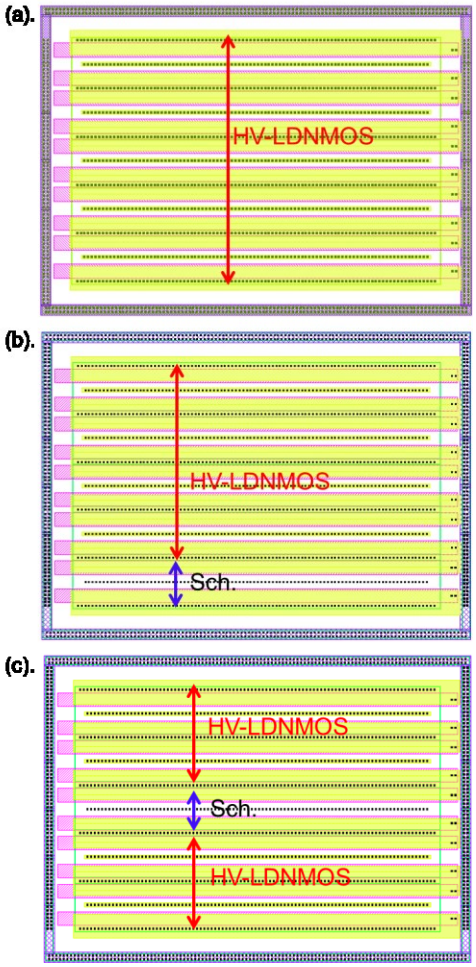

Figure 24: Layout of (a) HV-LDNMOS, (b) HV-LDNMOS with SB HV-LDNMOS at the edge, and (c) HV-LDNMOS with SB

HV-LDNMOS at the center.

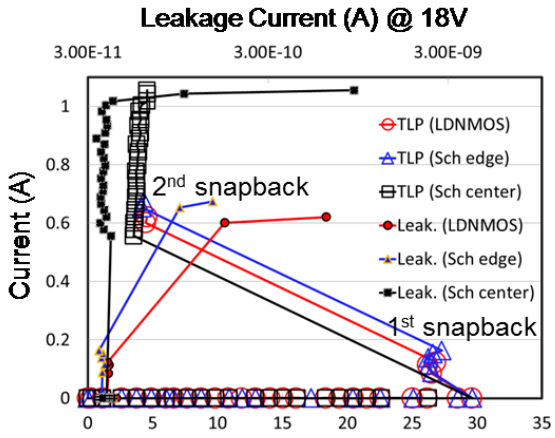

Figure 25: TLP IV characteristics of the three structures shown in Fig.20.

IV Conclusion

A novel use of Schottky barrier to achieve high ESD performance in a HV-LDNMOS is demonstrated in this paper. This implementation overcomes the well-known leakage increase and poor ESD performance associated with SB caused by defects and interface-state density. In this implementation, the SB induced interface-state density being buried inside the NDDD junction does not results in leakage current increase of SB HV-LDNMOS. With the npn bipolar and pnp bipolar, the SB HV-LDNMOS becomes an SCR during the ESD event, achieving higher ESD performance to provide protection to HV-LDNMOS.

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