

# Deep N-well Induced Latch-up Challenges in Bulk FinFET Technology

Chien-Yao Huang, Yu-Ti Su, Tzu-Heng Chang, Chia-Wei Hsu, Jam-Wem Lee,  
Kuo-Ji Chen, and Ming-Hsiang Song

TSMC, No 9, Creation Rd. 1, Hsinchu 300-77, Taiwan

Tel.: +886-3-5636688 ext. 7038251, fax: +886-3-5781548, e-mail: [qyhuang@tsmc.com](mailto:qyhuang@tsmc.com)

**Abstract** – DNW-induced latch-up characteristics and their temperature-dependence are investigated in bulk FinFET technology. DNW-enclosed NMOS in PNP and PNPNP structures causes low latch-up immunity with detrimental high-temperature degradation. Varied methods are explored for holding voltage improvement. In summary, the shunting-resistance reduction through process-design co-optimization plays a critical role in solving DNW-induced latch-up challenges in FinFET technology.

## I. Introduction

Bulk FinFET has been adopted in the leading edge system on chip (SoC) technology for 16nm and beyond [1-4]. With the excellent electrostatic integrity and short channel control, FinFET core/IO devices lead to high performance and energy-efficient digital characteristics [1-2, 5]. FinFET technology also offers excellent analog/RF characteristics such as high intrinsic gain, high cut-off frequency, and reduced 1/f noises, etc [1-2]. The improvements of both logic and analog/RF characteristics by FinFET scaling continuously enhance the performance, functionality, power-saving, and cost reduction of mobile SoC. Deep N-well (DNW) has been implemented in planar CMOS technology as a solution for reducing substrate noise in SoC as well as providing body bias design in digital/analog blocks [6-10]. Some trigger mechanisms for DNW-related “Latch-up” were investigated in 65nm planar CMOS [11]. In scaled SoC enabled by FinFET technology, DNW implementation becomes more common due to the high dense and monolithic integration of analog/RF/digital circuits in the same substrate. However, more DNW implants also increase the buried PN junction interfaces in a substrate, which results in more PNP structures and raises the concern of “Latch-up” susceptibility. To date, very few physical studies are conducted on this issue. The lack of understanding of DNW-induced latch-up characteristics in FinFET technology leaves a reliability risk toward SoC scaling.

In this work, DNW-induced latch-up paths in bulk FinFET technology are characterized through well-defined test structures. To serve the rapid growth of

automotive applications, the degradation of latch-up immunity in hot-temperature environment is also investigated. It is found some DNW-induced latch-up paths suffer low holding voltage ( $V_h$ ) with a detrimental temperature-dependence. The underlying physics of detailed latch-up characteristics and their temperature-dependence are disclosed through a well-established TCAD modeling. The mechanism of DNW-induced latch-up in a PNPNP structure is also studied. Furthermore, varied methods are explored for holding voltage improvement, and the corresponding impacts/limitations are reported. This work points out DNW-induced latch-up challenges and possible approaches in FinFET technology.

## II. Experiments and Conventional Holding Voltage Comparison: FinFET vs Planar

To characterize all DNW-induced latch-up paths in I/O circuits, a set of test structures are fabricated in bulk FinFET technology. Table 1 and Fig. 1(a) illustrate the anode-cathode combinations of latch-up paths related to DNW. In DNW-enclosed NMOS structure, the RW region is a p-type well in DNW, and its carrier concentration is slightly lower than that of PW. Fig. 1(b) shows the layout view of test structures which are used to extract the holding voltage of possible latch-up paths. The anode to cathode spacing ( $S_{pn}$ ) and anode/cathode fin area are fixed for fair comparison. Based on JEDEC I-test standard [12], the semiconductor-controlled rectifier (SCR) is activated by injected substrate current. If the voltage-difference between anode and cathode, i.e.,

VDD, is higher than the holding voltage ( $V_h$ ), a large current through the low-impedance SCR path can be hold. The steady high current conduction from anode to cathode is called “latch-up” state. The  $V_h$  is determined by the minimum voltage-difference between anode and cathode which can sustain the latch-up state. For I/O circuits, the high substrate noises during chip operation can easily activate latch-up paths. Therefore,  $V_h > VDD$  is required to prevent latch-up state, i.e., the  $V_h$  of each latch-up path should be designed to be higher than the maximum voltage-difference between anode and cathode. In general 1.8V I/O applications,  $V_h > 1.8V$  is required for all possible latch-up paths. In this work, the latch-up free design can ensure the functionality and reliability of I/O circuits.

A 125°C  $V_h$  comparison between FinFET and planar CMOS is conducted on the conventional latch-up path A-B, i.e., PMOS to NMOS. The  $V_h$  and related characteristics are listed in Table 2. As compared to planar CMOS, FinFET technology shows the degraded  $V_h$  which is attributed to the worse pick-up resistivity. As shown in Fig. 1(c) (d), we can understand the fin structure reduces contact area and increases current crowding effect in pick-up regions. In addition, the contact conductance is limited by the epitaxy quality in source/drain regions. These factors give rise to the higher pick-up resistivity of FinFET devices. In FinFET technology, the degraded  $V_h$  of conventional latch-up path A-B still can pass the  $V_h$  requirement for general 1.8V I/O circuits (Table 2). For high voltage applications, the baseline design should be improved, which will be discussed in Section IV.

Table 1: Anode-cathode combinations of DNW-induced latch-up paths.

Anode to Cathode	Possible Latch-up Path
A-B	P+/NW/PW+Psub/N+
B-D	P+/PW+Psub/DNW+NW/RW/N+
C-B	P+/DNW+NW/PW+Psub/N+
C-D	P+/DNW+NW/RW/N+
A-D	P+/NW/PW+Psub/DNW+NW/RW/N+

\*RW is a P-type Well in DNW

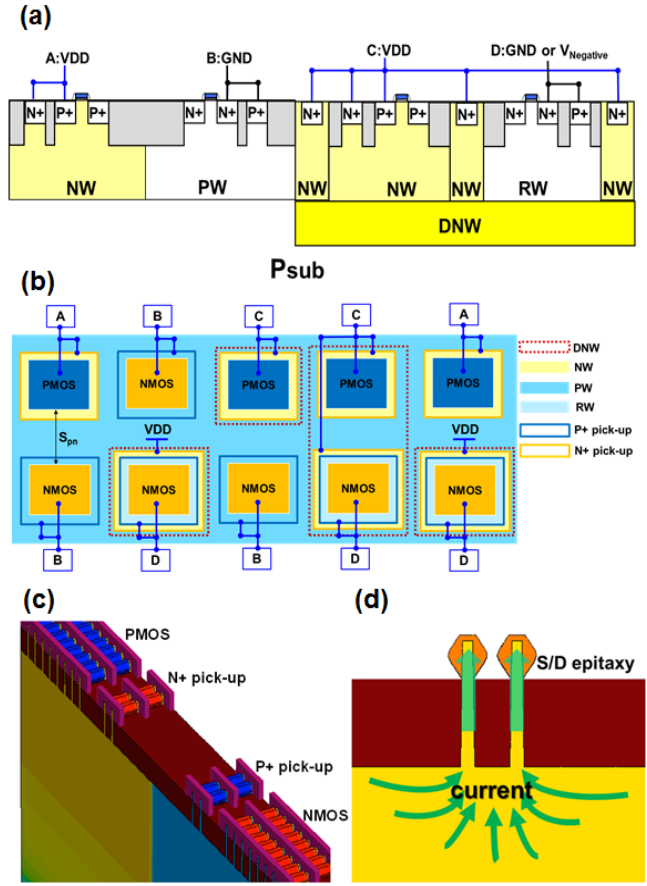


Figure 1: (a) Illustration of DNW-induced latch-up paths. (b) Layout view of test structures related to DNW-induced latch-up paths. (c) Conventional CMOS latch-up path (A-B). (d) Pick-up and current crowding illustration of FinFET devices.

Table 2: 125°C holding voltage comparison of conventional CMOS latch-up path A-B: FinFET vs Planar

Technology	FinFET	Planar
Holding voltage $V_h$ (V)	2.3V	4V
Pick-up resistivity (a.u.)	2.4x	1x
Well resistivity (a.u.)	0.97x	1x
$\beta_{pnp} \times \beta_{npn}$ (a.u.)	1x	1x

### III. DNW-induced Latch-up Characteristics and Temperature-dependence

To investigate DNW-related latch-up paths, the  $V_h$  of test structures and their temperature-dependence ( $75^\circ\text{C}$ - $175^\circ\text{C}$ ) are measured as shown in Fig. 2. As compared to conventional CMOS latch-up (A-B), path B-D, i.e., P-well to DNW-enclosed NMOS, has much lower  $V_h$ . With increasing temperature, B-D shows severe  $V_h$  degradation while other paths show saturated  $V_h$  curves. As a result, the  $V_h$  gap between B-D and other paths increases with increasing temperature. The poor latch-up immunity and detrimental temperature-dependence cause high reliability risk of DNW-enclosed NMOS structure.

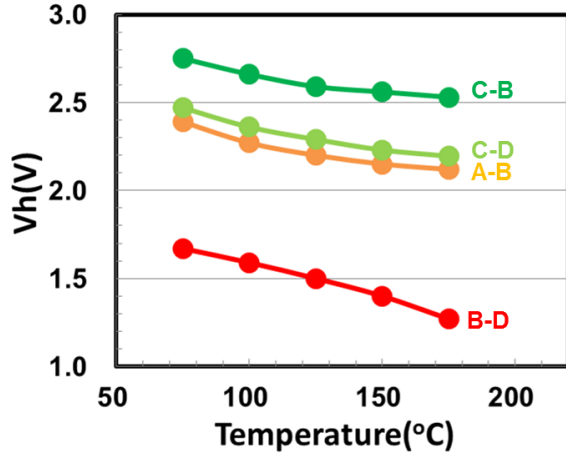


Figure 2: Temperature-dependent holding voltage  $V_h$  (experiment)

To understand the underlying physics of experimental results, a TCAD modeling is developed for quantitative analysis. Fig. 3 shows an equivalent circuit model and the definition of parameters (1)-(4) [13], which are used to extract the detailed latch-up characteristics from TCAD simulation.  $\Theta_{NW}/\Theta_{PW}$  represents the contribution of shunting resistance in N-well/P-well for latch-up prevention. The parameter  $\Theta$  directly reflects the influence of shunting paths in 3D structure without extracting the real resistance values.  $\beta_{npn}$  and  $\beta_{pnp}$  represent the current gain of parasitic NPN and PNP bipolar junction transistors (BJT), respectively. A general criterion for latch-up condition is expressed as an inequality (4). Holding current  $I_h$  can be defined as a total current level  $I_{total}$  when the latch-up criterion equals to unity. Fig. 4

shows the simulated characteristics of latch-up paths. Fig. 5 shows the corresponding I-V curves of PNP structure from high to low current conduction. Fig. 6 shows the current distribution of path B-D at low current ( $I_{total}=0.1\text{mA}$ ). Due to the large PW/DNW junction area, high electron current is injected to PW/Psub under a small forward bias. The high leakage  $I_{E1}$  from PNP BJT eliminates the shunting current  $I_{NW}$  and thus much lower  $\Theta_{NW}$  (Fig. 4). As compared to path A-B, the PNP structure of B-D has much larger emitter region in PNP BJT, i.e., PW/Psub instead of P+, and leads to one order increase of  $\beta_{pnp}$ . Similarly, the smaller base region in NPN BJT, i.e., RW instead of PW/Psub, contributes to the increased  $\beta_{npn}$ . The decreased N-well shunting current ( $\Theta_{NW}$ ) and increased current gain of parasitic BJTs ( $\beta_{pnp}/\beta_{npn}$ ) give rise to the shift of latch-up criterion to lower current level, which means the lower  $I_h$  and  $V_h$  (Fig. 4 and Fig. 5).

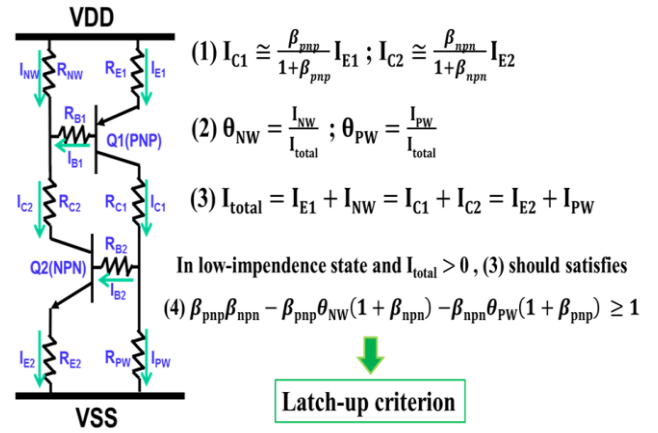


Figure 3: Equivalent circuit model and the definition of latch-up parameters.

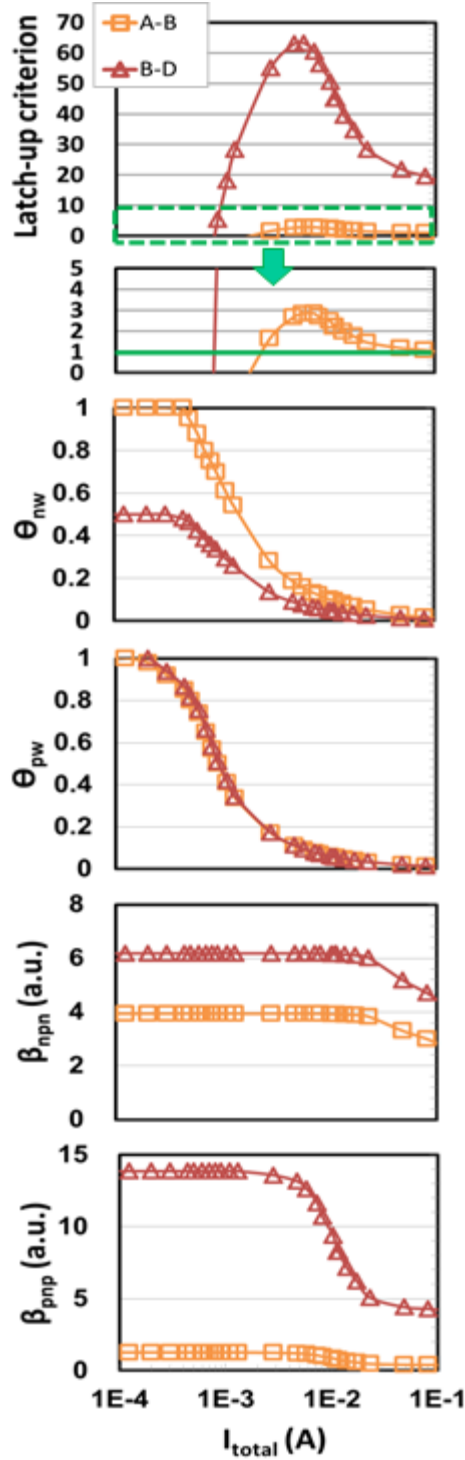


Figure 4: Detailed latch-up characteristics at  $T=125^{\circ}\text{C}$ : A-B vs B-D.

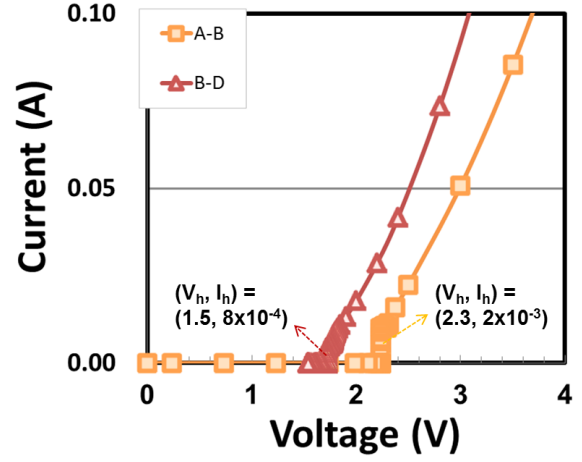


Figure 5: I-V curves of PNPN structures from high to low current level: A-B vs B-D.

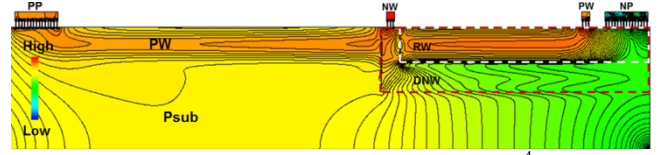


Figure 6: Current distribution of path B-D at  $I_{\text{total}}=10^{-4}\text{A}$ .

To study hot-temperature induced  $V_h$  degradation, detailed characteristics from  $75^{\circ}\text{C}$  to  $175^{\circ}\text{C}$  are simulated as shown in Fig. 7(a)(b). The behaviors of  $V_h$  and  $I_h$  at varied temperatures are extracted (Fig. 8(a)-(d)). At different temperatures, the slopes of  $V_h(T)$  and  $I_h(T)$  functions are shown in Fig. 8(b) and 8(d), respectively. The relationship between  $V_h$  and  $I_h$  is shown in Fig. 8(c). The simulated  $V_h(T)$  functions are well-matched to the experimental data (Fig 8(a)(b)). The arrows in Fig. 7(a)(b) indicate the shift of latch-up characteristics from  $75^{\circ}\text{C}$  to  $175^{\circ}\text{C}$ . In general,  $I_h$  and  $V_h$  decrease with increasing temperature because of the decreased shunting current ( $\Theta_{\text{NW}}/\Theta_{\text{PW}}$ ) and increased current gain ( $\beta_{\text{pnp}}/\beta_{\text{npn}}$ ). These temperature-dependences are consistent with empirical observations [14-15]. In comparison with A-B, B-D shows a significant decrease of  $\Theta_{\text{NW}}$  due to the dominance of increased PNP leakage current at higher temperature. Moreover, B-D shows more increase in the magnitude of both  $\beta_{\text{npn}}$  and  $\beta_{\text{pnp}}$ . These changes result in that B-D has an increasing  $I_h$  degradation rate with increasing temperature (Fig. 8(d)). By contrast, A-B has a decreasing  $I_h$  degradation rate with increasing temperature. Fig. 8 (c) shows the linearity between  $V_h$  and  $I_h$  in the investigated temperature range. It is found path B-D suffers a large  $V_h$  degradation by a small decrease of  $I_h$ . Consequently, a small increase of  $I_h$  degradation rate at higher temperature gives rise to the large  $V_h$

degradation rate on path B-D (Fig. 8(b)). Furthermore, we can understand the larger holding voltage gap  $\Delta V_h$  at higher temperature (Fig. 8(a)) is attributed to this detrimental temperature-dependence of path B-D.

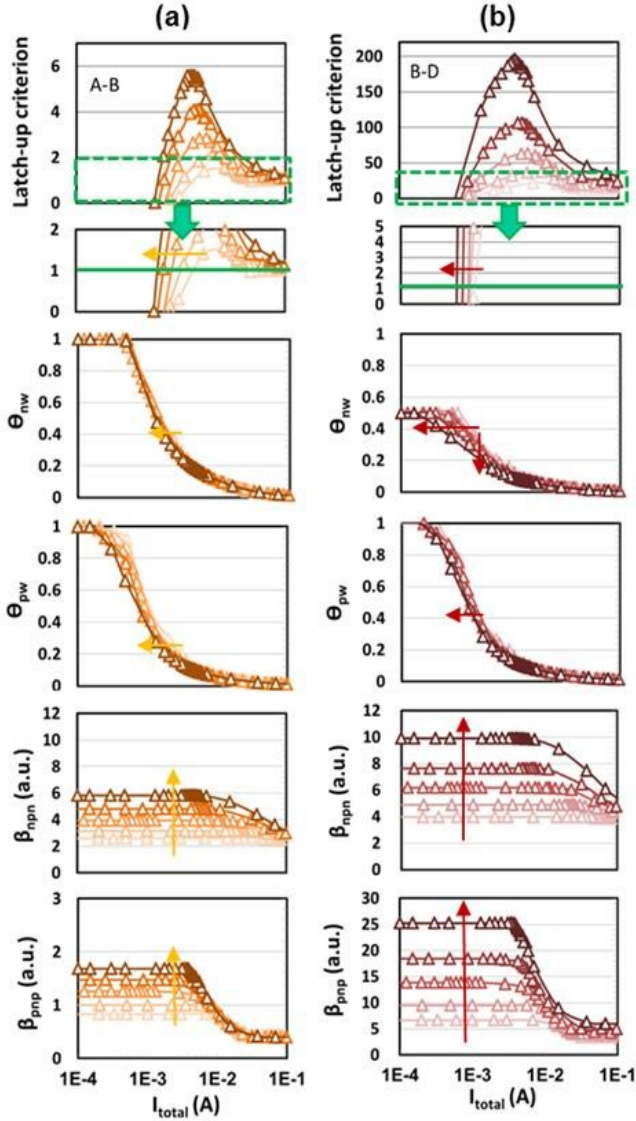


Figure 7: (a) Temperature-dependent characteristics of path A-B (75°C-175°C). (b) Temperature-dependent characteristics of path B-D (75°C-175°C).

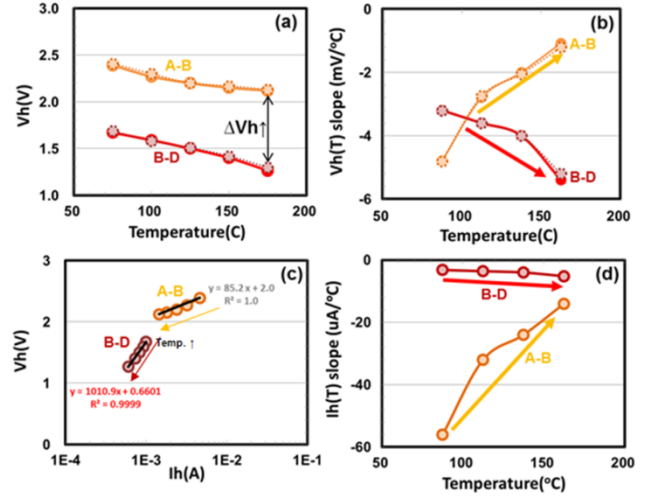


Figure 8: (a) Temperature-dependent holding voltage  $V_h$ . (b) The slope of  $V_h(T)$  at varied temperature. In (a)(b), the experimental results are marked by solid line, and the simulation results are marked by dotted line. (c) Holding voltage  $V_h$  vs holding current  $I_h$  at varied temperature (simulation). (d) The slope of  $I_h(T)$  at varied temperature (simulation).

## IV. Holding Voltage Improvement

For 1.8V I/O applications, path B-D, i.e., P-well to DNW-enclosed NMOS, has high latch-up risk due to the insufficient holding voltage ( $V_h=1.5V$ ) at 125°C. To meet the  $V_h$  requirement, the baseline design for path B-D should be improved. Here, varied design methods are explored. For conventional CMOS latch-up, enlarged anode-cathode spacing ( $S_{pn}$ ) can result in wider base region and larger base resistance of parasitic NPN BJT. These changes give rise to lower  $\beta_{nnp}$  and higher  $\Theta_{pw}$ , which effectively improve the  $V_h$ . Fig. 9(a) shows the experimental results of enlarged  $S_{pn}$ . Path A-B shows a significant  $V_h$  gain with increasing  $S_{pn}$ . Nevertheless, wider  $S_{pn}$  cannot effectively improve the  $V_h$  of path B-D. The  $V_h$  gain of B-D is less than 0.4V even with 3.6x  $S_{pn}$ . The poor  $V_h$  gain is attributed to no extended base effect in parasitic BJTs. Consequently, large anode-cathode spacing rule is required for path B-D, which significantly costs chip area. Guard-ring (GR) placement such as P+/PW or N+/NW insertion in the substrate is an effective design solution to suppress the turn-on of parasitic BJTs, which can improve the  $V_h$ . Fig. 9(a) shows path A-B has an significant  $V_h$  gain (0.6V) by GR insertions. However, GR insertions are not available in DNW-enclosed RW region as shown in Fig. 1(a)(b). This limitation makes it difficult for designers to suppress the turn-on of parasitic BJTs in path B-D.



In section III, we can conclude the low  $V_h$  of B-D is attributed to the higher current gain of parasitic BJTs and the decreased N-well shunting current. Therefore, the reduction of N-well shunting resistance is a practical way to save the poor  $V_h$ . Shunting resistance ( $R_{sh}$ ) consists of well resistance, fin/metal contact resistance, and backend metal resistance. As the device is scaled down to sub-20nm, contact and backend resistances dominate the overall impedance load which should be carefully controlled [16]. Here, we use TCAD to explore the NW/DNW shunting resistance effect quantitatively. Fig. 9(b) shows the simulated  $R_{sh}$  effect on  $V_h$ . As  $R_{sh}$  increases to 10x,  $V_h$  shows a significant drop of ~1V on both the path A-B and B-D. The severe  $R_{sh}$ -induced  $V_h$  degradation and variation indicate the control of contact/backend resistances is critical to the latch-up immunity of FinFET technology. With  $R_{sh}$  reduction to 0.1x, the  $V_h$  of B-D significantly increases to 2.8V. This indicates NW/DNW  $R_{sh}$  reduction can improve the latch-up immunity of B-D to the same level as the conventional latch-up ( $V_h=2.3V$ ). With further  $R_{sh}$  reduction to 0.01x, path A-B shows a continuous  $V_h$  improvement while B-D shows a limited  $V_h$  of 3V. Due to the limited  $V_h$  headroom of path B-D, enlarged  $S_{pn}$  is additionally required for high-voltage applications.

As compared to planar CMOS, FinFET technology suffers lower latch-up immunity, which is attributed to the higher pick-up resistivity. For conventional CMOS latch-up (path A-B), the  $V_h$  can be improved by re-designing the anode-cathode spacing ( $S_{pn}$ ) and Guard-ring (GR) placements. For DNW-induced latch-up, path C-B and C-D show higher  $V_h$  as compared to path A-B, which means the robustness against latch-up state in these paths can be ensured by conventional design. Nevertheless, path B-D suffers low  $V_h$  in FinFET technology which cannot be effectively improved by design solutions such as enlarged  $S_{pn}$  and additional GRs. Based on the above discussion, 0.1x NW/DNW  $R_{sh}$  reduction is the key for path B-D to achieve the  $V_h$  requirement. In the view point of layout design, increased pick-up area may be a solution for  $R_{sh}$  reduction. However, the limited pick-up area by RW regions is hard to achieve the desired 0.1x  $R_{sh}$  in practice. To solve this issue, the practical approaches include well-profile optimization, contact quality improvement, pick-up re-design, and metal-routing minimization should be considered. These approaches play a critical role in solving DNW-induced latch-up challenges in FinFET technology and largely rely on the efforts of process-design co-optimization.

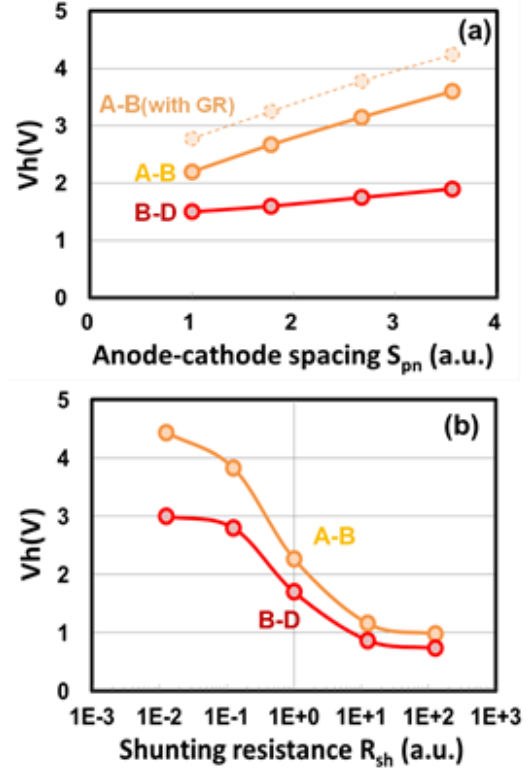


Figure 9: (a) Anode-cathode spacing  $S_{pn}$  vs.  $V_h$  at  $T=125^\circ\text{C}$  (experiment). (b) Shunting resistance  $R_{sh}$  vs.  $V_h$  at  $T=125^\circ\text{C}$  (simulation).

## V. DNW-induced PNPBPN Latch-up Mechanism and Prevention

A possible latch-up path A-D which consists of a P+/NW/PW+Psub/DNW+NW/RW/N+ (PNPBPN) structure, i.e., high-side PMOS to low-side DNW-enclosed NMOS, is investigated. In these test structures (Fig. 10(a)), a pair of P+/PW and N+/NW GRs is inserted between PMOS and NMOS. Fig. 10(b) shows the measured  $V_h$  and its temperature-dependence. As compared to the conventional latch-up path A-B, path A-D shows much lower  $V_h$  and severe hot-temperature induced  $V_h$  degradation. A PNPBPN structure consists of a P+/NW/PW+Psub/DNW+NW (PNPN) SCR and a DNW+NW/RW/N+ (NPN) BJT. The  $V_h$  of these components are also measured at  $125^\circ\text{C}$ . Fig. 11 shows the equivalent circuit and the corresponding  $V_h$  of each component. Based on the measurement, the low  $V_h$  (2.4V) of PNPBPN structure cannot come from the series of PNPN ( $V_h=2V$ ) SCR and NPN ( $V_h=5V$ ) BJT (Fig. 11). Here, we propose the PNPBPN latch-up mechanism by introducing a lumped circuit model of two PNPNs (Fig. 11). As the

negative trigger current is injected to substrate and collected by NW and DNW, these well potentials are decreased due to the large well resistance ( $R_{NW}/R_{DNW}$ ). When the base-emitter of Q1(PNP) is forward biased, the collector current flows to grounded substrate and builds up the potential of PW/Psub through a large substrate resistance ( $R_{sub}$ ). When the potential of PW/Psub is higher than that of DNW, both the Q2(NPN) and Q3(PNP) turn on. This causes high current injection to RW and further activates Q4(NPN). The lumped PNPNs form a stronger positive feedback, which results in lower  $V_h$  of PNPNPN as compared to conventional latch-up.

To prevent the activation of PNPNPN latch-up, the shunting resistance of DNW and PW/Psub should be substantially reduced to suppress the forward-biased PW/DNW junction. In this work, the trigger current level for PNPNPN structure is around a few hundred mA. Therefore,  $0.1 \times R_{sh}$  is reasonable for preventing PNPNPN latch-up during chip operation. In FinFET technology, the latch-up susceptibility of DNW-induced PNPNPN structure is highly correlated to the DNW/NW shunting resistance which should be carefully controlled.

The effect of enlarged  $S_{pn}$  is also investigated in PNPNPN latch-up. Fig. 12 shows the experimental results. In comparison with path B-D (Fig. 9(a)), the  $V_h$  gain of path A-D (Fig. 12) by wider  $S_{pn}$  is more significant. The stronger  $V_h$  gain is attributed to the extended base region of Q2(NPN) in lumped PNPNPN structure. With the aid of  $S_{pn}$  effect, the  $V_h$  of PNPNPN can be adjusted to meet the voltage target. While the spacing rules of path A-D should be larger than that of conventional CMOS latch-up for compensating the lower  $V_h$ .

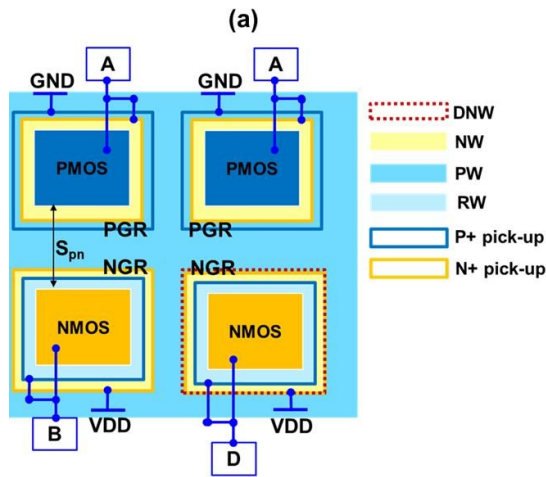


Figure 10(a): Layout-view of test structures with GR (path A-B and A-D).

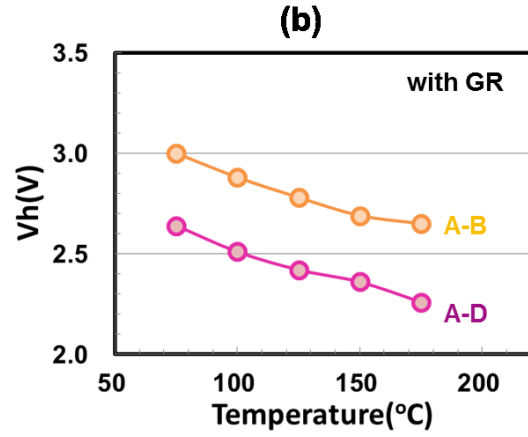


Figure 10 (b): Temperature-dependent holding voltage  $V_h$  with guard-ring GR: A-B vs A-D (experiment).

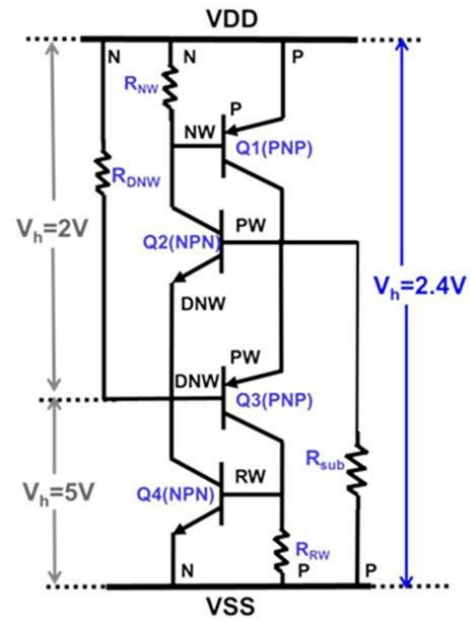


Figure 11: Lumped circuit model of PNPNPN structure and the corresponding  $V_h$  of PNPN SCR and NPN BJT components.

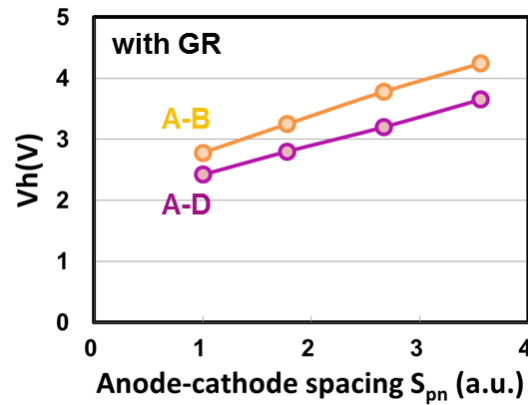


Figure 12: Anode-cathode spacing  $S_{pn}$  vs.  $V_h$  at  $T=125^{\circ}C$  (experiment). A pair of GRs is inserted between PMOS and NMOS.

## VI. Conclusions

DNW-induced latch-up paths in bulk FinFET technology are investigated. DNW-enclosed NMOS in PNP and PNPNP structures causes low holding voltage with a detrimental temperature-dependence. Detailed latch-up characteristics and their temperature-dependence are disclosed through a well-established TCAD modeling. It is found the low latch-up immunity is attributed to high current gain and junction leakage of parasitic BJTs formed by DNW-enclosed NMOS structure. Varied methods are explored for holding voltage improvement. By DNW/NW  $R_{sh}$  reduction (0.1x), the holding voltage of P-well to DNW-enclosed NMOS can be improved to meet the latch-up free criterion of 1.8V I/O. In addition, DNW-induced latch-up susceptibility in PNPNP structures can be significantly suppressed. This work pinpoints the reduction of shunting resistance plays a critical role in solving DNW-induced latch-up challenges in FinFET technology, which largely relies on the efforts of process-design co-optimization.

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