HV Latchup - Power Analog ICs Co-Design with Block Level Verification

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Abstract - - Power Analog ICs which contain both high voltage and low voltages cells require a unique approach to achieve latchup robustness. A methodology was developed to allow both schematic and layout block level latchup verification automation as applied to HV Latchup in Power Analog ICs design. The methodology enables co-design between schematic design and layout design, improving silicon success as well as shortening the design cycle.

I. Introduction

Power Analog ICs used in power management and automotive applications may have voltage ranges of more than 100V. The design of these power analog circuits using high voltage(HV) CMOS or BCD process technologies requires a complex set of HV latchup rules since the higher voltage domains require larger spacings and additional guardrings considerations. These rules require advanced floor planning involving both design and layout engineering. The layout requirements can increase circuit area which is counter to the need to maintain or increase cost margins. A co-design approach coupled with latchup verification tools at each part of the design flow is required.

The methodology used for HV latchup rules in power BCD processes in this study is based on the injector-victim interaction [1]. The injector is a silicon junction region connected to an I/O pin which can inject carriers into the substrate while the victim junction collects the injected carriers. These objects are identified in substrate isolated regions(pockets) of either N-type epitaxial region(N-epi) or n-well pockets. To avoid a HV latchup condition, the device spacing requirements may necessitate separation of these layout features by up to 300 μm depending on the type of pad connection, specific type of device pocket, latchup test temperature, voltage rating, and collection ring types along with their electrical connection resistance. This generates a set of interacting rules that can hardly be verified using manual checks, thus requiring automated latchup verification.

Automated latchup verification historically has required the completion of the layout to create the top-level cell containing the compete design hierarchy. At this point, the layout includes all the required external pads and functional blocks to match the schematic. The identification of the injectors and victims relies on the verification tool to check for any junction connected to an external pad. At certain levels of IC complexity, it becomes impractical to approach the layout design without proper placement and regular verification of the injectors (aggressors, emitters) and victims(collectors) in the circuit blocks as well as the corresponding placement of the collection rings. While the verification of the final full chip top cell layout with latchup verification is still required, it is hardly an effective design flow. The latchup checks, performed at the final stages of project completion (pattern generation) can generate floorplan errors requiring major changes to the physical database. Large scale redesign is hardly possible in the realistic timeline that would allow re-arranging of entire circuit blocks to resolve the verification conflicts. Therefore, block level verification is critical, particularly in case of modular, highly integrated IC's. These functional blocks may become library elements (IP blocks). which can also be re-used in future designs.

In this study, a novel co-design approach is implemented to enable automated verification steps on individual block levels starting from the schematic stage, rather than the final IC layout. The diverse content of material is organized as follows. First an outline of HV latchup rules is followed by the

reasoning and description of the main verification principles to be applied to the IC block level. In addition, some verification examples are presented to demonstrate this methodology.

II. HV Latchup Rules

Conventional latchup (LU) in low voltage (LV) CMOS processes can be subdivided into two main types, CMOS *I/O* latchup and Core latchup [2]. CMOS *I/O* and Core latchup essentially create conditions for a turn-on of a parasitic silicon controlled rectifier (SCR) structure formed in IC layout as the result of either current injection or overvoltage testing. In the case of *Core* latchup, the parasitic SCR structure can be formed by the high side (HS) PMOS with the source acting as the SCR p+-emitter and low side (LS) NMOS with its source acting as SCR n+-emitter. A forward biased junction in the remote I/O circuit block can become an injection source. In case of I/O latchup, the parasitic p-n-p-n SCR structure is already present in the I/O circuit block. One or both of the drains of the NMOS-PMOS driver pair are connected to an external I/O pad. During the latchup test, where the external pad is biased above VDD or below ground, carriers are injected directly into the structure. The typical LV latchup spacing rules for *I/O* are mainly focused on disabling the victim SCR with better isolation of emitter by bases (represented by well ties). The spacing rules are set to reduce the gain of n-p-n and p-n-p BJT that create the SCR. For *Core* latchup, a typical approach is to separate the core circuit from the injectors by a specified distance. The LV rules for the pocket spacing are usually satisfied with the minimum spacing as describe in the process design rules. A minimum width guard ring or guard bar is adequate to collect the injected carriers to reduce LV latchup risk.

In the case of high voltage (HV) BCD power processes, the basis of the spacing rules is in principle different. This is because both *I/O* components and the core circuits are typically isolated in separate N-pockets(n-wells). The focus of latchup spacing rules is N-pocket to N-pocket isolation and corresponding collection rings. The physical structure that represents the latchup scenario in HV BCD processes is an NPN formed by the LS pocket (acting as emitter), p-isolation (acting as p-base) and the HS n-pocket (acting as collector) (Fig.2). At minimum layout spacing rules, such an NPN structure cannot sustain high blocking voltage during the latchup injection conditions, thus requiring some complex spacing rules must be applied These rules are a function of the injection current level, test temperature, the pocket-to-pocket voltage and are injector and victim type specific.

There are two major types of latchup in HV BCD processes known as highside(HS) and lowside(LS) latchup. Figure 1 describes the basic conditions that defines these injections sources.

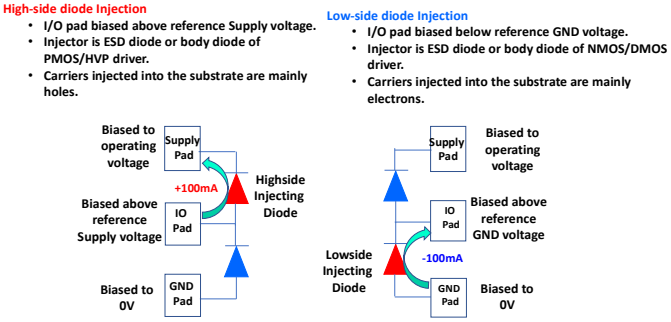

Figure 1. Definitions of low and high side injection

Highside latchup, which can occur when the holes are injected from the HS pocket by a forward biased junction pulled above the HV supply (Fig.2b) and LS injection when the electron injection occur from the forward biased junction connected to I/O junction pulled below the ground (Fig.2a). The corresponding pockets plays the roles of victim (Fig.2).

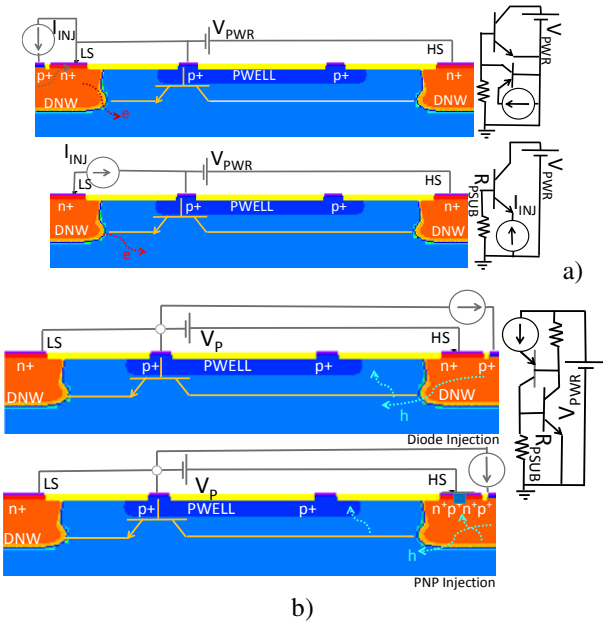

Figure 2: Cross-section and schematics to illustrate the DNW to DNW negative low side electron injectors latchup cases with the DNW and the diode connected to the I/O pin (a) and positive high side hole injection with P-type ring collection for the injecting diode without and with an additional P+ collector (b)

This generates spacing rules that are substantially more complex in comparison with the previously discussed LV CMOS latchup spacing rules. For example, in case

of the LS latchup, the injection level and the corresponding spacing rules depend on whether either the pocket is biased below the substrate ground level (Fig.2a upper cross-section) or the injection current is induced in the diode inside that pocket connected to a power supply (Fig.2a lower cross-section). In case of HS injection, a similar example can be made for the injectors having additional P+ collector (false p-collector) region in the n-well region directly connected to the n-well region. The result of this connection is a substantial reduction in the hole injection. (Fig.2b, lower cross-section).

The regions(victims) which collect the injected charge are defined as any cathode(n-junction) connected to supply, ground, or I/O pins. A HS victim would be an n-well region connected to ground or IO. These regions would collect holes. This definition can be extended to an n-well region connected to a 1V or 5V supply, since the voltage drop across the interconnect from the supply to the pocket may be large enough to make the region essentially connected to ground potential. These created many more HS victims in the layout. The LS victim on the other hand is a n-well region connected to supply or IO and would collect electrons. The HV spacing rules are a function of the injector type. The spacing required to reduce HV latchup risk increases with voltage. Table I shows values for the relative separation between a HS injector(anode) and a HS victim(cathode) as a function of HS injector voltage. A HS injector biased at 80V needs up to 15X more spacing distance from a HS victim when compared to 10V HS injector.

HS Injector Voltage	Relative HS Injector to Victim spacing
10V	1
30V	3.5
50V	10
80V	15

Table 1. Example HS Injector to Victim relative spacings.

Guard rings are added to collect the injected charge which improves the overall latchup robustness of the layout. The guard ring is typically a donut shape of N-type diffusion connected to supply for lowside collection or a P-type diffusion connected to ground for highside collection. The collection efficiency of the guard rings also critical. Additional guard ring checks include the primary N-type guard ring and secondary guard ring existence, width, interconnect resistance, and voltage level. This secondary guard ring may include N-type epitaxial or n-well ring connected to a supply or an unbiased ring [3] placed around the LS injectors. Correspondingly, a P-type ring is placed around HS injectors and HS victims and connected to the ground pad. In HV Power Analog devices, many times an internal voltage regulator is used for the LV circuitry. Guard rings attached to these supplies may be much less effective depending on the regulator current capacity. Both design and layout engineering needs to be consider these limitations as part of an effective co-design effort.

For HV BCD designs, a substantial test effort is required due to the coverage of multiple high voltage domains, collection rings structure and self-heating effects at high detection current during the injection. Establishing and verifying such latchup layout rules increasingly becomes a crucial task to ensure latchup-immune circuit design guidelines per JEDEC78 standard(+/- 100mA) [4].

III. Latchup Verification Approach using Parameterized Cells

The design process utilizes a hierarchical approach. Functional blocks are created and assembled to form the complete IC. The capability to analyze the latchup vulnerability at all levels of design hierarchy needs to be incorporated within the verification methodology. Historically, latchup verification was performed on the physical layout file generated from the top cell of the hierarchy. External pins were automatically identified by topological checkers using the passivation opening and possibly the inclusion of text labels in the physical layout [5,6,7]. This does not address schematic information nor can it be used at the block(cell) level where cells with passivation openings may simply not exist. The diffusions regions(junctions) connected to pads (external ports) that will be subjected to injection need to be identified as injector and victim location is critical for latchup analysis. A novel method was developed to add information detailing the external pad connection information as well as the pin operating voltage to both the schematic and layout. Thus, the first step in the desired co-design methodology is implementation of a method of annotation of the block-level schematic with information needed for latchup analysis. The co-design methodology entails the review of all the latchup related aspects for the design from the schematic to the floorplan through knowledge of the injection sources. Previous art relied on review by staff with specific latchup knowledge

which occurred in the latter stages of the design flow. One of the main constrains is due to varying levels of latchup expertise between the circuit designers and layout engineering teams. The trend toward the automatic place and route of blocks within the hierarchy is also adding to need for latchup review earlier in the flow.

To address the concerns outlined above, an innovative design element was added to the process library. The latchup information would incorporated into the design using a special parametrized cell (padnet). A parameterized cell [9] is a component whose functionality depends on one or more parameters and can have properties for both layout and schematic usage. The library cell or padnet exists as code which creates the correct structure depending on the input parameters. The padnet consists of three principle properties, the pad type, voltage value, and metal layer. The pad type, which is a label describing the pad function, what type of external pad the net is connected to, at the block level,. The basic pad types are input/output(IO) signal pins, supply pins (VCC), and ground reference(GND). The padnet Pcell can also be used to create pad types which can be used to address special functions, such as internally generated supplies as described previously.

The operating voltage of the pin is another key property of the padnet. The assignable voltage values labels match the Process Design Kits(PDK) range for the allowed operating voltages of the devices for that process flow. Examples of the voltage values might include 2V, 5V, 48V, and 80V. The metal layer property details what metal layer is used to place the labels of pad type and voltage type. In the layout, the metal layer property creates a non-drawing layer used to associate the pad type and voltage labels with a drawn metal layer. In this manner, the labels are attached to the correct metal layer. Metal layer is selectable from the available metal options as defined in the (PDK). The pad type and voltage values exist as properties which can be interpreted by the verification tool, in this case Calibre® Mentor PERC [10].

The padnet generation is controlled by the input parameters derived from the graphical user interface(GUI). The GUI (Fig. 3) allows the user to select the desired values for pad type, voltage value, and metal layer. The parameters, through use of a pulldown menu, offer a set of discrete values as discussed previously. The placement establishes latchup related properties in both the block level schematic and layout views.

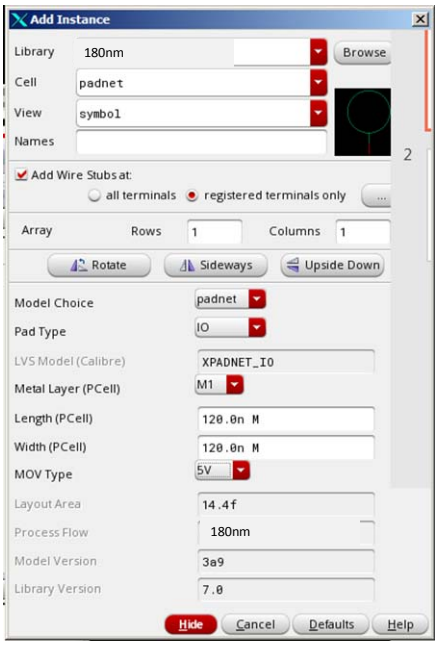

Figure 3: Padnet Pcell GUI

The pad type, voltage, and metal layer are assigned as the padnet Pcell is instantiated into the schematic. Figure 4 shows a representative HV block schematic view with three padnets symbols added to the nets which are connected to external pins. The padnet Pcell symbol displays the values of the pad type and voltage value.

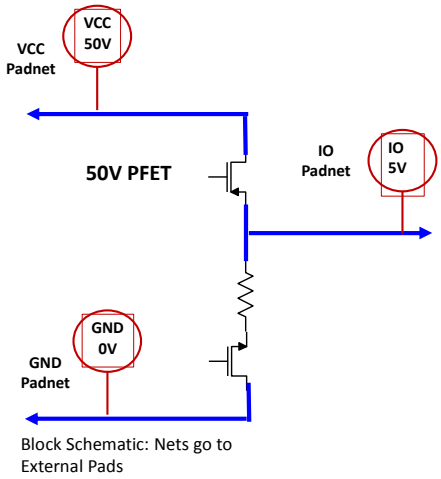

Figure 4: Padnet Pcell placement schematic example.

The layout view for the schematic is generated from either a schematic driven layout tool or from fully

custom polygon placement. In the first case, tools such as Cadence® Virtuoso Layout Suite XL will generate the layout based on the source schematic. The padnets Pcells, as part of the reference library, are placed along with the other circuit elements in the schematic. The padnets have a connectivity property which allows the layout engineer to view the connections between the schematic elements in real-time. Fully custom layout requires the padnets Pcells layout view be placed in block layout views based on the block schematic. The padnets, with its corresponding properties in both layout and schematic, are compared using the layout versus schematic (LVS) tool. LVS insures a consistent placement in both views, preventing pad type and voltages values form differing between layout and schematic views. The latchup verification using padnets must be completely free of shorts on any net for the results to be valid.

The padnet Pcell are recognized as devices in both the schematic and layout views. The verification tool extracts the pad type and voltage values as net properties in both the layout and the schematic. The schematic is analyzed using the latchup verification tool which locates devices which may be potential latchup injectors or victims. These devices are now noted in both schematic and layout considerations. Net types are created based on their connection to external IO pads, VCC pads, and GND pads as defined by the padnet assignments. Once assigned, the net information can be used to apply the latchup rules to either schematic or layout and at any level of the design hierarchy.

The padnet information is propagated throughout the layout view as dictated by the connectivity statements in the verification tool. These statements define how the metal, poly, and silicon are connected. Each net within the layout will also have a padnet associated with it.

The latchup specific definitions for the injectors and victims are applied to the devices, as defined for each Process Design Kit (PDK). If the layout is generated without the use of schematic driven layout, the padnets can be instanced as a layout elements manually. These rules assign latchup properties based on device pin connections to the pad types and voltages assigned as net types. In the layout case, the injectors and victims are defined in terms of the layers which comprise each device. A simplified set of such definitions are shown in Table 2.

Lowside Injector	**Lowside Cathode connected to IO padtype.** **Lowside Anode Connected to GND padtype.**
Lowside Victim	**Lowside Pocket connected to VCC or IO padtype.**
Highside Injector	**Highside Cathode connected to VCC padtype.** **Highside Anode Connected to IO padtype.**
Highside Victim	**Highside Pocket connected to GND or IO padtype.**

Table 2. Injector/Victim classification scheme.

The cathode would be any N-type isolation region(n-well) or any N-type diffusion in p-well whereas the anode would be a P-type diffusion in n-well. The above definitions are translated to code using the pad types and voltage level information which now exists in the netlist. The PERC code assigns the extracted device to the role of injector or victim. For example, the basic NMOS transistors pins are checked for connection to specific pad types, as derived from the padnet. An NMOS transistor is assigned to the role of lowside injector if the drain is connected to IO pad type and if the body is connected to GND pad type. The drain to body diode becomes the injecting junction during negative current injection on the drain pin. This classification defines all the latchup related regions in the hierarchy. In a similar fashion, voltage can be assigned to each net.

The devices in the schematic are annotated and flagged in the output of the verification tool as either victims or injectors. The voltage from the padnet Pcell are now also associated with the victims or injectors. All this information is also known for the layout based latchup checks.

IV. Latchup Verification on the Block Level

The padnet Pcell methodology can now be applied to block or top-cell level. The block level latchup verification flow is shown in Figure 5. The first step is defining the role of each pin as a supply, I/O, or ground

and the operating voltages for those pins. This pin function now defines the pad type and voltage level for the nets connected to external pins. The schematic is created and the latchup properties are added using the padnet Pcells. Once the block schematic is complete, the verification software is run to identify devices which may require placement consideration in the layout due to latchup guidelines. At this point all the elements of concern regarding latchup sensitivity are now identified. The high voltage devices are annotated for spacing concerns and required guard ring placement.

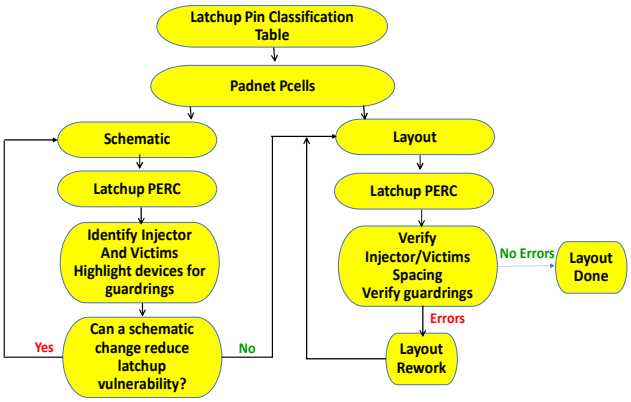

Figure 5: Block level latchup verification flow.

A check is also performed on the padnet for consistency of pad type and voltage throughout the hierarchy for each net. The devices on each net are checked against the latchup parameter definitions and identified accordingly as discussed in section III. The resultant database can be viewed using Calibre® RVE. A sample RVE output is shown in Figure 6. The check pinpoints a device that is a lowside injecting diode whose placement may need special consideration and review.

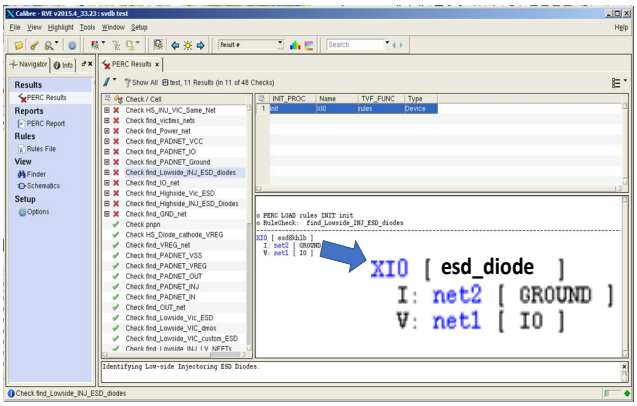

Figure 6: Devices flagged as Injectors and Victims.

To further illustrate the usage, an example schematic, shown in Figure 7, contains a block with all the placements of ESD devices located near the external pad cells. The verification tool is run on this block to identify all the latchup elements in the schematic. A resultant output is also shown in Figure 7. The high voltage injectors are highlighted by the yellow boxes, while the high voltage victims are indicated with red boxes.

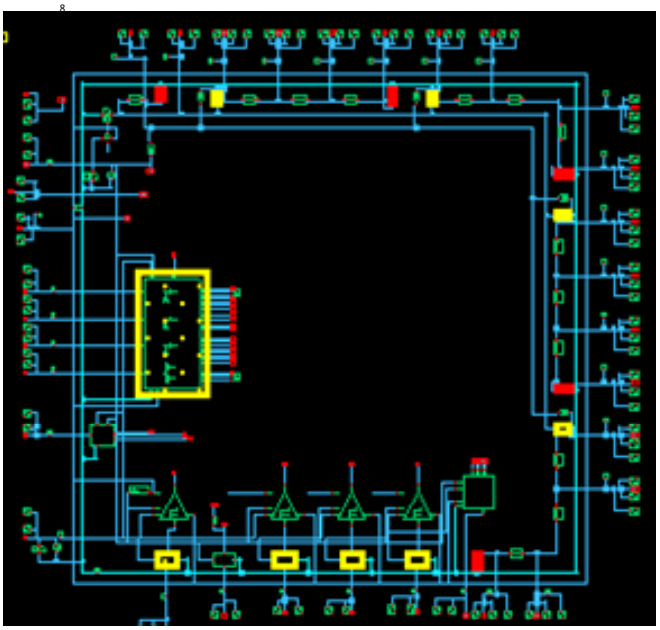

Figure 7: Highside Injectors(Yellow) and Victims(Red) flagged in the schematic.

Even though no topological layout input information is present at the schematic level, highlighting these devices in the schematic enables the appropriate future

considerations regarding the placement of these devices in layout. It is now possible to make schematic changes to reduce the latchup vulnerability since the design engineer is aware the latchup considerations earlier in the design flow. A very simple example would be the insertion of a series resistor between the injecting device and the external pad. The device can effectively be removed from the role of injector and thus remove as source of any potentially large spacing requirement for the layout placement, The PERC based schematic checker can further output information that can be analyzed by a program used to add text to the instances in the schematic. This additional text indicates whether the device is an injector or a victim or both as shown in Figure 8. This can be done to the schematic elements by the addition of properties to these schematic devices.

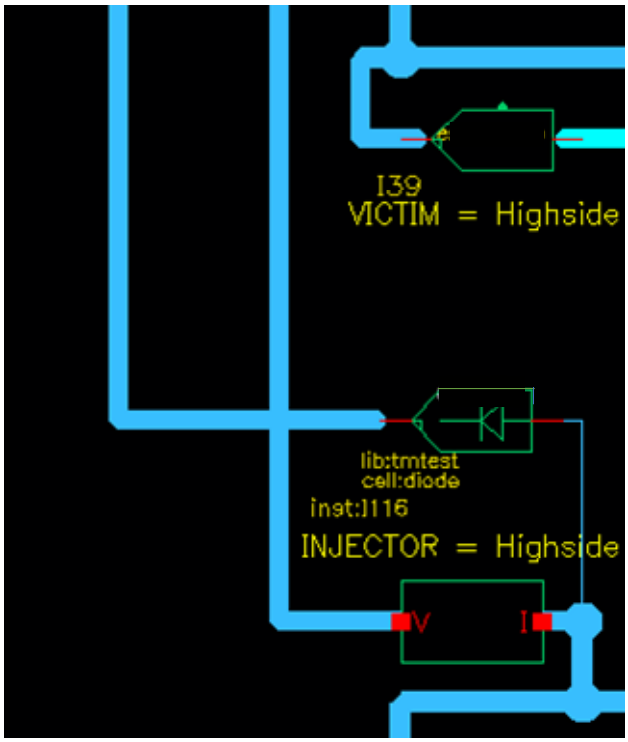

Figure 8: Schematic with properties added and displayed based on latchup check outputs.

It is also possible, if Cadence® Virtuoso Layout Suite XL is used, to create a constraint in the schematic to assist with placements of the devices in the layout. In figure 9, two 65V diodes are identified as a highside injector-victim pair. A physical constraint can be added in the schematic between Diode1 and Diode2. In this example, a minimum distance is set between the two devices. The distance constraint is translated to the layout shown in Fig 10. The yellow line and box indicates a physical constraint is present. The layout tool, Virtuoso XL, will not allow Diode 1 to be placed closer than the physical constraint value to Diode 2 if the rule is enforced. Schematic identification also allows for some level of automation specifically for guarding additions as well. Once the schematic latchup tool identifies an injector or victim device for example, a property can be set on that device to place the correct guard ring around the injector as part of the device Pcell.

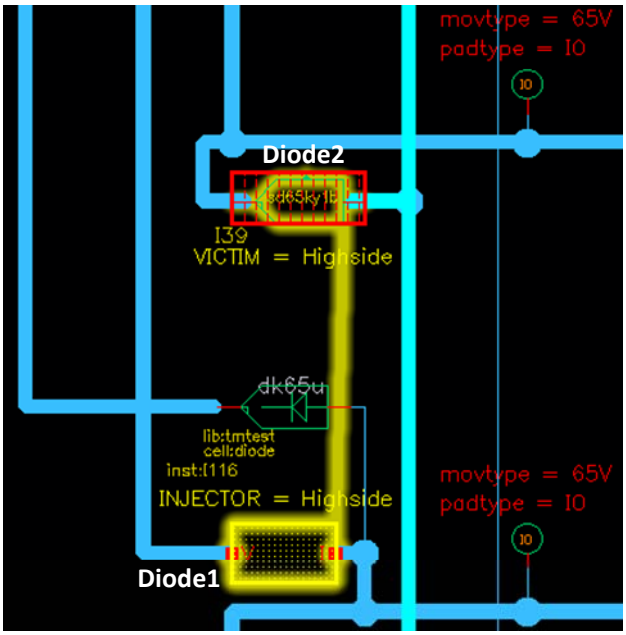

Figure 9: Highlighting the instance constraint added to a schematic.

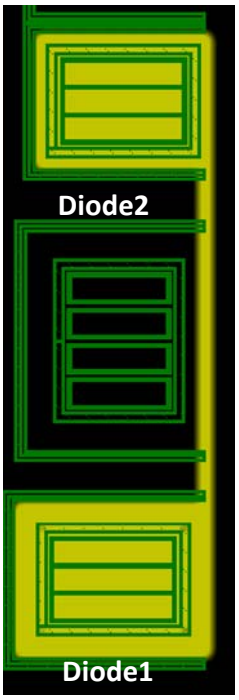

Figure 10: Distance constraint visualized in the layout of the devices constrained in Figure 9

Following the completion of the schematic, the layout of the physical representation can begin incorporating all the latchup properties established within the schematic. Once the block level layout is a complete and matches the schematic correctly, all the latchup checks, including the spacing rules are subsequently evaluated using the instantiated padnets in the layout database. Any errors can be addresses between the schematic owner and the layout engineer using the common latchup terminology developed between the two database views.

The identified injectors, victims, and nets can easily be displayed. The location of injectors and victims can be highlighted at the block level in the physical database. Figure 11 demonstrates HS injector(red) locations for a block cell based on the schematic in Figure 7.

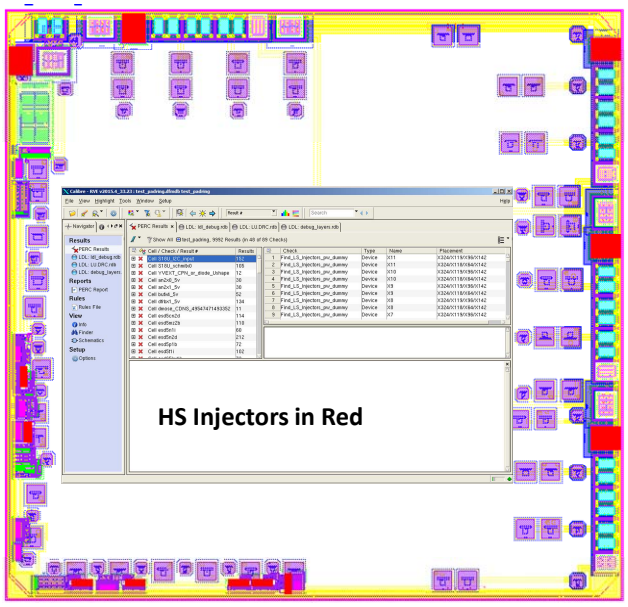

Figure 11: Block layout showing HS injecting diodes(red)

One of the additional advantages of the padnet usage in the schematic is the identification of devices which may not have been considered as injectors or victims, or merely overlooked. The N-type pockets of passive devices, for example, may be connected to an IO pin. These pockets will inject during negative stress. Another example might be an N-channel transistor used as a highside device (source follower). The body diode of such a device, with connection to IO and the N-type pocket connected to supply, will injection upon the application of positive current injection with levels of +100mA. Previously these devices may have only been detected during the latchup verification of the physical design database. The presence of these devices may now generate floor planning or schematic changes not previously considered. Devices which may indirectly contribute the latchup vulnerability [7] may also be augmented with padnets. The padnet can be used to avoid creating a connection through these devices in the verification code; thus, allowing design to check schematic options for latchup vulnerabilities. The placement of elements sensitive to injected current from power arrays can be easily reviewed by cross function teams to insure a robust latchup tolerant placement. The latchup verification output simplifies the review process by identifying the key elements in both layout and schematic.

High voltage lowside injection devices may require additional N-type collection guard rings. The schematic analysis can also be used to flag devices for guard ring usage by setting a property on the injecting

device. The layout engineer is thus notified of the need to place this additional guard ring around this device.

Previously the requirements for guard rings and the associated checks were detected in the finished layout, possibly requiring schedule delay for additions or modifications.

This methodology has been used on multiple high voltage products across both 90nm and 180nm. Several violations were found and subsequently fixed at the block level. First silicon success was achieved on these designs. This has saved an average about .25 man-months of layout redo on some recent designs.

V. Top-level Latchup Verification

It should be noted that even if all latchup errors are fixed at the block level, errors can still occur at the top level due to block to block interaction. As it can be seen in Figure 12, all the individual blocks now share neighborhoods. The placement of N-type pockets connected to ground within a block creates latchup concern as these regions as victims for highside injection. There may be no concerns if the block does not contain highside injectors, however the top cell floor planner can now be aware as this block may be placed near a highside injector in the overall hierarchy. Spacing and guard ring features checks can be performed on the layout both at the block and at the full chip top level cell. As discussed in previous works [7,8], the resistance of the interconnect from the pad to the guard ring is critical along with the interconnects ability to carry enough current to these guard rings during injection and application usage. The resistance of concern is from the pad to the guard ring, so the final checks for the path resistance are done at the top-level.

The guard rings are recognized by shape, no special marker layer is used. The guard rings are found in the layout and classified as a device with a pin. The guard rings are checked for width as well as connection to either a VCC or GND pad type, generating a flag if that connection is missing.

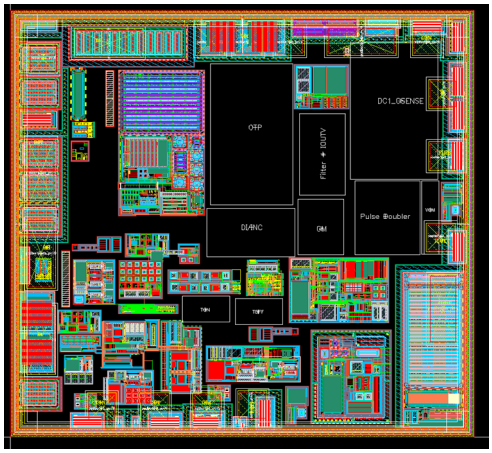

Figure 12: Blocks assembled in top-level cell

The voltage value from the padnet assigned to this net is also checked to verity the correct voltage rated pocket (n-well or deep n-well) is used; specifically, no high voltage connection is made to a low voltage pocket. Calibre PERC Logic Driven Layout Point-to-Point Resistance (LDL P2P and Current Density (LDL CD) are used to check the connection from the pads to the guard rings. This type is analysis is covered in detail in other studies [7,8].

VI. Conclusion

In summary, HV power analog IC latchup co-design methods have been implemented in the verification of the HV latchup rules using both Calibre® PERC™ verification tool along with Cadence Virtuoso XL. A co-design methodology has been used to analyze both the schematic and layout views on either the blocks within the hierarch or the top-level cell. This is achieved by introduction of parameterized cells in the design environment that incorporates latchup specific properties used in both the schematic and layout of the high voltage IC. By using an algorithm that combines the topological checks with electrical verification, a lower level latchup check is enabled at every level of hierarchy. As a result, a semi-interactive IC layout co-design has been enabled from the initial floor planning stage, under flexible definition of the blocks, followed by the multiple automated runs to check the layout results of the placements. This novel approach has enabled the analysis of the quasi real-time layout options and trade-offs including the circuit redesign options.

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