Charged device discharge measurement methods in electronics manufacturing

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Abstract – Electrical components with a lower CDM ESD immunity can require additional protection methods in manufacturing. Discharge current measurements and electromagnetic pulse detection gives valuable data for more detailed ESD risk assessments. However, both methods require sophisticated tools and trained personnel to get accurate data for control purposes.

I. Introduction

Decreasing charged device model (CDM) immunity of ICs has been one of the concerns of electronic industry. These electrostatic discharge (ESD) sensitive ICs can bring new challenges to electronics manufacturing where ESD risks have mainly been estimated by measuring electrostatic potentials, E-fields, and charges in the process area [1]–[8]. In addition, ESD events have been detected with indirect methods by using electromagnetic interference (EMI) detectors and by using oscilloscopes and antennas. Charged device ESD risks have also been reduced in practice, for example by choice of a lower limit of resistance for materials that make contact with the device in order to reduce ESD current levels [9]. This paper does not consider this approach, instead, it focuses on measurements for evaluation of charged device discharge risks.

Each measurement method has its own benefits and weaknesses. Especially, the measured quasi-static voltage is subject to change with DUT position and capacitance changes. Charge measurements are less prone to variation, but neither the measured voltage or charge values can predict the shape of the discharge current waveform. In addition, EMI measurements are challenging in electronics manufacturing with uncontrolled EMC noise sources, and noise can be indistinguishable from ESD when using simple EMI detectors.

With fast CDM type discharges, the positive and negative peak current and pulse rise time are the main parameters defining damage risks [10][11][18]. Therefore, charged device ESD risks should ideally be evaluated in manufacturing by measuring real ESD current waveforms. This is typically the only way to get the peak current and pulse rise time data for detailed analysis. These values could be compared to IC specific CDM qualification test current waveform results to estimate possible ESD risks. Unfortunately, accurately capturing the current waveform can be nearly impossible in working process equipment and has many uncertainties, requires fast oscilloscopes, wide bandwidth current probes, and competent specialist personnel. The presence of the measurement equipment is likely to alter the ESD conditions and the waveform that is to be measured. In addition, the CDM peak current or pulse rise time information is not currently available in component datasheets.

One more challenge comes after ICs are soldered on a printed circuit board (PCB). In this case the discharge event can be classified as charged board event (CBE) with varying discharge path *RLC* parameters. The measured ESD current waveforms cannot be meaningfully correlated with CDM qualification data. Only tailored case specific stress tests can produce more accurate test data for an ESD risk assessment [12].

In common practice, charged device ESD occurring in a manufacturing situation is often referred to as "CDM" ESD. In fact, the CDM waveform only occurs in the CDM ESD qualification tester. In this paper we recognise this difference and restrict our use of the term "CDM" to the CDM test performed in the tester or in the laboratory. For ESD occurring in the real world we refer to charged device discharges or charged device ESD.

CDM withstand voltages have a low correlation with electrical failures in electronics manufacturing when the CDM immunity of ICs is more than 250 V [2]. However, if the ESD immunity further decreases, the most sensitive I/Os can define the risk level and additional control measurement methods will be required.

In this study, methods of evaluating ESD sources, discharge current and EMI measurement methods are analysed in more detail.

II. Research methods

A. Measurement tools

CDM and charged device discharges in manufacturing have previously been analyzed with current, charge, and voltage measurement methods. In this study a commercial CDM test head with 36 cm^2 size ground plate and similar current probes as presented by Gärtner and Stadler are used for discharge current measurements [5]. These probes have a maximum ±0.3 dB non-linearity between 50 MHz and 11 GHz as shown in Figure 1. One of the probes with 4 mm long pogo pin is presented in Figure 2.

EMI pulse measurements are made with three antennas presented in Figure 3 and Figure 4. The 6 mm long monopole antenna is similar as introduced by Maloney [13]. A TEM antenna has a matched 50 Ω ±10 Ω impedance whereas the monopole and bowtie antennas have varying impedances below 3.5 GHz.

EMI measurements are done with a 1.5 – 2.5 GHz oscilloscopes in the laboratory and with a 500 MHz portable oscilloscope in manufacturing. The main focus is with ESD events having less than 250 V initial charging potential.

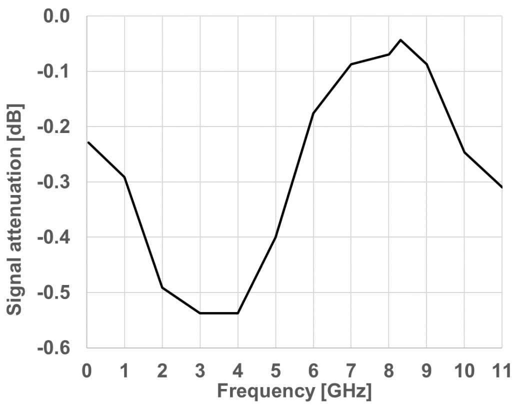

Figure 1: Frequence response of the current probe.

Antenna response depends on the polarization of the electromagnetic wave, close electrical environment, antenna positioning, and the antenna distance to a signal source. Figure 5 shows the TEM antenna horizontal radiation pattern in an EMC chamber when measured at 3 m distance. Here the attenuations due to RF cables, air path, and signal source have been compensated away.

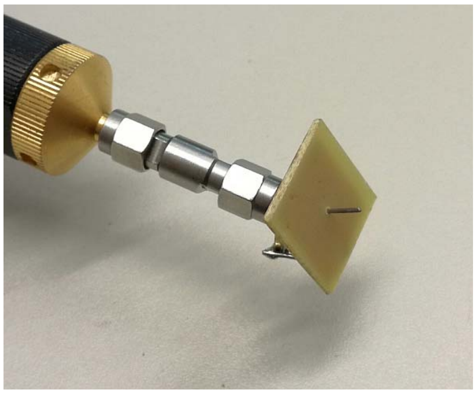

Figure 2: A current probe with 4.8 cm^2 size ground plate.

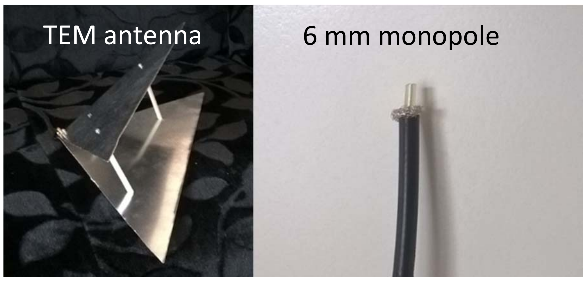

Figure 3: TEM antenna and monopole antenna.

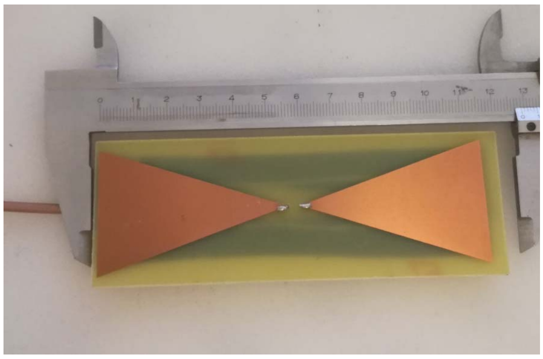

Figure 4: Bowtie antenna.

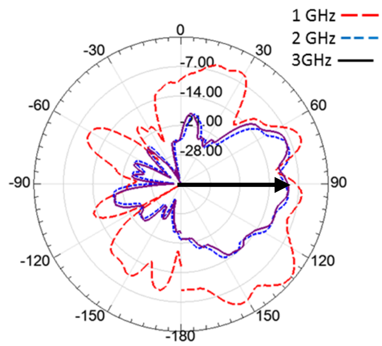

Figure 5: TEM antenna radiation pattern at 3 m distance in an EMC chamber. An arrow shows the main lobe direction.

Figure 6–8 show the measured and simulated antenna return losses between 50 MHz and 3.5 GHz. The TEM antenna is more sensitive and has a reasonable flat frequency response between 700 MHz and 3.5 GHz and is used as a reference antenna during the analysis. Simulations are made with HFFS software by using a 3D cad model of the antennas.

The 6 mm monopole antenna has a lower sensitivity due to a smaller size if compared to the bowtie or

TEM antennas. Therefore, 6 mm monopole antenna must be placed in near-field close to the ESD source to capture the EMI. The return loss of the monopole antenna is around 0.4 dB and the additional loss in Figure 6–8 comes from the coaxial cable and connectors between the antennas and oscilloscope.

The bowtie and TEM are directional antennas with the main lobe half power beam vertical width about 20°. The monopole antenna has an even radiation pattern around the end of the cable. With all three antennas used in this study the side lobes increase and the main lobe decreases above 3.5 Ghz. Therefore, these antennas are more accurate only below 3.5 GHz when the source of EMI is along the main lobe direction.

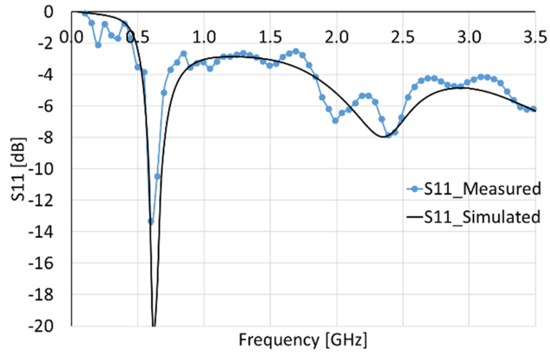

Figure 6: Measured and simulated bowtie antenna return loss with 1.5 m long coaxial cable.

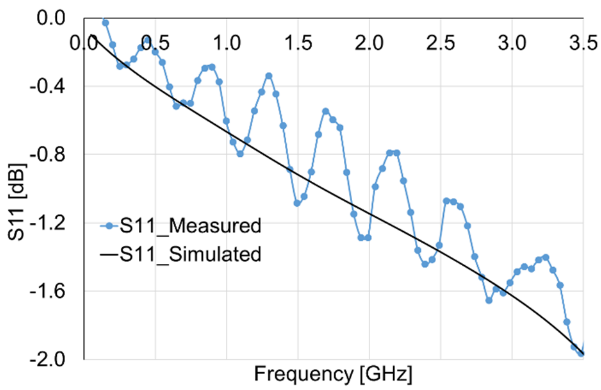

Figure 7: Measured and simulated 6 mm monopole antenna return loss with 1.5 m long coaxial cable.

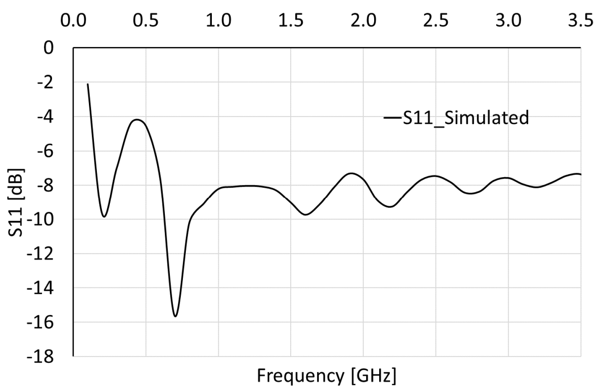

Figure 8: Simulated TEM antenna return loss with 1.5 m long coaxial cable.

B. Process analysis

Charged device ESD scenarios and risks were evaluated on-site in seven large size electronics manufacturing facilities having wafer handling, backend, component assembly, final assembly, and testing processes. Here portable spectrum analyzers and oscilloscopes with current probes and antennas were used to capture ESD current waveforms and EMI pulses.

C. Laboratory analysis

CDM and charged device ESD events and the main waveform parameters were analyzed in a laboratory environment with manual and semi-automatized methods. Here the relative humidity was less than 35 %. The manual CDM setup had a similar physical setup found in commercial CDM testers, but due to be manual operation, the test setup may not fully reproduce the same waveforms as found in automated CDM testers.

D. Simulations

SPICE equivalent circuit simulations are the main method to simulate charged device ESD events in this study. The simulations are made with the SPICE equivalent circuit shown in Figure 9 [14][15]. This is based on a field induction CDM test setup.

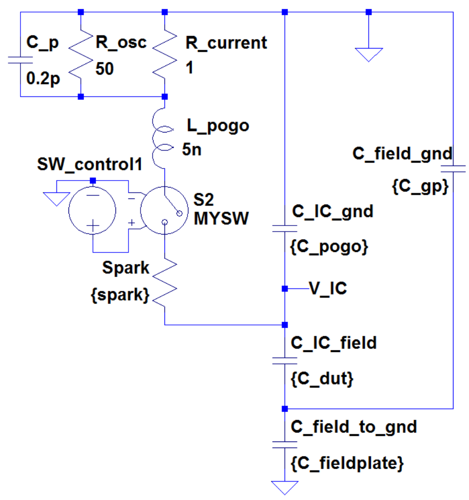

Figure 9: SPICE simulation model for the ESD analysis.

III. Results

A. EMI detection in manufacturing

One of the challenges with EMI detection in manufacturing is the background EMC noise as presented in Figure 10. When the ESD events are strong, the emitted EMI pulses are well above the electrical background noise level. However, when trying to detect EMI from discharges where single ICs or metal objects have less than about 250 V potential, the radiated electromagnetic pulse is relative weak. In that case, random transient pulses from operating process equipment give false alarms and the ESD detection level needs to be shifted up.

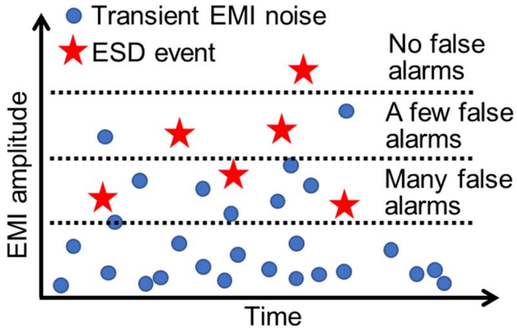

Figure 10: ESD detection with antennas and false alarms due to the background EMC noise.

Figure 11 presents three captured transient EMI events coming from a 4 – 8 meter distance. These transient pulses exist due to power switching in equipment and were captured with the TEM antenna and 500 MHz oscilloscope. The bandwidth of these example signals is <200 MHz which separates them from fast ESD events. However, the measured voltage waveforms with less than 200 MHz oscillation frequency may origin from a strong ESD event in the distance where high frequency components are attenuated. EMI pulses spread on a wide frequency bandwidth area and typically forces to use wide bandwidth antennas for example between 0.1 GHz and 3 GHz.

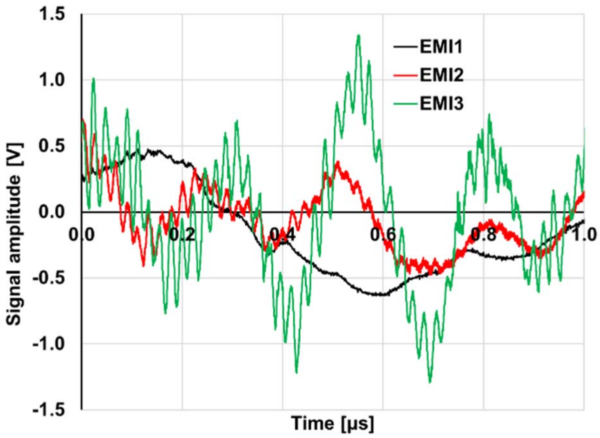

Figure 11: An example of the transient background EMC noise in a process area.

A high pass filter can be used to pass only fast transients to oscilloscope, but there can also be significant amount of high frequency noise in the manufacturing area. The noise level is highly varying between manufacturing areas and depends also on the processing technologies used. In each of the electronics manufacturing sites visited under this study the process areas had random EMI noise between 300 kHz and 3 GHz. This is equal to the ESD event noise amplitudes with about 100 V – 200 V initial voltage when an IC with about 5 pF source capacitance is discharged in a CDM test bench. For example, the electric flame-off process is a major source of EMI in wirebonding, thus hiding possible ESD events.

CDM peak current and EMI pulse amplitudes were compared with various ICs on a test bench. Figure 12, Figure 13, andFigure 14 presents the measured CDM peak currents and the 1st, 2nd, and 3rd highest EMI waveform peaks for the antenna signal using 1.5 GHz bandwidth. CDM events are made with 110 V in a test bench by using a commercial CDM test head and a constant contact speed. The TEM and bowtie antennas are kept at 75 cm distance, and the monopole antenna at 15 cm distance when 8 different types of ICs are tested. Here the discharges produce 20 mV – 1.2 V amplitude EMI pulses when the peak current varies between 0.2 A and 2.9 A with TEM and bowtie antennas. The monopole antenna gives only about 55 mV signals with 110 V.

Figures 15, 16, and 17 show results for 10 ICs with 500 MHz bandwidth oscilloscope and 530 V initial voltage. The higher potential was selected to get a better repeatability with the measurements and the 500 MHz was selected to compare results to EMI signals observed in manufacturing areas.

With a lower measurement bandwidth both the measured values of peak current and the EMI pulses are reduced. Measurements also show that there is only correlation between the measured antenna signals and CDM peak currents when the test setup is kept unchanged after calibration. In addition, it is challenging to estimate accurate ESD peak current values based on the measured EMI amplitude as different shape IC packages produce varying strength EMI pulses with the same charging voltage.

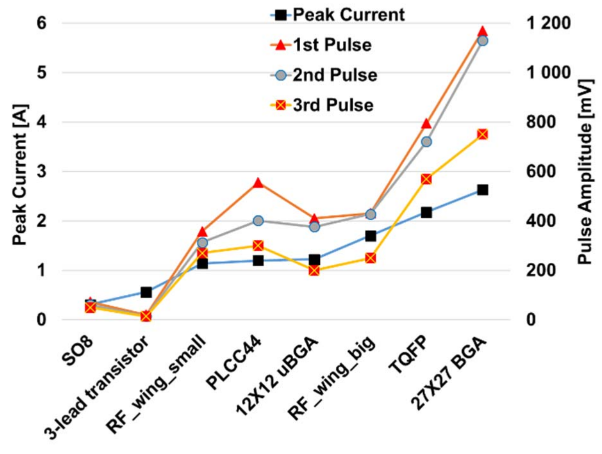

Figure 12: CDM peak currents and TEM antenna response with 110 V initial voltages. Measured with 1.5 GHz bandwidth.

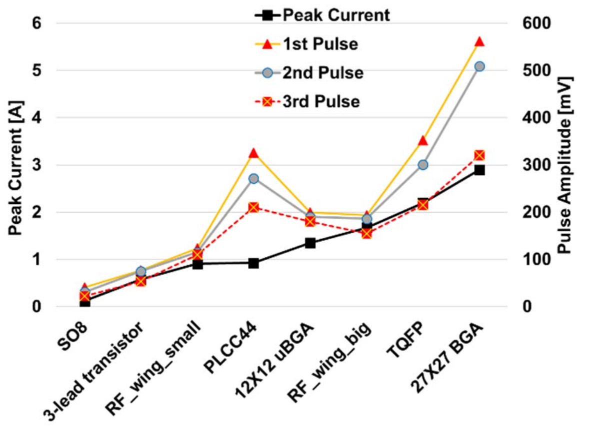

Figure 13: CDM peak currents and bowtie antenna response with 110 V initial voltages. Measured with 1.5 GHz bandwidth.

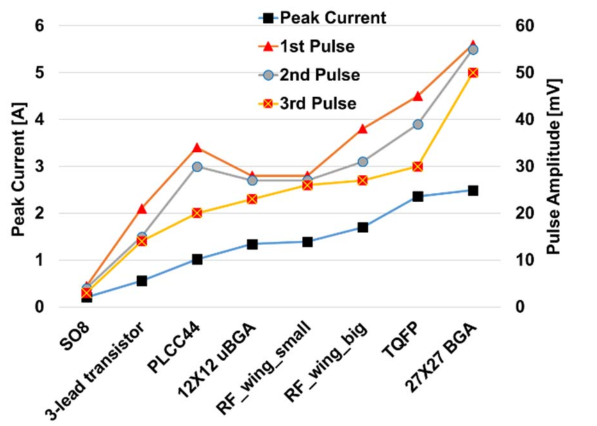

Figure 14: CDM peak currents and 6 mm monopole antenna response with 110 V initial voltages. Measured with 1.5 GHz bandwidth.

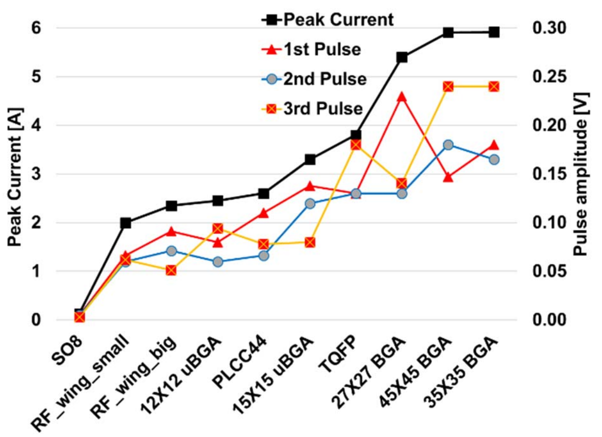

Figure 15: CDM peak currents and TEM antenna response with 530 V initial voltages. Measured with 0.5 GHz bandwidth.

The amplitude of the EMI pulse varies also if the charged object is discharged with a different size, orientation, and shape of metal object. This is shown in Figure 18 where a 15x15 mm size charged µBGA component is discharged by a constant speed contact with the CDM test head and other metal objects. The measurement bandwidth is 2.5 GHz and the figure shows the maximum and minimum detected peak EMI pulses with the TEM antenna.

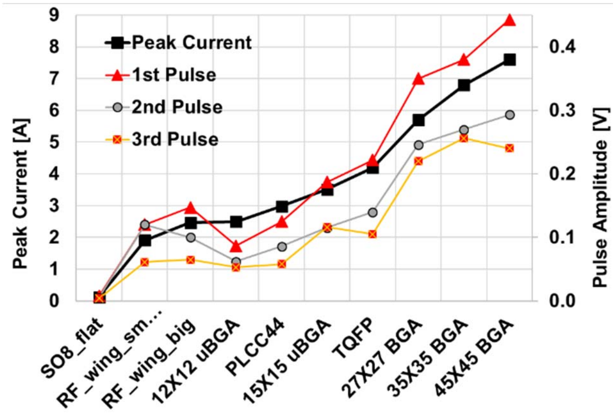

Figure 16: CDM peak currents and 6 mm monopole antenna response with 530 V initial voltages. Measured with 0.5 GHz bandwidth.

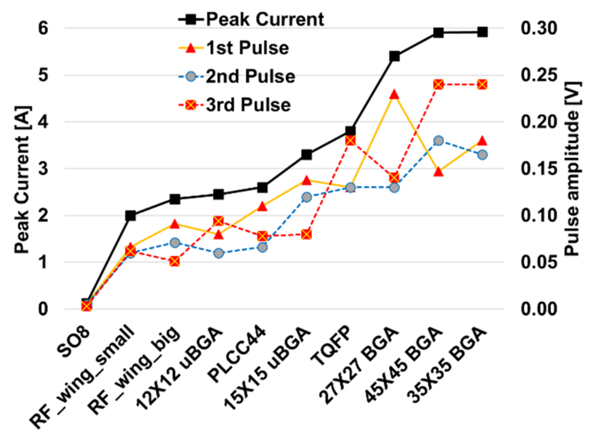

Figure 17: CDM peak currents and bowtie antenna response with 530 V initial voltages. Measured with 0.5 GHz bandwidth.

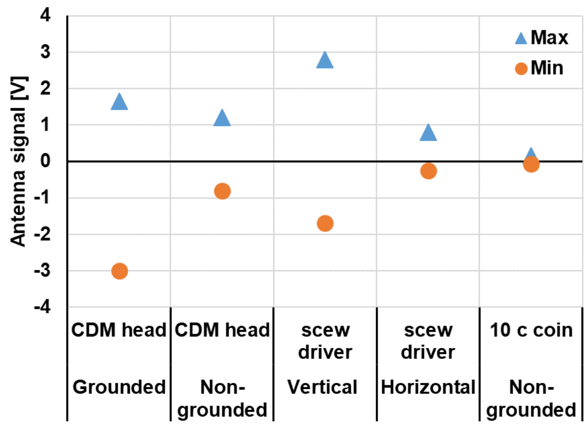

Figure 18: Measured peak EMI amplitudes when a charged µBGA component is discharged with various metal objects.

B. Transferred charge

Charged device discharges can be analysed based on the amount of quasi-static charge [6][7]. In the factory, the main benefit over DUT voltage measurement is that the amount of charge does not change with DUT position and capacitance changes, providing there is no charge added or subtracted by contact or nearby changing electrostatic field source. Charge can be measured with a hand held coulomb meter or an electrometer by discharging the charged object with a contact, or by placing the object into a Faraday cup.

In this study the charge transferred in the ESD is measured by integrating the discharge current waveform. Theoretical initial charge is also calculated based on the known capacitances and measured quasi-static potentials before and after the discharge event[12]. Measurement of the discharge current waveform in detail requires use of current probes and oscilloscopes with over 1 GHz bandwidth. Maloney [13] found that it requires to use 2-3 GHz bandwidth oscilloscopes to accurately measure current waveforms in a CDM tester with small ICs and with a small JEDEC calibration target. However, the transferred charge can be measured with a lower bandwidth system [7].

The main reason for testing with oscilloscopes slower than 1 GHz is to allow use of portable battery-operated tools. Oscilloscopes faster than 1 GHz are typically only used in a laboratory environment.

Figure 19 and Figure 20 compare the measured charge transferred and calculated initial charge with calculated DUT capacitance values with 100 V initial voltage in a CDM event. Here four ICs are placed on a 1.1 mm and 0.35 mm dielectric above a 108 pF field plate. The current measurement is made with a one–ohm shunt resistor and using a 500 MHz oscilloscope with 5 GSa sampling speed. The measured and theoretical calculated charge values have less than 17 % difference. The calculated DUT capacitance varied between 1.6 pF and 44 pF.

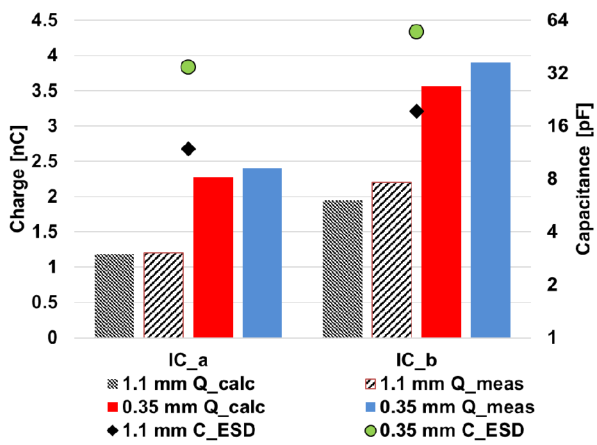

Figure 19: Measured and theoretical calculated transferred charge and capacitance values in CDM discharges.

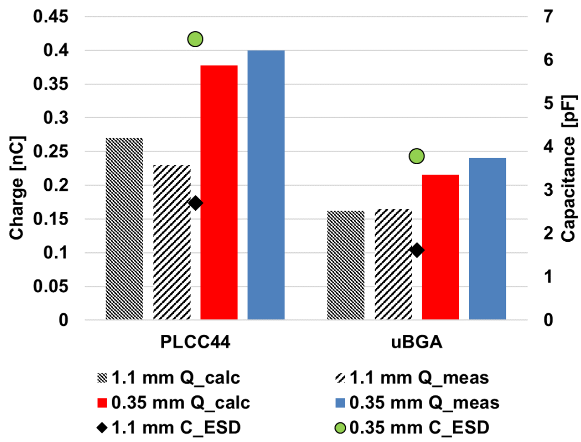

Figure 20: Measured and theoretical calculated transferred charge and capacitance values in CDM discharges.

One example of the measured CDM current waveforms both with a 2.5 GHz and 500 MHz oscilloscope is presented in Figure 21. Here the purpose of the measurement is to analyse how the measured CDM peak current and charge are reduced when using the 500 MHz oscilloscope. The measured peak current is reduced to about 50 % when the bandwidth is limited to 500 MHz, but the integrated charge is close to the same as measured using a 2.5 GHz instrument. The difference between the charge transferred is less than 10 %. Here it is necessary to compensate for possible small leakage currents affecting the integrated total charge value. This can be seen as an increasing or decreasing charge after the ESD event.

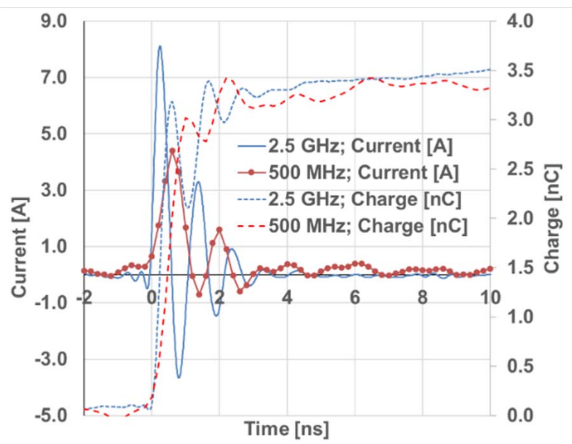

Figure 21: Measured and calculated transferred charge with two different bandwidth oscilloscopes.

Based on charge measurement experiments in manufacturing the amount of charge can be measured in most cases with less than 20 % error. The main sources of uncertainties with the measurement are related to the leakage current during the discharge event, accuracy of the instrumentation, and the amount of charge to be measured. When the charge is induced by an external electrostatic field the charge measurement has added uncertainties. The electrostatic field is changed by the presence if the contact probe and the charge measured is affected by the field changes.

C. Discharge Current Measurements

a) Required bandwidth for charged device ESD current measurements

The rise time of the current pulse defines the required measurement system bandwidth. The bandwidth can be calculated based on equation *BW* = 0.35/*pulse rise time*. In that case, at the 3 dB bandwidth frequency point the measurement system decreases the peak current amplitude about 30 %.

The calculated bandwidths are presented in Table 1, based on SPICE simulation of the equivalent circuit in Figure 9 with the following parameters; V_{IC}=250 V, R_{spark}=25 Ω, L_{pogo}=10 nH, $C_{fieldplate}$=33 pF, C_{pogo}=0.2 pF. and C_{gp}=17 pF. The rise time and peak current depends on the $C_{\_dut}$ and it is varied between 0.5 pF and 64 pF [16][18].

In the CDM qualification and manufacturing, 4 GHz bandwidth measurement setup can measure ESD pulses accurately if the ESD source capacitance is more than 1 pF and the series inductance is above 10 nH. However, in case of small charged metal objects with less than 1 pF source capacitance and below 5 nH serial inductance, the required bandwidth can be close to 10 GHz [17]. For the charged board discharges with >100 nH series inductance the required bandwidth can be below 500 MHz.

Table 1. Bandwidth requirements for charged device ESD current measurements calculated using a SPICE model.

DUT Capacitance (pF)	Peak Current (A)	Pulse rise time (ps)	Bandwidth requirement (GHz)
0.5	1.7	78	4.5
1	2.2	100	3.5
2	2.7	129	2.7
4	3.4	165	2.1
8	4.2	215	1.6
16	4.9	267	1.3
32	5.5	310	1.1
64	6.0	351	1.0

b) Repeatability of the manual charged device discharge testing

Repeatability of charged device discharges in a CDM tester have been studied in several papers. for example, Esmark [19] reported that the peak current varies between 5.5 A and 9.5 A with 500 V stress level. The variation increases when the discharge voltage is below 200 V or above 1500 V. In a FICDM tester the peak current values overlap below 200 V with small size ICs when the qualification is made with 50 V steps [20].

Charged device discharges in manufacturing environment can be measured with a similar manual discharge head as used in a FICDM tester [21]. The measurement method can produce current waveforms with less than 20 % difference to a CDM tester when the DUT is in similar capacitive environment in both cases. In addition, different contact discharge heads can be used to capture discharge waveforms [22].

There is less information available about the repeatability of the manual discharge current test method. In this study the manual test head has a flat 60 x 60 mm ground plate and a 6 mm long pogo pin in the middle with integrated one-ohm series resistor to measure the discharge current. This probe has a 3 dB bandwidth limitation at 2.7 GHz.

With manual discharge tests a varying speed of contact and an exact positioning of the test head increase measurement uncertainties. In addition, pogo pin arcing to neighbouring contacts can occur with over 1 kV voltages and less than 0.5 mm pin-to-pin spacing [23]. This uncertainty can be smaller when measuring discharges from a PCB with contact pads having isolated solder resists around.

Figure 22 and Figure 23 show results for manual FICDM tests where CDM peak currents are recorded with 100 V and 530 V initial charge levels using a 2.5 GHz bandwidth oscilloscope. In Figure 22 the DUT is a 20 mm diameter coin laying on a 0.35 mm dielectric above a 15 x 15 cm size induction plate with 108 pF capacitance. In Figure 23 the DUT is a 15x15 mm size BGA package with 1 mm ball grid. There is more variation with discharge peak currents with the non-flat BGA component due to the discharge contact variation on solder balls. In addition, as expected, there is more variation with the peak current when the voltage level decreases [11][16][20].

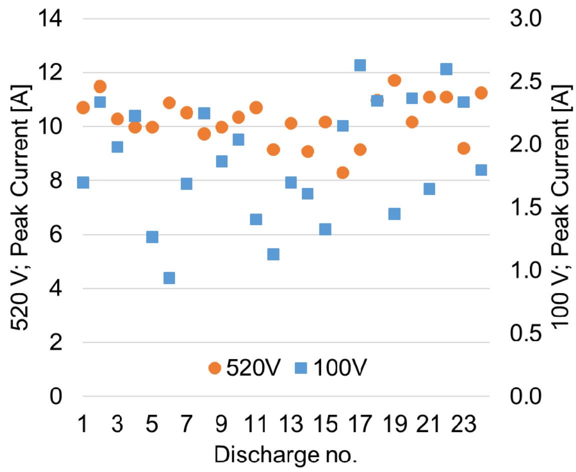

Figure 22: CDM peak currents with a manual CDM testing. DUT is a 10 cent coin.

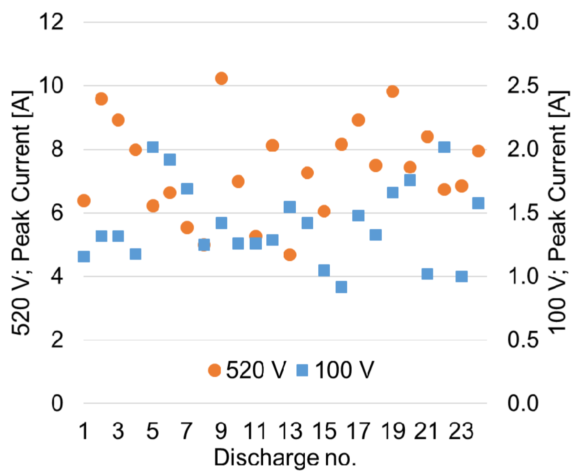

Figure 23: CDM peak currents with a manual CDM testing. DUT is a BGA with 1 mm ball grid.

The measured average, minimum and maximum discharge peak currents with manual CDM testing are presented in Figure 24 where the ground lead of the transistor IC is contacted 20 times with varying voltages.

Figure 24 shows that the peak current ranges can overlap when the stress voltage step is more than 100 V, and the stress level is below 300 V. Above 300 V stress level, the voltage increase must be over 250 V to avoid overlap of the range of peak currents. This variation is higher than found in an automated CDM qualification due to the varying manual contact speeds and pogo pin positioning. In addition, the measured current waveforms will be different if the contacting discharge head has a different physical construction [22].

The distribution of peak currents follows beta distribution with more recorded low peaks than current peaks above the median. This can be seen from Figure 25 where the distribution of 113 individual discharge events with 100 V and 200 V are presented by using a cumulative distribution. Here each step of the x-axis has a cumulative count of discharge peak currents found with the discharge events. This result may not be valid with over 1 kV potentials due to more varying spark plasma channels and with less than 100 V due to increased contact resistances.

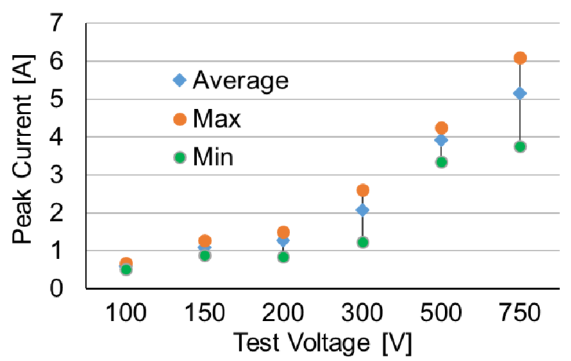

Figure 24: Manual CDM test peak current average, maximum, and minimum values.

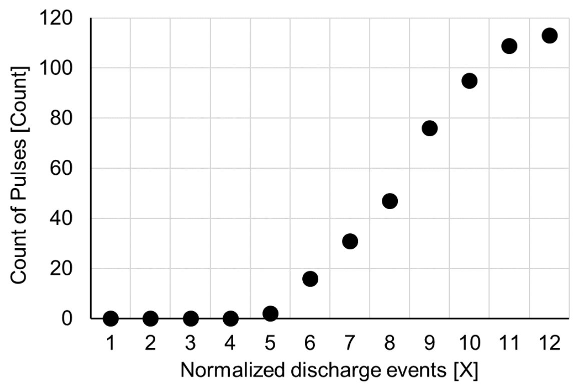

Figure 25: Cumulative distribution of peak currents with manual discharge testing.

D. Summary of the measurement methods

All measurement methods have their own benefits and challenges when controlling charged device ESD risks in manufacturing. A summary of the methods is presented in Table 2 with the following criteria;

- The accuracy of the measurement result depends on the measurement technology and tools used as well as the experimental situation. Bringing the measurement tool into the measurement situation can affect the result. A high score in the table represents a measurement that is likely to give a result that reflects the real-world value.
- The repeatability represents how nearly the measurement result can be expected to give the same result given the same initial conditions and circumstances in repeated tests. This depends, for example, on the tools used, competence of the user, and environmental parameters including some that may be unidentified or quasi-random. A high score in the table shows high confidence in a repeatable result.
- The reading of the instrument may not represent the real condition or parameter of the object. For example, the measured surface potential is correct only if the capacitance of the object and nearby electrostatic field sources are not changing. The result may need expert interpretation in the context of the measurement. A high score in the interpretation column shows a measurement that is unlikely to need expert evaluation.
- Measured discharge current waveforms would represent ESD risks in process, but measuring the real ESD current waveform can be practically impossible. Attempting to insert a current measurement system affects the discharge conditions. In contrast, quasi-static voltage and charge measurements represent the initial conditions before discharge rather than the ESD current waveforms. They can be used to estimate ESD stress level if other parameters are known or assumed. A high score in the "initial conditions"

column shows the measurement evaluates this well. A high score in the “actual damage threshold” column shows that the measurement relates well to this.

- Most backend and assembly process phases have a limited physical accessibility. This depends also on the measurement method used, and for example, a small size voltage or charge probe is more suitable for measurements inside process equipment. In addition, non-contact measurement methods can be used to measure moving ICs and PCBs. A high score in this column represents a technique that would be easy to use in a process.
- Cost of the tool and easy to use are optional parameters to classify control methods. Manufacturing facilities generally have a limited budget for ESD control tools. In addition, a generic competence level to use RF measurement tools and methods is limited in manufacturing. A high score in this column represents a tool that is reasonably low cost for the benefit it brings.

Using all available measurement methods brings typically the best results when evaluating charged device ESD risks in manufacturing. For example, the charged object is first measured with a voltage meter, the next measurement is to contact the DUT and measure the stored charge. This gives information for capacitance and energy calculations. If the calculated values, voltage, and charge values exceed certain limits, more analysis can be done with a discharge head and oscilloscope. The captured discharge waveform informs the shape of the ESD current waveform and gives dynamic charge and energy information for additional risk estimations. Still, even in an optimal case the measured ESD risk levels in the process area may have significant errors to the real ESD risk level.

The main challenge found in manufacturing is to access the process to measure static charges and ESD events. Typically, discharge current measurements are easier in final assembly area where most processes are open and commonly made by operators. In backend and surface mount processes discharge measurements may require to simulate discharge events outside the actual process area. This may increase errors to the real ESD risk level.

Table 2. Suitability of different measurement methods in electronics manufacturing to assess charged device ESD risks. Very poor=1, Poor=2, Fair=3, Good=4, and Very good=5.

Charge measurements	Accuracy	Repeatability	Interpretation of the measurement	Correlating with the process risks		Accessability in the process area	Easy to use	Cost of the tool
				Initial conditions	Actual damage thresholds			
Hand held coulomb meter	5	4	4	4	4	4	5	5
Electrometer with a probe	5	4	3	4	4	4	4	4
CDM tester	5	4	4	3	3	1	3	1
Manual 1-ohm CDM test head	4	3	2	4	4	3	3	3
High-ohmic ESD event receiver	5	4	2	4	4	3	3	3
Ground wire and CTx current probe	4	3	2	4	4	2	3	3
Current waveform measurement								
CDM tester	4	4	4	3	2	1	4	1
Manual 1-ohm CDM test head	3	3	2	4	3	3	3	3
High-ohmic ESD event receiver	3	3	2	4	3	3	3	3
CT6 or CT1 current probe	3	2	1	4	3	2	3	3
Voltage and E-field measurement								
Contact voltmeter	5	4	4	4	2	4	5	4
Non-contact voltmeter	4	4	3	3	2	5	5	5
Field Meter (voltage at 2.5 cm)	2	3	2	3	1	4	5	5
Field measurement (V/m)	3	3	2	4	2	5	4	5

IV. Conclusion

Combining voltage, charge, EMI, and discharge current measurements could give the most comprehensive and accurate information for charged device ESD risk analysis in manufacturing. However, the peak current and pulse rise time are the dominant parameters defining damage thresholds with fast CDM and charged device discharges. With total transferred discharge energy sensitive devices, the transferred charge and energy can be additional damage parameters.

Each measurement method has its own limitations and benefits. Discharge current measurements are especially difficult to perform in manufacturing environments and require fast oscilloscopes and RF measurement competence. Similarly, it is challenging to predict the discharge current of the ESD event based on the captured EMI waveform. Here even a small change in the component type, antenna orientation or the location of the ESD event can change measurement results. Random background EMI noise in manufacturing may also hide weak ESD events and limit the use of EMI detection technologies with ESD control.

Control measurements should be compared to known device ESD sensitivity. Unfortunately, the component CDM withstand voltage data cannot be used to directly estimate charged device ESD risks as these are related to ESD current waveform parameters. In the future, it would be more useful for component datasheets to present the absolute maximum rating peak current, rise time and charge transferred in the CDM ESD test, especially for highly sensitive components. This would enable process engineers to use discharge current data for ESD risk assessment and improved process development.

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