Empirical ESD Models for Cascode ESD Transistors

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Abstract - This work describes the development of empirical simulation models for snapback-based cascode nmos ESD transistors. Behavioral language VerilogA code was used to combine regular SPICE model with TLP characteristics, at triggering voltage dependent on two gate voltages. The use of empirical models for quantitative optimization of ESD protection was demonstrated on schemes and Si.

I. Introduction

The ability to perform dynamic simulation of ESD protection circuits, especially in customized designs, is crucial for validation of safe shunt of the ESD current during the ESD event. In particular, it is important to ensure appropriate clamping of the voltage drops along the ESD paths, below the breakdown voltage of victim devices placed in parallel in the core circuit. The concept of 'Empirical ESD Modeling' as a simple and effective method to simulate ESD protection circuits containing snapback-based devices, has been demonstrated lately [1,2]. The empirical models of ESD transistors are based on behavioral VerilogA code. Measured TLP characteristics of the ESD transistor are added in parallel to the regular SPICE model. The model representing the measured TLP curves, is activated at triggering voltage which depends on the simulated drain and gate voltages. The empirical ESD model concept and simulation flow were detailed by Aharoni *et. al.* [2]. The ESD event stress is simulated by a 'discharge circuit' connected to the stressed pins, generating force current ESD waveform. During the ESD event the parasitic drain capacitance of the ESD transistor is charged causing its voltage to rise with time. The gate voltage is also elevated because of the parasitic capacitive coupling between the drain and the gate, and the parasitic capacitance associated with the actual circuit connected to the gate. The devices and circuits behavior is handled by the regular SPICE model. The SPICE model enables simulation of the raised drain voltage due to the injected ESD charge (charging of capacitance associated to the device terminal node exposed to the ESD stress) and the increasing gate voltage (due to the response to the transient through the gate to drain capacitance). Once Vds(t) reaches Vt1(Vgs(t)), the characteristics of the device after snapback, as measured by TLP, are added. The ESD device Ron multiplied by the ESD current flowing through the transistor results in the voltage drop, in a dynamic manner. This enables modeling of the voltage drop through the bipolar (represented by the ESD device Ron(W) resistance derived from the TLP) and the channel (continuously simulated by the SPICE model). The empirical model can predict also damage to the ESD devices as it contains It2 dependency on transistor width. In principal it may also alert damage to core victim devices when the voltage drop built across them, during the ESD event, reaches their breakdown voltage. Finally, the model contains also the turn-off criteria of the triggered bipolar in the ESD devices. This new approach bypasses the challenging copying with the need to develop complex compact models dealing with the various physical phenomena related to snapback.

This work reviews the challenging extension of the empirical simulation to stacked ESD transistors in cascode configuration (in the same active area), used when over-voltage tolerance (OVT) of IC pins is required [3]. In this case Vt1 depends on the voltages developed on the two gates, simultaneously, during the ESD stress. A model taking into account the dynamic drain voltage as well as the top and bottom gate voltages during the ESD event, may enable an effective validation and optimization of the protection circuits making use of cascode ESD transistors, in various applications.

Figure 1 describes typical connections of cascode ESD transistors. The bottom-gate ('gbot') is either

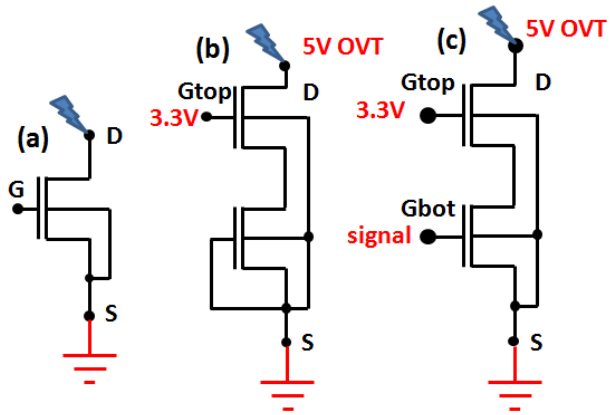


Figure 1. Examples of cascade ESD transistors connections. a. Single gate 3.3V ESD transistor. b. 3.3V cascade nmos for 5V power clamp (bottom gate is shorted to source). c. 3.3V cascade nmos for 5V IO.

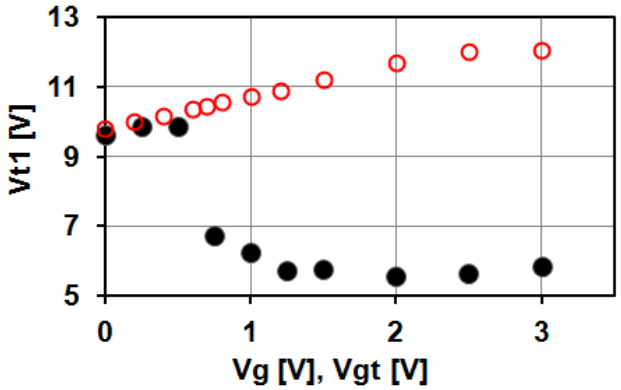


Figure 2. Vt1 vs. Vgs bias of a single gate 3.3V NMOS ESD transistor (solid black), and cascade 3.3V NMOS (red circles). W=480μm and bulk is shorted to source in both cases. Vt1 has been extracted from TLP measurements. The transistor source was grounded, while positive TLP pulses were applied on the drain. Vg bias has been applied between gate and source during TLP pulses. For the cascode, TLP pulses were applied on the drain of the top gate while grounding the source of the bottom transistor. Vgt bias voltage was put on the top-gate during the TLP pulses.

shorted to source (in case of power clamp) or connected to a pre-driver (in IO pin). A dc voltage is applied to the top gate ('gtop'), preventing the voltage drop between any pair of device terminals, to exceed the nominal voltage during IC normal operation, in order to avoid violations of gate oxide reliability limits. Miller *et. al.* [4] investigated the impact of layout and top-gate voltage (bottom-gate grounded) on the triggering voltage of cascoded NMOS transistors. Their motivation was to increase the ESD protection window of fully silicided (non ESD self-protected) cascode transistors by increasing Vt1. Souvrick *et. al.* [5] checked the dependency of Vt1 of (SOI) cascode ESD NMOS transistors, on different combinations of bottom and top gate biases. These results though, were used in a qualitative manner, to optimize the triggering of the cascode transistor. The empirical model, described in this work, enables a quantitative mean of optimization of ESD protection circuits employing actual simulation.

Creating ESD models for multi-gate ESD transistors poses new challenges. The measurement is more complicated as two gate voltages may vary simultaneously and affect the device behavior under ESD stress. Hence two gate biases ought to be applied during the TLP measurements, and the empirical models should contain functions fitted to the measured Vt1(Vgb,Vgt) values extracted from the TLP characteristics. The measurements, the analysis of the results, their fit to numerical functions taking into account possible interactions, as well as development and validation of the models, are reviewed in this work. In addition few examples of using the empirical models to simulate alternative protection ESD circuits involving cascode nmos, are described. One suggestion has been realized on Si. The results of the simulations were compared to TLP measurements.

II. Cascode ESD Empirical Models

Figure 2 depicts a comparison between Vt1(Vg) dependency of a single gate (see Fig. 1a) 3.3V ESD NMOS transistor and Vt1(Vgt) of a 3.3V cascode transistor with bottom-gate shorted to source (see Fig. 1b). In the single gate ESD transistor, Vt1 sharply drops once Vg passes the MOSFET threshold voltage. This is due to the substrate current generated in the transistor resulting in junction forward bias and lowering of the avalanche voltage [6]. Shorting the bottom-gate to source in the cascode device prevents this action since the bottom gate (and hence the whole cascode device) is off. Furthermore, higher Vgt also pulls up the voltage of the floating diffusion between the transistors, as the grounded bottom gate prevents its discharge. This causes body effect, increased top gate threshold voltage, and higher Vt1. Indeed the measured Vt1 of cascode transistor for power clamp shows monotonous increase with Vgt. This phenomenon may be an advantage in certain applications when high Vt1 is desired but may turn to be an obstacle when lower Vt1 is required for margin of the ESD design window. For example, the 3.3V MOS gate-oxide breakdown voltage is ~11V and drain to source breakdown under ESD stress may be even lower by few volts. A common way to overcome this issue is to add 'ESD implant' in the p-well underneath the drain of the cascode nmos, in order to lower the junction breakdown voltage and Vt1. The penalty is off course, additional process steps and higher IC cost. The increase of Vt1 by body effect may be resolved by alternative circuits,

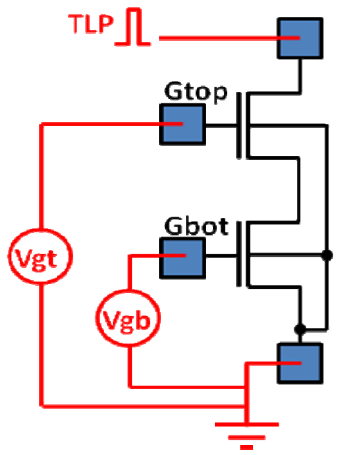


Figure 3. Measurement set-up, employing voltage bias on both gates.

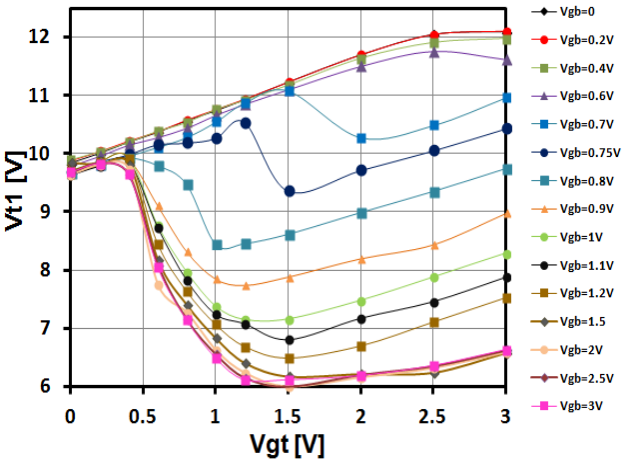
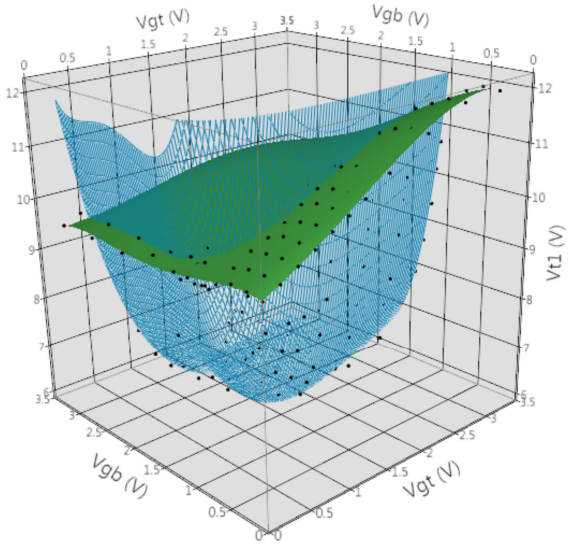


Figure 4. Measured Vt1 of 3.3V NMOS ESD cascade transistor, extracted in various combinations of bottom and top gate voltages. The lines connecting the measurement points were added for the clarity of the trends and are not the fitted functions.

ensuring discharge of the floating diffusion between the transistors during the ESD stress, as will be described in the next section.

A reliable model representing the impact of the two gates, and simulation ability, is essential to enable this effort. The measurement set-up, employing voltage bias on both gates, is illustrated in Figure 3. The device is drawn in black, the squares represent the pads added for probing, and the measurement set-up is denoted by red drawing external to the device. TLP pulses were applied on the drain of the top transistor while connecting the source of the bottom transistor to ground. The voltage biases between the top-gate and source (Vgt) and the voltage between the bottom-gate and source (Vgb) were set by external supplies during the TLP pulses. A 10nF capacitor (significantly bigger than the gate capacitance) was connected between

(a)



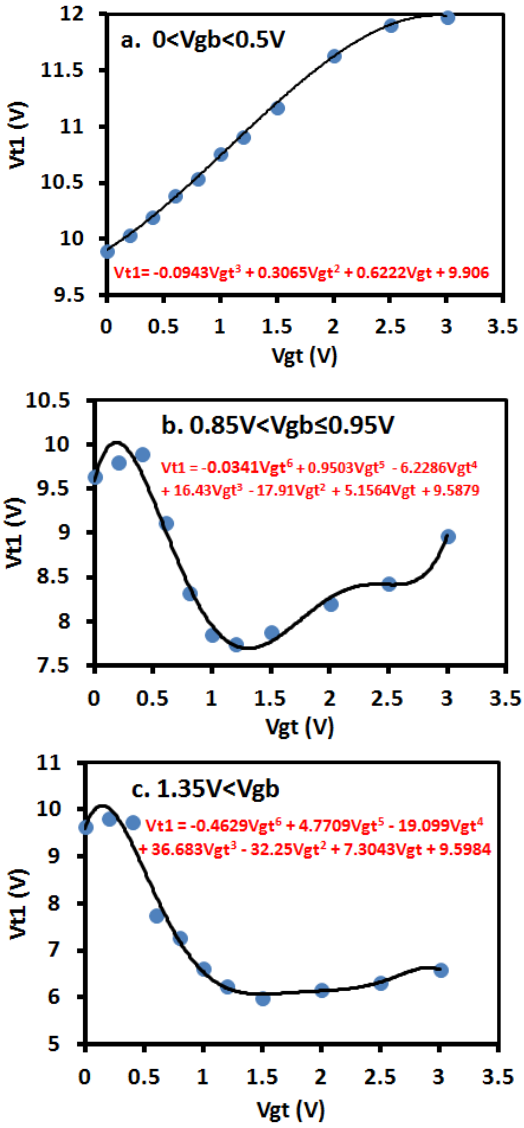
(b)

V_{t1} (Vgb,Vgt)=10.019-0.233 (V_{gt}-0.771)(V_{gb}-0.773) +0.85V_{gt}+0.096(V_{gt}-0.771)^2-0.073(V_{gt}-0.771)^2 -0.014(V_{gt}-0.771)^3-0.447V_{gb}-0.027(V_{gb}-0.773)^2 +0.233(V_{gb}-0.773)^3-0.078(V_{gb}-0.773)^4 — V_{gb}≤0.7V, V_{gt} ≤0.6V (green surface)

V_{t1} (Vgb,Vgt)=7.222-0.253 (V_{gt}-1.575)(V_{gb}-0.405) +0.056V_{gt}+0.769(V_{gt}-1.575)^2-0.591(V_{gt}-1.575)^3 +0.202(Vgt-1.575)^4-0.746Vgb+3.081(V_{gb}-1.405)^2 -3.832(V_{gb}-1.405)^3-1.359(V_{gb}-1.405)^4 — V_{gb}>0.7V, V_{gt} >0.6V (blue surface)

Figure 5. a. Surface representation of the fits by two 2D functions (green surface for Vgb≤0.7V and Vgt≤0.7V while the blue surface for the fit in the region Vgb>0.7V or Vgt>0.6V), to measured Vt1(Vgb,Vgt) points. The black points represent the values of measured Vt1 points extracted from the TLP measurements. b. Fitted 2D surface functions.

each biased gate and source pads in order to stabilize the DC voltage applied externally. The success criterion for reliable biasing was similar results for zero bias applied by the voltage supply versus actual metal short between the pads. Vt1 values at each Vgb and Vgt combination were extracted from the TLP curves. The dependency of Vt1 on both bottom and top gate voltages applied during the various TLP measurements is described in Figure 4. One can observe the increase of the triggering voltage with top gate voltage for Vgb≤0.6V, similar to the results shown in Fig. 2. For Vgb<Vt, the bottom transistor is off and there is no discharge of the floating diffusion between the gates. When Vgb is raised above Vt, the bottom transistor turns on, discharging the floating diffusion which results in a drop of Vt1 vs. Vgt. Further uplift of Vgb improves the discharge effectiveness, thus causing Vt1 to drop sharply even at lower values of Vgt.



d.

$0<V_{gb}=0.5V$	$V_{t1} = -0.094V_{gt}^3 + 0.307V_{gt}^2 + 0.622V_{gt} + 9.91$
$0.5<V_{gb}=0.65$	$V_{t1} = -0.126V_{gt}^3 + 0.388V_{gt}^2 + 0.573V_{gt} + 9.82$
$0.65<V_{gb}=0.725V$	$V_{t1} = -0.093V_{gt}^5 + 1.042V_{gt}^4 - 3.666V_{gt}^3 + 4.591V_{gt}^2 - 0.959V_{gt} + 9.727$
$0.725<V_{gb}=0.775V$	$V_{t1} = 0.082V_{gt}^6 - 1.104V_{gt}^5 + 5.069V_{gt}^4 - 9.764V_{gt}^3 + 7.198V_{gt}^2 - 0.9457V_{gt} + 9.729$
$0.775V<V_{gb}=0.85V$	$V_{t1} = 0.332V_{gt}^5 - 2.95V_{gt}^4 + 9.362V_{gt}^3 - 11.959V_{gt}^2 + 4.448V_{gt} + 9.567$
$0.85V<V_{gb}=0.95V$	$V_{t1} = -0.034V_{gt}^6 + 0.95V_{gt}^5 - 6.229V_{gt}^4 + 16.43_{Vgt}^3 - 17.91V_{gt}^2 + 5.1564V_{gt} + 9.588$
$0.95V<V_{gb}=1.05V$	$V_{t1} = -0.145V_{gt}^6 + 1.917V_{gt}^5 - 9.518V_{gt}^4 + 21.971V_{gt}^3 - 22.405V_{gt}^2 + 5.988V_{gt} + 9.64$
$1.05V<V_{gb}<=1.15V$	$V_{t1} = -0.085V_{gt}^6 + 1.38V_{gt}^5 - 7.741V_{gt}^4 + 19.349V_{gt}^3 - 20.871V_{gt}^2 + 5.717V_{gt} + 9.561$
$1.15V<V_{gb}=1.35V$	$V_{t1} = -0.26V_{gt}^6 + 2.901V_{gt}^5 - 12.694V_{gt}^4 + 26.826V_{gt}^3 - 25.945V_{gt}^2 + 6.57V_{gt} + 9.643$
$1.35V<V_{gb}$	$V_{t1} = -0.463V_{gt}^6 + 4.771V_{gt}^5 - 19.1V_{gt}^4 + 36.683V_{gt}^3 - 32.25V_{gt}^2 + 7.304V_{gt} + 9.598$

Figure 6. a-c. Examples of 1D Vt1(Vgb) fits to polynomial functions, to measured Vt1(Vgb,Vgt) points. d. 1D Empirical model functions.

Mathematical functions, fitted to the measured Vt1(Vgb,Vgt) points were used in the VerilogA ESD

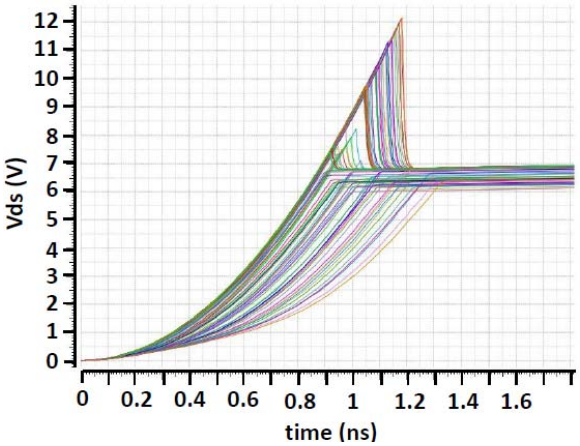


Figure 7. 2000V HBM simulation of 480µm ESD cascade nmos transistor. Vds(t) has been simulated applying various combinations of DC Vgb and Vgt, during the ESD event.

empirical model for the nmos cascode device. Two fitting methods were investigated. In the first method the measured Vt1 values were fitted to a 2D Vt1(Vgb,Vgt) function while in the second one the measured Vt1 values were fitted to a set of Vt1(Vgt) polynomials functions. In the first method two '2D' Vt1(Vgb,Vgt) functions, shown in Figure 5, were fitted in two Vgb-Vgt regions, employing non-linear least squares regression analysis. More than one dependency function was required due to significantly different shapes below and above bottom and top gate threshold voltages. The surface response functions are charted in figure 5a, where the fitted mathematical functions for the various regions of Vgb and Vgt are given in Fig. 5b. In the alternative fit approach shown in Fig. 6, 1D polynomial Vt1(Vgt) functions were fitted to the TLP data for each set of measurements having the same Vgb value. Each resulting Vt1(Vgt) function has been used for different Vgb range of values. Few examples of the 1D fits for various Vgb ranges are charted in Fig. 6, including the mathematical functions of the empirical model. The empirical model included off course, also other key parameters and dependencies, extracted from the TLP measurements, such as Ron(W), It2(W), Vh, and Ih. These parameters are used to simulate the dynamic (changed with ESD current over time during the event) voltage drop along the ESD cascode after triggering, damage by excessive current (at It2), as well as bipolar turn-off when the voltage/current through the ESD device goes down back to the holding current/voltage.

Figure 7 describes a set of simulations, performed to check the models accuracies, by simulating the voltage drop on a stand-alone cascode transistor vs. time, applying various combinations of DC biases on the bottom and top gates (961 simulations with

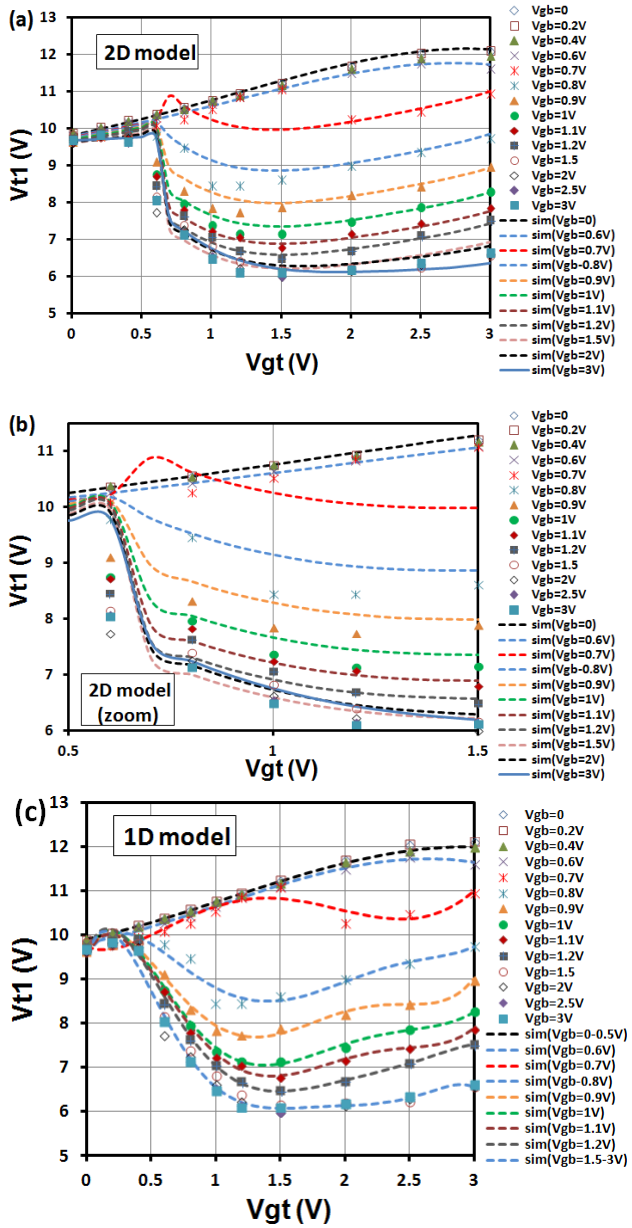


Figure 8. Comparison of Vt1 values extracted from HBM simulations applying various combinations of Vgb and Vgt, to TLP measured values. a. 2D surface fit. b. Enlargement of a portion of chart a. c. 1D polynomial functions fits for various Vgb ranges (first model revision).

combinations of Vgb=0 till 3V, step 0.1V, and Vgt=0 till 3V, step 0.1V). All the charts show, as expected, rise of the voltage with time to peak Vt1, and following drop to Vh due to the snapback. Vt1 and Vh values were extracted from these simulations and compared to measurements. This procedure was repeated for the two fit approaches. The run-time of the simulation using the 1D polynomial fits model was longer than the simulation using the 2D fit model, by about 10%. The comparison of Vt1 values extracted from the simulations to measured values, using the two approaches, is illustrated in Figure 8.

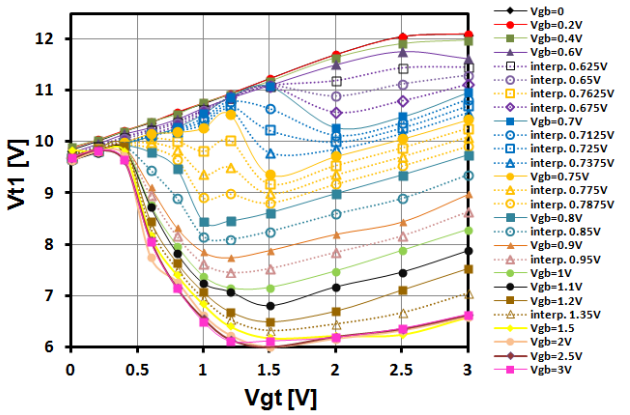


Figure 9. Measured (solid points) Vt1 of 3.3V NMOS ESD cascade transistor, extracted from TLP applying various combinations of bottom and top gate voltages (see Fig.4) with added Vt1 points (non-filled markers), interpolated from the measured valuess (dotted lines). The lines (solid for measured and dashed for interpolated) were added for the clarity of the trends and are not the fitted functions.

The comparison of the simulations using the 2D fit, to the TLP measurements, is shown in Figures 8a and 8b, while the comparison to the model employing the 1D polynomial fits, is illustrated in Figure 8c. In both fit approaches, the Vt1 values, extracted from the simulations are close to the measurements, shown in Figure 4. The use of the 2D fit, however, is less accurate in the region of the Vt1 drop (and sharp move from one fitted surface to the other surface) and for mid-Vgb values (see Fig. 8b). The 1D fit-based model is more true to the measurements due to the ability to achieve better numerical fit to non-monotonous curves. The slightly longer simulation run-time is a reasonable price for the higher simulation accuracy.

The first attempts to use the 1D polynomial fits revealed two concerns. The first issue was that in some regions the measurements of Vt1 had a big gap between two values of set Vgb. For example, if Vgt=1.2V, Vgb=0.75V will lead to Vt1=10.6V, while small change of Vgb to 0.8V will result with Vt1=8V. Such inaccuracy is not reasonable. The second problem may arise when simulated gate voltages are beyond the values set during the various TLP measurements. If the extension of the mathematical functions, fitted to the extracted Vt1 values, does not reflect reasonable extrapolation of the measured values (for Vgt>3V), the resulting simulation might be significantly wrong. Both issues may be resolved by adding further extensive measurements improving both resolution and range. On the other hand simple interpolation of intermediate Vgb between the measured curves, and rigorous fits taking into account

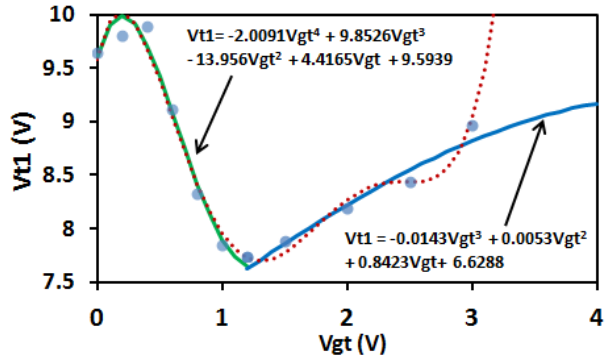


Figure 10. Example of improved 1D Vt1(Vgt) polynomial fit (Vgb=0.9V). The improved 1D fit is done in 2 parts (till 1.2V and above 1.2V), to improve accuracy. The doted curve is the previous revision of the 1D fit with rising extrapolation above measured Vt1 points.

V_{gb} range [V]	V_{gt} range	Vt1 [V]
$0<V_{gb}\le 0.5$		$0.0197V_{gt}^4-0.196V_{gt}^3+0.461V_{gt}^2+0.553V_{gt}+9.909$
$0.5<V_{gb}\le 0.6125$		$-0.005V_{gt}^5+0.082V_{gt}^4-0.455V_{gt}^3+0.847V_{gt}^2+0.375V_{gt}+9.83$
$0.6375<V_{gb}\le 0.6625$		$0.0002V_{gt}^4+0.026V_{gt}^3-0.309V_{gt}^2+1.219V_{gt}+9.656$
$0.6625<V_{gb}\le 0.6875$	$0<V_{gt}\le 2V$ $2V<V_{gt}$	$-0.597V_{gt}^4+1.58Vgt^3-1.008Vgt^2+0.91Vgt+9.692$ $0.036V_{gt}^3-0.496V_{gt}^2+2.305V_{gt}+7.643$
$0.6875<V_{gt}\le 0.70625$	$0<V_{gt}\le 2V$ $2V<V_{gt}$	$0.038V_{gt}^3-0.548V_{gt}^2+2.637V_{gt}+6.848$ $-0.979V_{gt}^3+2.321V_{gt}^2+0.443V_{gt}+9.73$
⋮	⋮	⋮
$1.425<V_{gb}$	$0<V_{gt}\le 0.6V$ $0.6V<V_{gt}$	$-35.729V_{gt}^3+22.063V_{gt}^2+3.158V_{gt}+9.84$ $0.079V_{gt}^4-1.044V_{gt}^3+4.878V_{gt}^2-9.227V_{gt}+12.154$

Figure 11. Portion of the improved 1D Vt1(Vgt) polynomial fit.

reasonable extrapolation beyond measurements, may improve the model accuracy.

Figure 9 shows the addition of Vt1(Vgt) dependencies points for intermediate Vgb values interpolated from the measured Vt1 points. The curves connecting the measured points are not the fitted functions yet and are shown for clarity of the trends. Mathematical functions were fitted to the measured Vt1 points as well as the interpolated ones. An example of a rigorous fit, taking into account reasonable extrapolation beyond measured Vt1(Vgt) values, is illustrated in Figure 10. A sample of the final Vt1(Vgb,Vgt) model is shown in Figure 11.

III. Simulations

The use of ESD simulation, employing the empirical ESD models of the 3.3V cascode nmos ESD transistor, is demonstrated in two suggested circuits, shown in Figure 12. In both circuits the bottom gate is grounded to Vss, to prevent leakage current through the cascode device during normal operation, and coupled to the stressed pin (drain of the top-gate) during the ESD event. In Figure 12a, a typical gate coupling triggering RC circuit is connected to the bottom gate. The capacitor is splitted to prevent device degradation by the over-voltage. During an

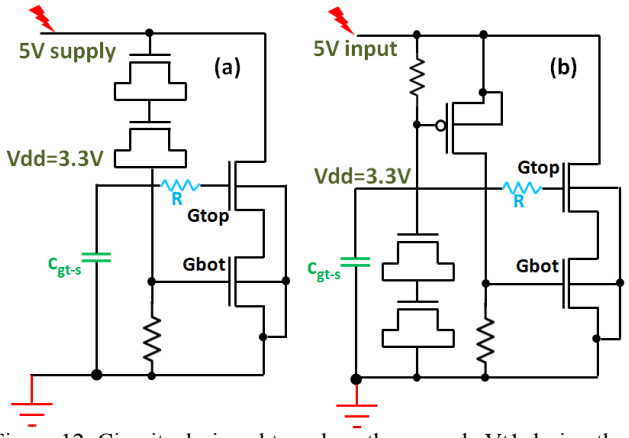


Figure 12. Circuits designed to reduce the cascode Vt1 during the ESD event. (a) Bottom gate capacitor coupling. (b) Bottom gate pull-up through pmos. The voltages in normal operation are designated in green. The capacitor c_{gt-s}, drawn in green, represents the potential parasitic capacitance between the top-gate to ground. The resistor, drawn in blue, was added in the simulations to reduce the impact of c_{gt-s}.

ESD event, the bottom gate is pulled-up due to the coupling capacitor. The turned on bottom transistor can discharge the floating diffusion between the two gates, enabling the decrease of Vt1. In the second scheme, shown in Figure 12b, the bottom gate is coupled to the pad through a pmos transistor. During normal operation the pmos gate follows the top drain voltage leaving it turned-off. However, during the ESD discharge the pmos gate is pulled down, the transistor is turned-on and the current flowing through it lifts up the cascode bottom gate voltage. The advantage of this circuit is the lower capacitance loaded on the cascode drain, enabling use of the protection circuit also for input pins. The pmos reliability concern, due to the over-voltage, should be also taken into account, by considering the actual cumulative stress time, use conditions, and actual overlapping gate-drain Miller capacitances. Off course the pmos may be also cascaded were an additional transistor, with grounded gate and normally open, helps to distribute the voltage and reduce the actual voltage to which the device is exposed to, at normal operation.

During the simulations 2000V HBM waveform has been applied between the cascode top-transistor drain and Vss, in the two circuits. The resulting simulations are shown in figures 13 and 14. Figure 13 describes the top and bottom gate voltages, as well as the cascode Vds, versus time, for the first circuit. Various couplings between the top-gate and Vss (see Fig. 12) were used to cause different triggering scenarios as Vgb(t) and Vgt(t) are determined by the specific chosen dimensions of the devices and circuit layout. In cases (a) and (b) the top gate was coupled to Vss by a capacitor of 1pF and 10pF, respectively. These

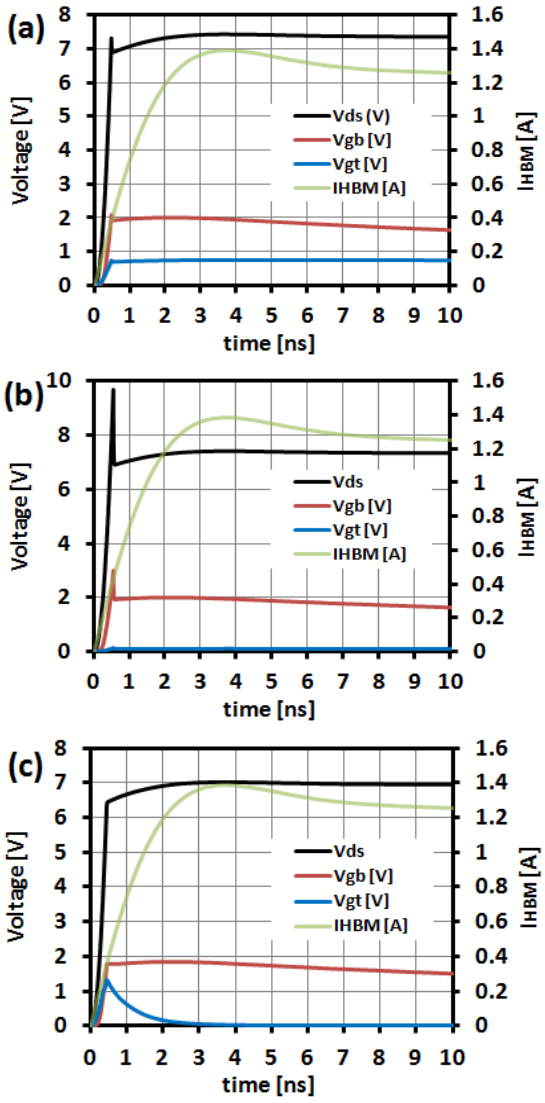


Figure 13. 2kV HBM simulation of circuit 12a (bottom-gate capacitor coupling) with (a) 1pF capacitor placed between cascode top-gate and Vss. (b) 10pF capacitor. (c) 10pF capacitor and 1kΩ resistor adjacent to the top-gate.

capacitors represent potential parasitic capacitance associated to the top-gate node, originating from the actual layout. The parasitic capacitance between the cascode drain and the top gate, and the externally added capacitor, are forming a dynamic capacitive voltage divider, affecting the rise of the top-gate voltage during the ESD transient. In case (a) the snapback occurs at 7.3V, where Vgb is raised to 2.1V and Vgt is jumping to 0.75V. In case (b) Vt1 is much higher, corresponding to the fact that the bigger external capacitor is pulling the top-gate voltage down to 0.15V. Adding a 1kΩ resistor between the 10pF capacitor and the top-gate, enabled higher Vgt and as a result lower Vt1. In all three cases, the values of the simulated Vt1 values matched very well with the

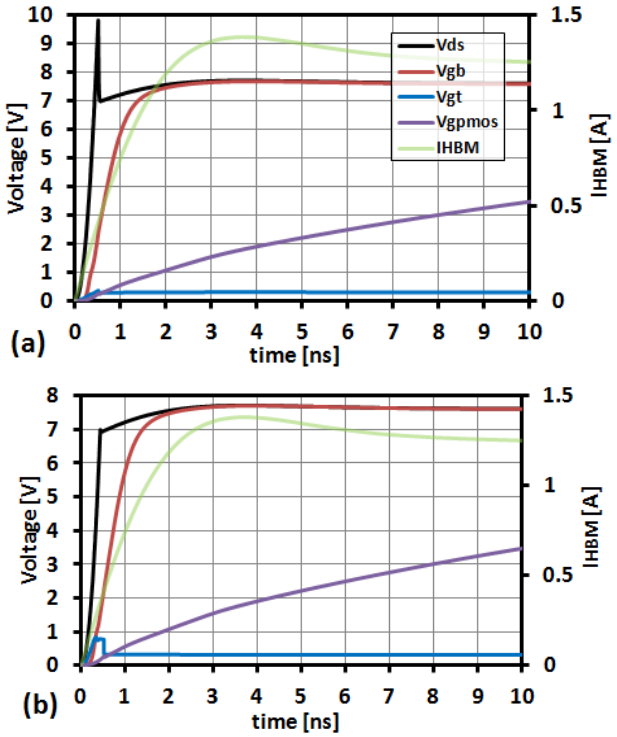


Figure 14. 2kV HBM simulation of circuit 4b (bottom gate pull-up through pmos). (a) 1pF capacitor placed between the top-gate and Vss. (b) 1pF capacitor and 1kΩ resistor coupling

measured ones at Vgb and Vgt values simulated at the snapback moment.

The simulations, depicted in Figure 14, are another evidence of how the triggering circuit can be optimized at various circuit scenarios, using the empirical simulation. In both examples, the voltage at the pmos gate is indeed kept low, during the rise of the ESD waveform, resulting in elevated Vgb. With a 1pF external capacitor coupling the top-gate and Vss, the low Vgt is causing high Vt1 (Fig. 14a). On the other hand, with the added resistor adjacent to the top gate, Vgb is jumping to 0.8V, sufficient to discharge the floating diffusion between gates and lowering of Vt1 to 7V, see Fig. 14b. Having snapback breakdown voltage of protected 3.3V core IC transistors about 9V, the reduction of the triggering voltage to ~7V, ensures a reasonable margin in the ESD design window and effective voltage clamping. Again, the fit of simulated Vt1(Vgb(t), Vgt(t)) to the measured values at Vgb and Vgt simulated at the moment of snapback, is good. Note that in these preliminary simulations Vgb jumps sharply and actually follows the top drain after some time. This may be restrained by better choice of the dimensions of the various triggering circuit devices, using the empirical simulation.

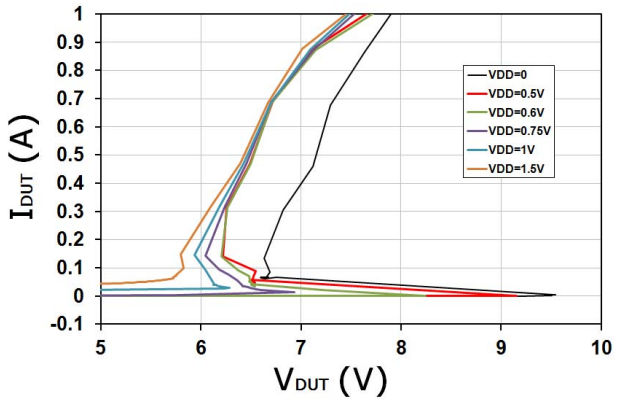


Figure 15. Snapback TLP pulse measurements of the circuit described in Fig. 12b, applied between VDD5 and VSS. Each characteristic is of different voltage bias between VDD pad and VSS.

IV Si Results

The circuit described in Fig. 12b has been realized on Si, in order to demonstrate, validate, and debug the cascode transistor empirical ESD model. The circuit was characterized by TLP stressing positive pulses between VDD5 and VSS pins, while applying various voltage DC bias between VDD pin and VSS. The resulting TLP curves are shown in Figure 15. The same circuit has been simulated, at scheme level, with various voltages applied between VDD and VSS pins (on the top-gate). An example of such simulation, for VDD=0.75V, is shown in Figure 16. A summary table comparing extracted TLP key-point with the simulations results is given in Figure 17. The TLP curves shown in Fig. 15 are evidence to the effectiveness of this circuit in discharging the floating diffusion between the gates by injection of current through the pmos to the bottom gate during the ESD event, turning it on. As the bottom gate is on, Vt1 is reduced for higher Vgt (forced during the TLP by the voltage applied on 'VDD' pin). In these measurements, in contrast to the simulation described in Fig. 14, there is no capacitive coupling of the top gate to VSS and Vgt is forced to a constant value by the applied voltage. From the ESD simulations of this circuit (Fig. 16a) one can extract simulated Vt1 and Vh for each value of VDD voltage. In all applied VDD voltages, Vgb at triggering time is high, causing a drop of Vt1 above the upper gate Vt. Indeed the pmos Vg stays low at the beginning of the HBM rise. Triggering at different times is causing Vgb achieving lower values, though sufficiently high to sustain the Vt1(Vgt) sharp drop above Vt. At later times, as shown in Fig. 16b, the pmos Vg coincides with VDD5 pin voltage, and the pmos is turned-off. As the injected current onto the bottom-gate is stopping, Vgb

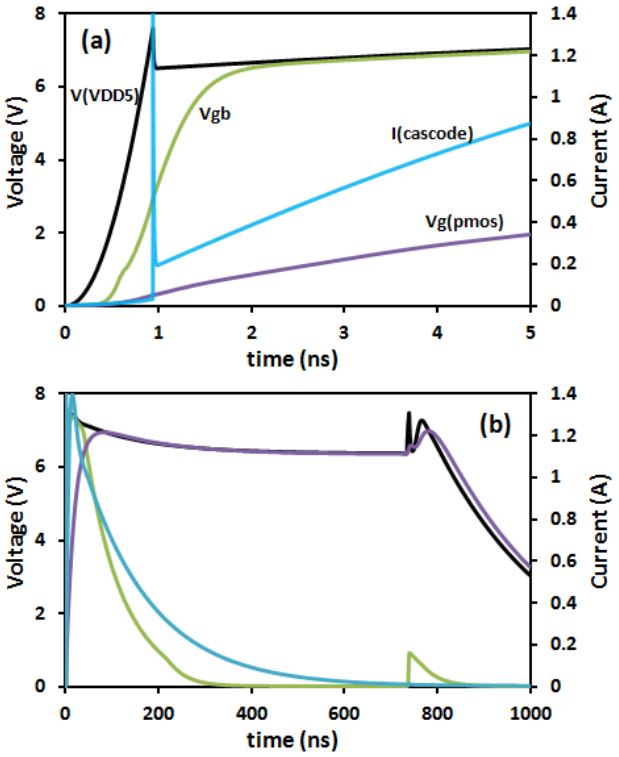


Figure 16. ESD simulation of the circuit described in Fig. 12b, with Vdd pin voltage (applied on top-gate)=0.75V. a. Zoom of the triggering time region. b. Simulation till 1µs, full decay of the HBM current.

	TLP		Simulation			
V(VDD) [V]	Vt1 [V]	Vh [V]	Vt1 [V]	Vgb [V]	t_trig [ns]	Vh [V]
0	9.55	6.59	9.84	4.28	1.065	6.4
0.5	9.15	6.22	9.31	3.94	1.036	6.4
0.6	8.25	6.2	8.17	3.24	0.97	6.4
0.75	6.95	6.05	7.56	2.92	0.94	6.4
1	6.3	5.94	6.84	2.64	0.91	6.4
1.5	5.85	5.83	6.16	2.5	0.9	6.16

Figure 17. Comparison between TLP measurements and ESD simulation of the circuit shown in Fig. 12b. Simulated Vgt was similar, offcourse, to the forced DC voltage value.

decays with time due to the discharge through the attached resistor. Anyway, all these changes are far beyond the transient and the peak current. The hump at ~700ns was explained in the previous work [2] by the turn-off of the bipolar leaving only the transistor channel to conduct the tail of the HBM current with higher impedance.

The summary table given in Fig. 17, reflects a good correspondence between simulated (HBM ESD) and TLP-measured Vt1 and Vh. Discrepancies between simulated and measured voltages may originate from a variety of causes; 1. SPICE models accuracy of the various devices, much beyond their nominal voltages. 2. The impact of TLP pulse stress may be different comparing to actual forced HBM current waveform. 3. TLP TDRO (Time Domain Reflection Overlap) measured voltage across the DUT was not constant

but changed with time. The integration time of the measured DUT voltage, was between 70 and 90 ns after the TLP rise. Integration at different time may result in different measured voltage hence also different Vt1 value. 4. Model resolution, even with the interpolation and model accuracy beyond the last measured point may be few tenth of a Volt. 5. The parasitics of the circuit in Si may modify the dynamic behavior. These parasitics are partially taken into account in the simulated scheme. Although all these possible reasons for discrepancies, the accuracy of the simulation of the triggering voltage is reasonable. The accuracy of Vh simulation may be improved by adding a Vh(Vgb,Vgt) dependency in a similar way. The changes in Vh for different combinations of Vgb and Vgt, which may be associated to complex coupling between the currents and fields generated in the triggered bipolar and MOSFET, are relatively small and in the current model an average value was used. Adding an empirical model for Vh can easily result in better prediction, and is planned to the next phase of the model fine tuning.

We plan to validate the model in additional circuits and more complex ones, especially add a circuit attached to the top gate, representing a more realistic case where a parasitic capacitance may be connected to the top-gate. A simulation of actual layout containing an ESD cascode transistor, after parasitic extraction, is planned as well. ESD protection circuits for OVT output or bi-directional I/O, may utilize also cascode ESD pmos transistor. We are going to create an ESD empirical model to this device as well, in order to enable optimization of circuits composed of both nmos and pmos cascode ESD transistors.

V Conclusions

The method used to establish a TLP-based empirical ESD simulation combined with regular SPICE model, has been successfully extended to cascode ESD nmos transistors having two gate voltages changing with time during the ESD event. Both Vgb(t) and Vgt(t) were determined by the regular SPICE model at any time, and TLP based model has been added when the cascode drain voltage reached Vt1(Vgb(t),Vgt(t)) fitted to the TLP measurements results. Two mathematical fit approaches, to the TLP results, were evaluated. Fit to 1D Vt1(Vgt) polynomials for various ranges of Vgb was found to be more accurate comparing to one 2D Vt1(Vgb,Vgt) function. The simulation run-time penalty was reasonable. Concerns related to the accuracy of the model were discussed, and the crucial process of the fit optimization was detailed. The benefit of using the empirical ESD model to design of ESD protection circuits combining cascode transistors has been demonstrated, especially for optimization of the triggering circuit. The elevation of Vgb during the ESD event and the discharge of the floating diffusion between the transistors enabled reduction of Vt1 caused by the dynamic raise of the top-gate voltage. This results in a better ESD design window without the need of costly ESD implant. A suggested circuit was realized on Si. TLP measurements, in particular extracted Vt1 and Vh values, were compared to simulated ones. The correspondence of the measured results to the simulated ones was good. Finally, future plans related to the empirical ESD modeling of cascode ESD transistors, were described.

Acknowledgments

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