# Cross-Domain Interaction at System Level Stress

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***Abstract*** – A scenario of unexpected failures of low voltage analog domains at system level stress has been studied both experimentally using test structures and through mixed-mode numerical simulation. The analysis of the failure mechanism and validated design fix measures are presented.

## I. Introduction

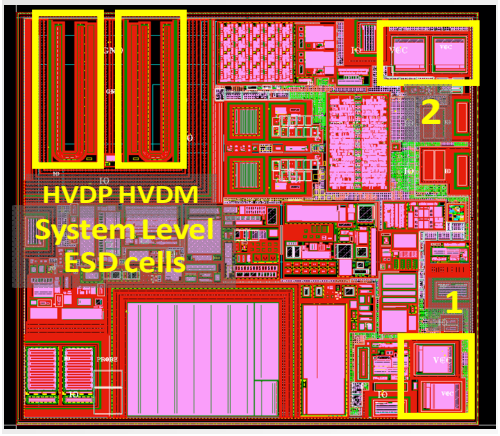
On-chip protection of system level pins often brings additional challenges due to interaction between the system level and other analog circuit blocks under ESD and surge system level stress. In power-on stress mode the high carrier injection and current path sharing may lead to a failure mode that is not common for the component level stress. The protection of system level pins is usually performed using on-chip local clamps with the protection capability verified in stand-alone mode for both power-off and power-on cases. Meantime the protection of the non-system level analog blocks is primarily developed to be a re-usable for different products. It is mainly designed to pass the component level qualification tests in corresponding power-off mode only.

This study was driven by a systematic case observed across a period of time. In several power analog power products with USB pins, similar failures during system level stress have been identified. A common signature was the damage of the low voltage (LV) analog domains at power-on negative system level stress, while passing test in both polarities at power-off and the positive stress in power-on mode.

The summary of test results for one such power analog IC with system level 6V switch pins, named HVDP and HVDM (high voltage differential plus and minus) (Table 1) shows underpass for both input pins under negative pulse stress in power-on mode. Contact gun test results were primarily found in agreement with the HMM test. Therefore for the volume of test experiments namely HMM test has been used followed by verification of the final product in the system level gun tests (not presented in this generic study). The HMM test was set for conditions of 10 zaps per 500V step with functional leakage test check at 7V between the steps.

In the IC design example (Fig.1a) the system level HVDP and HVDM pins have local clamps to the GND in the form of 6V-tolerant SCR. The conventional LV analog domains without the system level requirements have rail-based protection scheme with the rail diodes forming the network to the core active clamp.

Per failure analysis at the negative ESD stress in power-on mode the physical damage was localized in the NMOS power arrays of the 5V core clamps (locations 1 and 2 of Fig.1b), while in other modes the SCR failed.

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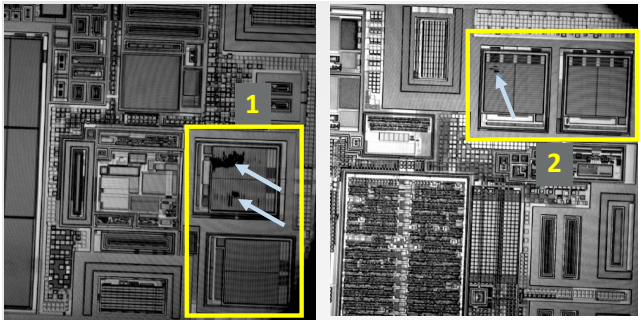



b)

Figure 1: Layout View of analog IC featuring a system level block with differential inputs protected by SCR's and two unrelated 5V and 3.3V analog domains (a) with observed clamp failures (b)

It is important for this study to consider the design of the core clamp itself. Switching power stages in analog IC products may create substantial power supply and ground bus ringing. It is often required, including the case shown in Fig.1, that the core clamp must not conduct a substantial current during normal operation to reduce power losses and maintain high efficiency. Thus, additional active clamp driver components are used to disable the clamp. As a side effect of these measures the core clamp also becomes effectively disabled in power-on mode at ESD stress with substantially reduced clamping current as will be shown in the next section.

The *purpose of this study* is to propose and verify a hypothesis that could explain the failure of the LV analog domains under the conditions described above as well as develop and validate a solution. A combination of both experimental data and simulation results is provided in the following sections to confirm the aforementioned hypothesis.

Table 1: Summary of the HMM test results for different pulse polarity and power modes

| Power-Off | + HMM Pass Level (kV) | | | - HMM Pass Level (kV) | | |
|---|---|---|---|---|---|---|
| Stressed pins | SN1 | SN2 | SN3 | SN4 | SN5 | SN6 |
| HVDP | >15 | >15 | >15 | >15 | >15 | >15 |
| HVDM | >15 | >15 | >15 | >15 | >15 | >15 |

| Power-On | + HMM Pass Level (kV) | | | - HMM Pass Level (kV) | | |
|---|---|---|---|---|---|---|
| Stressed pins | SN7 | SN8 | SN9 | SN10/11 | SN12/13 | SN14/15 |
| HVDP | >15 | >15 | >15 | 5 | 5 | 3 |
| HVDM | >15 | >15 | >15 | 3 | 5 | 3 |

# II. Core Active Clamp Versions

The conventional active clamp for rail based networks was proposed in [1]. It is composed of the power NMOS array that can be turned-on by a fast-transient pulse due to source and drain capacitive coupling and is switched off slowly by the driver based on inverter and RC-timer (Fig.2a). The elegance of this solution has resulted in wide application of this clamp in the industry over the last two decades. Various modifications of the driver circuit were made to address the specific analog circuit design requirements. In case of *power* analog circuits with power and ground rails "ringing" due to the switching of power stages the sensitivity to transients must be suppressed after power on state. It is typically achieved by making an additional feedback (latch) circuit enabled in power-on mode.

As mentioned above, suppression of the clamp turn-on in power-on state also disables it during system level stress in power-on mode. To demonstrate this in details, the active clamp circuit (Fig.2b), which was used in the case of the IC of Fig.1 is compared with the conventional clamp circuit (Fig.2a) by means of mixed mode simulation. The clamp (Fig.2b) includes additional components of a latch-type circuit to change the effective inverter ratio achieving higher turn-on threshold. The comparison of reaction on addition power supply voltage pulse in power-on state (Fig.2c) shows substantially lower current level from the noise rejection clamp (NR-clamp) (Fig.2b).

Indeed, according to the mixed – mode analysis both clamps provide similar HBM pulse waveforms while in the non-powered state (Fig.3a, for non-powered).

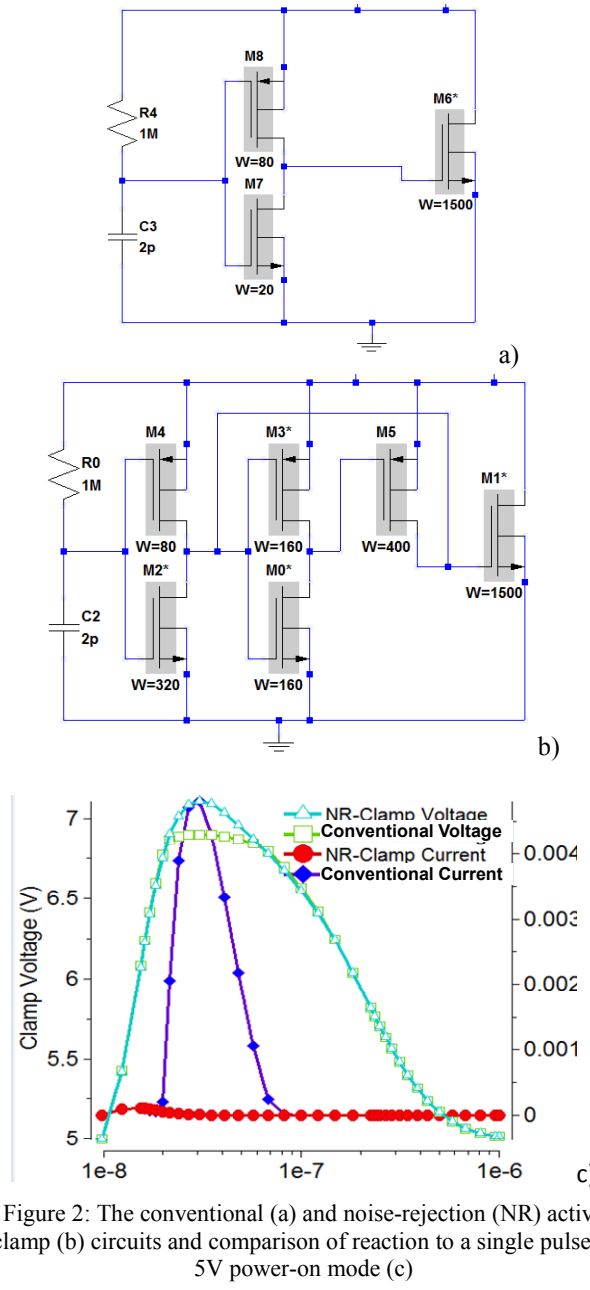



Figure 2: The conventional (a) and noise-rejection (NR) active clamp (b) circuits and comparison of reaction to a single pulse in 5V power-on mode (c)

However, in the power-on state only the conventional clamp (Fig.2a) provides adequate clamping characteristics reflecting the NMOS array operation in saturation regime (Fig.3a, for non-powered). On the contrary the NR-clamp has the gate array voltage kept much lower and NMOS array in the clamp must go into snapback regime to carry the ESD current. These regimes of NMOS arrays can be visualized by plotting the *I(t)-V(t)* characteristics of the clamps (Fig.3 b, c) which clearly demonstrate the S-shape characteristics for the NMOS array of the NR-clamp (Fig.3c). The S-shape I-V characteristic is similar to the one realized in snapback NMOS or NPN structures. Under these conductivity modulation conditions the NMOS array without silicide blocking region usually exhibits irreversible damage due to local current filamentation and burnout similar to Fig.1b.

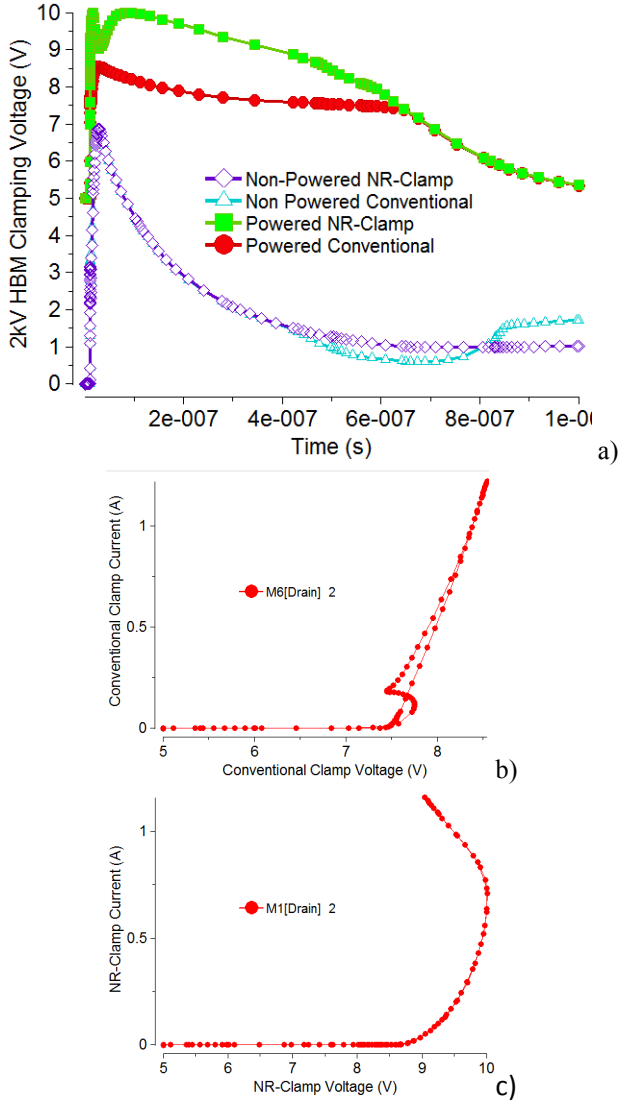


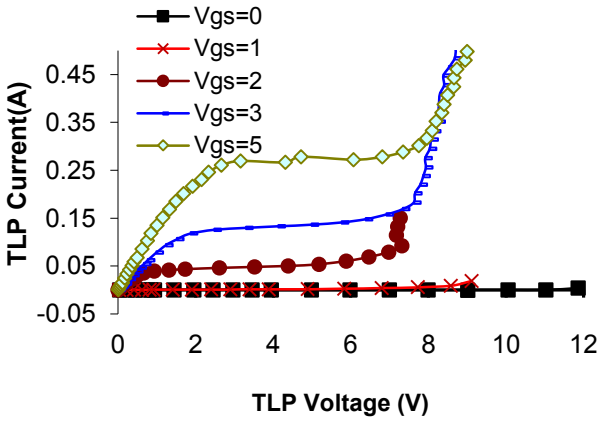

Figure 3: Comparison of clamping voltage waveforms for the conventional and NR-clamps in power-off and power-on modes for 2kV HBM stress (a) and corresponding I(t)-V(t) characteristics (b, c) for power-on mode

# III. Test Chip Design and Results

The test chip design of experiment has been driven by the hypothesis outlined at the end of Introduction. It was aimed at both quantifying the effect and validating the solution for 0.18µm BCD process technology on ESD IP components (Fig.4). The SCR (system level ESD cell) and low voltage core clamp elements were connected to the common thick metal (TM) ground bus (Fig.5a). The three design alternatives include: NR-Clamp Only; the same NR-Clamp with Snapback NMOS clamp in parallel and the Conventional Clamp. There were 4 versions included for each clamp type with 1X, 2X, 3X, and 4X instances connected in parallel (Fig.5a). In power-on state each core clamp has been powered to 5V with following stress of SCR with HMM pulse.

The TLP characteristics of the main test chip components are consolidated in Fig.4. The TLP SOA of the 0.75mm NMOS array are presented in Fig.4a). The array is similar to the one used in both active clamps with higher width scaling (Fig.5b). In addition the TLP characterizes the snapback NMOS clamp (Fig.4c) and system level SCR (Fig.4d) to complete the components list.

As can be seen the 5V NMOS array has a typical SOA for 5V device with relatively low critical current for failure in the sub-threshold gate bias. Both types of clamps have very similar TLP I-V characteristics for the ESD pulse regime (Fig.4b) that with 1-ohm bus resistance should provide the rail-based protection. The snapback NMOS clamp is designed with voltage reference components and can limit the voltage below the array critical regimes (Fig.4c). Finally the SCR clamp is similar to the one published in [3] (Fig.4d).

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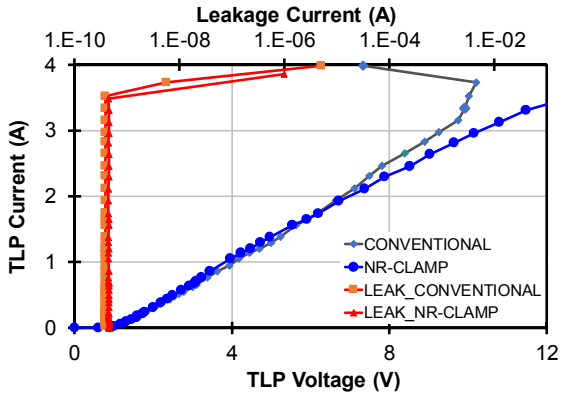


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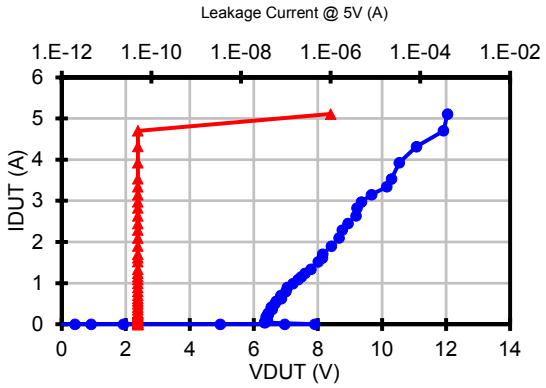


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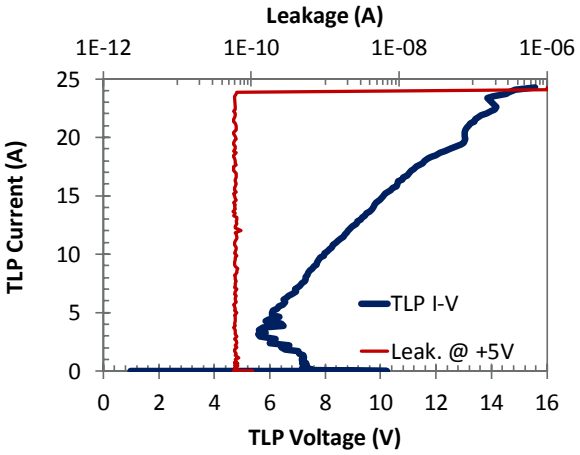



d)

Figure 4: Experimental data for test chip components. TLP characteristics for pulsed SOA of the 0.75mm portion of the NMOS array used in active clamps (a); comparison of the characteristics for the Conventional and NR active clamps (b); 5V snapback NMOS cell (c) and the system level protection SCR (d)

The summary of the test results for different clamp types (Fig.5b) demonstrates the expected width scaling dependencies. The results for NR-Clamp (Fig.5b, red) are the weakest with the clamp size dependent passing level. The Conventional Clamp shows overall the most robust performance independent of width scaling because SCR fails under HMM stress > ~12 kV or < -9 kV prior to the active clamps. However, this approach does not satisfy the noise rejection specification. The most promising is NR-Clamp + SNMOS (Fig. 4b, green) as it is almost independent of active clamp size while still satisfying the noise rejection requirements. Although it still has some limitations it allows to achieve 8kV level.

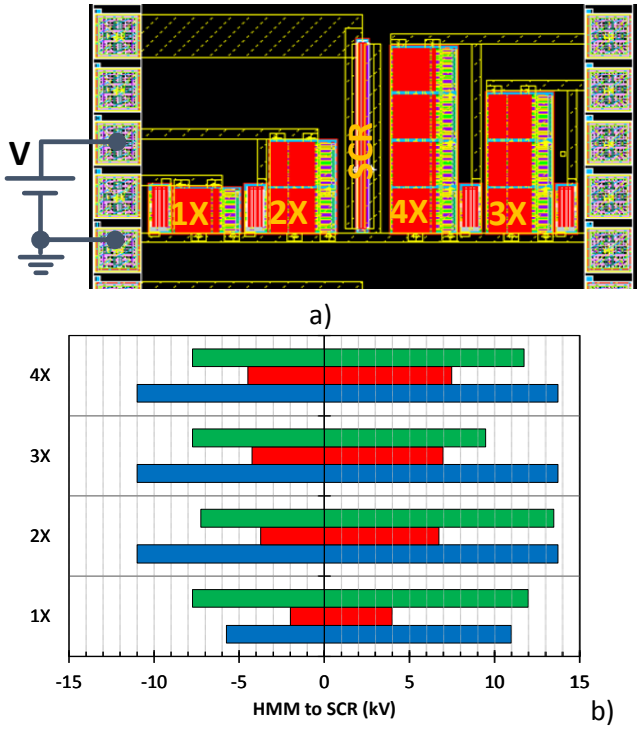



Figure 5: Test chip layout view (a) and graphical summary of the test results (b) for passing level of the three combination of the system level SCR and color coded different LV power supply domain protection design alternatives: Red: NR-Clamp; Green: A-Clamp with Latch and in parallel Snapback NMOS Clamp; Blue: Active Clamp with no Latch

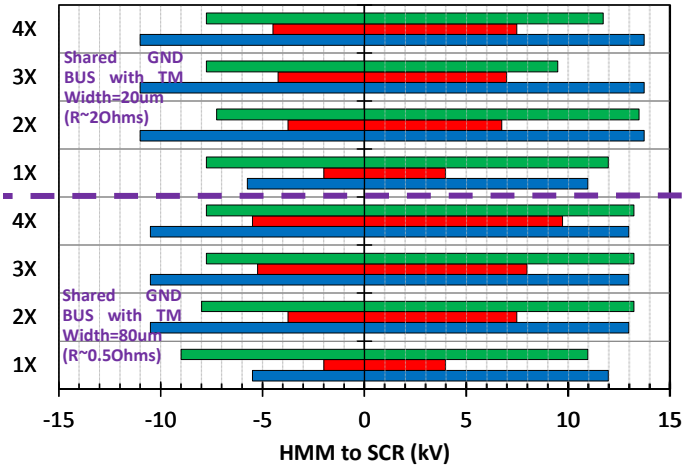



Figure 6: Graphical summary of the HMM test results for passing level of the three combinations of the system level SCR and color coded different LV power supply domain protection design alternatives for 20 and 80um ground bus metal width: Red: NR-Clamp; Green: A-Clamp with Latch and in parallel Snapback NMOS Clamp; Blue: Active Clamp with no Latch)

It is likely that another possible alternative would be a core clamp with the impractically large NMOS array implementing the features of a snapback cell.

Additional experimental results have been obtained for the thick metal (TM) width parameter of the ground bus. Results from shared TM ground bus with width of 20 (R~2Ohms) and 80um (R~0.5Ohms) (Fig.6) did not show significant difference in the HMM passing level of stressed pins.

# IV. Discussion

Instead of an empirical discussion of the experimental data the results of mixed-mode analysis are presented in this section to achieve a deeper understanding of the physical effects. To physically simulate the irreversible failure of the active clamp NMOS array in snapback mode a 2-transisor model is used. This method and the detailed justification is presented in [2]. It is used here to illustrate the failure of the NR-clamp as a function of the circuit and pulse parameters in comparison with the Conventional active clamp.

## A. Simulation Methodology

When a complex simulation analysis is targeted it is always proactive to envision the expected results in order to limit the range of numerical experiments and conditions involved. Phenomenologically, the observed NMOS array burnout of local drain-source spacing region is the result of the avalanche injection positive feedback mechanism and spatial current instability in 100-1000 ns time domain. Such characteristic time of instability has to include, not only a fast isothermal conductivity modulation phenomena, but longer characteristic times for self-heating. The electro-thermal conductivity modulation phenomenon induces an increase of the intrinsic carrier generation rate due to Joule self-heating. The overheating of the subsurface region can be expected in sub-microsecond time regime resulting in local electro-thermal filamentation leading to local rise in temperature above critical levels.

In the simulation analysis below, the NMOS structure was represented by 2 devices in order to account for the level of complexity that involves non-linear effects of local burnout. The power array in both active clamps presents itself as a genuine 3-dimensional (3D problem). In general, for electro-thermal runaway conditions such problem cannot be directly modelled with 2-dimensional (2D) numerical simulation approach. Thus the challenge is to "transform" such 3D non-linear problem into a physical "analogy" that would be reasonably compatible with the capability of the 2D numerical simulator.

Such an analysis of spatial instability in a large distributed system is typically focused on finding the parametric device and circuit conditions for growth of small local fluctuations in the NMOS array. In a numerical simulation a physical representation of fluctuation can be introduced by a small structure or circuit parameters, a thermo-electrical state deviation from the uniform conditions or even the numerical noise due to finite accuracy of the numerical solution [5]. Such an effective approach is the so called two-transistor model. The model represents just a parallel connection of a large size structure and a small size structure that physically enables current redistribution between devices. The 2D structure with large width scaling factor physically represents a main part of the array that remains uniform during current re-distribution in transient stress conditions. The same 2D structure with the small width scaling factor is used in order to enable and physically represent a region of the array with possible special current instability and local burnout.

Thus, such a two-transistor model can be used as an analogy to enable the analysis of the stability of distributed systems relatively current pumping fluctuations over the large to small structure. It is accounting for accurate parameters of the devices, circuit and the time domain under the electro thermal conditions far away from equilibrium. By other words, depending on complex set of non-linear system parameters, including in particular active clamp circuit with the system level current path, circuit the transient behavior of the current and temperature in the small structure it may or may not become unstable. Namely such response has to be found by transient mixed-mode simulation approach.

In the NMOS array case the runaway of the small structure physically represents the current and temperature instability related to the local burnout phenomena. In spite of taking substantial simplification steps such an analysis is the only and rather powerful method to analyze, understand and predict the behavior of large 3D semiconductor systems today. This will be in particular demonstrated below in application to this study goal.

The final step of implementation of the two-transistor model approach is to introduce some kind of small initial imbalance in order to physically represent a local fluctuation or structure or circuit level inhomogeneity. The structure parameters deviations can physically represent either certain type of local inhomogeneity or statistical variation of the doping

level or geometrical dimensions that do not result in a significant change of the device characteristics out of the specification limits. For example the result of a small change in gate dielectric or gate length is simulated. In addition an uneven segment connection in the array for example due to physical metallization routing or only lateral gate poly connection can also be simulated. However often the accuracy of the simulator solution – numerical is often sufficient to start the instability.

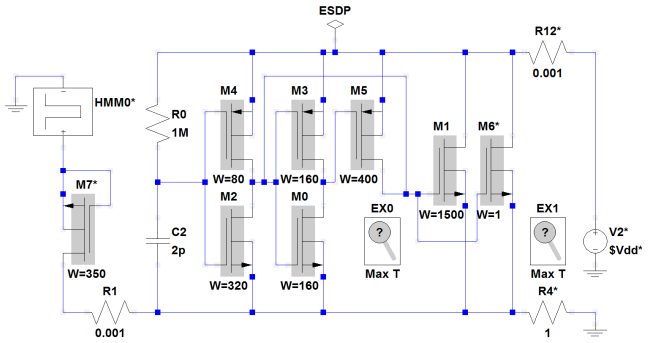
## B. Numerical Analysis of the Experimental Results

In this study the 2-transisor model approach was used to enable the circuit level time domain stability analysis for the current density re-distribution between two identical 2D devices with different width. The large segment represents the uniform region in the array M1 (Fig.6a), while the small segment M6 (Fig.7a) physically represents the area of current filamentation. The failure condition is detected by monitoring the peak temperature in the small component M6 (Fig.7a).

The distributed ground bus impedance is represented by the resistor R4. The failure criteria are peak temperature in the array fragment (M6) and the SCR (M7). From the peak temperature waveforms (Fig.7b) the main informative output is either peak temperature stay close to the initial level (PASS) or it rapidly rises above the critical level due to the thermal runaway (FAIL). At high bus resistance, the SCR ESD operation is not related to the NMOS failure. The HMM passing level (Fig.7b) becomes much higher with the ground bus resistance reduction (R4). However, when the bus resistance is reduced, thermal runaway in SCR becomes dominant (Fig.6b for R4=0.01 and HMM=15kV). The same mixed-mode simulation, but with a conventional active clamp (Fig.2a) shows the passing level of ~ 5.3kV at R5=0.5 Ohm which is substantially higher than the level of ~3.5kV achieved for the same conditions with NR-Clamp (Fig.7b), thus adequately capturing the trend.

# V. Conclusions

A case of unrelated LV circuit blocks failure under system level stress has been studied. Based on the experimental and mixed-mode simulation results it has been demonstrated that damage of the LV analog domains at negative ESD stress under power-on conditions is the result of the extra voltage drop induced on the ground bus by the ESD current under the conditions of disabled core active clamp. Unlike conventional active clamps which retain certain protection capability in power-on mode, the active clamp with power supply noise rejection provides comparatively inferior protection capability in power-on state. To satisfy the requirements of noise rejection protection of the low voltage domain can be carried out by a dedicated snapback NMOS or an avalanche diode clamp in parallel with active clamp to, essentially, protect the main clamp during the system level pulse event. This approach has been fully validated on the IC product level with minimum impact on the chip footprint in form of less than 1 bond pad size clamp.

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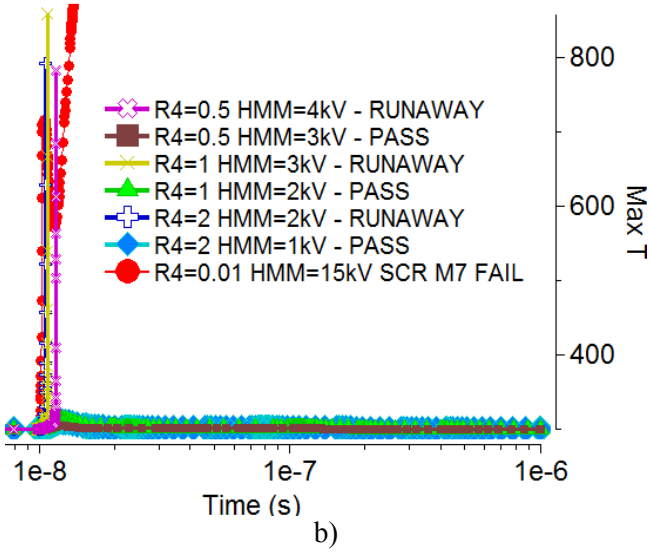


b)

Figure 7: Mixed-mode simulation circuit with 2-transistor array model used to reproduce experimental results with different active clamp options (a) and waveforms for peak temperature in device M6 and M7 for different ground bus resistance R4 and HMM pulse level (b)


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