Analysis and Solution to the ESD Failure Caused by Plasma Protection Diodes for MIM Capacitors

Jian Liu, Nate Peachey

Qorvo Inc., 7628 Thorndike Road, Greensboro, NC 27409, USA
tel.: 336-664-1233, e-mail: jian.liu@qorvo.com

Abstract – This paper introduced the analysis to an early ESD failure caused by the plasma protection diodes used for MIM capacitors in an SOI CMOS technology. TLP ESD testing on multiple designs and transient ESD simulations with various combination of schemes were employed to identify the reason for the early failure, which was confirmed later by OBIRCH. Solution was proposed and verified by both simulation and measurement.

I. Introduction

Reactive ion etching (RIE) is a widely-used technology in the advanced CMOS IC manufacturing process, which etches deposited materials on the wafer by using chemically reactive plasma [1]. As reported in [2-11], the plasma used in the RIE process for both bulk and SOI CMOS technologies can transfer charges to the wafer. And those charges will flow in partially formed circuits and gradually build up voltage across the transistor gate oxides or the metal-insulator-metal (MIM) capacitor dielectrics. As a result, it will cause oxide or dielectric plasma-induced damage on wafers and eventually leading to significant manufacturing yield loss.

To avoid the plasma-induced damage due to RIE process, discharge circuits, which are usually small-size plasma protection diodes (or plasma diodes), need to be added into the circuits to provide a bi-directional discharging path across the transistor gate oxide or MIM capacitor dielectric [12-22]. Thus, for some legacy designs without immunity to plasma damage, it often requires a thorough update to the existing circuits by adding plasma diodes to those elements which are vulnerable to the plasma-induced damage.

This paper will introduce a case of early electrostatic discharge (ESD) failure that is caused by adding plasma diodes to the legacy designs without consideration for ESD protection implication. The first part will discuss the early ESD failures observed on several prototype designs, and analyze the reason for ESD failure by referring to Transmission Line Pulse (TLP) ESD measurement and transient ESD simulation on several similar legacy designs. The second part will provide the solution which is demonstrated by transient ESD simulation and proved by the TLP measurement on ESD-improved designs. This will show that the ESD protection degradation issue caused by plasma diodes was fixed. In addition, the Optical Beam Induced Resistance Change (OBIRCH) results will further confirm the conclusion from the failure analysis. The initial hypothesis is based on the TLP measurement and transient ESD simulation that the additional plasma protection diode is the reason for early ESD failure.

II. ESD Failure and Analysis

Unprecedented ESD failures are found on the 5-V power supply pin VDD of multiple RF switch digital controller prototype designs in a 2.5-V SOI CMOS technology. TLP measurement is performed using the TLP tester from Grund Technical Solutions. TLP pulse width is 100 nS while its rise time is 10 nS. Typically a 1.50-A current level is used, approximating Human Body Model (HBM) 2.25 kV (based on HBM peak current) because of the product ESD rating requirement and sample reuse purpose.

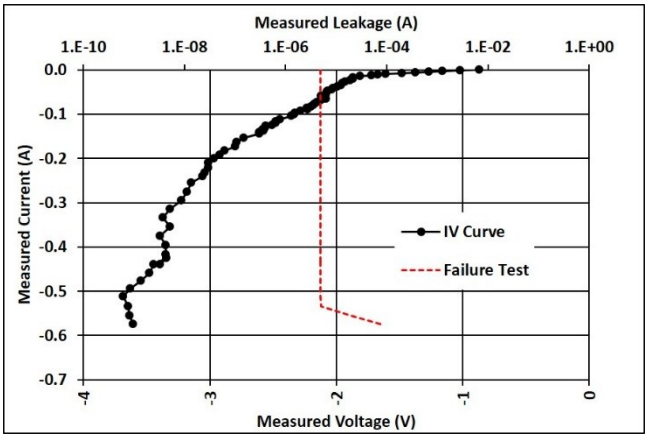

Figure 1: TLP I-V curve of design A-01: VDD-GND (-).

As shown in Figure 1 and Table 1, the ESD failures occur during negative TLP ESD zapping from VDD

pin to GND pin, with breakdown voltage (V_{BR}) lower than 4 V and breakdown current (I_{BR}) lower than 0.60 A, equivalent to 0.90-kV HBM voltage. This result is confirmed on multiple samples.

Table 1: ESD Failures at VDD Pins for Prototypes

Design under Test	VDD-GND (-)	
	TLP I_{t2} (A)	Equivalent HBM Voltage (kV)
A-01	0.51	0.77
A-07	0.54	0.81
B-01	0.43	0.65
B-07	0.47	0.71

To understand the root cause of this early ESD failure, first, the VDD scheme of those failed prototypes are checked. Second, TLP ESD measurements are performed on some other legacy designs with similar VDD schemes fabricated in the same SOI CMOS technology, some of which did not have any early failure at VDD pin. Third, transient ESD simulations are run with various VDD schemes from different designs, to further analyze the failure mechanism. Finally, OBIRCH test is performed to physically identify the failures on those failed samples.

A. VDD Schemes of Failed Prototypes

As presented in Figure 2, the VDD scheme of all failed designs are similar. First, their ESD protection circuit is composed by two parts: a 5-V dual-time-constant unlatching RC ESD clamp with stacked 2.5-V transistors [23] against positive ESD transient and double ESD diodes against negative ESD transient. Second, MIM capacitors are connected between VDD and GND pins with double plasma diodes against plasma damage from RIE process during wafer fabrication. Third, two RC filters are placed between VDD and GND pins, with single plasma diode for every MIM capacitor inside.

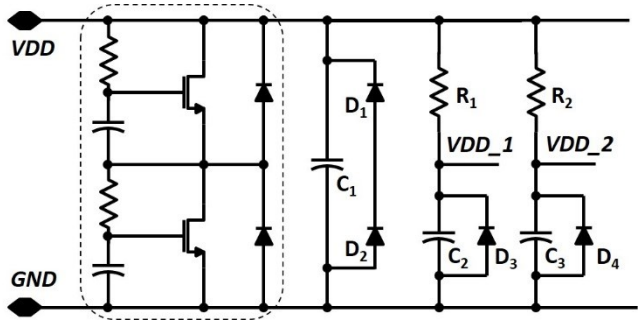

Figure 2: VDD scheme of prototypes with early failures.

Compared with the similar legacy designs without early ESD failure at VDD pin, the only major update performed to all failed prototypes is adding single or double plasma diodes for those MIM capacitors near their VDD pins. Therefore, to check if the additional plasma diodes cause the ESD failure in those prototypes, several relevant legacy designs are measured by TLP and their VDD schemes are analyzed. Among them, some pass 1.50-A TLP ESD zapping at VDD pin while some other fail early.

B. VDD Schemes of Legacy Designs and Their TLP Measurement Data

As shown in Figure 3, the design L-01 has similar 5-V VDD scheme as those failed prototypes but without any plasma diodes. Figure 4 confirms that legacy design L-01 VDD pin survives 1.50-A TLP current during TLP ESD test.

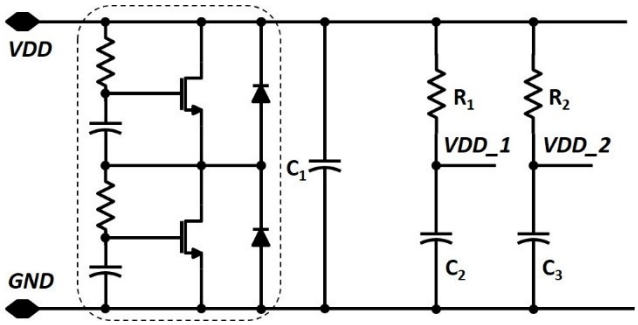

Figure 3: VDD scheme of legacy design L-01.

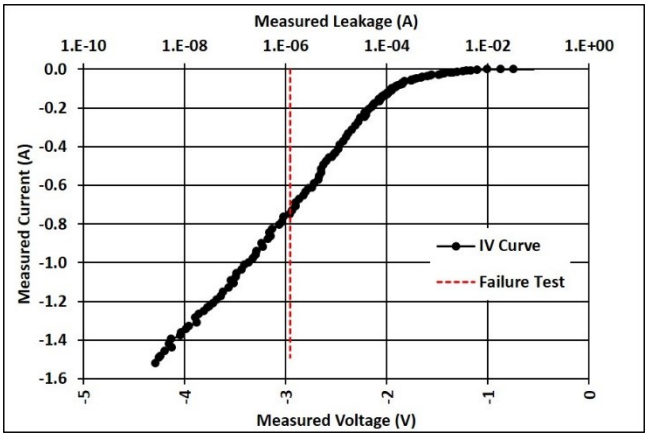

Figure 4: TLP I-V curve of design L-01: VDD-GND (-).

As presented in Figure 5, the design L-02 also has similar 5-V VDD scheme as those failed prototypes, however it only has single plasma diode being added to every MIM capacitor in RC filters but no plasma diode for the MIM capacitor between VDD pin and GND pin. TLP ESD testing on L-02 produces early failure at

VDD pin similar to those failed prototypes, as shown in Figure 6.

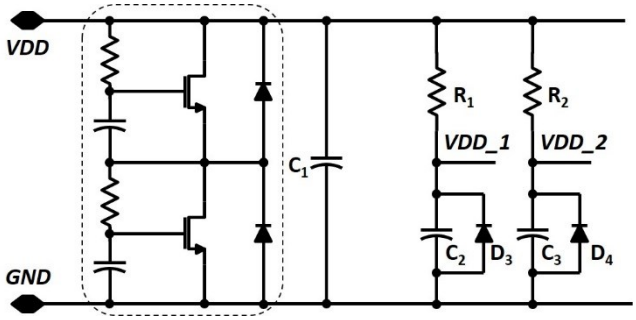

Figure 5: VDD scheme of legacy design L-02.

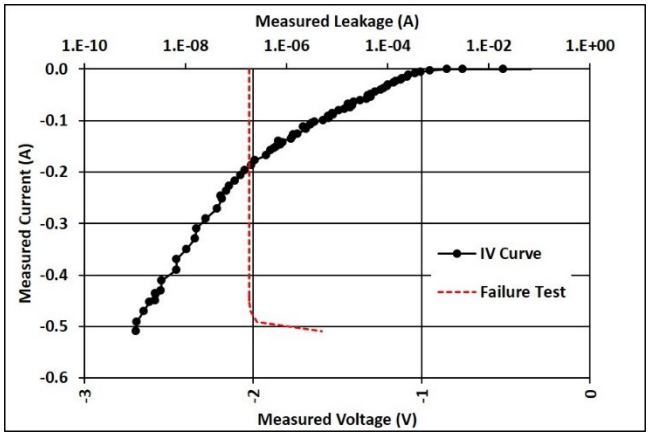

Figure 6: TLP I-V curve of design L-02: VDD-GND (-).

The third similar design under study is L-03, which has a 2.5-V power supply pin VDD. As indicated in Figure 7, design L-03 has single plasma diode for every MIM capacitor between its 2.5-V VDD pin and GND pin, where a 2.5-V dual-time-constant unlatching RC ESD clamp and single ESD diode act as its VDD ESD protection circuit. Similar to design L-01, TLP ESD measurement proves that design L-03 VDD pin survived 1.50-A TLP current, as indicated in Figure 8.

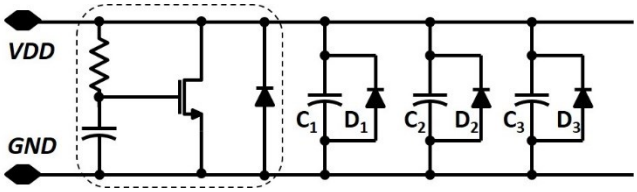

Figure 7: VDD scheme of legacy design L-03.

Table 2 summarizes the TLP ESD measurement results and plasma diode configuration in the schemes of various designs discussed above. Several conclusions could be drawn from the table. First of all, comparing the results between failed prototypes and the passed design L-01, the additional plasma diodes in failed prototypes seem to be the only major difference between their VDD schemes and therefore possibly the reason for the early ESD failures. However, plasma diodes are added to the failed prototypes at two locations, double plasma diodes at VDD pin and single plasma diode in the RC filters. Which part accounts for the early ESD failure at VDD pin? Further analysis gives the answer.

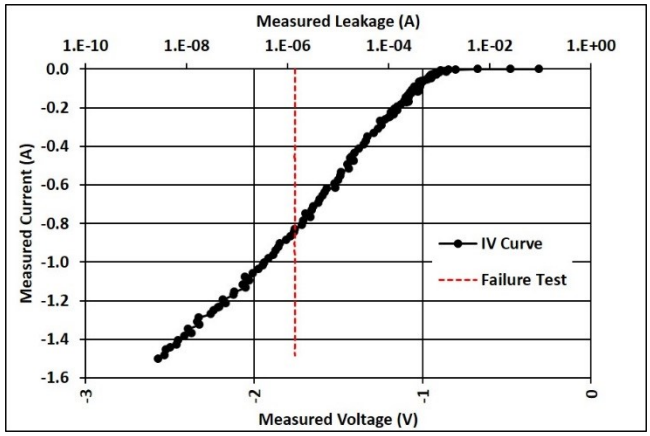

Figure 8: TLP I-V curve of design L-03: VDD-GND (-).

On the one hand, the design L-02 fails early at VDD pin, which has no double plasma diode at its VDD pin but contains single plasma diode in its RC filters. That means the single plasma diode in RC filters leads to the early ESD failure. On the other hand, the design L-03 has 3 single plasma diodes at its 2.5-V VDD pin, but all of them are successfully protected by the single ESD diode connected in parallel with them during negative ESD zapping. Therefore, it could be inferred that the plasma diodes at VDD pin will be protected by ESD diodes in parallel with the plasma diodes, if the plasma diodes and the ESD diodes have the same amount of diodes in series.

Table 2: ESD Failures and Plasma Diode Configuration

Design under Test	Early ESD Failure	Plasma Diode Configuration
Prototypes	Yes	Double at 5-V VDD and single in filters
L-01	No	None is used
L-02	Yes	Single in filters
L-03	No	Single at 2.5-V VDD

In summary, it is highly possible that the single plasma diode in the RC filters causes the early ESD failure at VDD pin during negative ESD zapping, while the double plasma diodes are protected by the double ESD diodes connected in parallel at VDD pin. To verify this assumption, transient ESD simulations are run with

different VDD schemes including ESD protection didoes, plasma diodes and resistors from the RC filters.

C. Transient ESD Simulation for VDD Scheme of Failed Prototypes

The process design kit (PDK) of the 2.5-V SOI CMOS technology employed here provides diode ESD model, which is a behavior model based on Verilog-A and TLP measurement for transient simulation in ESD high current region. Warning message will be shown during transient simulation if the ESD diode current exceeds its model failure current. Therefore, it could be used to analyze the ESD failure mechanism.

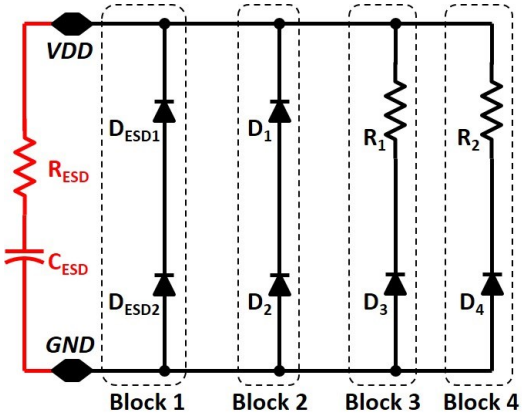

Figure 9: Transient ESD simulation test bench for failed prototypes.

As shown in Figure 9, the test bench uses HBM ESD transient pulse generator in simulation to zap the circuit and targets at the maximum HBM ESD voltage (max. HBM) the circuit can sustain and the ESD breakdown voltage (V_{BR}) at the VDD pin or on every plasma diode. As presented in the test bench, the HBM ESD transient pulse generator includes one 100-pF capacitor, C_{ESD}, and one 1.5-kΩ resistor, R_{ESD}. The circuit under stress is derived from the VDD scheme of failed prototype designs, which is composed by several blocks. Among them, block 1 has the double ESD diodes, D_{ESD1} and D_{ESD2}, while block 2 includes the double plasma diodes, D_1 and D_2. In addition, block 3 or block 4 has the equivalent RC filter branch with a 25-Ω resistor, R_1 or R_2, and single plasma diode, D_3 or D_4, separately. MIM capacitors are not included in the circuit because their high dielectric breakdown voltage (~ 15 V) means they are not likely to go to breakdown in this simulation. The total perimeter of each ESD diode is 210 µm, while the total perimeter of each plasma diode is only 2 µm. Then ESD transient simulation is performed with different blocks under ESD stress, to reveal the characteristics and distribution of ESD voltage or ESD current across or through every block in the circuit during ESD zapping. The results are summarized in Table 3.

Table 3: Transient ESD Simulation for Failed Prototypes

Block under Stress	Max. HBM (V)	V_{BR} (V)
Block 1 only	4076	5.30
Block 2 only	42	3.03
Block 3 or 4 only	41	2.16*
Block 1 and 2	1818	3.03
Block 1, 2, and 3 or 4	372	2.17*
Block 1, 2, 3, and 4	418	2.17*

*V_{BR} is always 1.51 V across D_3 or D_4.

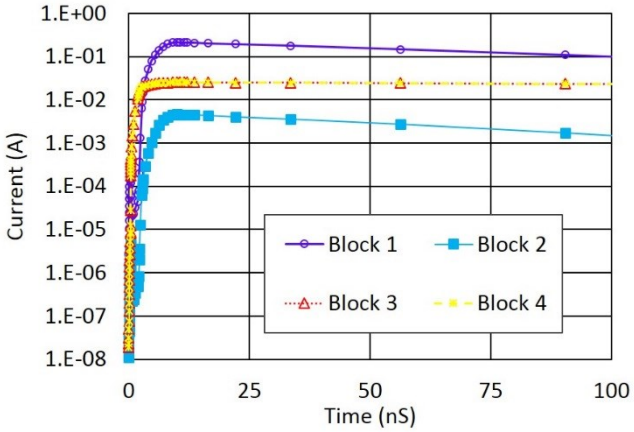

Figure 10: Block current distribution during transient ESD simulation with all 4 blocks for failed prototypes.

Table 3 presents the transient ESD simulation results, which confirms the assumption above that the single plasma diode in the RC filters causes the early ESD failure at VDD pin during negative ESD zapping. First, transient ESD simulation with block 1 shows that 210-µm double ESD diodes fails at 4076-V HBM voltage and their V_{BR} is 5.30 V. In addition, simulation with block 2, 3 or 4 separately proves that the 2-µm plasma diodes all fails at 42-V or 41-V HBM voltage and single plasma diode V_{BR} is always 1.51 V. Second, simulation with block 1 and 2 confirms the conclusion drawn from TLP data of L-03 in Table 2 that the plasma diodes at VDD pin will be protected by the parallel-connected ESD diodes if they have the same number of diodes in series, even though the simulated max. HBM, 1818 V, is slightly lower than the design target of 2-kV HBM voltage. Third, the rest of the simulations which includes both double ESD diodes and part or all single plasma diodes confirms the final assumption based on TLP data in Table 2 that single plasma diode in RC filters is the weakest instance in the prototype design

VDD scheme, because double ESD diodes are not able to clamp ESD voltage for single plasma diode below the single plasma diode V_{BR}. The VDD schemes of all failed prototype designs has to be redesigned.

Figure 10 shows the transient ESD current values through each block at different time when all 4 blocks are stressed by 417-V HBM ESD during transient ESD simulation. As presented, right before plasma diode breakdown, considerable amount of ESD current goes through block 3 or 4, even though the 25-Ω resistor from RC filter, R_1 or R_2, already exists in the block. With the increase of ESD zapping level, the ESD current flowing through plasma diode will rise up and finally damage the plasma diode. It further confirms the analysis above on the reason for the early failure.

D. Failure Analysis by OBIRCH

As presented above, a thorough failure analysis is performed based on TLP ESD measurement on prototype and legacy designs, as well as transient ESD simulation with various VDD schemes including ESD diodes and plasma diodes. In the meanwhile, failed samples are also submitted for OBIRCH test, to physically identify the failure location on the samples. As shown in Figure 11, it is confirmed by OBIRCH on multiple failed samples that the plasma diode in the RC filters at VDD pin is the failure point, by detecting its current going up after the scanning laser heated the area of circuit.

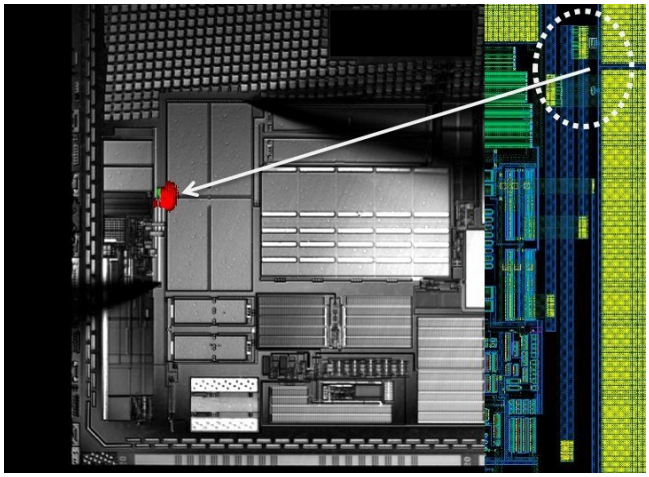

Figure 11: OBIRCH emission indicates failure location near the VDD pin of a failed prototype sample.

III. Solution and Verification

The transient ESD simulation not only explains the failure mechanism of the VDD pin in all failed prototypes, but also indicates the method to fix those early ESD failures.

Based on the failure mechanism revealed in Section II, improvement on ESD protection ability of those failed prototype VDD scheme could be realized in several ways. First, ESD diodes and plasma diodes connected in parallel should have the same number of diodes in series, to enable the plasma diodes survive negative ESD zapping from VDD to GND pin. Therefore, the number of plasma diodes in series should be two, same as the number of ESD diodes in series. Second, the ESD current going through the plasma diode block during ESD zapping needs to be restricted, to boost the V_{BR} of the whole plasma protection block and protect the plasma diode. Thus, a relatively large resistor could be added in series with the plasma diodes. It is important to note that these two methods proposed above will neither sacrifice too much layout area nor defeat the primary purpose of the plasma diode, which is to avoid the plasma-induced damage due to RIE process. Third, it is optional to increase the perimeter of double ESD diodes at VDD pin, to further reduce the ESD clamping voltage for the plasma protection block, since the size of current double ESD diodes is already big enough to meet the product 2-kV HBM ESD rating requirement.

A. Solutions to Improve the VDD ESD Protection Scheme of Failed Prototypes

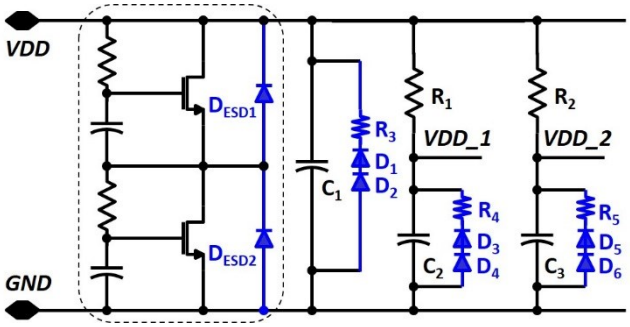

Figure 12: VDD scheme of ESD-improved prototypes.

As presented in Figure 12, two major improvements are applied to the VDD scheme of those failed prototypes. First, all existing single or double plasma diodes are replaced by double plasma diodes and a series 800-Ω resistor, to limit the current through the plasma protection branch and therefore boost the V_{BR} of the whole branch. Second, the size of double ESD diodes is increased almost 50% from previous 210 μm to the current 300 μm, to further reduce the ESD clamping voltage during the negative ESD zapping between VDD and GND and gain more ESD protection margin.

B. Transient ESD Simulation for VDD Scheme of ESD-Improved Prototypes

Transient ESD simulations are run again to verify the solution proposed above. As shown in Figure 13, the circuit under stress is composed by several blocks. Block 1 has the enhanced double ESD diodes, D_{ESD1} and D_{ESD2}, while block 2 contains the double plasma diodes, D_1 and D_2, and the series 800-Ω resistor, R_3. Moreover, block 3 or block 4 is the equivalent RC filter branch with a 25-Ω resistor, R_1 or R_2, and the plasma protection branch, which contains double plasma diodes and a series 800-Ω resistor, D_3 , D_4 and R_4, or D_5, D_6 and R_5, separately. Here MIM capacitors are not included in the simulation for the same reason as before. The total perimeter of each enhanced ESD diode is 300 µm, while the total perimeter of each plasma diode is still 2 µm.

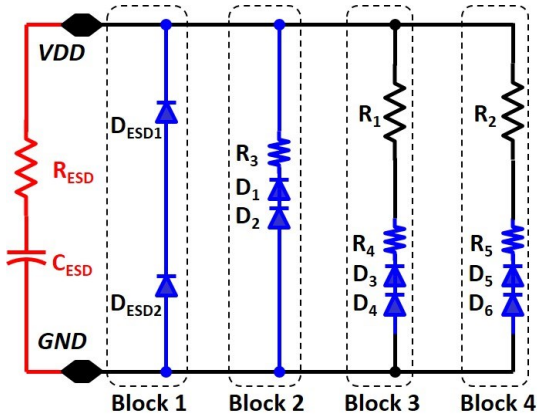

Figure 13: Transient ESD simulation test bench for ESD-improved prototypes.

Table 4: Transient ESD simulation for ESD-Improved Prototypes

Block under Stress	Max. HBM (V)	V_{BR} (V)
Block 1 only	5839	5.51
Block 2 only	62	23.25*
Block 3 or 4 only	62	23.75*
Block 1 and 2	5846	5.51
Block 1, 2, and 3 or 4	5845	5.51
Block 1, 2, 3, and 4	5858	5.51

*V_{BR} is always 1.51 V across every plasma diode.

ESD transient simulation is performed again with different blocks under ESD stress. Table 4 summarizes the transient ESD simulation results, which confirms that the solution proposed above significantly improves the VDD ESD protection performance in those failed prototypes. First, enhanced double ESD diodes fails at 5839-V HBM voltage and the block 1 total V_{BR} is 5.51 V, as shown by simulation with block 1 only. Second, simulations with only block 2, 3 or 4 presents that their 2-µm plasma diodes will all fail at 62-V HBM voltage, but the total V_{BR} of the entire block now all rise up to 23.75 V. As proved by the following simulations, this increased V_{BR} will greatly improve the ESD protection margin for the whole VDD scheme during negative zapping to GND. Third, the rest simulations with block 1 and one or all of the other blocks demonstrate that the redesigned VDD scheme fixes early ESD failures caused by plasma diodes and finally meet the ESD protection target, because the voltage at VDD pin is clamped by the enhanced double ESD diodes significantly below the V_{BR} of any other block with plasma diodes during negative ESD zapping.

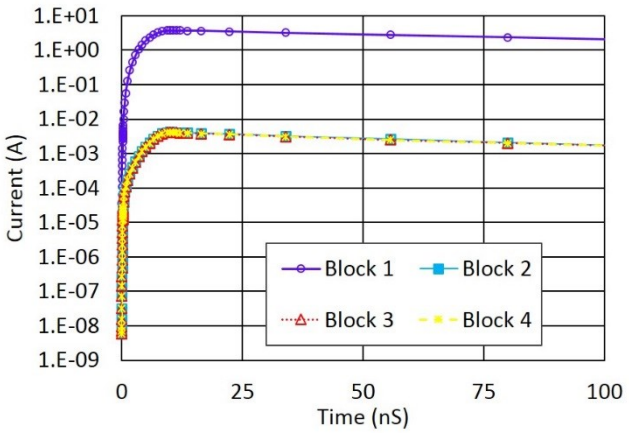

Figure 14: Block current distribution during transient ESD simulation with all 4 blocks for ESD-improved prototypes.

Figure 14 presents the transient ESD current values through each block at different time when all 4 blocks are stressed by 5857-V HBM ESD during transient ESD simulation. As shown in the figure, most ESD current now goes through block 1, which is the designed primary path with double ESD diodes to shunt ESD current, and as a result, the ESD currents flowing through the other blocks reduce severely. Therefore, plasma diodes in the ESD-improved VDD scheme are successfully protected by the ESD diodes during ESD zapping. It firmly predicts that the early ESD failure due to plasma diodes could be fixed by the solution based on failure mechanism analysis and ESD transient simulation.

C. TLP Measurement on ESD-Improved Prototypes

ESD-improved prototypes were fabricated in the same 2.5-V SOI CMOS technology after the solution was applied to the designs. Later TLP measurements are

performed on those ESD-improved prototypes, and the results, as shown in Table 5, are consistent for all the ESD-improved prototypes. Their VDD pins survive 1.50-A TLP current during negative zapping to GND, equivalent to 2.25-kV HBM voltage. As presented in the Figure 15, the TLP I-V curve of one ESD-improved prototype, A-17, demonstrates the new ESD protection scheme at VDD pin can provide significantly better ESD clamping and hence higher ESD protection level. In addition, all ESD-improved prototypes have been qualified at 2-kV HBM level through following the qualification procedure as described in the document ANSI/ESDA/JEDEC JS-001-2014 [24].

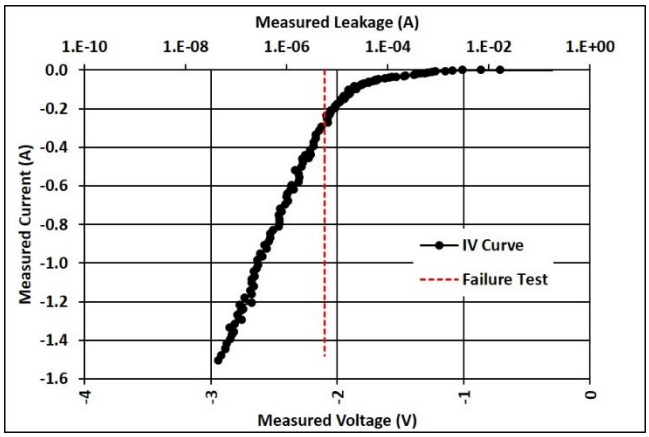

Figure 15: TLP I-V curve of one ESD-improved design A-17: VDD-GND (-).

Table 5: TLP Data at VDD Pins for ESD-Improved Prototypes

Design under Test	VDD-GND (-)	
	TLP I_{t2} (A)	Equivalent HBM Voltage (kV)
A-17	1.50	2.25
A-18	1.50	2.25
B-21	1.50	2.25
B-22	1.50	2.25
B-27	1.50	2.25
B-29	1.50	2.25

IV. Conclusions

This paper reports an early ESD failure caused by the plasma diodes. They are added to all MIM capacitors near VDD pins of several RF switch digital controller prototypes, in order to prevent plasma-induced damage due to RIE process in the 2.5-V SOI CMOS wafer production. The failure analysis is performed by gathering TLP ESD zapping data from different similar designs and running transient ESD simulations with various VDD schemes. It indicates that the single plasma diode in the RC filters causes the early ESD failure at VDD pin during negative ESD zapping, later confirmed by OBIRCH emission test on samples with same failures. The solution to improve the failed prototypes is provided based on ESD failure analysis and ESD failure mechanism, and pre-verified by transient ESD simulation and post-verified by TLP measurement.

This work proves the necessity and importance of ESD design review in circuit design, even when only minor changes are applied at the circuits around top IO pins. In addition, it also proves that the TLP measurement, combined with transient ESD simulation, could be an effective and timely tool to identify the reason for ESD failure, analyze the failure mechanism, and verify the solution before design tape out.

V. References

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