Abessolo-Bidzo, Dolphin

Dolphin Abessolo-Bidzo received his MSc in 2004 from ENSI Caen, France, and his PhD in 2007 from the University of Caen Basse-Normandie, France; both in electrical engineering. His PhD thesis was on test methodology for RF and microwave characterization of advanced microelectronics passive and active devices and their electrical modeling. He joined Philips Semiconductors (now NXP Semiconductors) in 2004 for his PhD work, as an R&D engineer. Since 2008, he has worked as a principal RF ESD/IO design engineer in advanced RFCMOS and BiCMOS technologies. Dolphin is also involved in the development and the ESD and latch-up qualification of I/O libraries as well as the ESD and latch-up consultancy before tape-out of RF and analog IC's. His focus is currently on IC packages modeling under CDM, the development of RF I/Os for high speed and millimeter wave applications, and ESD check tools. He also gives internal RF ESD design workshops to NXP's RF design community. Dolphin has published several papers in IEEE scientific journals, symposia, and conferences on ESD, RF, and time domain analysis. He has served as member of the technical program committee of the 2012 International Electrostatic Discharge Workshop, and the 2014, 2015, 2016, and 2017 EOS/ESD Symposia. He served as sub-committee chair and session moderator at the 2016 EOS/ESD Symposium.

Aharoni, Efraim

Efraim Aharoni received a BSc degree in physics in 1989 and a PhD in physics in 1994 from Technion, Israel Institute of Technology. His research at Technion was focused on high temperature superconducting devices. In 1993, he joined TowerJazz; where he worked in a variety of fields, in both engineering and management, in development as well as production. His engineering roles included process, device, yield, and reliability. In the past few years, he has led the ESD and latch-up activities at TowerJazz. This involves the development of new ESD devices and protection concepts, ESD characterization and design guidelines, creating libraries of ESD devices, PERC, and customer support. He works closely with the TowerJazz design center, device engineering, PDK group, customers, and production lines in sites worldwide. In addition, he is a member of the electrical engineering department at Kinneret College and lectures on a variety of courses. In 2015 and 2016, Efraim was a member of the IEW technical program committee, and in 2017 he is a member of the EOS/ESD Symposium technical program committee. Efraim is a member of the Industry Council of ESD Target Levels and participates on one of the sub-teams.

Ali, Muhammad

Muhammad Ali received his PhD in electrical engineering in 2008 from the University of Texas at Arlington. He joined the analog ESD team at Texas Instruments, Dallas, Texas, in 2008 as an ESD product specialist. After staying in that role for 6 years, Muhammad joined the analog ESD development team as an ESD technology specialist. His responsibilities include design and development of ESD protection structures in various analog and advanced CMOS technologies. He was elected member of the technical staff (MGTS). Muhammad has four US patents granted and one pending.

Alvarez, David

David Alvarez received his MS in solid state physics from Complutense University of Madrid, Spain, in 2000; and his PhD in electrical engineering from Catholic University of Leuven (KUL), Belgium, in 2007. Since 2004, he has worked for Infineon Technologies in the area of on-chip ESD protection for CMOS technologies. He has authored/co-authored several papers at EOS/ESD Symposia.

Ammer, Michael

Michael Ammer studied electrical engineering at Ostbayerische Technische Hochschule Regensburg

(OTH Regensburg), Germany. In 2015, Ammer received a MSc. Besides his studies, he worked within Continental Automotive in Regensburg, Germany, in the department of sensors advanced development of powertrain division as a working student. The research for his bachelor's and master's theses were also done in this department. During his studies, the course about EMC in automotive applications aroused Ammer's interest to this topic. In consequence, he joined the automotive division of Infineon Technologies at Munich to support the automotive power ESD team as a PhD student for system level topics.

Andreini, Antonio

Antonio Andreini, director of technology reliability qualification, ESD protections design, and front-end/back-end compatibility validation for smart power technologies within STMicroelectronics R&D. He graduated in physics from the University of Milan in 1983 and he started working at STMicroelectronics on the development of discrete power MOS components. He then moved to the development of mixed technologies dedicated to the design of power ICs, contributing to initiate the development of the BCD (bipolar CMOS DMOS) technologies. He has worked on different generations of this technology family, covering mainly the high voltage field, both junction and dielectric isolated. Since the late 1990's he progressively broadened his competences and responsibilities to technical fields related to the quality and the robust validation for those technologies. He started from the ESD protection design, being also responsible for STMicroelectronics in international funded R&D projects in the ESD field, labeled by the MEDEA consortium. Then, in 2005 he became manager of the technology reliability qualification and of the activities aimed at studying the silicon die – package interaction for all smart power and high voltage technology platforms. He published several technical papers and got many international patents in all the mentioned technical fields.

Angeli, Stefano

Stefano Angeli graduated in electronics from Polytechnic University of Milan in 2004, discussing a thesis on automatic analog layout generation through automatic generation software that was developed in STMicroelectronics in collaboration with NVM PDK team in more than one year on CMOS technologies. From 2004 to 2005, Stefano worked in the MTA industry in the R&D division as automotive fuse developer and QA responsible for electronics and electrical car components (corrosion, aging, ESD, melting, functionality in normal condition and in very aggressive automotive corners of temperature, pressure, voltage, current and humidity). Since 2005, he has been working in STMicroelectronics on different fields including DRC and LVS developer using Calibre tool of Mentor; generation of technology migrations tools (skill/c++/tcl-tk programs and/or methodology to apply them); Pcells generations through skill code or semi-automatic tools (for example Modgen generator); development of new ApenAccess (OA) technology file with incremental structures for technology at 90 nm, 65 nm, 40 nm, and 28 nm. Enabling of interoperability between tools using same OA database. (For example MSoT interoperability between Encounter and Virtuoso); and PERC CD file development to search and find any possible ESD discharge path inside a chip. Stefano has authored technical papers on automatic testing environment (in collaboration with Cadence) presented in EMEA CDN Live event in 2012; layout research and simulation of ESD paths inside a chip presented in EMEA U2U event in 2016.

Asam, Michael

Michael Asam received his Dipl.-Ing. degree in electronic engineering from the University of Applied Sciences, Augsburg, Germany, in 1997. Since 1997, he has been with Infineon Technologies (formerly Siemens AG Semiconductors) as an RF IC circuit designer for BiCMOS and CMOS transceivers and power amplifiers for wireless communications. Since April 2007, he has been with Infineon Automotive and Industrial Devices as

a senior staff engineer involved in the design of high current switches.

Backers, Ilse

Ilse Backers received a master's degree in electrical engineering from the Technical University KHBO in Ostend, Belgium. She joined Sofics (formerly known as Sarnoff Europe) in September 2006 as an ESD design engineer, and currently holds the position of senior ESD engineer. She leads multiple ESD projects. Her main focusses include low capacitance and IoT applications, in various technologies ranging from 180 nm down to 16 nm FinFETS. Furthermore, she was involved in the development of easy-to-use optimization and integration and verification tools. Ilse has authored and coauthored several papers and patent applications.

Banghart, Edmund

Edmund Banghart received his BS from the University of Michigan (Ann Arbor) in 1983 and received his MS and PhD from Purdue University (West Lafayette, IN) in 1989; all in electrical engineering. In his graduate research, he investigated high injection recombination mechanisms in silicon solar cells using semiconductor simulation tools. After graduation, he joined Kodak Research Labs (Rochester, NY); where he developed original simulation programs and applied leading commercial software packages for the design of CCD and CMOS image sensors. In 2013, he joined the TCAD simulation group at GLOBALFOUNDRIES (Malta, NY); where he supports logic device design and manufacturing activities using advanced numerical simulation tools for semiconductor process and device modeling. He has written a number of articles in leading technical journals, presented at international conferences, and co-written a book chapter on device simulation. He also holds several US patents in the field of semiconductor devices and technology.

Bhat, Navakanta

Navakanta Bhat (SM'02) received a BE in electronics and communication from the University of Mysore, Mysore, India, in 1989; a M.Tech in microelectronics from Indian Institute of Technology Bombay, Mumbai, India, in 1992; and a PhD in electrical engineering from Stanford University, Stanford, CA, USA, in 1996. He has been with the Indian Institute of Science, Bangalore, India, since 1999; where he is currently a professor. His research area includes device modelling and GaN technology.

Beetner, Daryl G.

Daryl G. Beetner (S'89–M'98–SM'03) received a BS in electrical engineering from Southern Illinois University, Edwardsville, IL, USA, in 1990; and a MS and DSc in electrical engineering from Washington University, St. Louis, MO, USA, in 1994 and 1997, respectively. He is currently professor and chair of electrical and computer engineering at Missouri University of Science and Technology (formerly the University of Missouri–Rolla); where he conducts research with the Electromagnetic Compatibility Laboratory on electromagnetic immunity and emissions from the integrated circuit to system level.

Besse, Patrice

Patrice Besse received a master's in electronics in 1999 and then a post master's in electromagnetic compatibility from the Blaise Pascal University in 2000. In January 2004, he received a PhD in electronics (ESD) from the University of Paul Sabatier, Toulouse, France. From 2000 to 2003, he developed ESD protections for BiCMOS technologies within the R&D group of Motorola. In 2004, he has joined the analog and mixed power division of Freescale Semiconductor in France; where he was responsible for the ESD protections for analog applications. His focus was on the development of integrated solutions to pass ESD and EMC system level stress and in particular for automotive applications. He has provided ESD trainings and design guidelines within the company

and he also delivers ESD/EMC courses to student engineers. Currently, Patrice leads the ESD and EMC central group delivering solutions for automotive analog and sensor products at NXP Semiconductors. In 2011, he received the best paper award at EMC-Compo. He serves on the TPC for the EOS/ESD Symposium, EMC Compo, APEMC, and ESREF. He holds 33 patent applications with several pending, he is author or co-author of 32 papers including tutorials.

Bogani, Antonio

Antonio Bogani is responsible for physical layout verification and introduction of new tools for STMicroelectronics' smart power design kits. He has been with ST since 1985. After three years as a layout engineer, he moved into the CAD team in charge of providing support for BCD technologies; where he began to work as developer of physical verification (DRC and LVS) deck files. In 1992, he was a member of the team that defined the first concept of DK in ST; between 1998 and 2007, he also took care of post layout simulation for the same platforms. Today, he acts both as responsible for physical layout verification and as coordinator for the activities for the introduction in smart power PDK of new EDA solutions.

Boschke, Roman

Roman Boschke received his master's in electrical engineering from the TU Dresden (Technical University Dresden) in 2005. Since 2005, he has been working on CMOS device development, integration, and characterization in AMD and GLOBALFOUNDRIES in Dresden. He also worked in research projects including sSOI and ferroelectric memory development. In 2013, he joined imec and KU Leuven as a PhD student. He focuses on implications of the usage of Ge in ESD protection devices.

Boselli, Gianluca

Gianluca Boselli completed his master's in EE at the University of Parma, Italy, in 1996. In 2001, he completed his PhD at the University of Twente, The Netherlands; where he worked on high current phenomena in CMOS technologies. In 2001, he joined Texas Instruments, Inc., Dallas, Texas; where he focused on ESD and latch-up development for advanced CMOS technologies, with particular emphasis on process and modeling aspects. In 2007, his responsibilities extended into ESD development of Texas Instruments' analog technologies portfolio. Dr. Boselli is now the manager of ESD and spice modeling teams. He authored several papers in the area of ESD and latch-up. He presented his work at major conferences, including EOS/ESD Symposia, IEDM, and IRPS. He has also presented many invited tutorials and papers at various conferences, including EOS/ESD Symposia, IRPS, IEDM, ESREF, IEW, and RCJ. Dr. Boselli has been the recipient of the best paper award on behalf of *Microelectronics Reliability Journal* in 2000. He received the best paper award at the 2002 EOS/ESD Symposium. He also received outstanding symposium awards at the EOS/ESD Symposium in 2002, 2006, and 2010. Dr. Boselli served multiple times as sub-committee chair for technical program committees (TPC) of EOS/ESD Symposia, IEDM, IRPS, IEW, and ESREF. He served as moderator and panelist in many workshops in ESD and latch-up areas. Dr. Boselli has served as TPC chair for the 2006 EOS/ESD Symposium, vice-general chair for the 2007 EOS/ESD Symposium, and general chair for the 2008 EOS/ESD Symposium. He is currently a member of the EOS/ESD Association, Inc. board of directors and president of the Association. Dr. Boselli is an IEEE senior member and holds over twenty patents with several pending. Dr. Boselli serves on the editorial board of *IEEE Transactions on Device and Materials Reliability (T-DMR).*

Bourgeat, Johan

Johan Bourgeat received his PhD in 2011 from University Paul Sabatier of Toulouse, France. During his PhD thesis (2008-2011), he worked on advanced ESD protection circuit based on SCR device for CMOS 32 nm node technology at STMicroelectronics. In 2011, he joined STMicroelectronics Crolles as a research engineer and focused his work on new ESD protection and strategies, developing new devices and concepts as bidirectional-SCR, Beta-Matrix network, and Point to Point Protection (PPP) structures. Today, he is in charge of all specific protections and support for space and RF activities. All his work leads to several international publications and patents.

Brown, Daniel P.

Dan is an engineering technician with IBM Systems, Supply Chain Engineering in Tape Storage. Dan has been with IBM for over 27 years, working on the development and modification of manufacturing assembly equipment for various tape products. Along with being responsible for head assembly equipment and tooling, Dan is responsible for the modifications and programming for the wire-bond machine. Dan is also responsible for capital and expense purchases for the tape storage engineering group, as well as managing capital accounts. Dan obtained a vocational degree in electronics, an associate's in computer science, and a bachelor's in management.

Cao, Yiquin

Yiqun Cao received an MSc in electrical and electronic engineering from Rheinisch-Westfälische Technische Hochschule (RWTH) in Aachen, Germany, in 2007. In the same year, he joined smart power technology R&D at Infineon Technologies in Munich, Germany. Since then, he has been involved in the research and development of high voltage ESD device, ESD modeling methodology, ESD measurement technique, and ESD troubleshooting for product qualification. Yiqun works currently as head of the ESD department in the automotive power technology platform at Infineon Technologies; where he is in charge of enabling mixed-signal and power product development by providing ESD, latch-up, and overvoltage robust solutions, involving ESD devices, concepts, ESD modelling, and verification, for component-level as well as for system-level ESD requirements. Yiqun has authored and co-authored more than 30 technical papers and 8 patents in the field of ESD. He was a recipient of the 2010 EOS/ESD Symposium best paper award, and the best paper and the best student paper awards in 2011. Yiqun also serves as a peer reviewer for several IEEE journals. Since 2012, he has been a member of the technical program committee for the EOS/ESD Symposium on a regular basis. He served as the chair of the TPC sub-committee on ESD protection in bipolar, RF, high voltage, and BCD technologies in 2015.

Cerati, Lorenzo

Lorenzo Cerati graduated in telecommunication engineering from Politecnico di Milano Technical University in 1998; discussing a thesis on a CdZnTe cross-connect for optical networks. Since 2000, he has worked for STMicroelectronics in the ESD protections development team for smart power technologies. He is now a senior member of technical staff and manager of the group responsible for ESD protections development, latch-up immunity, and bipolar parasitic analysis in smart power BCD processes. His responsibilities include the simulation of new solutions (both device- and circuit-level), the definition of layout and design rules, and their validation on silicon. He is also in charge of design team support to define, implement, and debug complex ESD architectures. Lorenzo represents STMicroelectronics in the EOS/ESD Association, Inc. standardization committees and has authored several papers on ESD presented at the major conferences, including EOS/ESD Symposia (where he is currently a member of the steering committee), IEW, and ESREF. In 2016, Lorenzo became an EOS/ESD Association, Inc. board of director and vice chairman of working group 5.5 – TLP.

Chang, Tzu-Heng

Tzu-Heng Chang received his BS and MS in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2006 and 2008, respectively. In 2008, he joined the Taiwan Semiconductor Manufacture Company Ltd. (TSMC), Hsinchu, Taiwan. He is currently with the EOS/ESD technology department. His research interests include device ESD/EOS reliability, on-chip ESD protection, and whole-chip ESD review.

Chang, Yi-Feng

Yi-Feng Chang received a BS from the department of physics, National Chung Hsing University, Taiwan, in 2003; and a MS from the department of electrical engineering, National Chiao-Tung University, Taiwan, in 2005. From 2005 to 2010, he was with the Nanya Technology Corporation, Taiwan, as a TCAD engineer working on device development. After that, he joined Taiwan Semiconductor Manufacturing Company, Taiwan. His research activity focuses on the ESD robustness prediction of semiconductor device and ESD device development through physical simulation.

Chen, Kuo-Ji

Kuo-Ji Chen received his BS and PhD from the department of electronics engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 1997 and 2002, respectively. He joined Taiwan Semiconductor Manufacturing Company (TSMC) in 2003 and is currently in charge of both the IO library department and ESD/EOS department.

Chen, Shih-Hung

Shih-Hung Chen received a BS from the department of material science and engineering at National Hu-Wei Institute of Technology, Yunlin, Taiwan, in 2000; a MS from the Institute of Material Science and Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 2002; and a PhD from the Institute of Electronics, National Chiao-Tung University, in 2009. In 2002, he joined the department of ESD and product engineering, SoC Technology Center, Industrial Technology Research Institute, Hsinchu, as an ESD design engineer. Since 2010, he has been with the ESD reliability group at imec, Belgium. He authored or co-authored more than 50 conference and journal publications. He is a peer reviewer for the IEEE *Transactions on Electron Devices*, IEEE *Electron Device Letters*, and IEEE *Transactions on Device and Materials Reliability*. His current research interests include ESD protections for sub-20 nm technologies and 3D integrations.

Chen, Zhong

Dr. Zhong Chen is currently an assistant professor in electrical engineering at University of Arkansas. He received his PhD in electrical and computer engineering from North Carolina State University; a master's in electrical and computer engineering from the National University of Singapore; and a bachelor's from Zhejiang University. Dr. Chen worked for seven years as an ESD specialist in analog technology development at Texas Instruments (TI). At TI, he provides ESD solutions for various analog and digital applications in automotive, power management, power interface, high-speed product, audio and imaging products, and motor drives. He was recognized as a TMG member of technical staff for his contribution and leadership at TI. In his research, Chen focuses on novel devices for harsh environment, integrated circuit (IC) and system level ESD and reliability; power electronics and power devices; and wide-bandgap material, devices, and packaging.

Chu, Li-Wei

Li-Wei Chu received a BS from the department of electrical engineering, National Sun Yat-sen University, Kaohsiung, Taiwan, in 2006; and a MS and PhD from the Institute of ElectroOptical Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 2008 and 2012, respectively. Since 2013, he has been with the Taiwan Semiconductor Manufacturing Company, Taiwan, as a principle engineer. His research interests

include device ESD/EOS reliability, and on-chip ESD protection for high speed circuits.

David, Florence

Florence David received her advanced technician's certificate in chemistry from University Joseph Fourier of Grenoble, France. She worked at STMicroelectronics (France) in 1996 in manufacturing and maintenance. Then in 2000, she joined the logistic department for maintenance. Since 2006, she has been involved in the ESD and latch-up qualification and characterization of the I/O STM offer. She also performs specific and dedicated ESD/LU measurements for R&D test chip and debug.

De Raad, Gijs

Gijs de Raad was born in Ede, The Netherlands, on October 26, 1969. He received his MSc in applied physics in 1995 from the University of Groningen, The Netherlands. He received a PhD in physics in 2001 from the Technical University of Eindhoven, The Netherlands, with the thesis "Voltage-dependent Scanning Tunneling Microscopy on the {110}-Surfaces of GaAs, AlGaAs, and their Heterostructures". Since 2000, he has worked for Philips Semiconductors; which later became NXP Semiconductors. He has been active as an ESD engineer since 2005, with particular interest in the physics of ESD devices.

Di Biccari, Leonardo

Leonardo Di Biccari graduated (summa cum laude) with a degree in electronic engineering at the University of Padova in 2010; discussing a thesis on ESD protection structures for 65 nm PCM memories. In the same year, he joined STMicroelectronics (Milan, Italy) in the R&D ESD protections development team for smart power technologies. As senior ESD engineer, his work includes the layout and design rules definition for all BCD technologies and the design support for complex ESD architectures implementation. In addition, he has been in charge of the investigation of new suitable ESD/EOS solutions (including TCAD and electrical simulations activities) and validation of solutions on silicon. The main focus of his activity is on automotive applications and system-level protections for BCD smart power technologies. Leonardo is author of several papers on ESD presented at EOS/ESD Symposia and IEW; where he is involved in technical program committees. He is also a member of the EOS/ESD Association, Inc. working groups WG25 (CBE) and WG26 (system ESD models). He graduated in piano from Bari Conservatory of Music in 2006.

Esmark, Kai

Dr. Kai Esmark is principal engineer for overvoltage robust designs at Infineon, Munich (Germany). He received his degree in physics (Dipl. Phys.) from the University of Hamburg, Germany, in 1997; and his PhD in electrical engineering about ESD device simulation from Swiss Federal Institute of Technology (ETHZ), Zurich, in 2001. Since then, he has worked on the development of ESD protection concepts for various different process technologies like smart-power, bipolar, BiCMOS, and CMOS technologies with Siemens and Infineon Technologies. Kai has authored and co-authored more than 30 technical papers and one book *Advanced Simulation Methods for ESD Protection Development* in the field of ESD and device physics. He holds 10 patents on the same topic. He received the best paper award of EOS/ESD Symposium 2007 and serves on technical program committees of IRPS, EOS/ESD Symposium, and International ESD Workshop on a regular basis.

Famulok, Nicolai

Nicolai Famulok received a diploma degree in technical physics (corresponding to an MSc) from Technical University Munich (TUM) in 2013. The focus of his studies was particle and nuclear physics. Afterwards, he continued working at TUM as a scientific assistant and worked on a project which involved material analysis using accelerator mass spectrometry, followed by a publication about

the work. In January 2015, he started at Texas Instruments as a failure analysis engineer in freising device analysis operations (FDAO). His work covers most of the typical failure analysis tools and techniques from verification, device preparation, failure isolation, and physical analysis such as IC delayering and cross-sections.

Fung, Rita

Rita Fung has been a senior component engineer at Cisco Systems, Inc. in Hong Kong since 2011. She has been actively engaged in ESD in semiconductor or manufacturing component reliability. She received her MSc in IC design engineering from HKUST and her MEng/BEng in electronic and information engineering from HKPU in Hong Kong. She worked as an ESD engineer in TSMC and Solomon Systech prior to joining to Cisco.

Gauthier, Jr., Robert

Robert Gauthier joined IBM in Essex Junction, Vermont, in 1995; where he focused on device design and TCAD simulations designing devices in 0.35 um technologies. In 1998, he expanded his role within IBM to also look at ESD and latch-up devices in 0.25 um and beyond. From 1998 through 2003, he worked on 0.25 um - 0.13 um technologies getting heavily involved in ESD and latch-up. In 2004, he became an R&D manager at IBM with emphasis on ESD/latch-up development and RF modeling. From 2004 to 2015, he continued to manage the ESD/latch-up team inside IBM along with various other functions such as TCAD. In 2015, he and the majority of his team joined GLOBALFOUNDRIES during an acquisition. Since 2015, he has led the worldwide ESD/latch-up team within GLOBALFOUNDRIES, including folks in USA and Singapore. He has over 250 issued patents with many others filed, he has more than 30 publications at major conferences and journals. He has served on the EOS/ESD Association, Inc. board of directors and is a former EOS/ESD Association, Inc. vice president of technical operations. He was one of the founders of the International ESD Workshop (IEW) and is a former general chair of the EOS/ESD Symposium.

Gebreselasie, Ephrem G.

Mr. Gebreselasie joined the IBM microelectronics division in 2001 after receiving his BS in electrical engineering from Arizona State University; and he received his MS in electrical engineering from the University of Vermont in 2009. Mr. Gebreselasie is responsible for RF device characterization, electrostatic discharge/latchup, ESD design applications and e-fuse development for multiple analog and mixed signal process technologies. He worked on technology development, parametric and functional characterization, reliability, and most lately ESD. He has authored or co-authored several publications and received his third IBM invention achievement award plateau. In July 2015, he transited to GLOBALFOUNDRIES; where he is currently working on the e-Fuse, ESD/latch-up technology enablement team. He received his first patent with GLOBALFOUNDRIES on April 19, 2016.

Gevinti, Elonora

Eleonora Gevinti graduated (summa cum laude) in physics from Insubria University of Como in 2005; discussing a thesis on interlinked parametric optical interactions in classical and quantum regime. Since 2005, she has been working for STMicroelectronics developing and modeling ESD protection architectures for smart power BCD technologies. Since 2011, she has been a senior engineer in developing ESD EDA checks addressed to smart power BCD IC’s. She has authored papers on ESD and ESD EDA presented at EOS/ESD Symposia, IEW, and DAC. Eleonora is a member of EOS/ESD Association, Inc.’s WG 18 - EDA and she is currently serving on the EOS/ESD Symposium technical program committee and 2018 IEW management committee.

Gieser, Horst A.

Dr. Horst A. Gieser is head of the analysis and test team at Fraunhofer-Institution for Microsystems and Solid State Technologies EMFT www.emft.fraunhofer.de. He received his diploma in electrical engineering and his PhD from Technical University in Munich. He has authored and contributed to more than 68 publications. Four papers in the field of electrostatic discharge (ESD) won awards at international conferences. His team received ERC grants in 2014 and 2016 from EOS/ESD Association, Inc. Horst is past-chair of the German ESD FORUM e.V.. He has been serving on standardization committees for ESD test methods and organizing several international conferences. Beyond CC-TLP, CDM, and system level ESD, his scientific interests are in the field of reliability and failure analysis of devices, circuits, and systems as well as characterization techniques with ultra-short transients.

Goh, Yohan

Yohan Goh is sales marketing manager of Everfeed Technology and is currently working in ESD training programs, ESD consulting, ESD risk assessment, and assisting in setting up electrostatic discharge protected area. He had conducted several ESD assessments, consultations, ESD/ESA contamination control workshops for multi-national companies in the Asia Pacific. He has been servicing in the field for more than nine years and has attended training for iNARTE certified ESD engineer and ESDA certified program manager. He has co-authored paper publications and presentations at Asian and Germany EOS/ESD Symposia for Factory Issues.

Gossner, Harald

Harald Gossner (M ‘07, SM ‘11) is senior principal engineer at Intel. He received his degree in physics (Dipl. Phys.) from Ludwig-Maximilians-University, Munich, in 1990; and his PhD in electrical engineering from Universität der Bundeswehr, Munich, in 1995. For 15 years, he has worked on the development of ESD protection concepts with Siemens and Infineon Technologies. In 2010, he joined Intel overseeing the development of robust mobile systems. Harald Gossner has authored and co-authored more than 100 technical papers and two books in the field of ESD and device physics; he holds 60 patents on the same topic. He received EOS/ESD Symposium best paper awards in 2005 and 2012; and was the recipient of EOS/ESD Association, Inc.‘s Outstanding Contribution award in 2015. He is a lecturer of tutorials at ESREF, IRPS, and EOSESD symposia. He has served in technical program committees of IEDM, EOSESD Symposia, and International ESD Workshop. In 2006, he became co-founder and co-chair of the Industry Council on ESD Target Levels. Since 2012, he has also been a member of the board of directors for EOS/ESD Association, Inc.

Groeseneken, Guido

Dr. Guido Groeseneken received an MSc degree in electrical engineering (1980) and a PhD in applied sciences (1986), both from the Katholieke Universiteit Leuven, Belgium. In 1987, he joined the R&D laboratory of imec (Interuniversity Microelectronics Center) in Leuven, Belgium; where he is responsible for research in reliability physics for deep submicron CMOS technologies. From October 2005 until April 2007, he was also responsible for the imec post CMOS nanotechnology program within imec’s core partner research program. Since 2001, he is a professor at the KU Leuven; where he is program director of the master’s program in nanoscience and nanotechnology, and where he is also coordinating a European Erasmus Mundus master’s program in nanoscience and nanotechnology. He became an IEEE fellow in 2005 and an imec fellow in 2007. He has made contributions to the fields of non-volatile semiconductor memory devices and technology, reliability physics of VLSI-technology, hot carrier effects in MOSFET's, time-dependent dielectric

breakdown of oxides, negative-bias-temperature instability effects, ESD-protection and –testing, plasma processing induced damage, electrical characterization of semiconductors, and characterization and reliability of high k dielectrics. Recently, he is also interested in nanotechnology for post-CMOS applications, such as carbon nanotubes for interconnect and sensor applications, tunnel FET's for alternative ultra-low power devices, etc. He has served as a technical program committee member of several international scientific conferences, among which the IEEE International Electron Device Meeting (IEDM), the European Solid State Device Research Conference (ESSDERC), the International Reliability Physics Symposium (IRPS), the IEEE Semiconductor Interface Specialists Conference (SISC), and the EOS/ESD Symposium. From 2000 until 2002, he also acted as European arrangements chair of IEDM. In 2005, he was the general chair of the Insulating Films on Semiconductor (INFOS) conference, organized in Leuven, Belgium. Finally, from 1999 until 2006, he acted as an editor of IEEE *Transactions on Electron Devices*. He has authored or co-authored more than 500 publications in international scientific journals and in international conference proceedings, six book chapters, and ten patents in his fields of expertise.

Grund, Evan

Evan Grund is the founder of Grund Technical Solutions (GTS), a Silicon Valley company specializing in ESD test equipment, including TLP, VF-TLP, HBM, MM, and HMM, and customized automation. Formerly, he served as vice president of Oryx Instruments and as a site manager with Thermo Fisher Scientific, working with ESD testing for both companies. Over the last decade, Evan has designed a variety of HBM, MM, latch-up, HMM, and TLP test equipment. He introduced Kelvin TLP and probe card based TLP. More recently, Evan and his GTS colleagues introduced 2-pin HBM testing; which has now been adopted by the ESD community. Evan began his career as an instrumentation engineer designing nanosecond pulse amplifiers and picosecond timing systems at the Stanford Linear Accelerator Center while completing his MSEE at Stanford University. Prior to joining Oryx, Evan served as an engineering department manager for several Silicon Valley companies, including KLA Tencor, Lam Research, and was a founder of Novellus Systems. Evan has patents issued in the fields of data processing, optical measurements, high power control systems, TLP, HBM, HMM, and pending patents on ESD testers. He has been a frequent presenter at ESD Forums, International ESD Workshops, and EOS/ESD Symposia; he is a member of the technical program committees for the above-mentioned conferences; and received a best paper award from the German ESD Forum. Evan is a lifetime member of EOS/ESD Association, Inc. and is active in EOS/ESD Association, Inc. standards working groups on device testing. He has been recognized with the EOS/ESD Association, Inc.'s Joel P Weidendorf Memorial Award, the Outstanding Contributions award, and President's award. Evan taught college level electronics and computer programming and is an EOS/ESD Association, Inc. instructor for TLP.

Guitard, Nicolas

Nicolas Guitard received his PhD in microelectronics from the University of Toulouse, France, at LAAS/CNRS, in 2006. He studied the capability of low noise characterization to detect latent defects in IC's due to ESD stresses. From 2006 to 2009, he worked at NXP Semiconductors (in The Netherlands) as an ESD/LU engineer. In 2009, he joined STM in Crolles (France); where he developed ESD protection I/O libraries in most advanced CMOS technologies and drives qualification activities for both ESD and latch-up. He has also driven several R&D activities in the field of EOS (one PhD student) and advanced ESD concepts, leading to several international publications. In 2016, Nicolas joined the TCAD team at STM. He is now involved in device and

process simulations for CMOS & BiCMOS technologies to support STM technology developments.

Gupta, Sayak Dutta

Sayak Dutta Gupta was born in Kolkata, India. He received his bachelor's degree in electronics and communication engineering from Institute of Engineering and Management, Kolkata, under West Bengal University of Technology, India. He then completed a master's in materials engineering from Indian Institute of Engineering Science and Technology, Shibpur, India. He is currently a project assistant in the department of electronic systems engineering at Indian Institute of Science, Bangalore, India. His primary research interest is Group III-V based semiconductors especially Gallium Nitride based high electron mobility transistors.

Hajjar, Jean-Jacques

Jean-Jacques Hajjar is a senior staff engineer and the engineering manager of the global ESD organization at Analog Devices. Dr. Hajjar currently manages a corporate-wide team whose primary responsibility is the development and design of ESD device/circuit protection solutions across all process technology platforms. The charter of the ESD organization is ensuring that all products within all business units meet the minimum ESD and latch-up robustness requirements. Dr. Hajjar received a BSc and a PhD in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, in 1983 and 1989, respectively.

Hellings, Geert

Geert Hellings received a BS and MS in electrical engineering from the KU Leuven, Belgium, in 2007. He obtained a PhD from the electrical engineering department (ESAT), Integrated Systems Division (INSYS) of the KU Leuven, Belgium, and the CMOS technology department at imec, Belgium, in 2012. The main topic of his work was the integration of advanced field effect transistors with high-mobility channel materials and heterostructure confinement for digital logic applications. From 2008 to 2011, he received a PhD grant from the Institute for the promotion of innovation through science and technology in Flanders (IWT-Vlaanderen), Brussels, Belgium. In 2012, he joined the device reliability and electrical characterization group in imec, Belgium, researching electrostatic discharge events in integrated circuitry. He won the 2008 IEEE Region 8 student paper contest and received the 2011 imec Scientific Excellence Award. He holds several patents and has authored or co-authored approximately 100 technical papers for publication in journals and presentations at conferences.

Hogle, Nicholas

Nicholas Hogle graduated from Vermont Technical College in May 2007 with an associate’s in electrical engineering technology. He started working at IBM Microelectronics in October 2009 as a BEOL engineerig tech in technology reliability. He worked on wafer-level stress migration and deep thermal cycling and module-level electromigration in cutting-edge technologies. In 2013, he joined the IBM ESD and latch-up development group, which became the GLOBALFOUNDRIES’ global ESD/LU development group in July 2015. His main focus is wafer level ESD and latch-up testing on active technologies from GF Dresden, GF Malta, GF East Fishkill, and GF Burlington sites.

Hosseinbeig, Ahmad

Ahmad Hosseinbeig received a BS in electrical engineering from Shahid Bahonar University, Kerman, Iran, in 2006; and a MS and PhD in electrical engineering from K.N. Toosi University of Technology, Tehran, Iran, in 2008 and 2013, respectively. He was an assistant professor at Islamic Azad University-Science and Research Branch, Tehran, Iran, until 2016. He has been a visiting assistant research professor with the EMC Laboratory at Missouri University of Science and Technology, Rolla, MO, USA, since February 2016.

His current research interests include mathematical modeling and computational electromagnetics, numerical modeling and measurement techniques related to electrostatic discharge, and electromagnetic compatibility in electronic devices.

Hsu, Chia-Wei

Chia-Wei Hsu was born in Taipei, Taiwan in 1986. He received a BS from the department of engineering and system science from National Tsing Hua University, Hsin Chu, Taiwan, in 2008; and a MS from the department of electronics engineering, National Chiao Tung University, Hsin Chu, Taiwan, in 2010. He joined Taiwan Semiconductor Manufacturing Company Ltd (TSMC) in 2010. He is presently with the EOS/ESD technology programs. His researches focus on the development and design of ESD protection technology for advanced semiconductor process.

Hua, Runbing

Runbing Hua is persuing her bachelor's in electrical engineering from Missouri University of Science and Technology, Rolla, MO, USA. Her estimated graduation date is May 2019. She is currently working as an undergraduate research assistant at the EMC Laboratory, Missouri University of Science and Technology, Rolla, MO, USA. Her research interests include ESD testing and circuit design.

Huang, Chien-Yao

Chien-Yao Huang received a BS in electronics engineering from National Chiao-Tung University, Taiwan, in 2008, and a MS in photonics and optoelectronics from National Taiwan University, Taiwan, in 2010. In 2011, he joined the new business unit in Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) and led successful R&D projects that set world records in thin-film photovoltaic. In 2015, he joined the EOS/ESD technology department in TSMC and currently focuses on ESD/latch-up R&D in advanced CMOS nodes. His research interests include ESD/latch-up, TCAD modeling, solar cell, and sensors.

Iben, Icko Eric Timothy

Icko Eric Timothy Iben is a senior engineer in IBM's tape head development group within the storage division. He earned his bachelor's in physics from the University of California, Berkeley, and his PhD in physics from the University of Illinois at Champaign-Urbana. Prior to working for IBM, Dr. Iben worked at AT&T Bell Labs and New York University doing biophysics research. He then worked for General Electric Research and Development in the areas of environmental remediation, medical instrumentation, and material characterization. He has been with IBM since 1997, performing work on the reliability and ESD testing and lately design of read/write heads used in magnetic tape storage drives. In 2008, he was awarded the best paper award of the EOS/ESD Symposium. He has authored 41 journal and symposium papers, has 68 granted and numerous pending patents, and is an IBM master inventor.

Jain, Ruchil

Ruchil Jain received a BE in electronics and telecommunication from National Institute of Technology, Raipur, India, in 2006; and a MT in microelectronics from the department of electrical engineering at Indian Institute of Technology (IIT), Bombay, Mumbai, India, in 2009. He worked as a research scholar for nanoelectronics research projects at Universita della Calabria, Italy, under the IITB-UniCal joint research program from September 2009 to July 2010. Since 2010 he has worked as Singapore-site TCAD team leader, in design enablement department at GLOBALFOUNDRIES Singapore Pvt. Ltd., Singapore.

Johnson, Craig

Craig Johnson received a BSEE from the University of Arizona. In 1991, he worked as device engineer at Burr-Brown in Tucson, AZ. He joined Motorola Semiconductor's products sector in 1992; where he

worked as device engineer for MOS2/3, then as modeling engineer, and eventually verification engineer. In 2004, Motorola Semiconductor became Freescale, and Craig wrote software for layout verification and dealing with difficult issues that require unique solutions. Craig worked with the verification group to develop technology independent MRC infrastructure that supports DRC/PERC/PERC-LDL checks.

Jokinen, Vesa

Vesa Jokinen is responsible for the product development and testing at Sievin Jalkine Ltd. Sievin Jalkine Ltd. is Northern Europe's largest footwear manufacturer, an international family-owned company founded in 1951. The company currently employs approximately 530 people, counting home country and abroad. The production facilities are located in Finland. Vesa Jokinen joined the company in 1978. With work experience and shoe specialist training received in the United Kingdom, Vesa is well acquainted with the different work stages that shoe manufacturing requires. Vesa Jokinen is also a member of the TEVASTA Association; which will introduce the Finnish aspect into development of EN ISO standards concerning safety shoes. He has more than 30 years of experience in the development of footwear for electrostatic control.

Kärjä, Eira

Eira Kärjä works as a marketing director at Premix Oy. She is also in charge of the sales of Premix's electrically conductive plastics in Finland and Central Eastern Europe. Eira joined Premix's sales team in 1999 after receiving her MS in industrial engineering and management from Tampere University of Technology.

Kaschani, Karim T.

Karim T. Kaschani received his diploma in electrical engineering from Technical University in Brunswick in 1990. For his research in the field of semiconductor power devices he received his PhD in electrical engineering from Technical University in Brunswick in 1996. In the same year he joined Siemens Semiconductors, which is now Infineon Technologies. From 1996 through 1999, he worked as a development engineer and project leader in the field of advanced ICs for switch-mode power supplies. From 2000 through 2003, he focused on the concept engineering of high voltage SOI technologies and on the development of high voltage ICs. In 2004, he joined Atmel Germany; where he became head of the ESD test and consulting group. In 2008, he was promoted to manager of product quality engineering. As such he was heading the reliability lab, the ESD lab, and the failure analysis lab of Atmel Automotive. In 2010, he joined Texas Instruments in Germany as a senior ESD engineer. He is currently responsible for the regional ESD and EOS support in Europe. He holds 12 patents with several pending and is author or co-author of 24 papers and conference presentations and 3 tutorials in the fields of semiconductor power devices, ICs, semiconductor technologies, ESD, and EOS.

Keppens, Bart

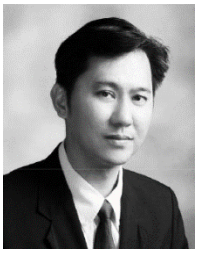
Bart Keppens received an engineer degree in electronics from the Technical University Groep T, Leuven, in 1996. His master's thesis, together with his colleague Steven Servaes, "Transmission Line Pulsing (TLP) Technique for Analysing ESD reliability", performed at imec, Leuven, Belgium, received the BARCO-award for best industrial engineer thesis. In 1996, Bart joined imec and was responsible for device electrical characterization, support for the ESD group, and for the non-volatile memories group for layout and testing. In May 2002, he joined Sarnoff Europe, Belgium, solving ESD related problems for customers worldwide, first as ESD engineer, later as technical leader and ESD design specialist. In 2006, Bart supported the business development initiatives as technical director for ESD. After a management buy-out in June 2009, Sarnoff Europe became SOFICS – 'Solutions for ICs'; where Bart is director of technical marketing, working with semiconductor companies worldwide. Bart has authored and

coauthored 25 peer-reviewed published articles in the field of on-chip ESD protection and testing, and non-volatile memories. Invited papers on ESD solutions and TLP analysis techniques have been delivered at the RCJ ESD Symposium in Japan in 2006, 2007, 2008, and 2009. He is a member of Sofics' confidential and proprietary 2017, the technical program committee for EOS/ESD Symposia (since 2003), and a member of the ESREF technical program committee in 2003, 2005, 2007, 2009, and 2010. Bart has participated as a workshop panelist on ESD topics during various conferences (EOS/ESD Symposium and RCJ) and presented an invited tutorial at the Taiwan ESD Conference in 2008. Bart holds several on-chip ESD protection design patents.

Koch, Sebastian

Sebastian Koch received a BSc in engineering physics in 2010 and a MSc in applied and engineering physics in 2012 from Technische Universität München, Munich, Germany. From 2013 to 2016, he worked as a PhD student with Intel Deutschland GmbH and he is currently finishing his dissertation with the University of the Armed Forces in Neubiberg, Germany. In 2017, Sebastian joined Infineon Technologies AG. His research interests include the robustness of high-speed interfaces regarding electrostatic discharge and electromagnetic interference.

Koh, Marcus



Dr. Marcus Koh is an EOS/ESD Association, Inc. certified ESD professional program manager; and an iNARTE certified ESD engineer. He was an instructor, technical session speaker, publicity chair, and co-sponsor for various EOS/ESD Association, Inc. EOS/ESD Manufacturing Symposia in Singapore and Malaysia between 2012 and 2017. He has numerous technical publications in conferences, transactions, journals and symposia. He has been proactive in supporting EOS/ESD matters in electronics assembly and manufacturing industries across Asia Pacific. His workshops are closely associated with ANSI/ESD S20.20 and IEC 61340-5-1 standards and best practices; and he is instrumental in guiding ESD practitioners in the region, leading them toward iNARTE ESD control certification. Marcus studied at the Nanyang Technological University, graduating with a BE (first class honors) and a PhD. There, he was awarded the PUB book prize for outstanding performance in the subject "power electronics and drives". Subsequently, he was on the Dean's List, and ranked as among the best in his graduating class. Marcus' current research area is in adult continuing education and learning, energy management, system reliability, and solving stochastic problems using statistical modelling.

Korpipää, Ari

Ari Korpipää graduated from Finnish Airforce Airplane technical school in 1977 and from the technical school in Tampere in 1981. He started his work and studies related to ESD in 1986. He wrote ESD training books between 1989 and 1991. Ari has attended several EOS/ESD Association, Inc. tutorials at multiple EOS/ESD Symposia. He started his career with ESD in 1989 at ARMEKA Engineering Ltd. first providing training in Finnish Air Force, and later in other sectors of defense forces. He started international audits and training in collaboration with Nokia in 1994. He was contracted with Nokia Mobile Phones in many different countries. In recent years, Ari has worked as an ESD control specialist, mainly in China, Russia, and India. He has developed an ESD STB epoxy flooring that is famous in electronics and automotive industry all over the world. Ari is a member of the Finnish standardization committee SK101 and IEC PT 61340-6-1. He is also a member of the Finnish STAHA Association.

Kranthi, N.K.

Kranthi received an M.Tech from the National Institute of Technology Calicut, Kerala, India, in 2014. He is currently pursuing a PhD with Mayank Shrivastava in the nano device lab (MSDLab) of the department of ESE at Indian Institute of Science, Bangalore, India. He was with STMicroelectronics, Noida, India, as a graduate trainee from 2013 to 2014; where he was involved in ESD related issues in 28 nm FDSOI technology.

Kraz, Vladimir

Vladimir Kraz is a founder and president of OnFILTER, a California-based manufacturer of innovative EMI filters. During his engineering career, he has designed state-of-the art equipment for wireless and wired communication, medical, industrial control, and other industries, and for ESD, EMI, and EMC applications. Prior to OnFILTER, he was a founder and president of Credence Technologies, a leading manufacturer of ESD/EMI instrumentation; which later became a part of 3M. Vladimir holds 23 U.S. patents with more patents pending; is an author of numerous articles for technical publications, papers at EOS/ESD Symposia, and other forums both in the U.S. and abroad; and has taught classes and conducted seminars on the subjects of ESD, EMI, and EMC around the world. Mr. Kraz is a member of several technical associations, including EOS/ESD Association, Inc., IEEE, and SEMI. He is a co-chair of SEMI's EMC task force and of SEMI's standards metrics committee. Vladimir is a member of EOS/ESD Association, Inc. standards working groups, and a contributor to ITRS/IRDS.

Kumar, B. Sampath

B. Sampath Kumar was born in Telangana, India. He received a MTech from VNIT Nagpur, India, in 2013. He is currently pursuing his PhD in electronic engineering and is with the advanced nano-electronic devices and circuits research group, Indian Institute of Science, Bangalore, India. His research interests include device and circuit co-design and co-optimization for ESD and long term reliability of high voltage devices for planar and FinFET CMOS technologies. Sampath was a recipient of honorable mention at the VLSID International Conference in 2017.

Lai, Da-Wei

Da-Wei Lai received his MSc in electronics engineering from National Chiao Tung University Taiwan in 2003. After he received his MSc, he worked at TSMC on I/O library design with a focus on general/customized I/O design and the corresponding ESD/LU design from 0.18 µm to 40 nm technology. In 2013, he joined NXP Semiconductors, The Netherlands. He works on the high voltage ESD design for security/automotive products. He has published several patents on ESD.

Laine, Jean-Philippe

Jean-Philippe Laine received his electrical engineering degree in 2000 and his PhD in 2003 from National Institute of Applied Sciences respectively at Lyon and Toulouse (France). Since 2004, he has been an ESD specialist to support display drivers products in 0.35 µm BiCMOS technology for Philips Semiconductors (now NXP) at Zurich (Switzerland). In 2005, he joined the I/O and ESD group at Crolles (France) for partner companies (STMicrolectronics, NXP, and Freescale). He participated in I/O library development for 65 nm and 45 nm CMOS technology platform. After Crolles2 alliance R&D program, he joined the automotive analog design center in 2007 at Toulouse (France) for NXP Semiconductors. He is now involved in ESD protection devices for automotive system level applications with analog ESD/EMC team. He is acting as ESD designer for ESD protection design, layout, simulation, characterization, and for training to analog designers.

Lam, Michelle (Ho-Yiu)
Michelle (Ho-Yiu) Lam is a senior engineer in IBM System, Supply Chain Engineering in Tape Storage. She has been with IBM for over 15 years overseeing a failure analysis laboratory and conducting characterization work in magnetic recording. She is responsible for ESD control in IBM world-wide manufacturing sites. In recent years, Michelle devoted most of her time to understanding the rapidly evolving digital world, seeking opportunities to apply artificial intelligence, big data analytics, and Internet of things to her area of expertise, hoping to assist in accelerating this vital industry transformation to a new cognitive era. Michelle holds a master's in materials science and engineering from Stanford University. She has been a member of EOS/ESD Association, Inc. since 2005 and is a certified ESD professional program manager.

Lee, Jam-Wem
Jam-Wem Lee received his BS and PhD in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1996 and 2002, respectively. During this period, he devoted his efforts on improving the reliability and scalability of nanoscaled thin dielectric films. From 2001 to 2002, he was with United Microelectronics Corporation, Taiwan, as an engineer working on the electrostatic discharge (ESD) circuit design. Since 2007, he has been with the Taiwan Semiconductor Manufacturing Company, Hsinchu, as a manager.

Lee, Jian-Hsing
Jian-Hsing Lee joined TSMC in 1989 and served as the TSMC academician for contributions to ESD, and latch-up; and in 2005, NVM in CMOS technologies. In 2013, he joined GLOBALFOUNDRIES as PMTS of ESD/latch-up engineering. He has published 62 technical papers in international conferences and journals; and has been granted 203 US patents.

Lee, Jongsung
Jongsung Lee received a BS and MS in electrical engineering from the University of California Irvine, Irvine, in 2002 and 2004, respectively. Since 2004, he has been with Samsung Electronics, Suwon, Korea. His current research interests include signal integrity, electrostatic discharge, and electromagnetic compatibility in both measurement and simulation.

Legenzoff, Zach
Zach Legenzoff received a BS in electrical engineering from the University of Missouri-Columbia in 2014. Since 2014, he has been with Honeywell. He is currently pursuing a MS from Missouri University of Science and Technology with emphasis in electromagnetic compatibility through a Honeywell fellowship program.

Lemke, Chris
Chris Lemke has a BS in technology management from the State University of New York (SUNY), Empire State Campus. Currently he is an active member of the Trek, Inc. sales team; where he provides technical and application assistance to customers. Since 1993, Chris has been affiliated with various sectors of the semiconductor / thin films industry, such as ENI Power Systems and Balzers, Inc. Chris also served in the USAF as an avionics technician, repairing RF communication and navigation equipment. In addition to his EOS/ESD Association, Inc. membership, he is presently a member of the American Vacuum Society and the Electrostatics Society of America. He presently holds an FCC general radio telephone license.

Leveugle, Claire
Claire Leveugle received a degree in microelectronics from ISEN, Lille, France, and a PhD in microelectronics on gate oxide quality from University College Cork, Ireland. She started at Analog Devices, Inc. in 2000; leading the parametric team in the process and fabrication group. After a diploma in project management, she

managed the process transfer group moving critical processes from and to different fabrication sites. She joined the EMC group at Analog Devices, Inc. in 2014; where she is currently focusing on EMC/ESD system simulation.

Levit, Lawrence

Dr. Levit is the owner of LBL Scientific, a consulting firm with expertise in ESD control, nuclear physics, and pulsed power. He is an iNARTE certified ESD engineer and a senior member of the IEST. He has provided ESD consulting to many leading semiconductor, disk drive, and flat panel corporations worldwide. Previously, he was chief scientist for Ion Systems, Inc.; where he was responsible for planning technology implementation for Ion Systems products in cleanrooms and was also responsible for the technical direction of the Ion Systems electrostatic management consulting practice. Before joining Ion Systems, Levit held technical rolls at LeCroy Corporation and Jandel Scientific Software. At LeCroy, he contributed to the instrumentation designs for six experiments which produced Nobel prizes in physics and participated in the development of high speed waveform capturing transient recorders and oscilloscopes. Levit also taught physics and conducted research in high energy and cosmic ray physics. Levit graduated from Case Institute of Technology, Cleveland, Ohio, with a BS in physics with honors. In 1970, he earned a PhD in experimental high energy physics from Case Western Reserve University.

Li, Darwin

Darwin Z. Li received his dual bachelor's degree in physics and public health from the University of California, Berkeley, in 2013. He has three years of experience as an engineer for Dassault Systemés and is working towards his master's degree in electrical engineering at EMC Laboratory, Missouri University of Science and Technology. His research interests include computational electromagnetics, biological models, and non-contact ESD.

Li, Guan

Li Guan received an AA in international business from Liaoning Normal University, Dalian, China, in 2014. She is currently a senior undergraduate student in the electrical and computer engineering department at Missouri University of Science and Technology, Rolla, MO. She has been working as an undergraduate research assistant in the electromagnetic compatibility laboratory (EMC Lab) on several electrostatic discharging projects since 2015.

Li, You

You Li received his BS from the University of Electronic Science and Technology of China, Chengdu, China, in 2003; and a MS and PhD from the University of Central Florida, Orlando, FL, in 2007 and 2010, respectively; all in electrical engineering. His PhD research work focused on the design of low-capacitance and high-speed electrostatic discharge (ESD) devices for low-voltage protection applications. From 2010 to 2012, he worked at Infineon Technologies North America as an application engineer responsible for the system-level ESD protection products. In 2012, he joined IBM as an advisory engineer in the semiconductor research and development center (SRDC), where he worked on the ESD device and model development in 22 nm and 14 nm SOI technologies. He joined GLOBALFOUNDRIES in 2015 and is currently working on ESD device design in several leading-edge CMOS Bulk/SOI technologies. He has authored/co-authored several papers at EOS/ESD Symposia.

Lin, Wun-Jie

Wun-Jie Lin received a MS in electronics engineering from the EE department at National Tsing-Hua University, Taiwan, in 2010. His research interests include semiconductor devices and embedded non-volatile memory devices, with current emphasis on ESD devices and IO/ESD network design. He has been with the ESD/EOS technology department in TSMC, as an engineer since April 2010.

Linten, Dimitri

Dimitri Linten received a PhD in electrical engineering from the Vrije Universiteit Brussel (VUB), Brussels, Belgium, in 2006. In 2001, he joined the wireless research group of imec in Leuven, Belgium. In 2006, he joined the ESD reliability group at imec as a post-doctoral research fellow. In 2012, he became the ESD team leader at imec. He is a senior member of the IEEE (SM13). His main research interests are on-wafer ESD testers, ESD reliable RF and high speed IO circuit design, and ESD reliability for sub-14 nm FinFET CMOS technologies. He has authored or co-authored more than 100 publications and patents in these fields.

Liu, Jian

Jian Liu received a BS from Nanjing University, China, in 2005; a MS from Tsinghua University, China, in 2008; and a PhD from the University of California, Riverside, CA, in 2012; all in electrical engineering. Throughout his graduate studies, he completed several internships focusing on ESD protection design at both IC foundries and IC design houses, including SMIC (Shanghai, China), GSMC (Shanghai, China), RFMD (Greensboro, NC), and Analogix (Beijing, China). In 2011, Dr. Liu joined the ESD group of RF Micro Devices (RFMD, now Qorvo), where he is working as a senior device engineer on the CMOS ESD protection design. Dr. Liu is an IEEE peer reviewer and has published over 40 technical papers in the conferences and journals. He has been a member of EOS/ESD Association, Inc. since 2012.

Luo, Sirui

Sirui Luo received a BS in microelectronics in Chongqing University of Post and Communications in 2010. He received a MS and a PhD in electrical engineering from the University of Central Florida, Orlando, in 2012 and 2015, respectively. In 2015, he joined Analog Devices, Inc. as a quality engineer in Wilmington. His current focus is on enabling the ESD capability from Bi-CMOS to submicron CMOS process; and developing solutions for high ESD risk product within the company. This includes custom ESD development for RF application, high voltage process, and any non-standard requirement, etc. He is also actively engaged with the design community for design review and simulations to insure the proper ESD strategy before tapeout as well as the ESD failure reproduction for customer return failure analysis.

Marathe, Shubhankar

Shubhankar Marathe received a BE in electronics and telecommunication from the University of Mumbai, Mumbai, Maharashtra, India, in 2013, and a MS degree in electrical engineering from EMC Laboratory, Missouri University of Science and Technology, Rolla, Missouri, USA, in 2017. He is currently working toward a PhD in electrical engineering at EMC Laboratory, Missouri University of Science and Technology, Rolla, Missouri, USA. His research interests include near-field scanning, near-field probe development, electrostatic discharge, EMC measurements, and signal integrity.

Marichal, Olivier

Olivier Marichal received his MSc in electro-technical engineering from the University of Leuven, Belgium, in 2003. He first worked as an ESD protection engineer at Sarnoff Europe, now SOFICS, and was involved in many different ESD projects. Currently, Olivier leads the development and commercialization of TakeCharge®, an intellectual property portfolio of on-chip ESD protection design solutions, silicon proven down to 16 nm today; and PowerQubic™, a set of ESD solutions specifically developed for HV applications. Olivier is responsible for an expert team of 10 ESD engineers. Olivier has authored and coauthored several published articles and patents in the field of on-chip ESD protection.

Maurer, Linus

Linus Maurer (SM, 14) received the diploma engineer degree in physics and his dr. technical degree from Johannes Kepler University, Linz, Austria, in 1997 and 2001, respectively. In 2002, professor Maurer joined DICE, an Infineon Technologies design center dedicated to the development of cellular RF-transceivers and ICs for automotive radar applications. Between 2007 and 2012, he was site-manager for the sense and control division of DICE, overlooking the automotive radar development activities. Since August 2012, professor Maurer has been the professor for electronic components and integrated circuits at the University of the Armed Forces in Neubiberg, Germany. He was IEEE distinguished microwave lecturer from 2007 to 2009, received the MTT-S outstanding young engineer award in 2010, received the ITG-F orderpreis in 2002, and the EEEfCOM-price in 2006. His main research interests are focused on wireless communication and mm-wave radar systems. He has authored and co-authored over 120 publications in these fields and has given numerous international presentations and tutorials.

Meeks, Terry

Terry Meeks is a Calibre product specialist in the North American sales organization at Mentor Graphics in San Diego, CA. He has responsibility for working directly with customers to utilize and enhance the Calibre tools, and insure customer success. Terry previously worked at Avanti (ISS) and Calma. He has over 40 years of experience in the industry. He holds an MS and a BS in computer science from California State University Fullerton.

Merlo, Luca

Luca Merlo graduated in physics from Bicocca University of Milano in 2012; discussing a thesis on nano-scaled materials and devices for non-volatile memories following work on PCM in LAB MDM IMM CNR. He is working for STMicroelectronics as a failure analysis engineer, first for the APG micro & digital group and later for the APG BCD-RF group. Since 2016, he has been involved in developing and characterizing ESD protection architectures for smart power BCD technologies with the qualification of ESD design solutions engineer. He authored and presented a paper on FA at the ESREF Symposium in 2014.

Mertens, Robert

Robert Mertens received a BS in electrical engineering and computer science from the Missouri University of Science and Technology, Rolla, MO, USA, in 2010, and a MS and PhD in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2015. He is currently with NXP Semiconductors, Austin, TX, USA; where he is involved in circuit design.

Mitchell, Todd

Todd Mitchell is currently a principle engineer at Maxim Integrated. His current area of responsibility is supporting ESD and latch-up verification tools as well as ESD IP development. Prior to joining Maxim Integrated in 2003, Todd worked for VLSI Technology and Motorola. Todd has over 37 year of semiconductor industry experience in the areas of process engineering, product engineering, test engineering, and ESD/latch-up design. He has co-authored several papers on wafer process development and yield enhancement. Todd has a BS in physics from the University of Arizona.

Natarajan, Mahadeva Iyer

Mahadeva Iyer Natarajan received his PhD from the University of Kerala, India. Prior to joining GLOBALFOUNDRIES, he worked at IME, Singapore (1994-2000); imec, Belgium (2000-2006), and Silterra, Malaysia (2006-2007). Currently, he is leading the North American 300 mm reliability engineering department and corporate ESD and latch-up engineering team, in Malta, NY. He is a senior member of IEEE and member of EOS/ESD Association, Inc. He has

published 78 papers and has over 40 patents that have been granted or are pending.

Niemesheim, Josef

In 1985, Josef Niemesheim joined the semiconductor division of Siemens; which became Infineon Technology in 1999. He was responsible for production and service of fab equipment. In 1999, he became involved in life tests for wireless products in the quality management group. Since 2002, he has worked on ESD/latch-up testing, first within the central library department of Infineon and then within Intel Mobile Communications in 2011. Special focus is the development, set-up, and improvement of ESD and latch-up test equipment.

Ozawa, Tadashi

Tadashi Ozawa received MS in physics from Waseda University, Tokyo, Japan, in 2000. From 2000 to 2009, he was an IP design engineer at Kawasaki Microelectronics. From 2009 to 2015, Tadashi was engaged in ESD at Kawasaki Microelectronics (which merged into MegaChips in 2013). Since 2015, he has managed the group handling general purpose libraries (core, memory, IO and ESD) at MegaChips.

Pamidimukkala, Keerthana

Keerthana Pamidimukkala is a graduate student at Missouri University of Science and Technology pursuing her master's degree in electrical engineering. She received her undergraduate degree in electronics and communication engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2015. During her undergraduate work she briefly worked with Research Centre Imarat, a division of Defense Research and Development Organization of India. She is currently working as an intern at Apple Inc., Cupertino, CA, in the EMC design engineering group.

Pandey, Shesh Mani

Shesh Mani Pandey received his MTech degree in solid state material in 1995 from Indian Institute of Technology Delhi, India. From December 1995 to October 1999, he worked at Semiconductor Complex Ltd. in Chandigrah, India, as a technology development engineer. He joined Chartered Semiconductor Manufacturing (presently GLOBALFOUNDRIES), Singapore, in December 1999. Since then he had been involved in development of different technologies ranging from 0.25 um CMOS to state of the art 7 nm. Presently he is TCAD manager for 14 nm / 7 nm programs in GLOBALFOUNDRIES, Malta, USA.

Parthasarathy, Srivatsan

Srivatsan Parthasarathy is a staff engineer with the corporate ESD department at Analog Devices, Inc. Srivatsan received his MS in electrical engineering from the North Carolina State University (NCSU). At Analog Devices he designs and develops ESD protection solutions for RF and microwave integrated circuits.

Patnaik, Abhishek

Abhishek Patnaik received a BE in electrical engineering from the Institute of Technical Education and Research, India, in 2010; and a MS in electrical engineering from EMC Laboratory, Missouri University of Science and Technology, Rolla, MO, USA, in 2015. He is currently working towards his PhD in electrical engineering at EMC Laboratory, Missouri University of Science and Technology, Rolla, MO, USA. His research interests include On-Chip ESD design, RF circuit design, EMC testing, grounding, and shielding techniques to improve electromagnetic compatibility.

Paul, Milova

Milova Paul was born in Delhi, India. She received an MTech from Delhi Technological University, India, in 2014. She is currently pursuing her PhD in electronic engineering and is with the advanced nano-electronic devices and circuits research group,

Indian Institute of Science, Bangalore, India. Her research interests include ESD exploration of advanced CMOS and FinFET technologies. Milova was a recipient of honorable mention at the VLSID International Conference in 2017. She has submitted several patents in the field of ESD in FinFET technology.

Peachey, Nathaniel

Nathaniel Peachey received his PhD in physical chemistry in 1994 from the University of Nebraska–Lincoln and then was awarded a director's funded postdoctoral fellowship at the Los Alamos National Laboratory; where he studied thin-film membranes for gas separation. In 1996, he joined Atmel Corporation in Colorado Springs as a thin-films process engineer. Over the next several years Dr. Peachey held various positions at Atmel including process engineer, technology development engineer, device engineer, and circuit design engineer. In 2003, he began focusing exclusively on ESD protection and I/O design issues. In 2005, Dr. Peachey accepted the position of engineering manager for the newly formed ESD design group at RF Micro Devices (currently Qorvo, Inc.). In this capacity, he was responsible for the development of ESD protection for all the technologies that Qorvo designed including both silicon and GaAs. Besides on-chip protection he led the development and improvement of the RF antenna ESD protection. Dr. Peachey has authored and coauthored over 30 technical journal submissions. He has also submitted 14 patents that have either been granted or are pending. Dr. Peachey is also a senior member of the IEEE. In 2009, Dr. Peachey was elected to the board of directors for EOS/ESD Association, Inc. He has been involved in various activities within EOS/ESD Association, Inc. Currently, he is serving as the Standards Business Unit Manager.

Peng, Po-Lin

Po-Lin Peng received a BS in electrical engineering and computer science from National Chiao-Tung University, Hsinchu, Taiwan, in 2012; and a MS from the Institute of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 2014. He joined Taiwan Semiconductor Manufacturing Company (TSMC) in 2015 and is in charge of the ESD/LUP design.

Pommerenke, David

David Pommerenke received a Diploma degree in 1996 and a PhD in electrical engineering from the Technical University Berlin, Berlin, Germany, in 1996. After working at Hewlett Packard for five years, he joined the electromagnetic compatibility laboratory at Missouri University of Science and Technology, Rolla, MO, USA, in 2001; where he is currently a professor. He has authored or coauthored more than 200 papers, a co-owner of a start-up company on EMC scanning, and has 13 patents. His research interests include system-level ESD, electronics, numerical simulations, EMC measurement methods, and instrumentation. Dr. Pommerenke is an associated editor for the IEEE *Transactions on EMC*.

Poro, Richard

Richard A. Poro joined the IBM microelectronics division in 2012 working on ESD testing, test software development, and tester hardware improvements. He received his BS in electrical engineering technology from Vermont Technical College in 2014. In July 2015, Richard transitioned to GLOBALFOUNDRIES working in the ESD/latch-up development group. Currently, he is working on ESD and latch-up tester development, and designing and characterizing latch-up test structures.

Prabhu, Manjunatha

Manjunatha Prabhu received a MS in microelectronics from BITS PILANI in 2010; and a BE in electronics and communications from National Institute of Technology Karnataka in 2003.

He joined GLOBALFOUNDRIES in 2010; where he worked on ESD protection design and device design for advance nodes. Prior to GLOBALFOUNDRIES, he worked as an I/O design engineer at ARM, Inc., Sarnoff, and STMicroelectronics. He holds eight patents, and has twelve more patents pending. He has authored or co-authored five peer-reviewed research papers.

Raghavan, Srinivasan

Srinivasan (Vasu) Raghavan obtained his BE and ME in metallurgy from the Visvesvaraya Regional Engineering College (Now VNIT) in Nagpur, and the Indian Institute of Science in Bangalore, respectively. Following his ME, he obtained his PhD in materials science and engineering from Pennsylvania State University. Presently, he is an associate professor at Centre for Nanoscience and Engineering, Indian Institute of Science, Bangalore. His research interest includes growth of group III-A (In, Ga, Al) nitride compound semiconductors.

Rajagopal, Krishna

Krishna Praveen Mysore Rajagopal completed his BE in electronics and communication from Visvesvaraya Technological University, India, and a MS in electrical engineering from San Jose State University, USA. He joined National Semiconductor Corporation in 2010 and subsequently Texas Instruments in 2011. He has been involved in ESD IP and technology development in various high voltage BCD technologies. He has published several technical papers and has filed many patents in the ESD field.

Rataj, Michael

Mr. Rataj has a BS in biology and psychology from the University of Illinois as well as an MS in biology from the University of Illinois with an MBA in operations management from Illinois Institute of Technology. He gained 10 years of experience in the fields of pharmaceutical manufacturing and R&D with Abbott Labs and the Amoco Technology Company. He has 21 years of experience in the contamination control industry with Aramark as director of quality assurance and with the IEST as a past president, and working group chairman for RP CC 3.4 - Garment Considerations for Cleanrooms and Other Controlled Environments, RP CC 23.2 - Microorganisms in Cleanroom, and RP CC 48 - Guidance for the design, testing and maintenance of Sterile compounding facilities per USP 797.

Reiman, Collin

Collin Reiman received a BS in electrical engineering and a BS in physics from Lehigh University in 2014. He is currently working towards a PhD in electrical engineering from the University of Illinois at Urbana-Champaign. His research interests include the modeling of system-level ESD, the development of high-speed, self-protecting I/O circuitry, and noise-monitoring circuits.

Reinprecht, Wolfgang

Wolfgang Reinprecht is principal engineer of ESD/EOS at amsAG ((austriamicrosystems) and responsible for development of ESD protection circuits, libraries, and rules in 0.35 and 0.18 um HV technologies. He supports design engineers to ensure ESD, over voltage, and latch up robust products. He finished his education in communication engineering and electronics 1985 in Graz. From 1986 to 1996, he worked for amsAG as design and layout engineer and was responsible for analogue IP block development. In 1997 he founded Mikro-Elektronik Design Service GmbH and led the development of IP-blocks, libraries, ESD protections, and check tools for various technologies. In 2006, he joined the ESD/EMC group at amsAG. Since 2010, he has participated in standardization meetings and working groups related to ESD, EOS, and latch-up topics.

Rezaei, Hossein

Hossein Rezaei received his master's degree in electrical engineering from Shiraz University of Technology, Shiraz, Iran, in September 2011. He joined the EMC Laboratory at Missouri University of Science and Technology in 2016 as a graduate

research assistant. He is currently pursuing his PhD in the EMC lab under the supervision of Dr. Pommerenke. His interest is in ESD, EMI, SI, PI, and system-level ESD design.

Rosenbaum, Elyse

Elyse Rosenbaum received a BS (with distinction) from Cornell University in 1984, a MS from Stanford University in 1985, and a PhD from the University of California, Berkeley, in 1992. All of these degrees were in electrical engineering. From 1984 through 1987, she was a member of technical staff at AT&T Bell Laboratories in Holmdel, NJ. She is currently a professor in the department of electrical and computer engineering at the University of Illinois at Urbana-Champaign. Dr. Rosenbaum's present research interests include design, testing, modeling, and simulation of on-chip ESD protection circuits, system-level ESD reliability, latch-up, design of high-speed I/O circuits, and charged device model ESD (CDM). She has authored or co-authored well over 100 technical papers. She has presented tutorials on reliability physics at the International Reliability Physics Symposium, the EOS/ESD Symposium, and the RFIC Symposium. She was the keynote lecturer at the 2004 Taiwan ESD Conference, and has given invited lectures at many universities and industrial laboratories. From 2001 through 2011, she was an editor for IEEE *Transactions on Device and Materials Reliability*. She is currently an editor for IEEE *Transactions on Electron Devices*. Dr. Rosenbaum was the technical program chair for the 2016 International Reliability Physics Symposium. Dr. Rosenbaum has been a visiting professor at Katholieke Universiteit in Leuven, Belgium, and National Chiao-Tung University in Hsinchu, Taiwan. She has been the recipient of a best student paper award from the IEDM, an outstanding paper award from the EOS/ESD Symposium, a technical excellence award from the SRC, an NSF CAREER award, an IBM faculty award, and a UIUC Bliss faculty scholar award. She is a fellow of the IEEE.

Rupp, Andreas

Andreas Rupp studied physics at Technische Universität München (TUM) in Germany. In 1997, he received his degree in physics (Dipl. Phys.). In 1998, he joined Hitachi Semiconductor in Landshut; where he was responsible for etching process and process integration. Finally, he worked in the design department for foundry business. In 2011, he changed to Infineon Technology in Munich and is responsible for ESD development in high integration smart power technologies.

Russ, Christina C.

Christian Russ received a MS and PhD in electrical engineering from the Technical University of Munich, Germany, in 1991 and 1999, respectively. He has spent over 20 years in the field of ESD: from 1994 through 1998 he was with imec, Leuven, Belgium; and from 1998 through 2003, he worked for Sarnoff Corporation, Princeton, New Jersey, USA. In 2003, he joined Infineon Technologies, Munich, Germany. In 2011, he transferred to Intel Mobile Communications where he developed ESD concepts for planar and FinFET CMOS technologies (28 nm, 14 nm, and below). Since spring 2017, he has been at Infineon Technologies as principal engineer for ESD solutions in automotive sensor technologies. Christian was recipient of several best paper awards at EOS/ESD Symposia (1993, 1996, 1998, 2000, 2001, 2005, and 2012) and at the ESREF Conference (1993 and 1995). He has published over 75 conference and journal publications and has been awarded over 70 patents in his field.

Salcedo, Javier

Javier Salcedo is a technology development engineer manager at Analog Devices, working on technology development for interface circuits and quality management systems. Javier received a MS and PhD in electrical engineering from University of Central Florida College of Engineering and Computer Science and the executive MBA from Boston University Questrom School of Business.

Salles, Alain

Alain Salles received his engineering degree in electronics in 2003 from National Polytechnic Institute (ENSEEIHT) and his master's from Paul Sabatier University at Toulouse (France). Then, he received a PhD in micro-electronics in 2008 from the Paul Sabatier University at Toulouse. During his PhD thesis, he worked at LAAS-CNRS Laboratory on the integration of inductors dedicated to the low power DC/DC conversion applications. In 2008, he joined the analog and mixed power division of Freescale Semiconductor at Toulouse; where he is in charge of ESD structures characterization for automotive applications. He is involved in ESD GUN and TLP measurements for all automotive products as well as the test bench development and standards deployment in collaboration with the analog design group.

Salzone, Gabriele

Gabriele Salzone received a master's in electronic engineering from the Engineering School Polytechnic in Milan, with specialization in nanotechnologies, in November 2009. From April 2009 to October 2009 he worked in an innovative project titled "Creation of a Smart Meter for Remote Control of the Consumption of Water Pipes in a Building"; in which the main activity was the programming of a microcontroller microchip family 18fxx 64-pin. Additionally, he worked on the proportion of command (power electronic) to force current output to a solenoid. In May 2010, he joined STMicroelectronics in the physical design kit group; which is the technology research & development department inside the central CAD and design solutions. Since January 2015, he has mainly worked on layout physical verification (DRC/LVS), development of DK (design kits) in smart power BCD processes, and primarily provided support and development of new verification tools for important customers of STMicroelectronics. He is implementing automated ESD checks with Mentor PERC.

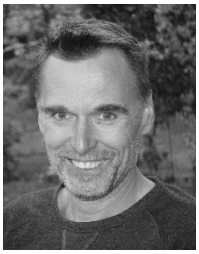
Sambandan, Sanjiv

Sanjiv Sambandan is a cross-appointed faculty at both applied physics, Indian Institute of Science and the department of engineering, University of Cambridge. His research interests are in disordered semiconductors and flexible electronics.

Sauter, Martin

Martin Sauter studied physics at Technische Universität München (TUM) in Germany. In 1992, he received a degree in physics (Dipl. Phys.). Professor Sauter joined Siemens AG in the corporate R&D department for the development of bipolar and BiCMOS processes in 1993. In parallel, he worked on his PhD thesis on lateral bipolar transistors on SOI. In 1996, he received the Dr.-Ing. degree from the University of the Armed Forces in Neubiberg, Germany. Between 1995 and 1999, he was CAD engineer for BCD technologies at Siemens semiconductor division. Since 1999, Professor Sauter is professor of general and theoretical electrical engineering at the University of the Armed Forces in Neubiberg, Germany.

Scheucher, Wolfgang



Wolfgang Scheucher was born in Bruck/Mur, Austria, in 1968. After graduating from HTL Graz-Goesting, he joined Mikron (which became later Philips, and subsequently NXP) in 1993. At the beginning, he worked on various engineering positions until he started to deal with the first ESD challenge in 1998. Since then Wolfgang has been focusing on ESD as a design engineer, but also working as an ESD coordinator responsible for the NXP site in Gratkorn, Austria.

Scholz, Mirko

Dr. Mirko Scholz is an ESD specialist at imec in Leuven, Belgium. He received his PhD in electrical engineering from Vrije Universiteit in Brussels (VUB) in 2013 for the thesis "Closing the

Design Gap between System-Level and Component-Level Electrostatic Discharge (ESD)". Since 2005, he has been working on ESD reliability. In 2007, he joined the ESDA device testing working groups. He currently chairs working group 5.6 on human metal model. He served as a seminar chair for the 2016 IEW, as a sub-committee chair for the 2016 ESD Symposium and on the ESDA advanced topics committee. He is a peer reviewer for several IEEE journals like TDMR, TIM, EDL and TED. He has authored and co-authored more than 100 publications, tutorials, and patents in the field of ESD reliability. He is co-author of the book *System-Level ESD Protection*. His current research interests include ESD analysis and protection design for sub-20 nm technologies, 2.5/3D integration, ESD testing, and system-level ESD. He regularly teaches ESD tutorials, courses, and seminars to internal and external audiences for imec and EOS/ESD Association, Inc.

Secareanu, Radu

Radu Secareanu received his MS from Polytechnic University of Bucharest in 1990 and his PhD degree from the University of Rochester in 2000; both in electrical engineering. He was with Baneasa SA Semiconductors in Bucharest from 1990 to 1995. In 2000, Radu joined Motorola (then Freescale and now NXP) where his primary technical contributions are in the areas of signal isolation, EMC, and latch-up across technologies for analog/RF, and mixed-signal, as well as digital designs. Radu is active in SRC/GRC, University, and IEEE. He is a recipient of the 2007 SRC Mahboob Khan Mentor award. He is an associate editor and TPC member of IEEE journals and conferences. He has authored and coauthored numerous patents and referenced papers. Radu has also been teaching EE classes at ASU since 2002.

Sengupta, Rudrarup

Rudrarup Sengupta received his bachelor's degree from the department of electronics and communication engineering at Heritage Institute of Technology, Kolkata, India, in 2016. He is currently working as a project assistant, at the department of electronic systems engineering at Indian Institute of Science, Bangalore, India.

Seva, Ramu

Ramu Seva graduated from Missouri University of Science and Technology with a master's degree in computer engineering in December 2016. He was a graduate research assistant at Missouri S&T with digital and analog IC design, verification, and testing as his areas of interest. He worked on multiple projects which included design of ESD sensors, study of EMC effects on ICs, and design of novel approaches for efficient stochastic computing. He is currently working at Monsanto, Saint Louis, as an FPGA engineer; where he is developing real-time systems for implementing image processing applications.

Shankar, Bhawani

Bhawani Shankar received a ME in electrical engineering with specialization in power electronics from Birla Institute of Technology and Science (BITS), Pilani, India, in 2013. He is currently pursuing a PhD in advance power semiconductor devices with the Indian Institute of Science, Bangalore, India. His research interest is reliability of GaN-on-Si power devices.

Sharma, Anmol

Anmol Sharma received his master's from Indian Institute of Technology, Madras. He is currently a member of technical staff at Texas Instruments; where he has been working since 2000. He has a broad experience in analog circuit design ranging from switching regulators, LDOs, battery chargers, precision references, and low power. He has published several technical papers and received many international patents in the mentioned technical fields. He is an elected senior member of IEEE.

Shibkov, Andrei

Andrei Shibkov has been working in the device design, reliability, process development, TCAD, and EDA area for over 18 years, starting with his graduate work (MS in engineering physics in 1993 and PhD in semiconductor physics in 1996) at Moscow Institute of Physics and Technology (MIPT), and continuing at Samsung Electronics (1995-1997), PDF Solutions (1997-2002), Sequoia Design Systems (2002-2007), and Angstrom Design Automation (2007 – present). During this time, he was involved in all aspects of semiconductor process and device development, and optimization, characterization, yield management, ESD, and reliability, sub-wavelength lithography simulation and optimization, and TCAD-related work.

Shinde, Satyajeet

Satyajeet Shinde (S'15) received a BE in electronics and telecommunications from the University of Pune, Pune, Maharashtra, India, in 2010; and a MS in electrical engineering from EMC Laboratory, Missouri University of Science and Technology, Rolla, MO, USA, in 2014. He is currently working toward a PhD in electrical engineering at EMC Laboratory, Missouri University of Science and Technology, Rolla, MO, USA. His research interests include radio frequency interference, radiated emission modeling, and EMC.

Shrivastava, Mayank

Professor Mayank Shrivastava received his PhD from Indian Institute of Technology Bombay. He has over 70 international publications and 35 patents. Professor Shrivastava's current research deals with experimentation, design, and modelling of beyond CMOS devices using Graphene and TMDCs, wide bandgap material based power semiconductor devices, and ESD reliability in advanced and beyond CMOS nodes. Between 2010 and 2013, he held positions at Infineon Technologies, Munich, Germany; Infineon Technologies, East Fishkill, NY, USA; IBM Microelectronics, Burlington, VT, USA; Intel Mobile Communications, Hopewell Junction, NY, USA; and Intel Mobile and Communications, Munich, Germany. He joined Indian Institute of Science Bangalore as a faculty member in September 2013. He is among the first recipients of the Indian section of the American TR35 award (2010). He is also the first Indian to receive IEEE EDS Early Career Award (2015). In addition to this award, he is an IEEE senior member and has received several other awards and honors including a few best research paper awards; excellence in research award for his PhD thesis in 2010, and an industrial impact award from IIT Bombay in 2008. More details related to his group or work can be found at: http://mayank.dese.iisc.ac.in/.

Sinha, Rajat

Rajat obtained his bachelor's degree in electrical and electronics engineering from Birla Institute of Technology, Mesra, in 2015. He joined IISc Bangalore in 2015 and is currently pursuing his PhD with Professor Mayank Shrivastava and Professor Sanjiv Sambandan. His research focuses on ESD reliability of flexible electronics. Rajat likes to travel and explore new places; and is a foodie at heart.

Smallwood, Jeremy

Jeremy spent seven years as an electronics designer before returning to Southampton University to do a PhD researching measurement of electrostatic discharge (ESD) ignition of pyrotechnic materials. He later worked at ERA Technology Ltd. on electrostatics R&D projects and consultancy. In 1998, he started Electrostatic Solutions Ltd, specializing in training, consultancy, test, and R&D for the electronics industry, electrostatic hazards avoidance, and electrostatic materials and applications development. Jeremy was presented with the 2010 EOS/ESD Association, Inc.'s Industry Pioneer Recognition award. In April 2017, he was awarded the European Working Party on Static Electricity in Industry (EFCE) International

Fellow award for “notable contributions to the advancement of the field of industrial electrostatics as a researcher and a teacher”. Jeremy has over 60 publications in the fields of electrostatics, measurements, ESD ignition hazards, and ESD prevention; and is a regular speaker at international conferences and workshops. He is active in British standards panels and IEC panels on handling of electrostatic sensitive devices and control of undesirable static electricity. Between 2000 and 2012, he was chairman of the IEC TC 101 (electrostatics). TC 101 is responsible for world standards in electrostatics. He held a two-year part-time post from 2013 to 2015 as senior research fellow at Southampton University’s high voltage group working on an EU funded research project while maintaining his Electrostatic Solutions Ltd consulting and training activities.

Smedes, Theo

Theo Smedes received his MSc and PhD from the Eindhoven University of Technology, in 1986 and 1991, respectively, with theses on compact device modelling. After he received his PhD, he worked at Delft University of Technology on layout-to-circuit extraction with a focus on substrate coupling. In 1995, he joined Philips Semiconductors (now NXP Semiconductors), The Netherlands. He worked on the development of tools for statistical design for submicron CMOS processes. Currently, he is fellow for ESD and latch-up within NXP Semiconductors. He has published several papers on ESD and introduced an ESD design course within NXP. Theo is a member of all EOS/ESD Association, Inc. device testing working groups and is chair of the TLP working group. He was co-recipient of the 2007 EOS/ESD Symposium Best Paper Award and the 2009 Outstanding Paper Award. Theo was a member of technical program committees of EOS/ESD Symposia, IEW, IEDM, IRPS, IPFA, and ESREF. He has served as TPC chair, vice general chair, and general chair of EOS/ESD Symposia from 2011 to 2013.

Song, Ming-Hsiang

Ming-Hsiang Song received a BS in physics and a MS in electrical engineering from National Taiwan University, Taipei, Taiwan in 1988 and 1990, respectively. From 1996 to 1999, he worked as DRAM circuit design in TI-Acer. In 1999, he joined Taiwan Semiconductor Manufacturing Company (TSMC) after the merge. He is currently deputy director of ESD and IO team in RD. His research interests include device ESD/EOS reliability, on-chip ESD protection, I/O interface circuit, single-event effect, and hardened circuit.

Soni, Ankit

Ankit Soni obtained a BTech in electronics and communication engineering from National Institute of Technology, Hamirpur, Himachal Pradesh, India. He became a PhD student at Indian Institute of Science, Bangalore, India, in 2015. His research interests include computation modelling of GaN HEMT. He is also involved in design and fabrication of high power HEMTs.

Sorgeloos, Bart

Bart Sorgeloos received his MSc in electro-technical engineering option applied electronics in 2004 from the University of Ghent, Belgium. His master’s thesis is entitled “Design of a RF Tuner with Double Conversion”. He joined Sarnoff Europe in 2005 as an ESD design engineer. After June 2009, Sarnoff Europe became Sofics - ‘Solutions for ICs’. He is now working as an ESD design specialist in different advanced CMOS projects (28 nm – 65 nm), RF applications, ESD verification tools, high ESD performance clamps (system level, surge test), and IP protection. His main focus is development of new ESD clamps and support of customers worldwide. He has authored and coauthored multiple peer-reviewed papers and patent applications.

Stadler, Wolfgang

Wolfgang Stadler received his diploma degree in physics and a PhD from the physics department of the Technical University Munich in 1991 and 1995, respectively. In 1995, he joined the semiconductor division of Siemens; which became Infineon Technologies in 1999. His focus was on development of ESD-protection concepts in CMOS technologies and on innovative ESD topics. In this role he was coordinator of several European and German ESD funding projects. In 2003, he became responsible for the measurement characterization of I/O cells and PHYs. In 2011, he joined Intel Mobile Communications (IMC); which is now Intel Deutschland GmbH. He is responsible for ESD/latch-up testing and qualification, for ESD control programs, and ESD risk assessment and fab support. Wolfgang holds several patents in ESD-related topics. He is author or co-author of more than 100 technical papers and has co-authored a book on ESD simulation. He received several best paper awards and regularly teaches courses on ESD device testing, ESD qualification, and ESD control measures (e.g., TR53 ESD technician certification). He is an active member of EOS/ESD Association, Inc. working groups related to device and system testing, ESD control, and process assessment. He is also a member of STDCOM and TAS. Since 2011, he has been the committee chair of the working group 5.4 - transient latch-up. Since 2013, he has been co-chair for working group 17 - process assessment. He was elected in 2014 and 2016 to serve as a board of director for EOS/ESD Association, Inc. through 2019. In 2015, he was appointed as education business unit manager. Since 2015, he has been acting president of the German ESD FORUM e.V.

Stockinger, Michael "Michi"

Michael "Michi" Stockinger received a MS and PhD in electrical engineering with highest honors from Vienna University, Austria, in 1996 and 2000, respectively. His doctoral research focused on the optimization of ultra-low-power CMOS transistors. In 2000, he joined Motorola's semiconductor products sector in Austin, Texas; which became Freescale Semiconductor in 2004 and then NXP Semiconductors in 2016. Michael has been working in the field of ESD protection for advanced CMOS products since 2000. He is currently the technical leader of ESD design in NXP's 32-bit microcontroller division. Michael's on-chip ESD solutions have been implemented in the Qorivva, Kinetis, and ColdFire microcontroller product lines, to name a few. His latest research interests are in the field of on-chip protection solutions for system level (IEC) transient immunity. Michael was awarded the 2001 EOS/ESD Symposium Best Paper award, the 2003 EOS/ESD Symposium Best Paper and Best Presentation awards, and the 2013 EOS/ESD Symposium Best Paper and Outstanding Paper awards. He has authored and co-authored over 30 technical papers and teaches an EOS/ESD Association, Inc. tutorial. He has served in the TPC of several EOS/ESD Symposia and International Reliability and Physics Symposia and as A/V co-chair of the International ESD Workshop (IEW). Michael holds 21 patents on ESD design, with several others pending.

Su, Yu-Ti

Yu-Ti Su received a BS from the department of applied physics, Tung-Hai University, Taiwan, in 2004, and a MS from the department of electronics engineering, National Tsing-Hua University, Taiwan, in 2006. From 2006 to 2011, he worked for Winbond Technology Corporation and Nuvoton Technology Corporation, Taiwan, as an engineer for ESD device development and ESD whole chip circuit design. He joined TSMC in 2011 and serves as a section manager of the ESD/EOS technology design department.

Tamminen, Pasi

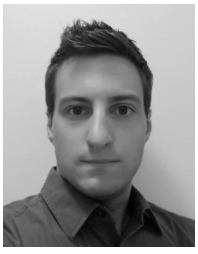
Pasi received a MSc in electronics engineering from Oulu University, Finland, in 1997; and continued to work for NOKIA Networks for four years with

automated production technologies, testing, machine vision, process control, and design for manufacturability. From 2001 to 2005, he was at VTT Technical Research Centre of Finland and worked with risk management, EMC/ESD, and cleanroom control methods. He received iNARTE ESD engineer certification in 2005. Between 2005 and 2012, Pasi worked for NOKIA Mobile Phones by managing cleanroom technology and ESD/EMC/ EMI control and design related projects globally in manufacturing and supported R&D, sourcing, and quality. Between 2014 and 2015, he worked at Microsoft R&D with product designs. In parallel, Pasi has worked with IEC and ANSI standardization bodies to complete research on electrostatics, EMS/ESD failures, qualification, and control methods at Tampere University of Technology. He received a PhD in science and technology in January 2017.

Thomas, Eric

Eric Thomas received his high school degree in electronics in 1984. He joined Philips in 1984 to work on wireless telephone development. He joined Philips Semiconductors in 1996 (now NXP Semiconductors) to characterize in lab RF PLL for mobile phone application. After a strong experience in lab and product management, Eric is now involved in RF integrated circuit development as top layout and reliability checks engineer. He's become the local ESD expert for his department, in close cooperation with Dolphin Abessolo-Bidzo, to improve the robustness of RF IC. He participated in NXP internal ESD symposia and produced together with Dolphin Abessolo-Bidzo an ESD guideline for RF IC development.

Thomson, Nicholas



Nicholas Thomson received a BS in electrical engineering and a BS in computer engineering from the Missouri University of Science and Technology in 2010. He received a MS in electrical engineering for his developments in ESD emulation techniques at the University of Illinois at Urbana-Champaign in December 2015. He is currently pursuing a PhD at the same university, with work towards understanding and detecting soft-failures resulting from system-level ESD. He joined Intel Corporation in February 2017.

Trivedi, Nitesh

Nitesh Trivedi received an MTech degree in reliability engineering (microelectronics discipline) from Indian Institute of Tech, Mumbai, in 2000. He joined Philips (now NXP) Semiconductor and worked there for ten years. From 2010 until May 2017, he worked for Infineon Technologies. Nitesh is currently working at Intel, as senior staff in the area of ESD protection. He gathered experience as a product engineer in the manufacturing fab and as a designer for I/Os and ESD at Philips/NXP. Since 2005, he has worked in the area of ESD verification methodology. Nitesh authored/co-authored papers at EOSESD Symposia and also at IEW, including one wining the outstanding paper award in 2009. Nitesh is an active member of the EOS/ESD Association, Inc. EDA working group.

Tsai, Tsung-Che

Tsung-Che Tsai received his MS in science from K.U. Leuven and National Chaio Tung University in 2010, and a BE in electronics engineering from National Chiao Tung University in 2008. He joined GLOBALFOUNDRIES in 2014; where he works on ESD and latch-up protection design for multiple technology nodes. Prior to joining GLOBALFOUNDRIES, he worked at Taiwan Semiconductor Manufacturing Company.

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James Tsan received his MS in engineering management from Santa Clara University and his BS in electrical engineering from Cal Poly, San Luis Obispo. He has over 10 years of industry experience. He joined Cisco Systems, Inc. in San

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Tseng, Wei-Jhih

Wei-Jhih Tseng was born in Taichung, Taiwan (R.O.C.), on August 30, 1985. He received a BE and ME in electrical engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2006 and 2008, respectively. He received his PhD from KULeuven/imec, Leuven, Belgium, with a research topic in photoelectrochemical study of III-Nitride semiconductors. In 2015, he joined the front-end innovation center of NXP Semiconductors, Nijmegen, Netherlands, as a device physicist. His current research interests include high voltage and power electronics, and TCAD simulation.

Van Camp, Benjamin

Benjamin Van Camp received his MSc degree in electro-technical engineering from the University of Leuven, Belgium, in 2002. He joined Sarnoff Europe (now Sofics) in 2003. Since then, he has lead several ESD and research projects. Currently, he is responsible for the long term R&D targets with the company. Benjamin has authored or coauthored several papers and patents.

Vaserman, Yosi

Yosi Vaserman received a BSc in physics in 2002 and an MSc in solid state physics in 2013 from Technion, Israel Institute of Technology. His research focused on noise measurements of high temperature superconducting devices. In 2004, he joined TowerJazz and worked in a variety of fields. His engineering roles include process, device, and ESD. In the past few years, he has worked in the ESD and latch-up group. This involves the development of new ESD devices and protection concepts, ESD characterization and design guidelines, creating libraries of ESD devices in PDK, PERC, and customer support as well as infrastructure for ESD design validation and simulation.

Vashchenko, Vladislav

Since 2011, Dr. Vladislav Vashchenko has been the ESD group director at Maxim Integrated Corp. His group covers a broad range of aspects related to analog ESD design, including IP libraries and rules, TCAD, new process technologies development, analog IC product ESD/latch-up co-design and reviews, and system level qualifications tests as well as latch-up, layout, and schematic rules and checkers development. Prior to Maxim, he led the ESD group at National Semiconductor Corp. for more than a decade. He received a MS as an engineer-physicist, and a PhD in physics of semiconductors from Moscow Institute of Physics and Technology; followed by a habilitation degree in doctor of science in microelectronics in 1990 after a decade of industrial R&D work in the field of reliability of discrete Si and GaAs microwave components. Over the last 12 years, he has been a regular TPC member of EOS/ESD Symposia, IEW, and IRPS; and has delivered a number of tutorials for at EOS/ESD Association, Inc. and IEEE events. He is also an author of 150 US patents and over 120 papers in the ESD field, as well as the Springer text books *Physical Limitation of Semiconductor Devices* (2008), *ESD Design for Analog Circuits* (2010), and *System Level ESD Protection* (2014).

Viheriäkoski, Toni

Toni Viheriäkoski began his electrostatic career while employed by Nokia Networks between 1986 and 2007. Toni established a calibration and electrostatics laboratory services for Nokia. He completed his technical supervisor studies in information technology in 1994. He was the chair of measuring methods working group of Finnish STAHA (electrostatics control) technology program in 2001 and 2002. He received iNARTE ESD engineer certification in 2004. Toni transferred to Nokia Siemens Networks from Nokia in April

2007; where he continued his work as an electrostatics specialist and senior sourcing engineer until he moved on to his own company, Cascade Metrology, which was previously established in 2005. Currently, his principal occupation is as a senior electrostatics specialist. He is working in the field of electrostatics and ESD risk analysis for electronics, automotive and chemical industries. Toni has written more than 20 publications related to electrostatics or ESD. He has been a chair of the Finnish STAHA Association since 2006. He was nominated a chair of Finnish Standardization Committee SK101 in 2016. He is also a member of WG5 of IEC TC101 and a project leader of PT 61340-6-1.

Weber, Johannes

Johannes Weber received his master's in physics from Technical University Munich (TUM) in 2015. He wrote his master's thesis in the research area of nuclear, particle and astrophysics at Max Planck Institute for Extraterrestrial Physics. Afterwards, he joined the team of analysis and test at Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT as a PhD student. He is currently working under the 2016 ERC Grant from EOS/ESD Association, Inc. in the field of ESD test methods with a focus on pulsed high current characterizations of highly integrated circuits and systems.

Wei, Pengyu

Pengyu Wei is currently working toward a MS in electrical engineering at EMC Laboratory, Missouri University of Science and Technology, Rolla, Missouri, USA.

Weil, Geoffrey

Geoffrey Weil is recognized internationally for his skills as a high speed analog design engineer. He has focused on high speed, high voltage applications through most of his career. He attended Harvard University in physics and mathematics before entering the field of professional engineering. At MIT he worked as a member of the technical staff for the Rei Weiss group. He designed, built, and tested power supplies, signal conditioning, and data acquisition components of the balloon borne experiment to measure the cosmic ray microwave background. During this time, he also participated in a search for gravitons. He joined Hyperion Industries of Massachusetts as an electronics engineer. He gained experience there designing custom switching power supplies. He worked at KeyTech Instrument Corporation of Massachusetts, joining as an engineer and later promoted to director of research and development. The company designs and manufactures ESD simulators including ultra-fast CDM simulators; which offer sub-nanosecond rise time and multi kilovolt swings. He patented the technique of HV switching with gas-filled relays. After KeyTech, Mr. Weil worked for Datacom in Washington, an Ethernet cable tester manufacturer. He was director of advanced technology products. Among his accomplishments, he designed a 350 MHz handheld cable tester. In the past 6 years, he has worked on a variety of analog projects under the name Anodyne Research having designed an non-contacting electrostatic voltmeter, an ESD-induced EMI detector, a charged plate monitor, an ESD target current viewing detector, and other ESD related projects. He has teamed with LBL Scientific on high speed high current power switching projects. Mr. Weil holds four patents in electronic engineering technology.

Wolf, Heinrich

Heinrich Wolf received his diploma degree in electrical engineering from the Technical University of Munich (TUM) and his PhD from the Technical University of Berlin, Germany. He joined the chair of integrated circuits at TUM as a member of the scientific staff working on electrostatic discharge related issues. This involved modeling of ESD-protection elements, parameter extraction techniques, and test chip design. In 1999, he joined the Munich branch of the Fraunhofer Institute for Reliability and Microintegration (IZM); which became the Fraunhofer Institution for Microsystems

and Solid State Technologies EMFT in 2010. He was involved in the investigation of ESD phenomena for CMOS and smart power technologies. Furthermore, he published on the development of ESD test methods and tester characterization. Currently, he is coordinating the ESD related activities at EMFT including the development of ESD test systems and the design of protection structures for deep submicron technologies. He is also working in the field of RF simulation and characterization in the frequency range up to 110 GHz.

Wong, Richard

Richard Wong received his MS in electrical engineering from Santa Clara University and his BS in chemical engineering from UC Berkeley. He has over 30 years of industry experience. He joined Cisco Systems, Inc. in San Jose, CA, in 2006. He has been engaged in IC component technology reliability assurance, soft error upset, wafer level reliability, electrostatic discharge, failure analysis, and reliability modeling. Prior to Cisco, he worked on ASICs, FPGAs, TCAMs, and memories. He has 18 patents and has authored or co-author over 200 published papers.

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Shaojie Xiang is an undergraduate student of electrical and electronic engineering at Huazhong University of Science and Technology, Wuhan, China. He was a visiting student at EMC lab of Missouri University of Science and Technology, MO, USA, in 2016. His research interests include VLSI circuits design and digital signal processing.

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Carol Rouying Zhan received her PhD in electrical engineering from Illinois Institute of Technology, IL, USA, in 2005. She joined Freescale Semiconductor the same year. She is currently a principal ESD design engineer at NXP Semiconductors. She has been responsible for delivering HV ESD library cells and design collaterals for NXP/Freescale's advanced smart power technologies. Her job duties also include providing ESD protection guidelines, supporting new products, performing and supporting circuit-level ESD simulations, and interfacing with technology/modeling/PDK teams. Her focus is on ESD protection for automotive applications on both IC and system levels. She holds more than 20 U.S. patents, and has authored or co-authored more than 30 technical papers on ESD devices, ESD failure mechanisms, and full-chip ESD design verification.

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Friedrich zur Nieden received a PhD in electrical engineering from TU Dortmund University, Germany, in 2014. From 2007 to 2012, he was a research and teaching assistant at the on-board systems lab at TU Dortmund University. In 2010, he received a scholarship from the German Academic Exchange Service staying at Missouri University of Science and Technology, Rolla, USA; where he continued his work in the field of system level ESD simulation. Since 2012, he has been a member of the central ESD department with Infineon Technologies AG, Munich, Germany. At Infineon he is responsible for ESD topics with regard to ESD characterization and device testing, and ESD system level and production support.