On-chip Monitors of Supply Noise Generated by System-level ESD

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Abstract - Two supply noise monitor circuits are demonstrated on a 130-nm test chip. These monitors are capable of providing quantitative measurements of on-chip supply voltage perturbations resulting from system-level ESD. Circuit-level simulations reproduce all trends found in the measurement results.

I. Introduction

The chip-level manifestations of system-level ESD can be inferred only indirectly, e.g. from the presence of application-level errors or physical damage to the IC. Efforts have been made to obtain more information in order to guide design improvements. For example, by inserting voltage probes on a circuit board [1] and by placing glitch detector circuits on a test chip [2] it was shown that ESD energy propagates from the system-level to the chip-level in the form of glitches (noise) that appear at IC pins. However, there is also indirect evidence that some soft-failures are the result of ESD-induced noise inside a chip's power delivery network [2]. This work introduces on-chip supply voltage monitors that respond to ESD noise. The operation of the monitor circuits is verified in the context of a 130-nm CMOS test chip.

II. Supply Noise Monitors

A. Supply Voltage Monitor

Two types of supply voltage monitor circuit are introduced; the over-voltage (OV) monitor measures the peak positive excursion above the nominal power supply voltage, while the under-voltage (UV) monitor measures the peak negative excursion. Different versions of these circuits are needed for the IO and core power supply domains; the high voltage ("HV") IO supply was 3.3 V in this work, and the low voltage ("LV") core supply was 1.5 V. Figure 1 illustrates the four voltage monitor circuits. In all cases, the circuit consists of a sample and hold, a Flash analog-to-digital converter (ADC), and latches that store the digital output value until readout occurs at a later time.

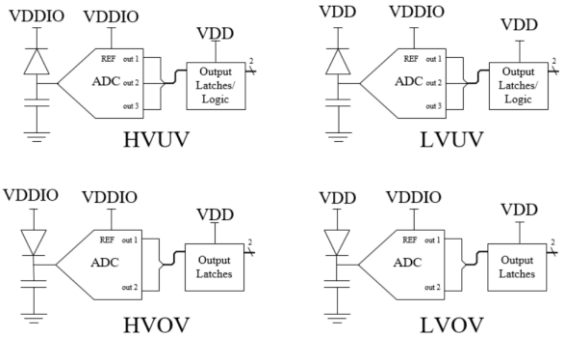


Figure 1: Overview of the four voltage monitor circuits. HV circuits measure over-voltage (OV) or under-voltage (UV) on the high-voltage IO supply. Similarly, LV circuits measure voltage deviations on the low-voltage supply for the core logic.

The sample and hold circuits are illustrated in Figure 2. The capacitor voltage, V_C, is initially at the nominal value of VDD. During ESD, if a negative [positive] excursion on VDD is large enough to turn-on the diode-connected MOS in Figure 2a [2b], the capacitor will begin to discharge [charge]. When VDD subsequently returns to its nominal value, the transistor will be cut-off and the sampled voltage will be held on the capacitor.

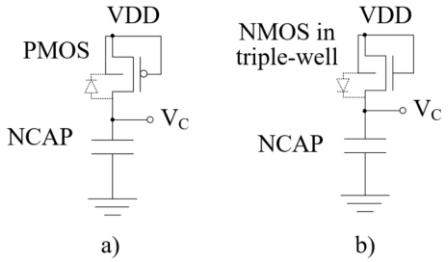


Figure 2: Sample and hold for (a) under-voltage and (b) over-voltage monitor circuits.

The UV monitors use a PMOS diode because its body effect beneficially reduces the on-voltage. If VDD dips significantly below the value stored at the

node labeled V_C, the PMOS will experience a forward body-bias, which reduces its threshold voltage. Furthermore, the parasitic PNP formed between the PMOS and the P-substrate will help to discharge the storage capacitor. Similarly, the OV monitors use an NMOS diode to take advantage of the forward body-bias that will occur during a supply over-voltage.

The storage capacitor is an accumulation-mode NCAP since this provides the highest capacitance per unit area. The NCAP is implemented using triple-well isolation. The alternative is illustrated in Figure 3a, and, as shown in the picture, a parasitic PNPN is formed between VDD and VSS, which poses a possible latchup hazard. To remedy this, the capacitor is placed in an isolated N-well, as shown in Figure 3b. The capacitor and the diode-connected transistor are sized to strike a balance between response time and retention time. Each NCAP is on the order of 100 fF.

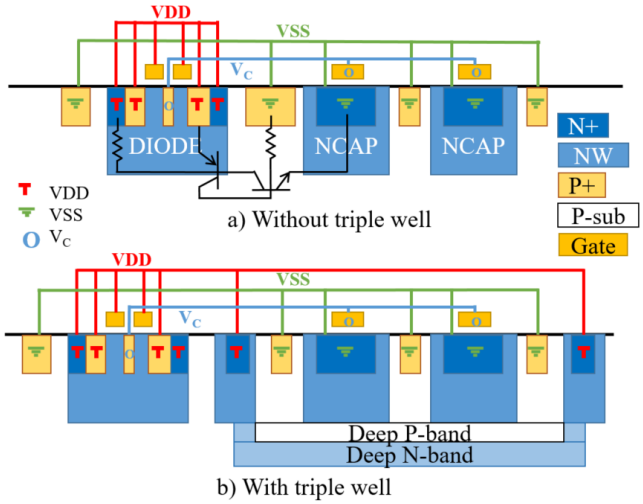


Figure 3: Cross-section of PMOS diode and NCAP. The design without triple-well isolation in a) contains a parasitic PNPN with large NPN emitter area. The layout with triple-well isolation in b) removes this vulnerability.

The Flash ADC compares the voltage stored across the capacitor to the reference voltages provided by a resistor chain. Filter capacitors are included on the resistor chain to stabilize the references. The voltage monitor operates properly even if the ESD-induced supply noise is so severe that the ADC temporarily becomes nonfunctional; proper operation results because the ADC input is held on the NCAP for a much longer duration (tens of µs in most cases) than the supply disruption. The UV monitors provide three levels of resolution and the OV monitors provide two levels; the UV ADC output undergoes 3-digit thermometer code to 2-digit binary code conversion following the storage latches. Note that it is straightforward to increase the number of voltage levels (i.e., ADC bits) if silicon area is not a concern.

Using simulation, the ADC output can be plotted as a function of its DC input voltage. However, during an ESD event, the node labeled V_C in Figure 2 will not be at same instantaneous potential as VDD because the sample and hold response time is limited by the diode on-voltage and the circuit's RC time constant. Therefore, the input-output characteristic of the supply voltage monitor circuit should be obtained from pulse testing. Standalone voltage monitor test structures were fabricated in 130-nm CMOS so that the input-output characteristics could be obtained under ESD conditions. Voltage pulses with 200 ps rise-time and variable pulse-width are injected onto the test structure's power supply through a bias-tee. The on-chip supply voltage is monitored through a high-impedance pick-off; Figure 4 shows an example measurement. If a negative pulse is injected, the minimum supply voltage is denoted as V_{MIN}, whereas if a positive pulse is injected, the maximum supply voltage is denoted as V_{MAX}. Table 1 lists the voltage-monitor output codes resulting from VFTLP and TLP injection onto a 1.5 V supply; both OV and UV monitors were connected to the supply. The measured values are compared against the DC-simulated ADC reference voltages. The pulse amplitude would need to be increased in fine increments to identify the precise thresholds for the monitor output levels; however, the data of Table 1 are sufficient to establish that during pulse testing, the thresholds for the monitor output levels track the simulated DC reference levels. The offset between the thresholds obtained from 100 ns TLP measurements and the DC levels appears to be roughly equal to the PMOS threshold voltage of 210 mV. As expected, a slightly larger pulse amplitude is needed to obtain a given output level when 4 ns VFTLP is used rather than 100 ns TLP, highlighting the importance of choosing a suitable pulse-width for calibrating the circuit. The output characteristics of the 3.3 V over- and under-voltage monitor circuits are provided in Table 2.

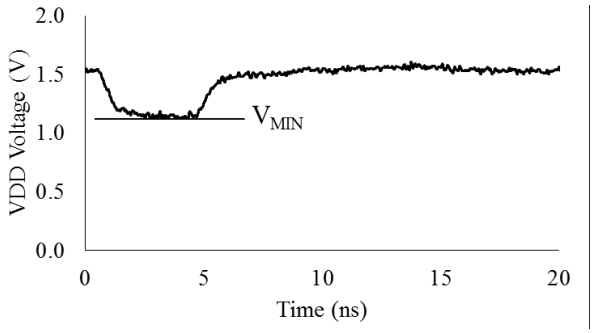


Figure 4: An example of a 4-ns-wide pulse with -0.5 V amplitude applied to a low-voltage (1.5 V) power supply.

Table 1: The LV monitors' output codes are compared with the measured under-voltage, V_{MIN}, and over-voltage, V_{MAX}. Nominal VDD is 1.5 V.

LVUV			
Output Code	Meas. V_{MIN} (t_{width} = 4 ns)	Meas. V_{MIN} (t_{width} =100ns)	ADC input range (DC simulation)
00	1.34 V	1.34 V	$V_{in} > 1.36$ V
01	0.74, 0.94, 1.15 V	0.9, 1.13 V	$0.9 < V_{in} \leq 1.36$ V
10	0.34, 0.54 V	0.49, 0.71 V	$0.45 < V_{in} \leq 0.9$ V
11	0.13 V	0.10, 0.28 V	$V_{in} \leq 0.45$ V
LVOV			
Output Code	Meas. V_{MAX} (t_{width} = 4 ns)	Meas. V_{MAX} (t_{width} =100ns)	ADC input range (DC simulation)
00	1.71, 1.9 V	1.7 V	$V_{in} < 1.65$ V
01	2.1 V	1.92 V	$1.65 < V_{in} < 1.82$ V
11	2.29, 2.47 V	2.15, 2.31, 2.47 V	$V_{in} > 1.82$ V

Table 2: The HV monitors' output codes are compared with the measured under-voltage, V_{MIN}, and over-voltage, V_{MAX}. Nominal VDD is 3.3 V. An ellipsis indicates too many data points to list.

HVUV			
Output Code	Meas. V_{MIN} (t_{width} = 4 ns)	Meas. V_{MIN} (t_{width} =100ns)	ADC input range (DC simulation)
00	2.13, …, 3.11 V	2.26, …, 2.89 V	$V_{in} > 3$ V
01	1.56, 1.75, 1.94 V	1.86, 2.06 V	$2 < V_{in} \leq 3$ V
10	0.57, …, 1.36 V	0.81, …, 1.66 V	$1 < V_{in} \leq 2$ V
11	0.17, 0.36 V	0.14, 0.38, 0.58 V	$V_{in} \leq 1$ V
HVOV			
Output Code	Meas. V_{MAX} (t_{width} = 4 ns)	Meas. V_{MAX} (t_{width} =100ns)	ADC input range (DC simulation)
00	3.67 V	3.53, 3.73 V	$V_{in} < 3.34$ V
01	3.88, …, 4.45 V	3.94, …, 4.73 V	$3.34 < V_{in} < 4.15$ V
11	4.66, …, 5.23 V	4.92, 5.13, 5.34 V	$V_{in} > 4.15$ V

B. Flip-flop Monitor

A bistable circuit element, i.e. a flip-flop, may be used as a detector of relatively severe supply noise. Although these circuits cannot provide as fine resolution of the supply voltage excursions as can the voltage monitor circuit, they have some advantages. First, a flip-flip based supply noise monitor can respond to supply voltage excursions less than 1 ns in duration. Second, the flip-flop monitor consumes far less chip area ($\frac{1}{16}\times$ in this work).

The flip-flop monitor, shown in Figure 5, is essentially a static latch circuit whose output will change state if there is a severe, transient over- or under-voltage on its supply line. Each of the cross-coupled inverters is defined by the parameter $\beta = \frac{(W/L)_P}{(W/L)_N}$. The flip-flop is designed to have $\beta_{FF} > \beta_{FB}$, where β_{FF} and β_{FB} describe the feedforward and feedback inverter, respectively. Prior to each ESD test, the latch input is reset to logic-high. As illustrated in Figure 6, the input to the feedforward inverter is initially high but this node is coupled to VSS through the gate capacitance (C_{GN}) of the NMOS. Similarly, the input to the feedback inverter is initially low but it is coupled to VDD through the gate capacitance of its PMOS.

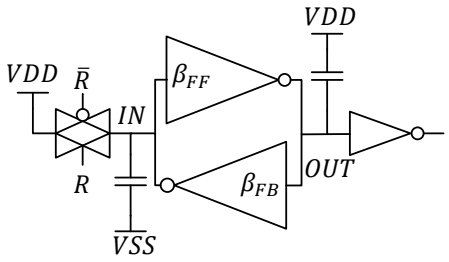


Figure 5: Flip-flop based supply noise monitor. The input to the transmission gate is connected to VDD through a tie-high cell. β represents the ratio of the pull-up device W/L to the pull-down device W/L.

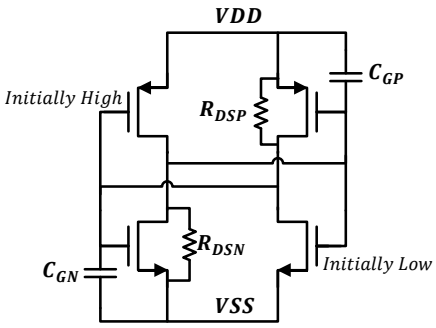


Figure 6: Circuit view of the cross-coupled inverters.

First, the case of a supply over-voltage transient is considered. Denote the inverter switching threshold as V_{TH}; if $\mathrm{VDD}(t) - V_{IN}(t) > V_{TH}$, node OUT will start to go high which in turn will further pull down IN, resulting in the flip-flop changing state. The fast transient associated with ESD can indeed cause such a state change, referred to as data *upset*; if VDD increases due to ESD, V_{IN} lags behind due to the effect of C_{GN}.

Under normal operating conditions, $V_{IN} = VDD$ and, therefore, a non-zero $|V_{IN}(t) - \mathrm{VDD}(t)|$ is indicative of a glitch. If the over-voltage between VDD and VSS is taken to be a pulse with rise-time t_r and amplitude V_A, one can show that the amplitude of the negative-going input glitch at time t_r is given by:

$$|V_{IN}(t_r) - VDD(t_r)| = \frac{V_A}{t_r} R_{DSP} C_{GN} \left(1 - e^{\frac{-t_r}{R_{DSP} C_{GN}}}\right)$$

In the limit of $R_{DSP}C_{GN} \gg t_r$, the glitch obtains its maximum amplitude of V_A.

Based on the preceding analysis, to increase the sensitivity of the flip-flop to supply noise, both the gate capacitance and the drain-source resistance of the

feedback PMOS and the feedforward NMOS should be made large. In this work, that design objective was met by using the minimum channel width for all transistors and non-minimum channel length for the feedforward NMOS and the feedback PMOS. Specifically, the transistor sizing is given by

$$\beta_{FF} = \beta_0 \frac{L_{nFF}}{L_{min}} = \beta \qquad (1)$$

In (1), β_0 is the pull-up to pull-down size ratio for a minimum-sized inverter. For simplicity, the feedback inverter is sized using $\beta_{FB} = \frac{1}{\beta_{FF}} \equiv \frac{1}{\beta}$; this requires that $L_{pFB} = \beta_0 L_{nFF}$.

Circuit simulation is used to illustrate how the flip-flop upset depends on β, t_r, and V_A. The results, shown in Figure 7, confirm that for sufficiently small t_r, the flip-flop changes state (upsets) at a fixed value of V_A and, for slower rise times, the β value determines the noise amplitude needed for upset. Circuit simulation was utilized to select the values of β used for the noise monitors in this work. In the simulation, a flip-flop monitor is connected to the on-chip supply and an IEC zap is applied to an IO pin. A parametric sweep of the transistor channel lengths was used to determine the β necessary for the monitor to upset at a given zap level. Table 3 lists the simulation-derived inverter sizes used for a set of monitors connected to the 1.5 V supply.

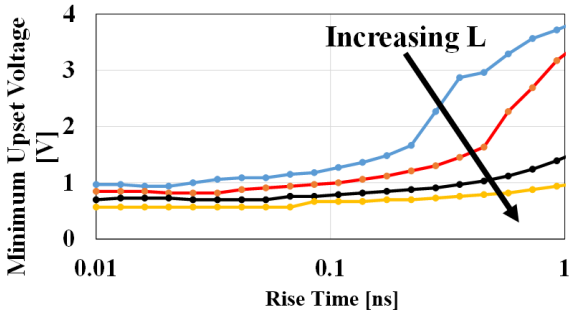


Figure 7: Simulated upset voltage for flip-flip monitors with variable L_{nFF} and L_{pFB}. A positive square-pulse is superimposed on V_{DD}; upset voltage is the minimum pulse amplitude that will upset the latch for a given rise-time t_r.

Table 3: β value that results in the flip-flop monitor upsetting at a specific IEC stress level (negative zaps). Monitor #1 is the most sensitive while Monitor #4 is the least. Simulation results.

Monitor	**1**	**2**	**3**	**4**
Upset Level [kV]	-3	-4	-5	-9
$\boldsymbol{\beta}$	17	11	7	5
$\boldsymbol{\Delta(VDD - VSS)[V]}$	1.1	1.4	2.0	4.1
$\boldsymbol{d(VDD - VSS)/dt\,[V/ns]}$	4.4	4.9	5.1	8.1

Next, the flip-flop monitor's response to a supply under-voltage transient is considered. During an under-voltage event, the initially high V_{IN} will be reduced by an amount that depends on the fall-time, pulse-width, and amplitude of the disturbance. The reduced supply voltage decreases the overdrive on the transistors, thereby increasing the channel resistances of the transistors in the feedforward and feedback inverters. This causes the flip-flop input to be even more strongly coupled to VSS and its output to be more strongly coupled to VDD. When the supply recovers, displacement current will flow from VDD to OUT through C_{GP}. If the time-derivative $d(VDD)/dt$ is sufficiently large, the displacement current will pull up OUT and cause the latch to flip (i.e., the voltage at OUT will increase faster than at IN, flipping the latch's state).

The flip-flop designs given in Table 3 are quite sensitive to under-voltages. It is more useful to have the monitors trigger at distinctly different ESD levels. The monitors' sensitivity to under-voltages is adjusted by activating the pass-gate between IN and VDD, i.e., by setting $R = 1$; see Figure 5. In this work, the pass-gate was too small to actively reset the latch, i.e., too small to overcome the effect of the feedback inverter; the pass-gate's primary effect is to augment the feedback inverter's PMOS, i.e., reduce R_{DSP} of Figure 6. When the supply recovers at the tail-end of the under-voltage event, the pass-gate will help pull IN back to its initial high state; therefore, when the pass-gate is active, a larger displacement current through C_{GP} is needed to flip OUT relative to the case that the pass-gate is off. Circuit simulation is used to predict the sensitivity of the flip-flop to ESD when the pass gate is active, i.e., when $R = 1$; the results are shown in Table 4. These simulations confirm that the upsets occur during recovery from an under-voltage and also a high immunity to over-voltage induced upset.

Table 4: Same monitors as for Table 3 but with $R = 1$ to provide a varying sensitivity to under-voltages. Simulation results for positive discharges.

Monitor	**1**	**2**	**3**	**4**
Upset Level [kV]	3	4	6	7

The preceding analyses provide a general understanding of how under-voltage and over-voltage supply transients can upset a flip-flop. An alternative design of an under-voltage detector may be found in [3].

III. Other Noise Detectors

A. Out-of-Range Input Detector

The out-of-range input detector (ORID) circuit [4], shown in Figure 8, is triggered if the signal appearing at an input (or IO) pin goes outside the range [VSSIO, VDDIO], where VDDIO and VSSIO are the power and ground references, respectively, for the IO circuits. In essence, the ORID detects (large) glitches at a signal

pin. Examination of Figure 8 reveals that the body diodes of the n-channel and p-channel pass transistors form a dual-diode secondary input protection circuit. The output of the upper latch, ORIDH, will be set if the voltage applied to the pad exceeds VDDIO by an amount equal to the smaller of $V_{D,on}$ and $|V_{Tp}|$, where $V_{D,on}$ is the diode on-voltage and V_{Tp} is the PMOS threshold voltage. Similarly, the output ORIDL will be set if the pad voltage falls below VSSIO by an amount equal to the smaller of $V_{D,on}$ and V_{Tn}.

B. Logic Circuits

Any logic circuit that can experience bit flips due to supply noise or glitches at input pins may be considered to be an ESD noise detector. Sequential logic circuits are especially convenient detectors since these can be read out following an ESD event to determine if an upset (bit flip) has occurred, provided that the state of the circuit prior to the discharge was known. In light of this observation, several shift registers were placed on the test chip used in this work; see Figure 9. These 4-bit shift registers utilize a three-wire interface. One pin provides an input to the first register (MSB first). The second pin is used to strobe data through the shift register. The third pin enables a set of dedicated output registers, which store the data and provide a parallel output. The parallel output can be read-out following ESD. Further, by subsequently toggling the latch enable pin (LE), it can be observed whether the data in the register's input stage (serial stage) was corrupted by the ESD.

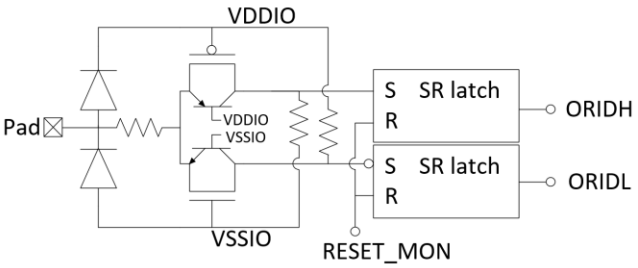


Figure 8: ORID circuit. If the voltage at the pad is greater than VDDIO then the top latch will set ORIDH high; otherwise, the pull-down resistor will keep the set signal low. Similarly, if the voltage at the pad falls below VSSIO, then the bottom latch will set ORIDL.

Dynamic logic circuits are also susceptible to ESD-induced glitches since, in contrast to static logic, the correct logic state is not restored when the glitch subsides. The test chip includes a dynamic OR gate; as shown in Figure 10, the OR gate has all but one of its inputs tied low and the remaining input is driven by an external signal.

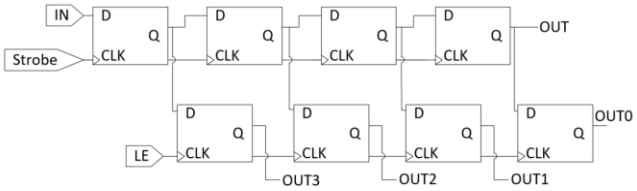


Figure 9: Shift register schematic.

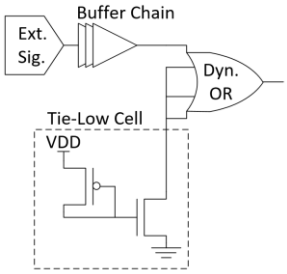


Figure 10: Test chip implementation of dynamic OR gate.

IV. Experiment

A 130-nm test-chip was designed and fabricated; its layout is shown in Figure 11. The chip uses a 3.3 V supply, VDD33, to power most of the IOs; VDD is an externally-supplied source that powers the core logic and a small number of low-voltage IOs. Active rail clamp circuits suitable for power-on ESD protection are connected to VDD33 and VDD [5]. Supply noise monitors are connected to both VDD33 and VDD. Those for VDD33 are located in Monitor Bank 1 and those for VDD are located in Monitor Bank 2.

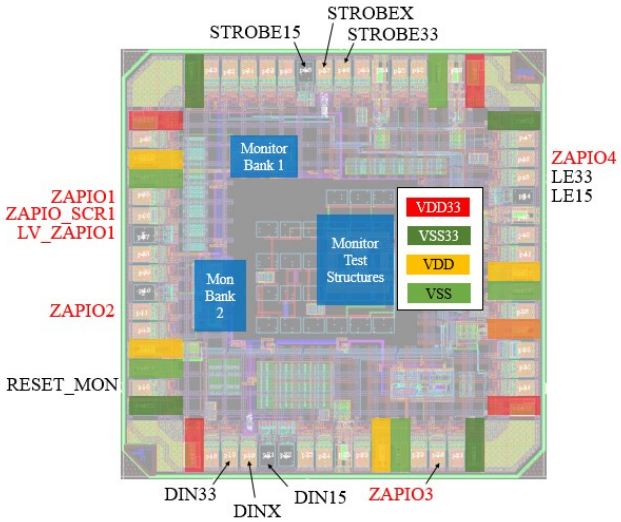


Figure 11: Test chip layout. Important pads and monitor blocks are indicated. Dedicated zap IOs are labeled in red.

The shift registers described in the previous section are placed in both monitor banks. The circuits in the two banks are copies of one another, and are powered by VDD; however, there is one difference. The external signals that drive the shift registers in Monitor Bank 1 are provided by ordinary (3.3 V) IO circuits whereas

those that drive the shift registers in Monitor Bank 2 are provided by special, low-voltage (1.5 V) IO circuits. The low-voltage IO circuits have a reduced noise margin.

The dynamic OR gate described in the previous section is located in Monitor Bank 2. Its inputs are provided by 3.3 V IO circuits that contain ORID circuits.

The IO pads labeled in red are subjected to contact ESD. ZAPIO1 through ZAPIO4 are 3.3 V cells with dual-diode (DD) ESD protection. ZAPIO_SCR is a 3.3 V cell with local clamp protection. ZAPIO_LV is a low-voltage cell with DD protection.

The IO pads labeled in black are not directly subjected to contact ESD; all of these receive important control or input signals. RESET_MON is a global signal that is used to reset all of the supply voltage monitors and ORIDs. The strobe and data-in signals for the dynamic OR gate are provided by STROBEX and DINX. The latch-enable, strobe and data signals for the shift registers in Monitor Bank 1 are provided by LE33, STROBE33, and DIN33. The corresponding shift registers in Monitor Bank 2 have their external signals provided by STROBE15, DIN15 and LE15. All external strobe and LE signals are driven low during ESD testing.

A 4-layer circuit board was designed to support the experimental work. The circuit board can be powered by a DC supply or by a battery pack. An LDO supplies 3.3 V for the IO circuits in the VDD33 domain. A variable LDO provides 1.5 V for the VDD domain. Decoupling capacitance is included on each of the power nets. The ESD gun is discharged into the test points on the periphery of the board. These test points are copper pads that lead to the corresponding on-chip IOs through on-board traces.

V. Measurement Results

A. Contact discharge to IO trace

ESD gun discharges were performed using multiple test chips and with the board powered by either a battery pack or an external DC supply; these are referred to as the mobile and tethered configurations, respectively. The absence or presence of a tether had no significant impact on the measured noise amplitude or observed soft failures, and thus the aggregated results are reported. For a given precharge voltage and zapped trace, a minimum of 5 discharges were applied. After each zap, the output of every supply noise monitor circuit was read-out (automatically). Table 5 lists the most severe noise reading that appeared in at least 40% of trials at a given condition. A non-zero table entry indicates that the supply voltage monitor recorded an excursion from the nominal value.

An examination of the data in Table 5 reveals the following. Zaps to the 3.3 V IO pins—ZAPIO1, ZAPIO4 and ZAPIO_SCR—induce noise on the 1.5 V supply, as evidenced by the resulting non-zero output codes from the LVUV and LVOV monitors. This result is not unexpected for a wire-bonded IC [5]. Positive zaps cause larger under-voltages on the supplies than do negative zaps; this result is reproduced in simulation (see Section VI). Zaps to IOs located close to the monitor banks cause the largest measured under-voltages, but even zaps to distant IOs create significant supply noise. This shows that the disturbance extends throughout the chip's entire power distribution network.

The response of the flip-flop monitors is also shown in Table 5. A number between 0 and 4 indicates how many of the monitors upset; a 1 indicates that only Monitor 1 upset, a 2 indicates that Monitors 1 and 2 and upset, etc. Without exception, if the i^{th} flip-flop monitor upset, the lower numbered monitors, 1 through $i-1$, were also observed to have upset. Since the voltage monitors indicated that positive zaps create larger under-voltages than do negative zaps, the flip-flop monitors were configured as under-voltage detectors (i.e., $R = 1$ in the circuit of Figure 6) when positive zaps were applied. The flip-flop monitors' response confirms that supply noise is not generated uniformly across the chip; zaps to IO pins located nearby the noise monitors induce more upsets than do zaps to distant pins.

The status of the dynamic OR gate and the shift registers was monitored during the experiments used to generate the data for Table 5. Table 6 summarizes the occurrence of OR gate upsets. The upset occurrence increases with the ESD level, but does not appear to be strongly correlated with zap polarity. If these upsets are the result of power supply noise, they are expected to show the polarity dependency indicated by the LVUV and LVOV monitor circuits. Instead, the upsets are attributed to 0→1 glitches at the gate's input pin, DINX. As shown in Figure 12, in 100% of the trials in which the ORIDH signal was set, the dynamic OR gate was observed to upset, consistent with the hypothesis that the upsets are caused by 0→1 glitches at the input. Although the OR gate upset without ORIDH being set in almost 20% of the trials, this observation does not contradict the hypothesis; the nominally-low DINX signal does not need to go above VDD33 to be interpreted as a logic-high signal, whereas it does need to swing above VDD33 to set ORIDH.

Table 5. Voltage monitor output levels after IEC stress. The flip-flop monitors were configured with $R = 0$ for negative zaps and $R = 1$ for positive zaps.

IEC level (kV)	HVUV ZAPIO 1	HVUV ZAPIO 4	HVUV ZAPIO SCR	HVUV ZAPIO LV	HVOV ZAPIO 1	HVOV ZAPIO 4	HVOV ZAPIO SCR	HVOV ZAPIO LV	LVUV ZAPIO 1	LVUV ZAPIO 4	LVUV ZAPIO SCR	LVUV ZAPIO LV	LVOV ZAPIO 1	LVOV ZAPIO 4	LVOV ZAPIO SCR	LVOV ZAPIO LV	Flip-flop monitor ZAPIO 1	Flip-flop monitor ZAPIO 4	Flip-flop monitor ZAPIO SCR	Flip-flop monitor ZAPIO LV
-5	0	1	1	NA	2	1	2	NA	1	1	2	NA	2	2	2	NA	2	0	0	NA
-4	0	1	1	1	2	1	2	2	1	1	1	3	2	2	2	2	1	0	0	4
-3	0	0	0	0	2	1	2	2	1	1	1	3	2	2	2	2	1	0	0	0
-2	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
-1.5	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
-1	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0
-0.5	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0.5	0	0	0	0	1	1	1	0	1	0	0	1	0	0	0	2	0	0	0	0
1	1	0	0	0	2	1	1	1	1	1	1	1	1	0	0	2	0	0	0	0
1.5	1	1	0	0	2	2	1	1	2	1	1	2	1	1	1	2	0	0	0	0
2	2	2	1	0	2	2	1	1	3	1	2	2	2	1	1	2	0	0	0	0
3	3	2	2	0	2	2	1	1	3	1	3	3	2	2	2	2	3	0	0	1
4	3	2	2	0	2	2	1	1	3	2	3	3	2	2	2	2	3	0	3	2
5	3	2	2	1	2	2	1	2	3	2	3	3	2	2	2	2	3	0	4	2

Table 6: Upset percentages for the dynamic OR gate.

Vpre (kV)	ZAPIO 1	ZAPIO 2	ZAPIO 3	ZAPIO 4	ZAPIO LV
-5	80%	100%	100%	100%	-
-4	100%	100%	100%	100%	100%
-3	100%	100%	100%	100%	100%
-2	100%	100%	0%	40%	100%
-1.5	60%	80%	0%	0%	100%
-1	0%	0%	0%	0%	40%
-0.5	0%	0%	0%	0%	0%
0.5	0%	0%	0%	0%	0%
1	0%	0%	0%	0%	0%
1.5	100%	100%	20%	0%	0%
2	100%	100%	20%	60%	0%
3	100%	100%	100%	100%	20%
4	100%	100%	100%	100%	10%
5	100%	100%	100%	100%	0%

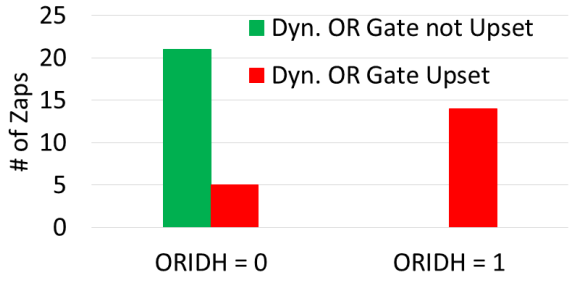


Figure 12: Correlation between ORIDH = 1 and upset of the dynamic OR gate. ORID circuit is in the DINX pad cell; DINX is the data input to the OR gate.

Table 7 summarizes the occurrence of bit flips in the shift registers. The shift registers in Monitor Bank 2 were disturbed at all but the lowest stress levels, whereas those in Monitor Bank 1 were mostly unaffected by ESD until ±3 kV. Recall that the key difference is that the input and control signals for the registers in Monitor Bank 1 are supplied by 3.3 V IOs while those in Monitor Bank 2 are supplied by 1.5 V IOs. Furthermore, the 3.3 V receivers contain Schmitt triggers for noise resilience whereas the 1.5 V input cells do not. Given that the registers in both banks are connected to VDD15 but those in Monitor Bank 1 are driven by receivers with a higher noise margin, one concludes that the shift register upsets are the result of glitches at the DIN15 and DIN33 pins.

Table 7: Percentage of zaps resulting in bit flips in the shift registers. Zaps were applied to ZAPIO1. There are separate shift registers in monitor banks 1 and 2.

V_{pre} (kV)	Mon. Bank 1	Mon. Bank 2
-5	100%	-
-4	100%	-
-3	100%	-
-2	15%	100%
-1.5	0%	100%
-1	0%	20%
-0.5	0%	0%
0.5	0%	0%
1	0%	80%
1.5	0%	100%
2	0%	100%
3	100%	-
4	100%	-
5	100%	-

B. Impact of TVS

A bi-directional TVS was placed between the signal trace that connects to ZAPIO1 and ground, and then IEC discharges were applied to the ZAPIO1 trace. The TVS shunts (most of) the ESD current to the board ground. As a result, much less supply noise is generated on-chip, as evidenced by the results shown in Table 8. This demonstrates that if a TVS is placed on the signal

trace that gets zapped, the ESD can be increased to much higher levels before it disturbs the system. The data in Table 8 suggest that a -12 kV zap to a TVS-protected trace induces less on-chip supply noise than a -4 kV zap to an unprotected trace, which is supported by the observation that none of the flip-flop monitors undergo upset in the first case but several do in the second.

C. Discharges to board ground and HCP

In another set of experiments, the ESD gun was discharged either into the USB connector shield or the horizontal coupling plane (HCP) near the USB shield (indirect discharge). The connector shield is connected to the board ground plane.

Table 9 summarizes the experimental results. Less supply noise was generated in these experiments than when the TVS-protected IO was zapped, which is a sign that the TVS did not completely prevent ESD current from entering the chip. Zaps to the board ground and to the HCP both generate relatively small supply noise. Zaps to the board ground appear to generate slightly more supply noise, perhaps due to ground bounce. In both cases, however, the noise primarily results from EMI, i.e., emissions from the ESD gun. Although EMI does not cause much supply noise, it can produce soft failures by inducing glitches at signal pins [2] [4].

D. Input Glitches

ESD zaps to IO pins that are not protected by the TVS, i.e. self-protecting IO, cause glitches to appear at other signal pins of the IC as detailed in [6] and as suggested by the measurement results presented in Section V.A. Here, it is investigated whether such glitches appear when a TVS is used on the zapped signal trace, or when the discharge is directed to the system ground, or when an indirect discharge test is performed. A glitch detector circuit [2] was included in a 3.3 V IO cell (labeled GDIO in Figure 11) immediately after the Schmitt trigger and level shifting circuits; the glitch detector's output switches from low to high if a logic-threshold crossing glitch is received at the input pin. The IO circuit with the glitch detector is not the same IO that is zapped; zaps are applied to ZAPIO1. Table 10 summarizes the experimental results. It is observed that the TVS was effective in eliminating the glitches that result when a signal trace is zapped, and that ground zaps did not cause glitches. Indirect discharges induced no glitches until the ESD level exceeded 10 kV. It is noted that the glitch detector was placed at an input that has a fairly large noise

Table 8. Comparison of voltage monitor output levels after IEC zaps at ZAPIO1 without TVS protection (N) and with TVS protection (Y). The test board was battery-operated.

IEC level (kV)	HVUV		LVUV		HVOV		LVOV	
	N	Y	N	Y	N	Y	N	Y
-12	NA	0	NA	1	NA	2	NA	2
-10	NA	0	NA	1	NA	2	NA	2
-8	NA	0	NA	1	NA	1	NA	2
-6	NA	0	NA	1	NA	1	NA	2
-4	0	0	1	1	2	1	2	2
-2	0	0	1	0	1	1	1	1
2	2	0	3	1	2	1	2	1
4	3	0	3	1	2	2	2	1
6	NA	0	NA	1	NA	2	NA	2
8	NA	0	NA	1	NA	2	NA	2
10	NA	0	NA	1	NA	2	NA	2
12	NA	0	NA	1	NA	2	NA	2

Table 9. Voltage monitor output levels after IEC zaps to the USB shield and the HCP. The test board was battery-operated.

IEC level (kV)	USB Shield				HCP			
	HVUV	LVUV	HVOV	LVOV	HVUV	LVUV	HVOV	LVOV
-10	0	1	1	2	0	1	0	1
-8	0	1	1	2	0	0	0	0
-6	0	1	1	2	0	0	0	0
-4	0	0	0	1	0	0	0	0
-2	0	0	0	0	0	0	0	0
2	0	0	0	1	0	0	0	0
4	0	1	0	1	0	0	0	0
6	0	1	1	2	0	0	0	0
8	0	1	1	2	0	1	0	1
10	0	1	1	2	0	1	0	1
12	0	1	1	2	0	1	1	1

Table 10. Percentage of zaps causing glitches as reported by the glitch detector after discharges to (i) a signal trace (ZAPIO1) without and with TVS, (ii) USB shield (i.e. board ground), and (iii) HCP. The test board was battery-operated. The discharge location is listed in the top row of the table.

IEC level (kV)	ZAPIO1 w/o TVS	ZAPIO1 w/ TVS	USB Shield	HCP
-12	NA	0%	0%	80%
-10	NA	0%	0%	0%
-8	NA	0%	0%	0%
-6	NA	0%	0%	0%
-4	100%	0%	0%	0%
-2	8%	0%	0%	0%
2	83%	0%	0%	0%
4	100%	0%	0%	0%
6	NA	0%	0%	0%
8	NA	0%	0%	0%
10	NA	0%	0%	0%
12	NA	0%	0%	0%

margin, and thus care should be taken in extrapolating these findings to lower-voltage IO and/or those without Schmitt trigger or other noise rejection circuits. Evidence that concern is warranted is provided by a glitch detector circuit that was placed in a 1.5 V IO cell that did not contain any noise rejection circuitry, e.g. Schmitt Trigger (LVGDIO in Figure 11).

Zaps to other IOs (with or without TVS protection), the USB shield, and the HCP all consistently produced glitches at LVGDIO once the precharge level reached ±2 kV.

VI. Simulation

It is worthwhile to consider whether supply noise could have been predicted accurately by circuit simulation rather than needing to include circuitry on-chip to measure the ESD-induced supply noise. A netlist is constructed to simulate the effect of IEC zaps to the battery-operated board, with the zap points being either ZAPIO1 or ZAPIO4. A conceptual view of the netlist is shown in Figure 13. The netlist includes models of the ESD gun, the on-chip ESD protection in the IO cells, the on-chip ESD protection between supply and ground nets, the anti-parallel diodes (APD) between isolated ground busses, the package RLC parasitics, the on- and off-chip decoupling capacitors (decaps), and the supply voltage monitor circuits. The extracted bus resistances of the on-chip power distribution network are also included. The ESD gun model is based on the one described in [7] but the parameters are modified to generate a current pulse whose rise-time, amplitude and duration match those measured at the gun tip by an F-65A current probe when a signal line is zapped and the board is battery-operated. The netlist does not include models of the signal traces on-board. The models of the on-chip ESD protection devices are suitable for the high current level simulation. The models of the off-chip decaps include estimated ESR and ESL [8] as well as the trace inductances connecting them to the power planes.

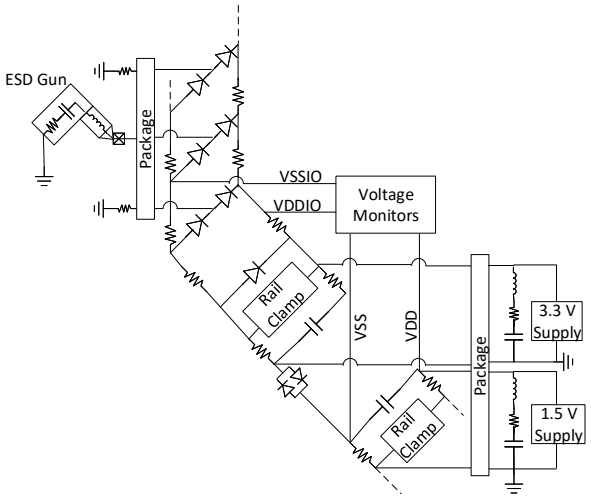
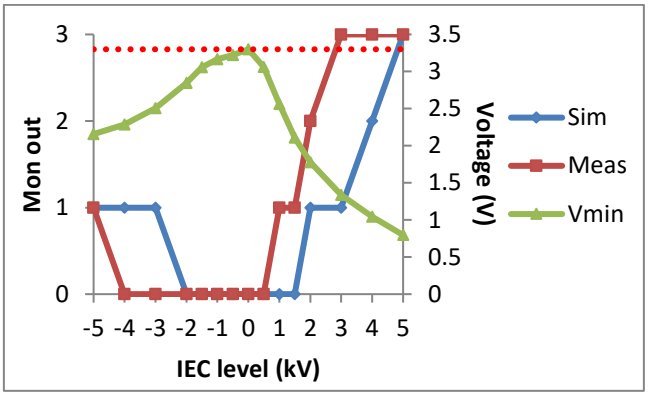
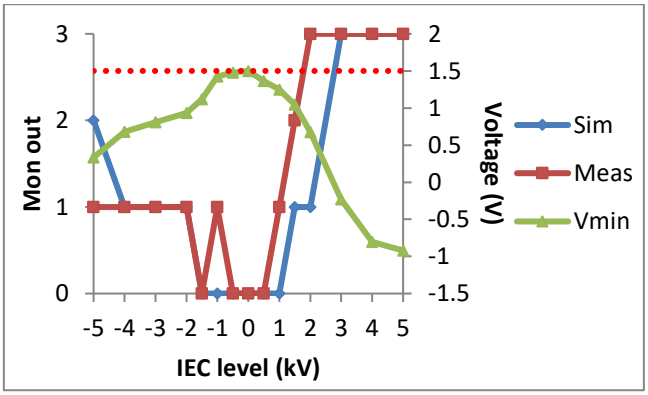


Figure 13. Conceptual view of the netlist used to simulate the response of the voltage monitors during system-level ESD. An RLC package model is used based on the geometry of the bond wires.

Figure 14 and Figure 15 show the simulated outputs of the under-voltage monitors following IEC zaps to ZAPIO1 and ZAPIO4, respectively. The value of the supply voltage at the peak of the disturbance is also included on the plots. Consistent with the measurement results, simulation predicts that positive ESD zaps cause larger supply voltage excursions than do negative zaps. Simulation also predicts that the monitor output will be larger if the zap pin is close to the voltage monitor circuit, i.e., it predicts that zaps to ZAPIO1 will cause the monitor to detect a larger noise voltage than will zaps to ZAPIO4; this too is consistent with the measurement results.



(a)



(b)

Figure 14. Simulated (in blue) and measured (in red) output levels of (a) HVUV, and (b) LVUV after IEC zaps at ZAPIO1. The minimum voltage on the corresponding on-chip supply is shown in green. The normal VDDIO or VDD voltage is indicated by a dashed line.

However, there is not complete agreement between the simulated and measured values of the monitors' outputs. These discrepancies are attributed to imperfect representations of the ESD tester, PCB and IC package in the simulation model. In particular, the model does not accurately capture the magnetic coupling between adjacent traces or between neighboring bond wires. Magnetic coupling induces current in the opposite direction at IOs that neighbor the zapped IO, resulting in the neighboring IOs providing additional return paths for the ESD current. Similarly, magnetic coupling between the bond wire of the zapped IO and

that connected to a power or ground pin alters the impedance of the current return path through the power distribution network (PDN). In short, magnetic coupling affects the distribution of ESD current between the VDDIO, VSSIO, VDD and VSS nets on-chip and it is these currents that cause the supply voltage fluctuations [5].

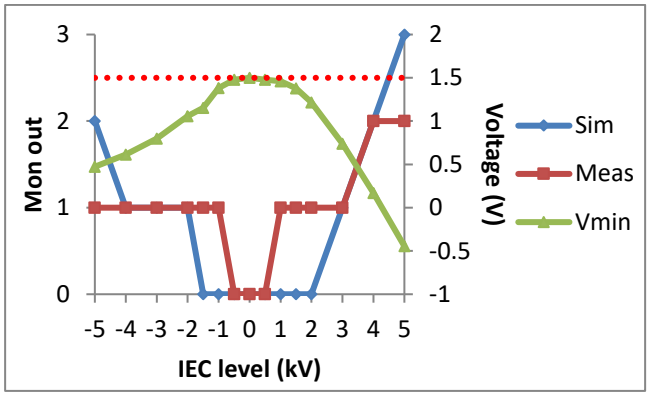


Figure 15 Simulated (in blue) and measured (in red) output levels of LVUV after IEC zaps at ZAPIO4. The minimum voltage on VDD is shown in green and the normal supply voltage is indicated by the dashed line.

Given the qualitative agreement between simulation and measurement, simulation may be used to further understand the measurement results or to formulate design guidelines. Simulation indicates that the under- and over-voltage transients are caused by there being unequal induced voltages on the supply and ground bond wires [3]. The large supply voltage transients are at the chip-level; the on-board decaps enable the on-board supply voltage to stay relatively quiet. Simulation indicates that the fluctuations of the "core" (low-voltage) on-chip supply voltage does not have a strong dependence on the type of ESD protection at the IO (i.e., dual diodes or local clamp). This prediction is consistent with the LVOV and LVUV measurement results in Table 5.

The rail clamp used on this test chip turns on quickly and has low on-resistance during power-on ESD, thereby limiting the amplitude of the over-voltage transients. This is not clearly visible from the voltage monitor output data since the OV monitors have low trigger thresholds; however, it is evident in simulation. This finding confirms the importance of using a rail clamp that is specifically intended for power-on ESD protection.

VII. Conclusion

A variety of supply noise monitors were demonstrated on a 130-nm test chip. Measurement results show that system-level ESD globally affects the on-chip supply, albeit with polarity and location dependencies. Supply noise is produced by conducted ESD currents within the system, and also by radiation from electrostatic discharges occurring near the system.

Positive discharges to IO pins create larger amplitude noise on the IO circuits' power supply than do negative discharges. Discharges to IO pins also induce significant supply noise in a separated power domain on-chip, i.e., a supply that is isolated from the supply that powers the IO circuit. The characteristics of ESD-induced on-chip supply noise can be predicted reasonably well using circuit simulation but the quantitative agreement with measurement is imperfect.

Although contact discharge into a signal trace that is not protected by TVS was observed to cause supply fluctuations measured in hundreds of millivolts and even volts, digital circuits were observed to be fairly robust against the noise.

Bit flips were shown to occur within sequential logic at very low ESD levels. Those upsets were the result of glitches at input pins. Low voltage IOs without Schmitt triggers or other filters, e.g. those used for high-speed data transmission, may remain sensitive to the residual ESD noise even if TVS are used.

Acknowledgements

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