Novel SCR structure for power supply protection in FinFET technology

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Abstract - A FinFET SCR embedded ESD clamp for power supply protection with low leakage current is demonstrated. The proposed clamp is suitable for low power applications since it reduces ~87% of leakage current per bigFET width and improves ESD robustness to ~2X per footprint compared to the conventional RC-triggered clamp.

I. Introduction

While the CMOS field-effect transistors (FETs) are keeping downscaling to sub-20nm or beyond, it's not possible to use the conventional planar FETs for the poor short channel effect (SCE). In improving the on-off current ratio and lowering the power consumption, FinFETs with higher gate control capability which can reduce the SCE and leakage current are widely employed instead [1]. However, owing to a smaller effective silicon volume for thermal dissipation, a FinFET device is usually more vulnerable to electrostatic discharge (ESD) than a planar one. The requisition of ESD protection with great robustness to protect the internal circuits becomes more important especially in FinFET technology.

Silicon Controlled Rectifiers (SCRs) have been widely used for its excellent capability to sink high current under ESD events in cross technology nodes [2,3]. This is highly attributed to the regenerative feedback and double-current injection mechanism during ESD events that make an SCR more robust than other mainly used ESD device, e.g. GGNMOS and diodes.

A novel SCR is proposed and realized in 3D FinFET process in this paper. By embedding a P+/Nwell diode in a conventional RC-triggered power clamp (shown in Figure 1), this so-called Power-Clamp-Triggered SCR (PTSCR) shows low dynamicon-resistance. TCAD / SPICE simulation, Human Body Model / Transmission Lin Pulse (HBM/TLP) and very fast TLP (VFTLP) were performed to further analysis this proposed PTSCR. With this novel PTSCR, the ESD robustness is enhanced while the layout footprint is reduced.

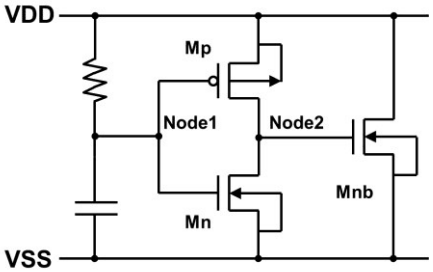


Figure 1: Schematic of a conventional RC-triggered power clamp.

II. Proposed Structure

Silicon Controlled Rectifiers (SCRs) with high ESD robustness and low capacitance are generally used as ESD protection for high-speed circuits. However, large voltage overshoot caused by slow turn-on speed of SCRs can cause damage to the internal circuits in a fast-transient Charged Device Model (CDM) event [4,5]. SCRs usually have snapback behavior and higher trigger voltage during ESD events, which narrows the ESD design window [6,7]. Also, the low holding voltage of SCRs which is lower than the supply voltage would keep SCRs in high conductive state after external noise triggers SCRs under normal operation conditions. This leads to unwanted power consumption. Several approaches are reported, such as tuning the trigger voltage and

holding voltage by adjusting the layout style and the stage of parasitic devices [8]. In this paper, an RC-triggered SCR device [9,10] without snapback behavior during ESD events is reported to gain the ESD design window. In this approach, since the RC circuit turns on the diode-NMOS series, the SCR can be triggered in a faster way as the substrate current is increased.

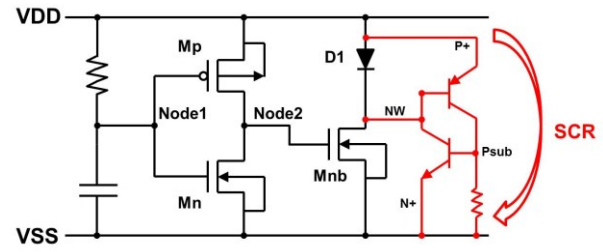


Figure 2: Schematic of the proposed PTSCR in FinFET technology.

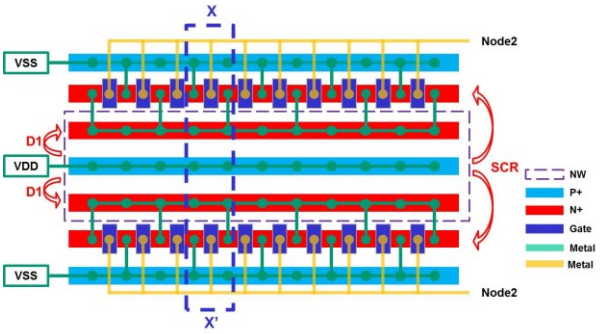
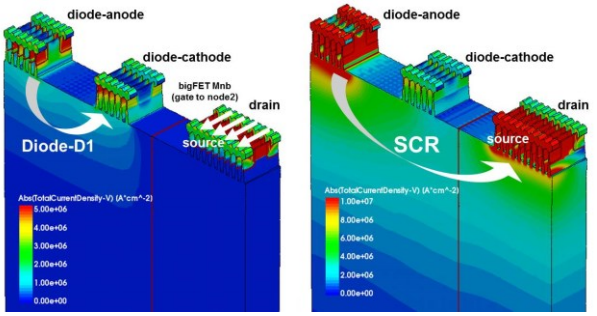


Figure 3: Layout top view of the proposed PTSCR. (The trigger circuit is not shown.)

The schematic of the proposed PTSCR is illustrated in Figure 2. It consists of an RC-timer (a metal resistor and a NMOS capacitor), an inverter consisting of a PMOSFET Mp and a NMOSFET Mn, a P+/Nwell diode D1 and a big NMOSFET (big FET) Mnb. The top view of the proposed structure is presented in Figure 3, which is just for illustration and not drawn to scale. By embedding a P+/Nwell diode D1 in a conventional RC power clamp, the anode P+ diffusion region/Nwell of diode D1 and the Psub/N+ diffusion region on the source side of the big FET Mnb form a "P+/Nwell/Psub/N+" SCR path.



(a) (b)

Figure 4: 3D-TCAD simulation results of the proposed PTSCR before (a) and after (b) SRC's turn on with 1ns VFTLP pulse stress. (X-X' in Figure 3.)

An 3D-TCAD VFTLP simulation is performed to further analyze the turn-on mechanism of this proposed PTSCR in Figure 4. The power clamp in this structure is enabled during fast-edge ESD events and disabled during power-up or normal operation by the RC-timer in Figure 2. During ESD zapping from VDD to VSS, node1 is coupled to ground with help of the RC-timer. Node2 thus is pulled up to high voltage potential by the PMOSFET Mp while the NMOSFET Mn turns off. As a result, the big FET Mnb turns on when the voltage at node2 is higher than the threshold voltage Vth. In Figure 4 (a), the ESD current is firstly injected from VDD pad into the diode D1, flows into the big FET Mnb through metal

Table 1. Differences between a conventional RC power clamp and the proposed PTSCR.

Characteristics	**RC power clamp**	**Power clamp triggered SCR (PTSCR)**
Leakage path	Single stage NMOS	Single stage diode + single stage NMOS in series
Operation during ESD events	RC inverter drives the big NMOSFET	1. RC inverter drives the big NMOSFET 2. Both the diode and big NMOSFET in series are on 3. Voltage potential Vbe is built in the diode as well as the P+/NW/Psub 4. The underlying P+/NW/Psub/N+ SCR is triggered
Main ESD current path	NMOS channel	Underlying P+/NW/Psub/N+ SCR

connection, then both D1 and Mnb are turned on. In Figure 4 (b), as the ESD current flows through the diode-bigFET series (D1-Mnb), triggering of the inherent P+/Nwell/Psub/N+ SCR is accomplished by forward biasing the junction of P+/Nwell diode D1 as well as the emitter-base junction of the P+/Nwell/Psub. The operation differences between a conventional RC power clamp and the proposed PTSCR are listed in Table -1.

III. Leakage Benchmark

The PTSCR test structure is designed with big FET total width around 567um and fabricated in FinFET technology. An RC power clamp with big FET width around 1200um is used to make comparison. The PTSCR and RC power clamp share the same RC trigger circuit (RC-inverter). The layout footprint of the RC power clamp is about 1640um^2 while that of the PTSCR is 1345um^2, which is only 82% layout footprint of the RC power clamp due to layout constrain.

To cover all possible ranges of DC application, SPICE simulations are completed in both typical-typical (TT) corner at room temperature 25°C and fast-fast (FF) corner at high temperature 125°C. Table 2 summarized the leakage current normalized to the big FET total width at DC voltage=1V. Note that an SCR is not included in the SPICE model, due to the negligible leakage current of the reverse-biased Psub/NW in normal operating conditions. Since the total width of the inverter in the trigger circuit is less than 10um, leakage contribution of the RC-trigger circuit is negligible compared to the diode-big FET series. On the other hand, the total width of the big FET in the PTSCR is about half of that in the RC power clamp while the leakage current is reduced 96.35% rather than 50% in the FF corner. So the leakage reduction can be mainly attributed to the stacking of the diode and big FET. ‘

Table 2. SPICE simulation of the normalized DC leakage current at 1V, for both TT corner, 25°C and FF corner, 125°C.

Normalized leakage (a.u.)	TT corner, 25°C	FF corner, 125°C
PTSCR	1.54E-09	2.49E-06
RC power clamp	9.93E-06	6.82E-05
Leakage reduction	99.84%	96.35%

IV. Experimental Results

A. DC testing

DC test result of the PTSCR is shown in Figure 5, in which the DC current is normalized to the big FET width. Table 3 presents the measured and simulated DC leakage currents results at DC voltage=1V. The 87% reduction of DC leakage currents guarantees the lower power consumption of the proposed PTSCR. Additionally, the experimental result is covered in the range between TT and FF corner in 25°C.

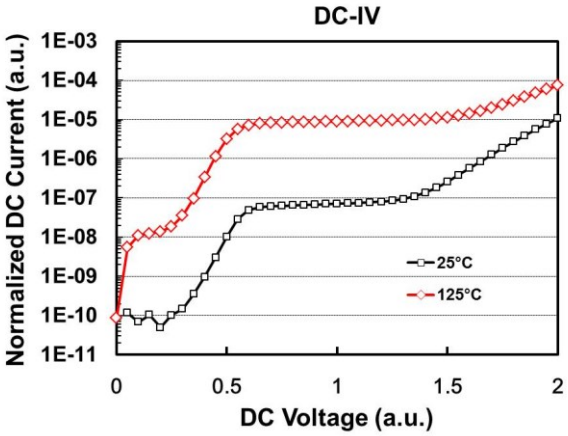


Figure 5: DC test results of the proposed PTSCR under room temperature 25°C and high temperature 125°C.

Table 3. Improvement of the normalized DC leakage current at 1V, 25°C in both SPICE simulation and experiment.

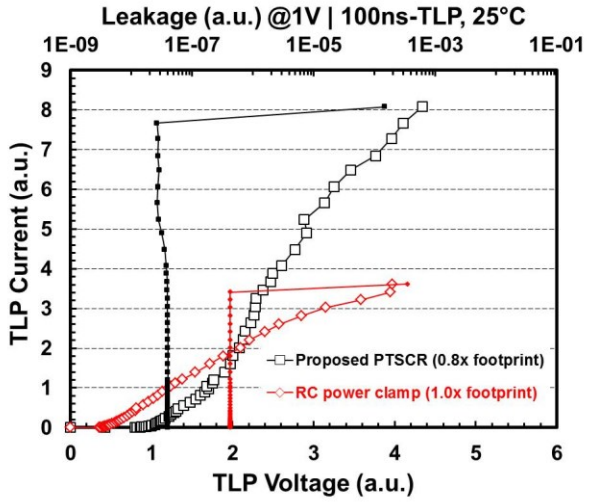
Normalized leakage (a.u.)	Simulation	Experiment
PTSCR	1.54E-09	7.05E-08
RC power clamp	9.93E-06	5.69E-07
Leakage reduction	99.84%	87.61%

B. Device Level ESD Testing

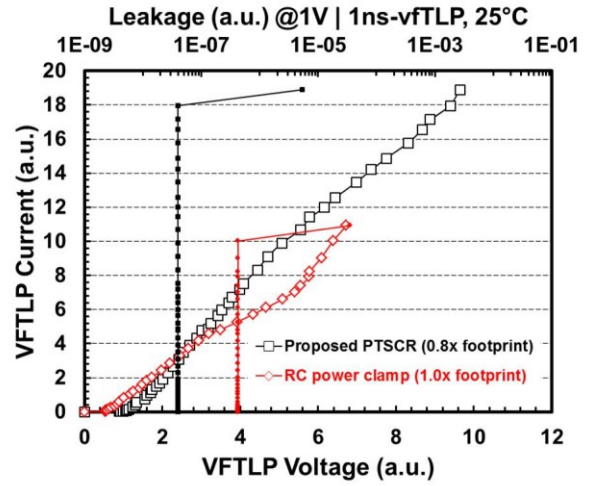
The turn-on behavior during ESD events and the secondary breakdown current (It2) of the PTSCR is evaluated by a transmission line pulsing (TLP) system (Hanwa HED T5000) with 10-ns rise time and 100-ns pulse width. As shown in Figure 6 (a), the TLP-measured It2 of the PTSCR is 7.66a.u., which is more than twice that of the conventional RC power clamp (3.41a.u.).

Fast-edge transient behavior in the time domain of the charged-device-model (CDM) ESD events is also captured by another very fast TLP (VF-TLP) system (Hanwa HED T5000, also) with 0.2ns rise

time and 1ns pulse width. In Figure 6 (b), the VFTLP-measured It2 of the PTSCR is 17.95a.u. while the conventional RC power clamp is about 10.04a.u. Note that the layout area of the PTSCR is only about 82% of the conventional one. Based on these experimental results, the proposed PTSCR is successfully verified to perform fast turn-on during the CDM events.



(a)



(b)

Figure 6: TLP-measured results of the proposed PTSCR under (a)100ns-TLP and (b) 1ns-VFTLP compared with RC power clamp.

The VFTLP turn-on waveforms of which the VFTLP overshooting voltage is around 7a.u. are shown in Figure 7 for both the PTSCR and RC power clamp. In the waveform of the PTSCR, the full width at half maximum of the voltage overshoot is approximately 0.4ns, which implies the time needed for the PTSCR to be triggered on and a plateau (0.6ns~1ns) follows, as the VFTLP voltage is clamped by the turned-on PTSCR. The clamping voltage of the PTSCR (0.6ns~1ns) is about 2a.u. lower than that of the conventional RC power clamp, which indicates that the SCR is effectively turned on with lower dynamic on-resistance.

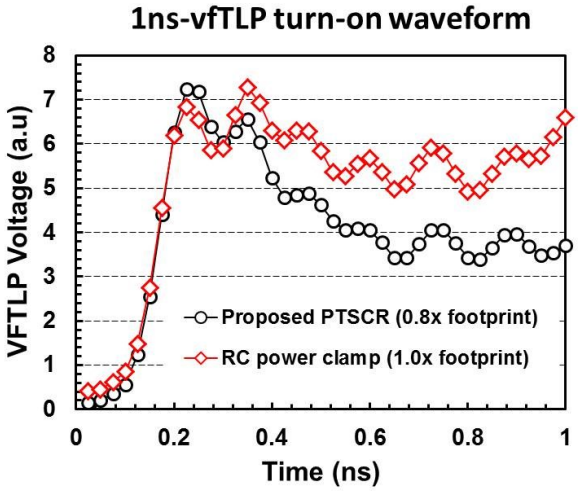


Figure 7: 1ns-VFTLP voltage waveform of the proposed PTSCR compared to the RC power clamp with the same overshooting voltage.

Also, the HBM level was captured by Hanwa HED W5100D ESD tester for comparison. Table 4 presents the ESD capability of the RC power clamp and PTSCR. It shows that the PTSCR with smaller footprint (0.8x) has higher HBM level, TLP and VFTLP It2 per layout footprint, which are larger than two times that of the conventional RC power clamp.

Table 4. ESD robustness comparison of the RC power clamp (1x footprint) and the PTSCR (0.8x footprint).

ESD capability	RC power clamp	Proposed PTSCR
HBM (kV)	5kV	≥10kV
TLP It2 per footprint (a.u.)	1.00	2.81
VFTLP It2 per footprint (a.u.)	1.00	2.23

Table 5 shows the comparison results of the TLP It2 per layout footprint between this work and the referred literatures [11-13], which are all RC power clamps. The PTSCR represents the highest result (6.06a.u.) with large silicon volume for heat dissipation, while the RC power clamps sink the ESD current by channel.

Table 5. Comparison results of the normalized TLP It2 per layout footprint between this work and the prior arts.

Reference	ESD current path	Normalized TLP It2 (a.u.)
This work	BigFET with SCR	6.06
[11]	Big FET	1.00
[12]	Big FET	1.59
[13]	Big FET	2.26

V. Discussion

A. Inrush current simulation

Inrush current is one of the key parameters for RC-triggered ESD clamp. In real chip applications, for example, in Figure 1, as the power bus voltage is ramped up from ground to VDD, the PMOS Mp of the inverter turns off while the NMOS Mn turns on. However, the sub-threshold leakage of the PMOS Mp charges the gate of the big FET Mnb during this ramp-up period, which leads to the inrush current.

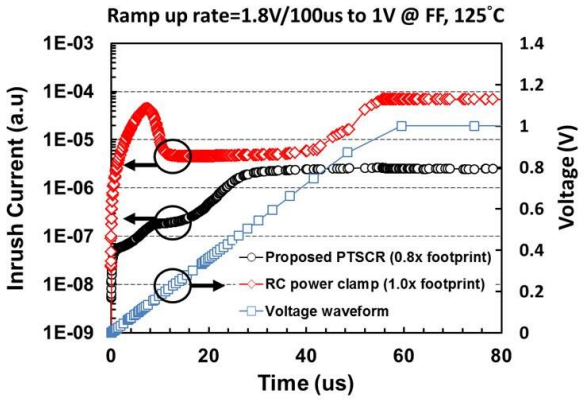


Figure 8: Inrush current estimation with SPICE of the proposed PTSCR compared to the conventional RC power clamp in FF corner, 125°C.

The inrush current comparison via SPICE simulation of the proposed PTSCR to the RC power clamp is shown in Figure 8. A common ramp-up rate 1.8V/100us is used while the power is ramped up from ground to 1V. In this case, the peak current of the RC power clamp occurs on 7.5us, which is 4.46E-5 a.u. If the RC trigger circuit is not well designed, this peak current might be much greater than the stable leakage. In contrast to the RC power clamp, the inrush current is not an issue for the proposed PTSCR. The inrush current is suppressed due to the higher turn-on voltage of the diode-big FET series in this DC ramp-up condition. Also, the leakage of the proposed PTSCR is lower than that of the RC power clamp as the voltage is ramped up to 1V, which corresponds to the aforementioned SPICE simulation and DC experiment.

B. Holding voltage enhancement

The holding voltage is always the key item to be considered to keep SCR based ESD devices from latchup in normal operating condition. To ensure the reliability of this proposed PTSCR, the holding voltage should never be lower than the power supply voltage.

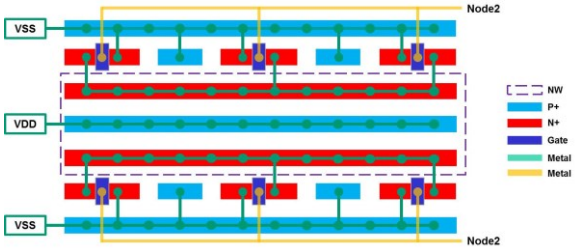


Figure 9: Layout top view of the modified PTSCR with P+ pickup dots inserted. (The trigger circuit is not shown.)

Figure 9 shows the PTSCR layout top view with P+ pickup dots inserted in the NMOS (Mnb in Figure 2.) and tied to ground to lower the substrate resistance for higher SCR holding voltage. The layout top view is just for illustration and not drawn to scale. Several PTSCR testing patterns with different pickup dot densities, i.e., the ratio of the total P+ pickup dot area over the total N+/P+ active area in the NMOS, ranging from 0% to 11.7% are designed and fabricated.

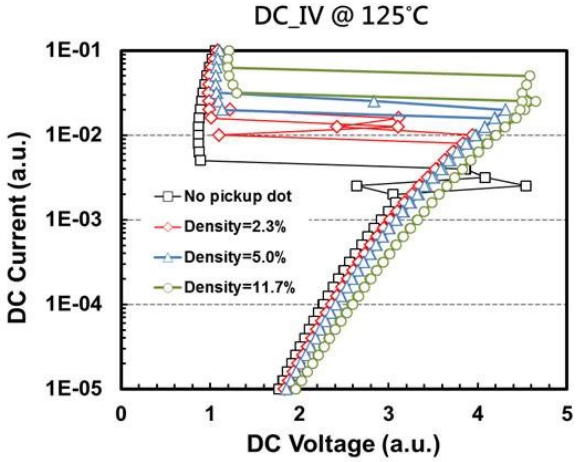


Figure 10: Snapback-DC-IV curves of the modified PTSCRs with different pickup dot densities.

DC test results of these testing patterns with different pickup dot densities at high temperature 125°C are shown in Figure 10, respectively. This measurement is completed with Agilent 4156C by forcing current to sense the voltage. The holding voltage of the PTSCR is improved from 0.87a.u. to 1.2a.u., which is greater than VDD=1V. for low power application by increasing the pickup dot density from 0% to 11.7%. Note that as the cathode area of the PTSCR is reduced from 100% to 88.3%, the dynamic on-resistance is slightly degraded but still comparable to that of the RC power clamp. Also, the high VFTLP It2 is still kept, which is 50% higher than that of the RC power clamp.

VI. Conclusion

A novel SCR with high ESD robustness for power supply protection is realized in FinFET technology. By embedding a P+/Nwell diode in an RC-triggered power clamp, the PTSCR is triggered by diode injection as soon as the RC circuit detects the ESD signal and turns on the diode-NMOS series. This trigger mechanism results in a non-snapback characteristic directly.

Experimental results show that the PTSCR has much lower DC leakage current and higher ESD protection capability compared with the conventional RC-triggered power clamp. As compared to RC power clamp, 87% reduction of DC leakage current is achieved and a two times normalized TLP It2 is observed. To prevent latchup, holding voltage enhancement is also achieved by inserting pickup dots in the PTSCR for low power application.

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