EDA Checker for Identification of Excessive ESD Voltage Drop – Implementation to Smart Power IC's

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Abstract - A customized checker able to calculate HBM voltage drop and to identify product circuitry prone to excessive over voltages is ideated, implemented, and successfully applied to Smart Power products. This checker is conceived as part of a complete verification flow covering all main aspects of IC designs ESD compliance.

I. Introduction

Electronic Design Automation (EDA) addressed to ESD design verification becomes more and more common nowadays in the IC's world, and it is increasingly covering many ESD requirements [1]. It is crucial to reach, during an ESD checking flow of a design, a beneficial trade-off between a sufficient verification coverage, short run-times, as well as straightforward use of the EDA tools. This is the main reason why, although valid commercial ESD tools currently on the market are able to satisfy many verification aspects, further efforts should be dedicated to build tailored checking solutions tuned to meet the aforementioned trade-off.

During the accumulation of our experience in building an ESD EDA verification kit customizing Calibre® PERC™ tools suite [2], we went through various phases. The primary need was to check the protection network and IO protected stages ESD compliance from topological and parametric viewpoints [3]. Later on we added the control of the maximum ESD current densities (CD) and verification of parasitic resistance along ESD interconnections [4]. Finally, to conclude the ESD verification process, it is now essential to identify and estimate the voltage drop (V_{DR}) developed by the ESD protection network at each pin-pair combination and to verify that this value is sustainable by the protected stages in the IC.

In the present work, the ideation of this functional checker is presented. This investigation is especially challenging in Analog designs, where I/O protected circuitry is extremely customized, depending on the application requirements, and thus not known a priori (not General Purpose IO library approach). The main feature of our check solution is an advantageous trade-off among accuracy, implementation ease, and run time.

The following sections describe the work as follows: Section II introduces the ESD V_{DR} problem. The developed checker is described in Section III. In Section IV we explain how this ESD checker is integrated in our whole verification flow. Section V shows the checker application to two Smart Power BCD IC's. Finally we conclude in section VI.

II. The ESD V_{DR} Problem

An ESD protection network can be considered suitable if it contemporarily fulfills the requirements of self-robustness, effectiveness, and speed during the ESD stress, together with transparency in operating conditions. Let's focus on effectiveness, which means the ESD network ability to prevent the protected circuitry from failing during the ESD event. Once pin

A is stressed by an ESD event while pin B is shorted to ground, the corresponding protection network activates and shunts the whole or part of the ESD current from A to B (see Figure 1). Obviously, several protection paths may be present between A and B, which are contemporarily triggered in parallel; therefore the ESD current distributes among them in weighted portions. While shunting the ESD discharge, the resulting protection network develops a certain global V_{DR} between pins A and B, equals to the sum of all the V_{DRs} contributors (ESD diodes, ESD clamps and metal interconnects). An effective protection network should be able to avoid excessive current density into interconnections and to limit the global V_{DR} to a safe value such that the protected blocks in parallel do not fail by overvoltage (in on-state or off-state). While the control of the maximum current densities flowing in metal lines during the ESD event has been already successfully developed [4], an effective control of possible over-voltages is still missing. Compliance to a safe bias condition when the ESD is applied can be verified by evaluating the effective V_{DR} developed by the protection network and by comparing it with the maximum voltage sustainable by any parallel protected stage without failing. For any protected device the HBM Maximum Stress Voltage (MSV) can be defined as the highest voltage not causing any irreversible degradation.

Anytime V_{DR} > MSV, the safe condition is violated reflecting a possible weakness. This effectiveness control is pretty challenging, since it requires an accurate evaluation of V_{DR} value developed by the ESD network and a deep knowledge of the protected circuitry, topology, and features. The ideated way to develop this checker is described in next sections.

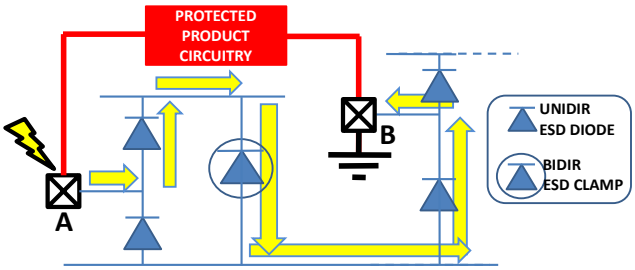


Figure 1: Protection Network Activation during ESD

III. ESD V_{DR} Verification Method

During normal operation of a product all the internal nodes voltage levels are well defined. On the other hand, under ESD stress the whole circuit biasing state depends on the pins-pair combination involved in the stress (e.g. supply pins may be either grounded or left floating in specific pin stress combinations). For this reason the existing static commercial tools are unsuitable to cover the V_{DR} aspect, as they typically consider well defined bias states (e.g. Vcc=5V in all operating conditions) and a strong customization is needed. This fact led the development of our V_{DR} checker.

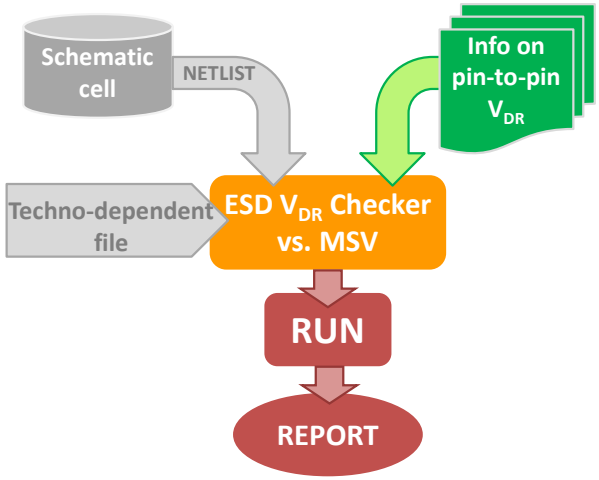


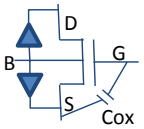
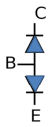
Figure 2: ESD V_{DR} Checker – Verification Flowchart

The custom V_{DR} flow utilizes the engine and features provided by Calibre® PERC™ (statements, commands, environment and graphical interfaces). The main elements featured by our verification method are illustrated in Figure 2. The various items are explained in next sub-sections.

1. Techno-Dependent File

This file contains information specific to the involved technology. The technology information is written in an editable excel file, automatically converted to a .txt (tab delimited) file. The .txt file is finally interpreted by the engine as SVRF (Standard Verification Rule Format) language. The file contains information on the ESD protection devices, the protected components (MOSFETs, bipolar transistors, diodes, and capacitors), the names of all the terminals of each protected component, and the MSV value between each pair of terminals (see Table 1).

Table 1: Techno-Dependent File Information – MSV's of the Protected Circuitry Components

NMOS (dual for PMOS)	NPN (dual for PNP)	diode	capacitor
			
MSV_{GS} MSV_{DS} MSV_{SD} MSV_{DB} MSV_{BS} MSV_{SB} MSV_{BD}	MSV_{BE} MSV_{EB} MSV_{BC} MSV_{CB}	MSV_{AK} MSV_{KA}	$MSV_{PLUS/MINUS}$

Each MSV value is derived from specific characterizations described in this section. Particularly explicative is the extrapolation of the MSV_{DS} value for a specific NMOS: this value is extracted from standard 100ns Transmission Line Pulse (TLP, 2ns rise time, 100ns duration) characterizations, keeping S shorted to ground and biasing G to a constant voltage value [5]. The measured I_{DS} curves are shown in dependence of V_{DS}. Each curve is obtained with a fixed V_{GS} (see the representative example in Figure 3). Plotting these curves allows the extraction of the $MSV_{DS}(Vg)$ values. In fact a Safe Operating Area (SOA) can be identified, constituted by (V_{DS}, I_{DS}) values sustainable by the MOS without failing for each different V_{GS} biasing. This area is delimited by a curve (dashed red) obtained from interpolation of (V_{DSMAX}, I_{DSMAX}) points, being (V_{DSMAX}, I_{DSMAX}) the maximum voltage and current sustained by the MOS without failing. Since, during our V_{DR} check, there is no information about the biasing state of the protected MOS (turned-off – V_{GS}=0 –, or biased at a certain V_{GS}>0), the worst case must be considered, i.e. the one corresponding to the V_{GS} with the lowest V_{DSMAX} value. The lowest V_{DSMAX} is identified as the specific MOS MSV_{DS} and included in the techno-file.

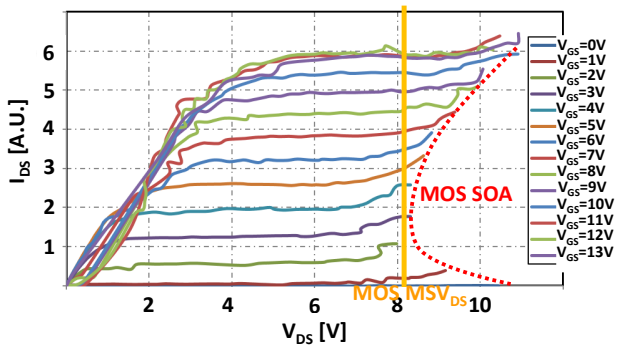


Figure 3: SOA TLP I_{DS}-V_{DS} Curves of a Low Voltage NMOS

All the MSV values of Table 1 are extracted through similar TLP characterizations together with the collection and processing/elaboration of various technology data.

MSV_{GS} value, the maximum voltage for which the oxide is not damaged, is derived in the following way: the MOS gate-oxide is stressed with TLP pulses on G while connecting S terminal to ground. For voltages higher than MSV_{GS}, failures characterized by oxide degradation are then observed by increase of G-S current leakage. Analogous considerations and extracted limits are also valid for capacitors, featuring the same MOS gate oxide. Similarly to NMOS, MSV values of PMOSs devices are also obtained applying the proper voltage bias to the test-structures, adopting similar failure criteria.

TLP characterizations are used also to extract diodes MSV_{AK} values: dedicated test-structures are stressed in forward mode to identify the maximum current and voltage levels leading to device destruction. MSV_{KA} value is derived by analogous TLP characterizations performed stressing the diode in reverse mode up to its failure. The same approach is implemented to define MSV values for all Body/Drain and Body/Source diodes (DB, BD, SB, BS) inside MOS transistors.

Finally, for the specific case of bipolar transistors, the SOA limits are defined according to the lowest breakdown values (Base/Emitter, Base/Collector) measured in DC and pulsed conditions.

To summarize, MSV values can be related to different device working modes: forward-biased pn junction, reverse-biased pn junction, MOSFET channel conduction, and oxide voltage capability. Therefore MSV value identifies the maximum ESD voltage sustained by a couple of terminals by working in any mode without damaging, not necessarily related to the current transport.

2. Pin-to-Pin V_{DR}

V_{DR} value for each ESD stressed pin-pair is the sum of all V_{DR} contributions of diodes, clamps, and metal interconnections composing the global ESD discharge path (yellow path in Figure 1). Hence, V_{DR} information should be derived from a layout database, in order to take into account also V_{DR} contributions resulting from metallization interconnections.

In our case, we found an effective way to extract this information elaborating data coming from the report of PERC Current Density (CD) Checker [4], which extracts all resistive networks for a specific HBM stress. This tool performs a static analysis on the simplified resistive network, highlighting both the local current densities and related voltage drops. In order to perform the calculations of CD and V_{DR}, the tool necessarily should be informed first about the resistance of each element composing the discharge path. Contributors of any discharge path may be either metallization layers (metals, contacts, vias) as well as ESD devices (diodes, clamps, etc.). While the resistance of each metallization layer is taken from the technology data and included as linear resistance in the initialization file, specific functions R=f(current, dimensions) are calculated from TLP measurements in which devices having various sizes are stressed at different TLP current. In the example shown in Figure

4, a HV dynamic protection (Darlington clamp [6] [7]) is measured for different widths up to the failure level, which typically occurs just after snapback (dedicated leakage measurements are anyway performed to verify potential degradation even before snapback triggering).

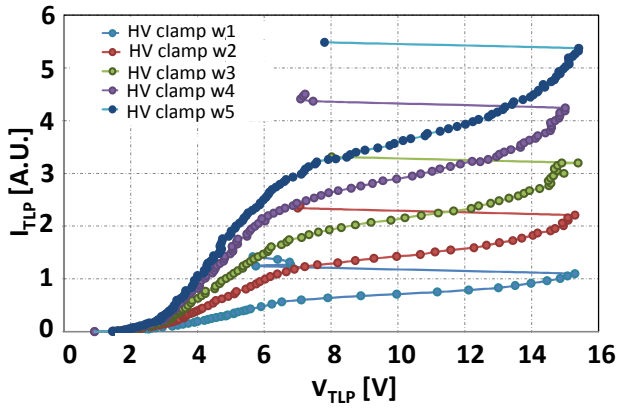


Figure 4: 100ns TLP Characterizations of HV Darlington Clamp – Different Widths Measured for Extrapolation of ESD Clamps Resistance Functions

Following collection of TLP data for different sizes and several TLP current injection levels, selected functions R=f(current,dimension) are fitted to the measurements and included in the PERC CD tool initialization file. In particular, functions corresponding to TLP pulses of 0.75A, 1.5A and 3A (correlated to 1kV, 2kV, and 4kV HBM peak currents, respectively) are extracted. Figure 5 illustrates an example of R function dependency on the width for a HV clamp, during a TLP current shunting of 1.5A.

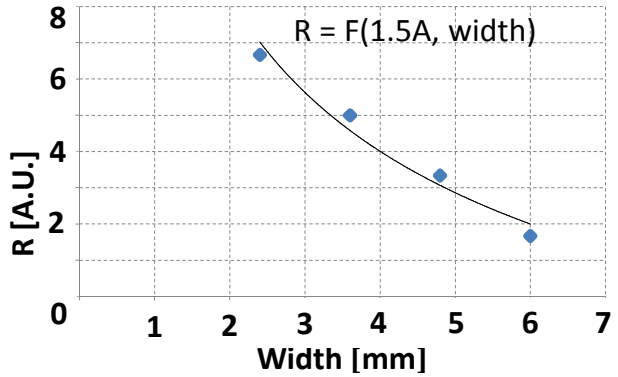


Figure 5: R Function Fit for Results of Different Widths – 1.5A Injected.

The current density limit values for metallization layers are extracted from dedicated TLP characterizations performed on properly chosen metal patterns [8].

With this methodology, the tool is equipped with all the necessary initialization information to perform the static analysis on the layout GDSII file of a design under check.

In Figure 6 an example of a colored visualization of currents in the IC, is presented: a pin-to-pin 2kV zap on a whole chip is analyzed. The color plot indicates a current range from the highest amount (warm colors) to the lowest (cold colors).

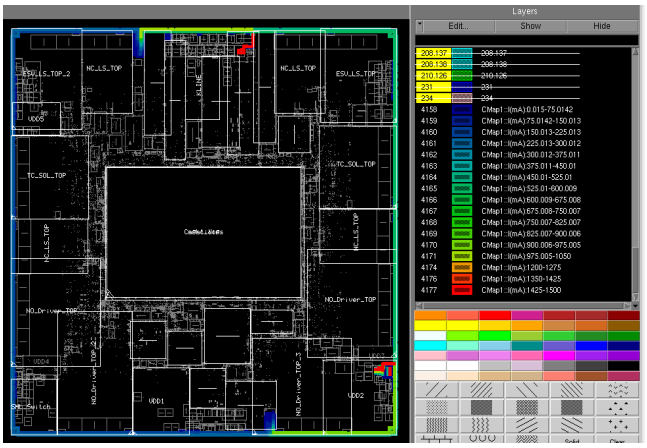


Figure 6: PERC CD – Currents Visualization on Layout View

In order to extrapolate the V_{DR} value using PERC CD tool, the following method has been implemented. For an analyzed pin pair, PERC CD:

1. Searches for all the protection paths, in parallel, between source and sink pad.
2. Divides all the found paths in polygon layers and performs a static analysis of the resistive partition composed by the equivalent resistors polygon layers.
3. Generates for each analyzed polygon (it may be a metal level or a contact or via) an output report containing a list of several physical results as reported in the following paragraph.

A simplified representation of textual output report in Calibre® RVE (Results Viewing Environment) format is shown in Figure 7. A list of the analyzed paths is given on the left. On the right, a table is shown for any path, where each line is representing several physical data corresponding to one specific polygon: calculated CD value, CD error percentage, current level, net name, layer type (metal-n, contact or via-n layer), and geometrical position. Moreover, essential information is given under the column "ΔV": the total voltage drop between each analyzed polygon and the sink pad. Therefore this column is the one containing pin-to-pin V_{DR} information. In the specific, among all ΔV values given in the column, V_{DR} is the maximum one.

Using a post-processing flow applied to the CD output report, it is possible to obtain the required input information for the V_{DR} tool. The V_{DR} values developed between any source-sink pair are calculated through automated analysis of each "ΔV" column, while the names of the source and sink pins involved in each zap are taken from the left column (see Figure 7).

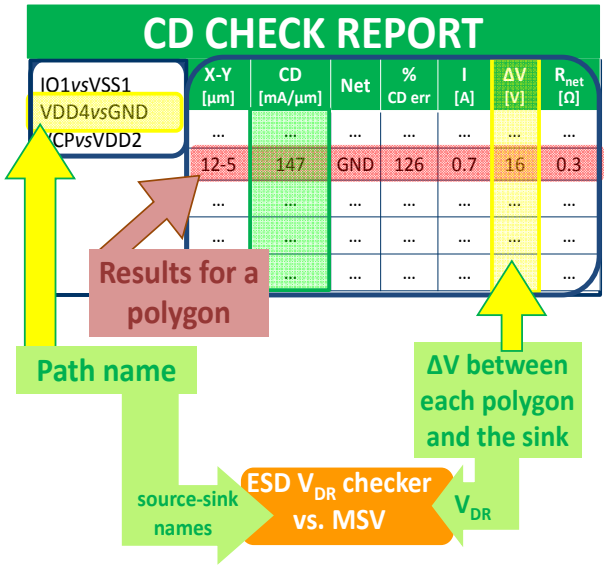


Figure 7: PERC CD Output Report containing Necessary Information for V_{DR} Tool – V_{DR} Values and Pin-pairs Names

A script is then implemented to extract and convert these data to a readable format to be then compared with the devices MSV values once the V_{DR} tool research algorithm has run.

There are alternative ways to obtain these values, such as using dynamic SPICE simulations with ESD models [9] [10] [11]. The main differences between dynamic and static approaches is the ability to observe different ESD paths vs. time triggering in parallel. The static approach may be too pessimistic in some cases; on the other hand there is a great benefit of using a commercial static tool able to run in relatively short times and having all the infrastructure for visualization on layout. In our implementation, regardless of the way the ESD V_{DR} information is achieved, the proposed V_{DR} checker is able to accept this input as long as it is provided in a simple txt file (tab delimited) format (see example in Figure 8).

```
source PVDD1    sink DIGIO1    MaxValue    10.6751
source PVDD2    sink DIGIO2    MaxValue    9.78296
source DIGIO1   sink DGND      MaxValue    10.3704
source DIGIO2   sink AVDD      MaxValue    10.6644
source AVDD     sink PVDD2     MaxValue    6.07713
source DVDD_    sink PVDD2_    MaxValue    5.02316
```

Figure 8: Input File with Pin-Pair Names and Associated V_{DR}

3. ESD VDR Checker

ESD V_{DR} checker algorithm is coded by a rule file which is written in a way it would be compatible with any technology node. It uses tcl (tool command language) which is readable by Calibre®.

Basically the checker gets source/sink pins names from the Input file of Figure 8 and, starting from source, the proposed algorithm searches for any series of protected elements connected between source and sink. In Figure 9 several examples are proposed. Whenever multiple pins devices (e.g. MOS and BJT transistors) are involved in the stressed path, the specific MSV values related to the involved pins are considered: see for example case F where Gate-to-Source MSV is considered for transistor #1 and Drain-to-Source MSV is considered for transistor #2.

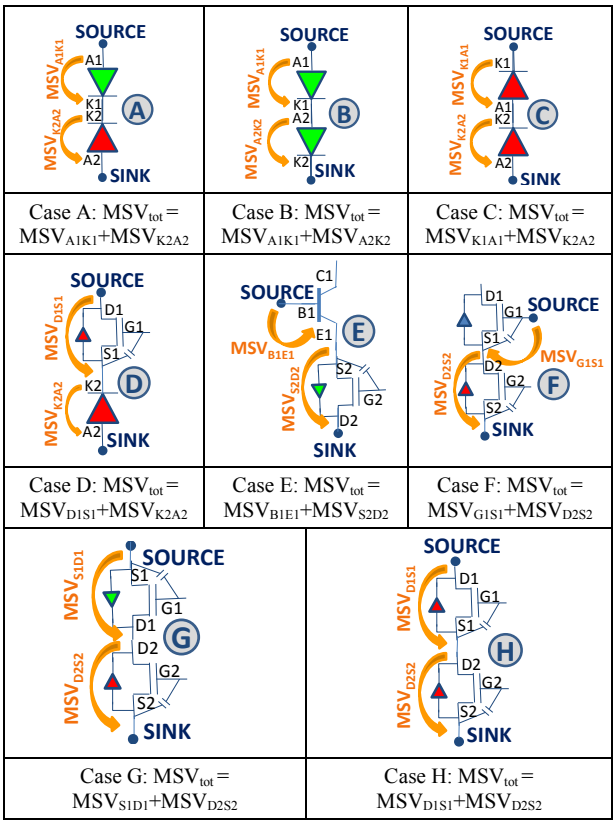


Figure 9: Some Examples of MSV_{tot} Calculation – Couples of Terminals in "Series" for Protected Circuitry

The manual check in this step ("search of protected paths") is not trivial in Analog applications since the circuitry blocks are usually not standard:

- Many different variations may exist as circuits are often customized to the specific application needs.
- Besides the general purpose IO circuits, many internal nodes may be connected to pads, either directly or through a simple switch.

The tool assigns to each identified series a total MSV (MSV_{tot}) as sum of the "series" components MSVs (see Figure 9 for MSV_{tot} calculation examples). Anytime MSV_{tot} is lower than V_{DR}, the tool outputs a violation. Figure 10 presents the studied problem and Figure 11 shows the simplified flowchart of the developed verification algorithm.

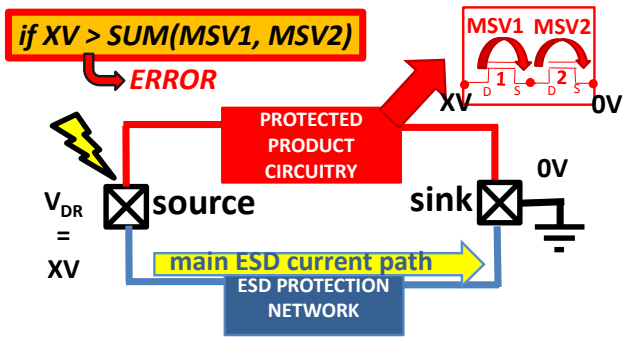


Figure 10: An Illustration of MSV Violation Condition in Protected Path Parallel to a Main ESD Current Path.

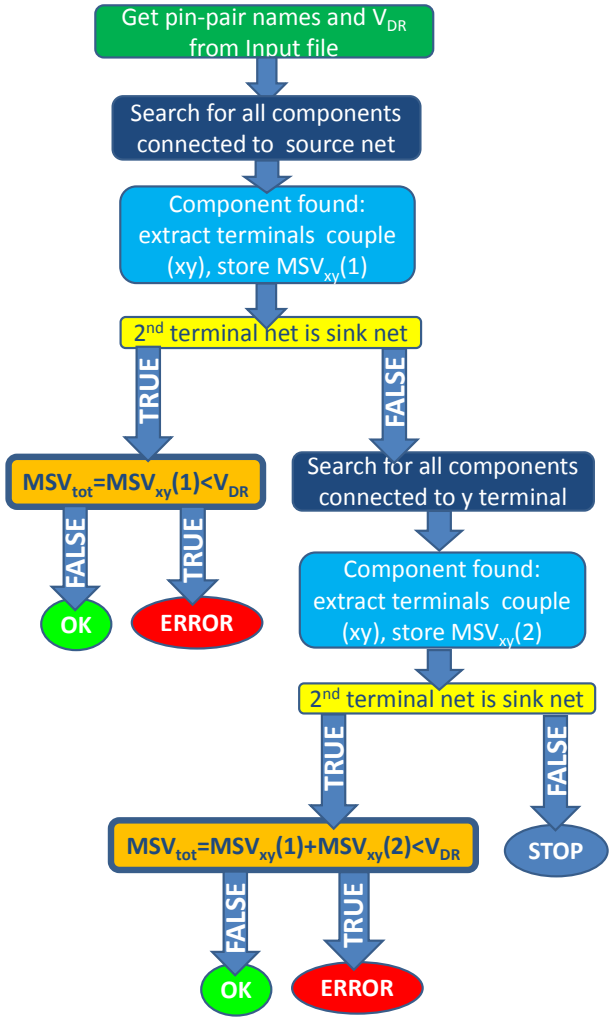


Figure 11: ESD V_{DR} Verification Flowchart – The Depicted Flow is Executed for any Found Component

Once the run is terminated, a report collecting the errors describing the weak paths found is automatically generated in RVE format (see Figure 12). Results view was customized to highlight source-sink pin pair names, ESD V_{DR} input values, and the calculated MSV_{tot} values. In addition, an option to directly probe the weak components in the schematic is given.

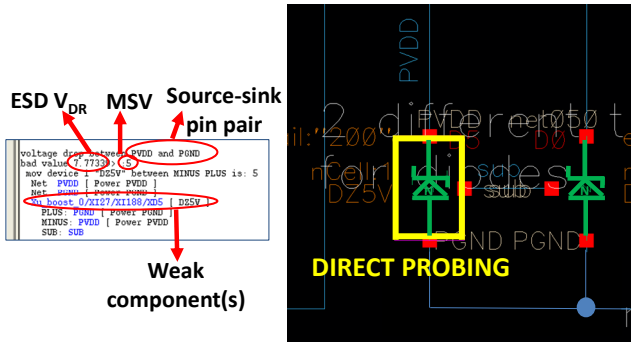


Figure 12: V_{DR} Tool – RVE Results View Format

To prevent the runtime from 'exploding', we put in place various limitations and filters in the algorithm. In specific, we chose to search for a maximum of two protected components in "series". This is due to the fact that in general, the less the number of protected components in "series" subjected to the ESD V_{DR}, the higher is the danger on each of them, since ESD V_{DR} overstress is divided among less components.

Moreover, a study on the trade-off between the ability to reveal all the paths at risk and the runtime was carried out on a 100-pins Smart Power product (see Table 2).

Table 2: Analysis of V_{DR} Tool Performances – Dependence on Maximum Number of Weak Components in Series Detected

Maximum number of detectable components in "series"	Percentage of found paths at risk	Runtime
2	90%	8 mins
3	100%	9 hours
4	100%	>2 days

The results showed that a reasonable compromise is achieved by searching paths featuring a maximum of two components in "series". In order not to limit too much the tool operating range by searching only for paths with maximum of two components in "series", and also to further speed up the code flow, we put in place some other expedients especially for resistors:

- Resistance values below a certain threshold are automatically considered as short-circuits.

- Very high resistance values are considered as open-circuits and excluded from the search algorithm.

Furthermore, some specific configurations are automatically ignored by the algorithm illustrated in Figure 11. For example all forward biased diodes with size bigger than a certain value as well as all dedicated ESD bidirectional protections (light blue devices in Figure 1) are not considered by the tool as associated with a weak path. In fact they may be the main contributors for the ESD shunting, and not weak protected components. In these cases the ESD V_{DR} value is mostly developed by these structures which themselves shunt the ESD discharge.

IV. Complete Verification Flow

The V_{DR} checker was actually developed in a much wider verification context, using Calibre® PERC™ tools suite. For this purpose, a significant customization and integration of ESD features were implemented.

After the formal verification of the ESD network and IO stages (first step in Figure 13 [3]), a check of the metal interconnections is done using PERC CD (second step [4]) and finally the V_{DR} checker assesses the global robustness of the ESD design (third step).

The strength of this flow is the extreme level of simplicity. A single input directly coming from the product datasheet is used to trigger the complete process and each tool gets automatically the required data from the previous step.

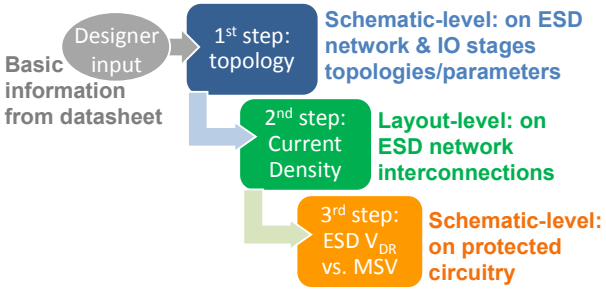


Figure 13: Complete ESD Verification Flow

For better clarity, the main checked rules and the link factors between each verification step are detailed in Table 3.

The whole verification process has been conceived in order to be run in time during the design phase.

Calibre PERC™ accepts only "clean" databases (ERC free netlists), therefore the major challenge during the design phase is to have a clean design database in order to apply the complete ESD verification flow, make potential fixes and re-run it. We adopted an efficient approach addressed to apply a complete verification flow composed of three steps starting from the very first layout design phases.

Table 3: Complete ESD Verification Flow – Rules, Features & Links among the Three Steps

1st step: Topology	
Needed input information (from datasheet)	Pads connectivity and functionality, AMRs, ESD robustness requirement type and level
Checked file	Schematic netlist of whole product
Checked field	Both HBM & CDM
Rules	On ESD network: Authorized components, correct polarities, minimum sizes; On IO stages: resistors at gates, clamping diodes and resistors at critical V_{GS}, minimum MOS width, IOMOS usage, proper resistors implementation if bringing part of the ESD, particular weak topologies protection
2nd step: Current Density	
Needed input information (from 1st step)	Pin-pair zap combinations, functionality of each pin (IO or Supply)
Checked file	Layout netlist of ESD ring
Checked field	HBM
Rules	Maximum Current Density threshold fulfillment by metallization layers belonging to ESD network
3rd step: ESD V_{DR} vs. MSV	
Needed input information (from 2nd step)	Pin-pair names and ESD V_{DR} developed for each zap
Checked file	Schematic netlist of whole product
Checked field	HBM
Rules	Protected branches of the product able to sustain the ESD V_{DR} developed by the protection network

This approach consists in the following checks organization:

1. The first step (schematic level topology checks) is applied to the whole product schematic netlist since this database is usually available at an earlier design phase.
2. The second step (layout level current density) may be applied to the ESD ring only. This approach enables extracting CD information on the entire ESD network and calculating V_{DR} values

(representing ESD voltage drop developed by the only ESD network) simultaneously. With this approach, protected circuitry is not taken into account by the tool as potential ESD current path. This simplification therefore leads to the worst-case V_{DR} values.

3. V_{DR} values are given in the input of the third step (schematic level, weak circuitry against V_{DR}), which this time is applied to the whole product schematic database in order to take into account all the potential weak branches belonging to the investigated product.

This dedicated workflow is actually helping the complete verification of many Smart Power products, allowing a realistic detection of the main violations over any of the three checked fields and, in the same time, an effective coverage of the whole ESD verification during the design phase.

V. Application to IC's

Successful application of the whole verification flow to two Smart Power BCD IC's (A and B, see Table 4) is presented with main focus on V_{DR} checker implementation (third step). The run times of the single steps are given in Table 5.

Table 4: Smart Power BCD IC's under Test – Features

prod	market	Techno	Pins	Domains	HBM req
A	consumer	160nm	80	-7/+20V	2kV
B	automotive	110nm	64	-20/+70V	4kV

Table 5: Complete Verification Flow – Run-Times

	1st step	2nd step (only CD errors)	2nd step (all results)	3rd step
Prod A	30 secs	20 mins	~ 9 hours	4 mins
Prod B	50 secs	30 mins	~ 11 hours	6 mins

One can observe the similar run times behavior in both products. The first step (topology, schematic level) requires a few tens seconds to complete, since no simulations are performed, while paths searches, conditions verifications and parameters comparisons only are executed. The second step (CD verification of the interconnects, layout level) reporting only CD errors takes tens of minutes to run on the ESD ring GDSII, while part of the second step addressing V_{DR} takes much longer time (around 10 hours). The long run time is attributed to the need to store physical results for all the analyzed polygons and not only for the ones in error. In the next section the future solution in plan to overcome this run time issue is presented. Finally in the third step (V_{DR} against MSV) the runtime for complete schematic products is in the order of few minutes only. Furthermore, in this case no simulations are performed, therefore reasonable runtimes are obtained even for computation of whole product schematic netlists.

While several findings were highlighted by the first and second verification steps on both products and consequently fixed, we will concentrate in the third step analysis and violations.

First release of product A failed below 1kV during HBM validation tests for pin-pair stress combinations +/- IO1 vs. VDD2. Failure analyses showed that ESD network protecting IO1 vs. VDD2 in both directions (Figure 14, yellow arrows) was intact, while a protected LV switch was damaged.

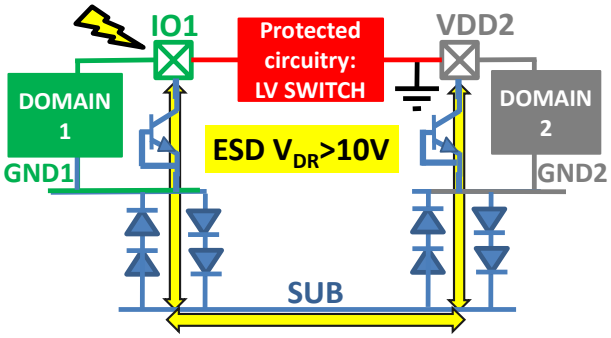


Figure 14: Product A – Red Box Failing for V_{DR} Overstress

Each domain was well-protected, and the failed LV switch was functional as a cross-domain block between IO1 and VDD2, and placed in the region of domain 1 (see geometrical representation of top product layout in Figure 15).

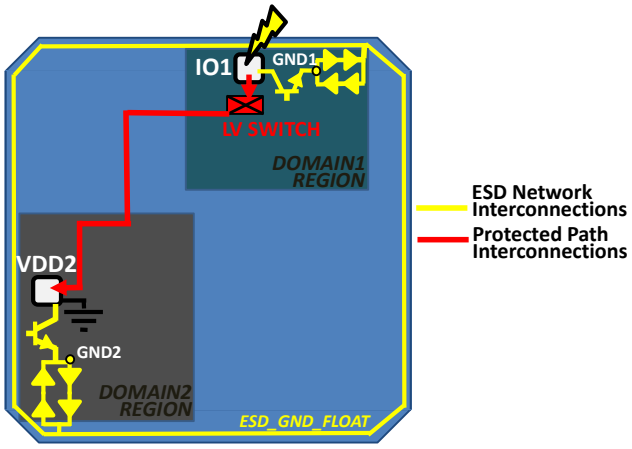


Figure 15: Product A – Top Layout Representation

TLP characterizations were performed in order to investigate the I-V behavior of the symmetrical failing combinations. The results of the TLP stress on IO1 vs. VDD2 (+) TLP are shown in Figure 16.

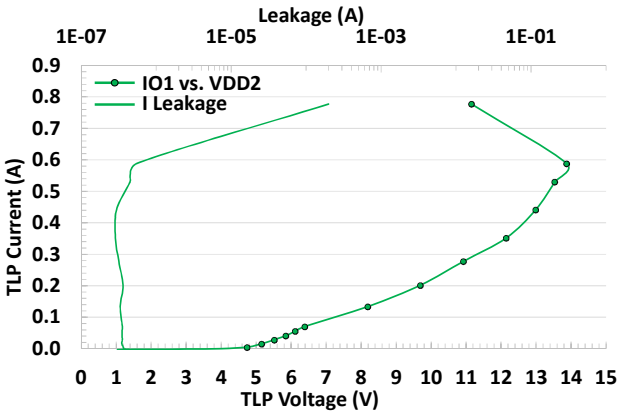


Figure 16: Product A – TLP curve for IO1 vs. VDD2 (+)

A catastrophic failure can be noticed at about 0.6A injected TLP current with a developed V_{DR} higher than 14V.

Applying our complete verification flow during post-design investigation, V_{DR} checker exactly detected a violation below 1kV HBM occurring on both (+) and (-) IO1 vs. VDD2 stresses. In both cases the error report showed that V_{DR} > 10V has been developed by the ESD network, while the protected LV switch featured a global MSV < 10V in both directions. This finding allowed us implementing a new protection strategy able to develop a voltage less than 10V during the HBM stress. It consisted in adding static cross-domain clamps to create a low-impedance protection path between IO1 (IO2) pin and GND2 (GND1) pin (see Figure 17): its effectiveness was validated with the complete verification flow.

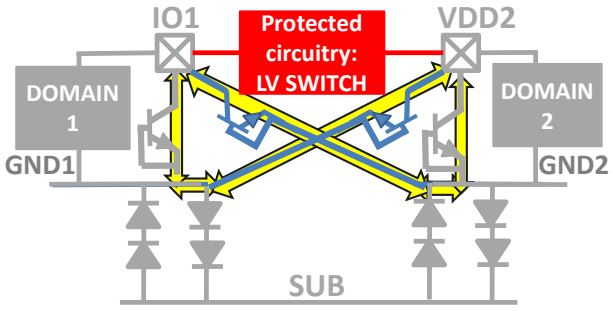


Figure 17: Product A – Solution Implementation – Dual Cross-Protection with Further Static Clamps

The second release of product A, containing the modifications, finally passed all HBM validation tests.

In product B the complete verification flow was run during the design phase. Therefore, different from product A, no characterization data on the following highlighted issues were available. Two violations were reported by the V_{DR} checker in correspondence of stress (+) IOHV1 vs. IOHV2. These pins have the same ground as depicted in Figure 18. Anyway the second pin can switch down to -20V in operating conditions. For this reason, additional static clamps in series are placed on that pin, leading to an extension of the ESD protection path (higher V_{DR}). The first violation involves a protected HV switch (see red box) and the second one is related to the red ESD upper diode. From V_{DR} checker indications, the activated ESD network (yellow arrows) is developing a global V_{DR} higher than 70V, whereas both protected HV switch and red ESD upper diode feature a MSV below 70V. In order to fix the weaknesses detected by the tool, we decided to substitute the central static protections series (light blue box) with a single dynamically-activated clamp. By running again the complete verification flow on modified design schematic, it returned clean reports. The new protection network developed a V_{DR} < 70V. Thanks to this protection optimization implemented during the design phase, the first release of product B passed all HBM validation tests.

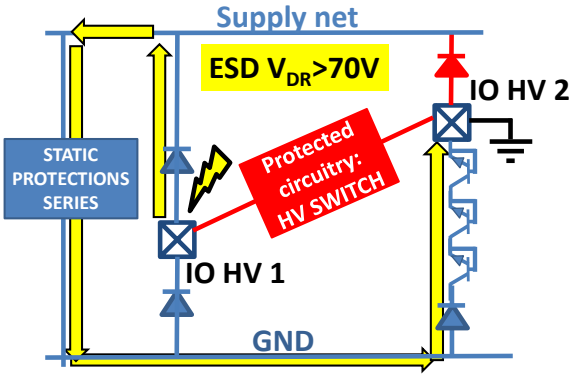


Figure 18: Product B – Red Elements Failing for V_{DR} Overstress

VI. Conclusions and Next Steps

In the present work, a customized checker able to identify circuitry prone to overstress due to developed HBM V_{DR} is described in terms of its ideation, implementation, and successful application to Smart Power products. The V_{DR} checker conception as last step of our internal ESD verification flow is also shown. The strength of this V_{DR} checker and in general of the whole developed verification flow is to provide results which are a suitable compromise among accuracy, implementation ease, and run time. The next steps will be concentrated in increasing the number of search steps for weak circuitry (bringing it from max 2 devices in series to max 3 devices in series) without exploding the run time. Moreover, a cooperation with Mentor is on-going in order to add

the possibility to automatically obtain a CD output report containing V_{DR} information for all the polygons of the ESD path (and not only for those in error). This improvement will allow to perform PERC CD runs searching for real CD_{MAX} violations only and getting at the same time the necessary V_{DR} information on any pin-pair (also on those not in error). This methodology allows to initialize the third step process. Finally, we plan to expand the tool to catch also parasitic weak "series" involving isolation Nwell rings of MOS devices and Nwell/Pwell terminals of resistors. This feature may help in identifying risky situations where unwanted weak junctions are involved in sustaining the ESD voltage drop developed by the protection network or also in carrying part of the discharge. Such a schematic-level methodology may be used in parallel to a layout-level parasitic finder in order to cover all the possible records.

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