Oscillation of RC Power Clamp inside IC Package

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Abstract - RC-type active clamp would be triggered by a certain dimension of steep voltage edge between power node and ground due to EM noise or ESD event even in operating state. Though this itself is decent, one trigger could lead to continuous oscillation when it comes to some clamp types of RC with multiple-stage inverters. It won't happen even with multiple-stages if the clamp is not triggered, but principle solution of this is adopting 1-stage inverter. Transient behaviors of clamps with multiple-stage inverters and one with 1-stage-inverter after triggering are discussed.

I. Introduction

Among various ESD protective schemes on power nodes, it is very common using some kinds of RC-trigger active clamp which consists of BigNMOS, resistor, capacitor and inverters (Figure 1). Number of inverter stages seems to be decided without any concern except for ESD robustness, but an RC-trigger active clamp with multiple stage inverters could oscillate after being triggered by a steep power up, EM noise or powered ESD (PESD) zapping during operating state. Although Stability of multiple stage inverters from the AC point of view has already been well discussed before [1,2, 3], transient phenomenon has not been known very well. The major contributions of this paper are introducing the measured oscillating voltage waveform, elucidating the cause of the phenomenon by seeing the transient behavior of each node in SPICE simulation and consideration on stability of power clamps depending on number of inverter stages.

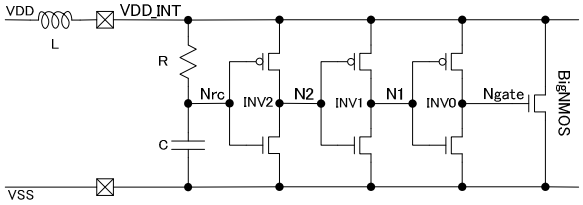

Figure 1: Active Power Clamp (3 stages)

II. Power Node Oscillation

Among various power clamps, types of simple RC-trigger are widely used. The RC-trigger clamp consists of BigNMOS which clamps voltage by flowing massive ESD current, inverters to drive the BigNMOS and R and C for time constant. One, two or three as number of stages of inverters seems to be in widely use. The RC unit generally occupies about 1/3 to 1/2 of the area of the clamp as well as BigNMOS.

Robustness against high voltage ESD which has recently been getting required from many IC customers. Some of them require IEC 61000-4-2 to ICs even if it is excessive [4]. ESD protective circuits occupy broad area in some ICs. Especially for RC triggered active clamps, R and C are objects to save area by putting them into one unit per multiple bunches of BigNMOS. It appears, for one RC and multiple BigNMOS, that multiple stages of inverters instead of one stage would be desirable to avoid the large amounts of parasitic capacitances between gate and source of the PMOS of final stage inverter (INV0) which degrade the trigger performance of the clamp (Figure 2, Figure 3). The multiple-stage type will show good reaction within normal ESD zapping.

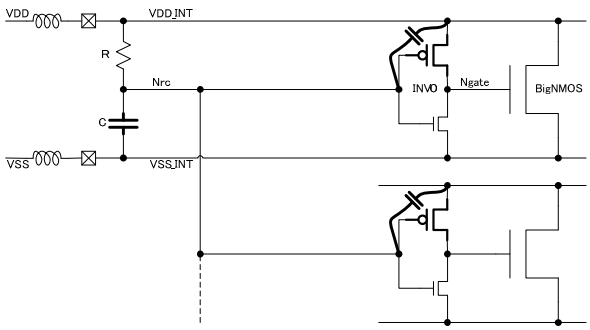

Figure 2: Single Stage for Multiple Bunches

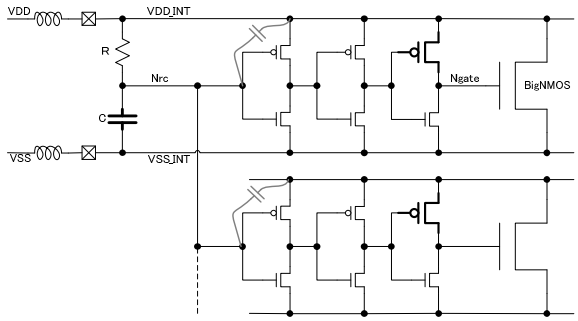

Figure 3: Three Stages for Multiple Bunches

The trouble is that a trigger action of power clamps at or after power on might cause continuous oscillation. A waveform in Figure 4 is one of the observed ones on a generic PCB board by triggering the clamps in an IC during powered state. In that case, the power source was voltage of 1.2V without any stabilizing devices such as bypass condensers or ferrite beads so that it is easy to observe oscillating waveforms. The clamps of the power node contained 3-stage inverters in the trigger circuit. Current consumption during the oscillation exceeded 100mA. Smaller amplitude has been observed on stabilized power nodes, or the oscillation been indirectly observed by a surge in current consumption, which might overheat the package after zapping some noise, or DC voltage drop accompanying with it.

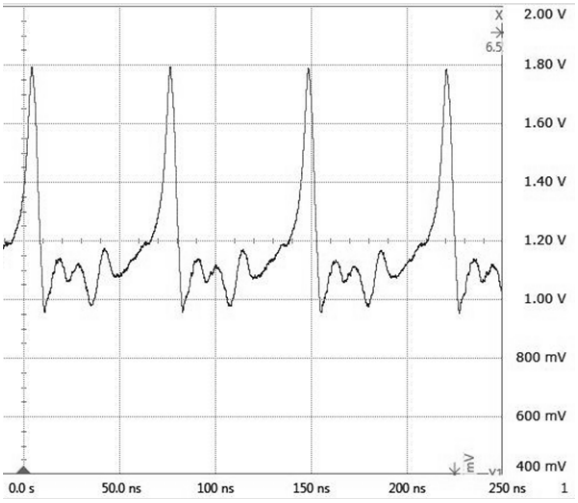

Figure 4: Observed Oscillating Voltage of Power Node

These facts probably indicate that it may happen even with ideal power nodes outside the package. To confirm that, a simplified test bench of a clamp connected to an ideal power source (VDD … 1.2V) only by an inductor (5nH) was simulated and oscillation was observed (Figure 5). The waveform shows that the voltage of the internal power node (VDD_INT) reaches 3.4V and current consumption is around 300mA. This tells us that there can be strong oscillation inside the package even if we don't see any oscillation outside the package. Once it happens, the certain way to stop this is choking the power supply off instead of signal control such as some resets because the oscillating loop is irrelevant to any signals. Mechanism of the oscillation is explained in the section III based on the simulated waveforms.

Note that the oscillation never happens in an IC inside an adequately noise-immune system or under sufficiently slow power-on slope, where any clamps won't be triggered.

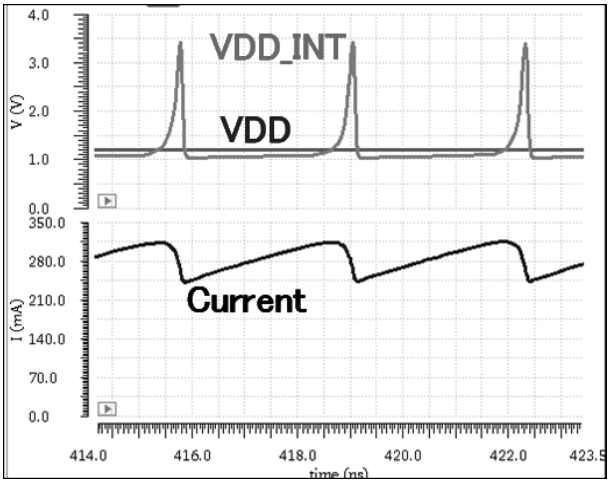

Figure 5: Simulated Waveform of 3-stage Clamp

III. Mechanism

Since this is a non-linear phenomenon as indicated in the waveform (Figure 5), transient approaches are taken to consider of this. The oscillating loop which consists of roughly 3 steps is considered in the case of 3-stage inverters (Figure 1) with transient behavior of the internal nodes (Figure 6).

1) BigNMOS turns on because of rising voltage edge of VDD_INT which is connected to ideal voltage source VDD by package inductance.
2) The BigNMOS begins to turn off after certain duration which comes from propagation delay along through the multiple series inverters. Hence derivative of the current (dI/dt) flops into negative and it reaches about -0.5e9A/sec.

3) The negative derivative of the current rises the voltage of VDD_INT up to the triggering level of the active clamp due to counter electromotive force (EMF) by the inductance of bonding wires in the package. In this case, 5nH generates +2.5V for -0.5e9A/sec. Inductance less than 1nH may cause the oscillation in some cases. Then it returns to 1).

It is notable that voltage of gate of the BigNMOS (Ngate) touches VDD_INT in every cycle, which forces Ngate keeping high. This determines whether the system oscillates or converges. Case of 2-stages related to this will be discussed in IV-C.

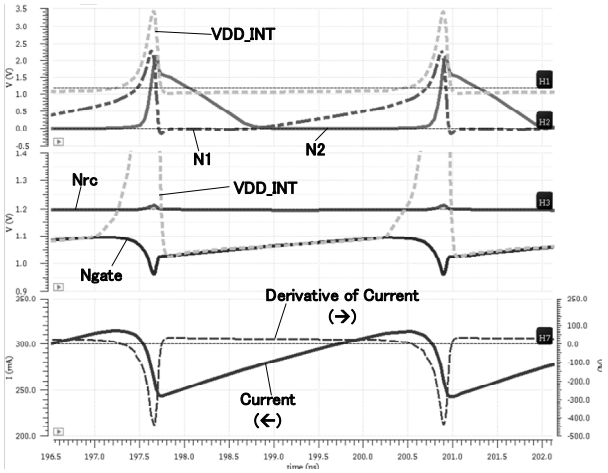

Figure 6: Waveform of the Internal Nodes

After the BigNMOS turns on, V(VDD_INT) is plunged into below V(VDD) and it increases relatively as slowly as about 33mV/nsec accompanied with current increase or positive dI/dt. It might seem to be strange a little that current increases after turn-on. This is explained as below.

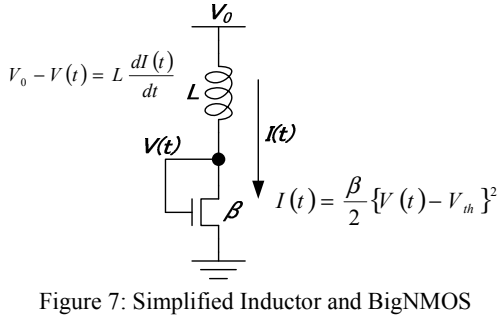

Figure 7: Simplified Inductor and BigNMOS

The BigNMOS can be regarded as in diode-connection after the re-turn-on because voltage of the Ngate is equal to V(VDD_INT) by PMOS of the INV0. A simplified model is now emerged (Figure 7). There are two $V(t)$ and $I(t)$ related equations with regards to EMF and saturation current of the BigNMOS in diode connection respectively (Figure 7). V0 is ideal voltage source and $V(t)$ represents V(VDD_INT) and V(Ngate). A following equation on overdrive voltage of the BigNMOS ($V(t)$-V_{th}) is derived by combining both equations.

$$\frac{d}{dt}\{V(t)-V_{th}\}=\frac{1}{\beta L}\left\{\frac{V_0-V_{th}}{V(t)-V_{th}}-1\right\} \quad (1)$$

The equation indicates positive derivative of the overdrive voltage because of $V(t) < V_0$ (V(VDD_INT) < V(VDD)). Thus, the current ($I(t)$) increases.

Here is a rough estimation on derivative of the overdrive voltage or $V(t)$.

V_0=1.2 [V]
L=5 [nH]
V_{th} = 0.45 [V]
$V(t)$=1.0 [V]
β=2 [A/V2] (Since $I(t)$=302.5 [mA])

d{$V(t)$-V_{th}}/dt
= 1/(2*5e-9) * {(1.2-0.45)/(1.0-0.45)-1} [V/sec]
= 36.36 [mV/nsec]

Decent number is derived.

IV. Solution

Inductance of 0nH between the ideal power source and internal power node on silicon should be one of the solutions. But it may be almost impossible to reduce the package inductance into non-oscillating level, because efforts on reducing or optimizing the package inductance should already have been done and some power sources would require unrealistically drastic reduction of the inductances.

Measures and effects when facing the oscillating problem after triggering clamps are discussed based on SPICE simulations in this section. Note that totally noise immune system to avoid triggering power clamps is the first priority, because infiltration of such a strong noise should cause other troubles than this problem.

A. Consideration on PCB

Economic measures on PCB to resolve the problem are expected by changing or adding discrete devices, but they are not promising.

1. More Stable Power Line

Efforts on getting the power line on PCB more stable with such as bypass capacitors or ferrite beads cannot be solution, since the phenomenon is realized even with the ideal power source outside the package (Figure 5).

2. Damping Resistor

Higher impedance of power supply with damping resistors seems effective because it would tighten power consumption for the oscillation. However, the oscillation accompanied by voltage drop and lower current still occur under the range of realistic resistance if the voltage of Ngate keeps higher than Vth of the BigNMOS (Figure 8). Damping resistor is not the solution neither.

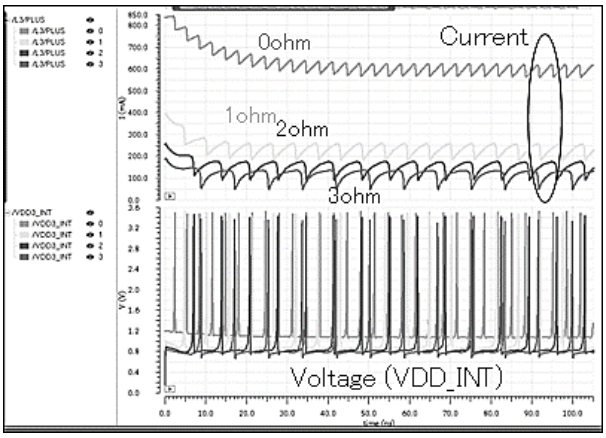

Figure 8: Dependency on Damping Resistance

B. Consideration on Silicon

Two possible measures regarding on power source stability and clamp circuit are considered.

1. Decoupling Capacitance

Stable power line inside the package is expected to avoid the oscillation, but simulated waveforms indicate that a large amount of capacitance up to 1nC cannot stop the oscillation (Figure 9). Furthermore, adding capacitance may induce oscillation, which will be considered in the case of 2-stage inverters of clamp in IV-C.

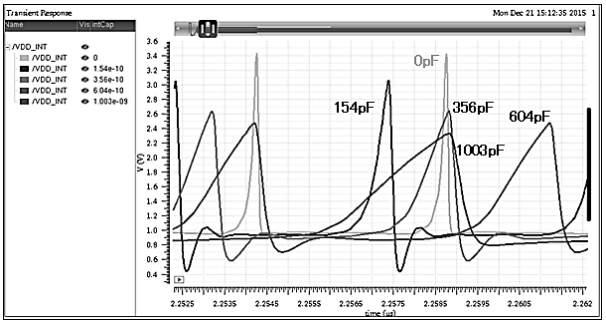

Figure 9: Dependency on Decoupling Capacitance

2. Number of Inverter Stages

Multi-stage inverters have been known as potentially unstable [1]. Transient simulations indicate that clamps with multiple inverter stages might not be able to stop oscillation and 1-stage inverter is possibly the solution (Figure 10), while there are some conditions of 2 stages converging into stable (Figure 11).

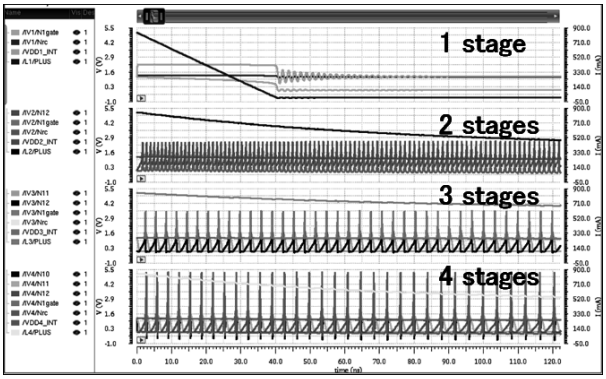

Figure 10: Dependency on Number of Stages of Inverters

C. Two-stage Inverters

Two-stages should be considered carefully whereas it might be a solution in some cases. There are conditions of 2-stages which seems to be concluded as non-oscillating, but it might be a misjudge. Non-oscillating test benches may not include de-coupling capacitance. Adding de-coupling capacitance of several pF to the test bench might cause oscillation.

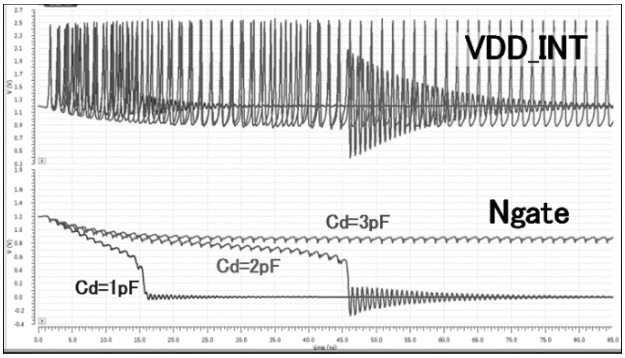

Figure 11: Dependency on De-cap (2-stage)

De-coupling capacitance of 3pF makes the system oscillate while that of 2pF converges (Figure 11). Difference between 3pF and 2pF is that voltage of Ngate is higher or lower than Vth of the BigNMOS. The reason is considered as follows (Figure 12). Note that the voltage between Nrc and VDD_INT is almost constant because of large RC constant.

1) VDD_INT increases due to negative derivative of current following *V*(Ngate) drop due to *V*(N1) increase. Larger decoupling capacitance makes pace of the voltage increase slower.
2) *V*(Nrc) increases coupled with VDD_INT and it reaches threshold voltage of INV1. Longer duration of on-state of the INV1 (Ton) pulls down *V*(N1) lower during Ton. Shorter Ton doesn't pull down *V*(N1) low enough. Larger decoupling capacitance makes Ton longer.
3) *V*(N1) keeps dropping lower after MN1 turning off because of coupling capacitance with VDD_INT through MP0 of INV0.
4) In case of larger decoupling capacitance, INV0 drives *V*(Ngate) higher. Contrary to that, light capacitance keeps *V*(N1) high, so that INV0 doesn't drive *V*(Ngate) high.

Heavy decoupling capacitance makes *V*(Ngate) touch *V*(VDD_INT) in every cycle, which results in continuous oscillation. In case of light one, *V*(N1) doesn't drop to the ground level within a cycle. The *V*(Ngate) gets lower and eventually turns off the BigNMOS.

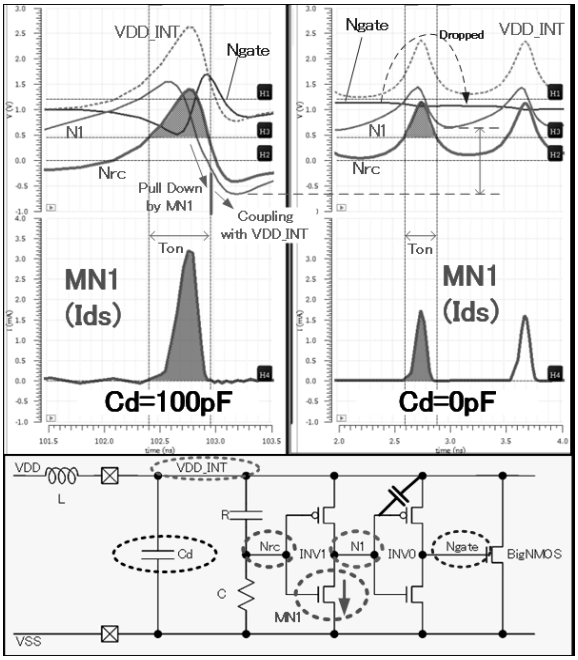

Figure 12: Waveforms on 2-stages

D. One-stage Inverter

Clamp current (I_{CLMP}) of the BigNMOS with the one-stage type (Figure 13) declines linearly and eventually stops, which is in a sort of metastable state (Figure 14). After something triggers the clamp by steep rising edge of *V*(VDD_INT) under powered state, *V*(Ngate) increases and reaches the threshold voltage of the BigNMOS (V_{THC}) because slow RC time constant keeps *V*(Nrc) around *V*(VDD) which becomes roughly half of *V*(VDD_INT). The point is that *V*(Ngate) is at intermediate potential of *V*(VDD_INT) instead of at the same potential as *V*(VDD_INT) unlike the multi-stages.

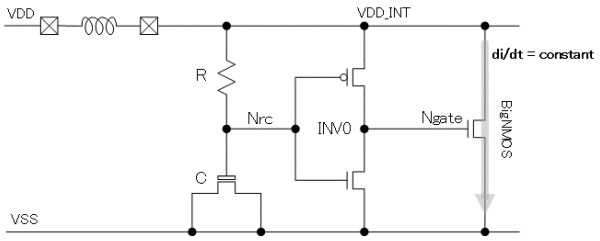

Figure 13: Clamp with 1-stage Inverter

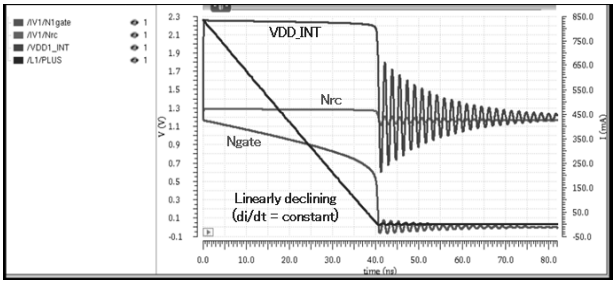

Figure 14: Behavior of the 1-stage Inverter Clamp

Since V(Nrc) is stable enough, derivative of V(Ngate) and V(VDD_INT) are proportional to each other because of the short channel effect of MOSs of INV0, where dV_{GATEC} is much larger than dV_{DDINT}. This indicates that change of V(Ngate) doesn't cause major impact on V(VDD_INT). Thus, this phenomenon is approximately delineated in equations derived from EMF and saturation current of the BigNMOS as follows.

$$V_{DD} - V_{DDINT} = L\frac{dI_{CLMP}(t)}{dt}$$

$$I_{CLMP}(t) = \frac{\beta_C}{2}\left(V_{GATEC}(t) - V_{THC}\right)^2$$

$$\Rightarrow V_{DD} - V_{DDINT} = \beta_C L\left(V_{GATEC}(t) - V_{THC}\right)\frac{d}{dt}\left(V_{GATEC}(t) - V_{THC}\right)$$

$$\Rightarrow V_{GATEC}(t) - V_{THC} = \sqrt{\left(V_{GATEC}(0) - V_{THC}\right)^2 - 2\frac{V_{DDINT} - V_{DD}}{\beta_C L}t}$$

$$\Rightarrow I_{CLMP}(t) = \frac{\beta_C}{2}\left(V_{GATEC}(0) - V_{THC}\right)^2 - \frac{V_{DDINT} - V_{DD}}{L}t \qquad (2)$$

V_{DD}: Ideal Power Source Voltage
V_{DDINT}: Internal Power Node Voltage
L: Package Inductance
$I_{CLMP}(t)$: Clamp Current through BigNMOS
β_C: Drivability of BigNMOS
$V_{GATEC}(t)$: Voltage of BigNMOS Gate
V_{THC}: Threshold Voltage of BigNMOS

Following the equation, slope of I_{CLMP} is minus 180mV/nsec by supposing V_{DDINT}=2.1V, V_{DD}=1.2V and L=5nH, which is jibe with the simulated waveform (Figure 15).

V. Conclusion

RC-triggered active clamps with multiple-stage inverters could cause power node's oscillation in IC package after some intensive noise is zapped. Though noise immune system which doesn't let clamps in the IC turn on is the priority, the effective solution to avoid this is to replace the multiple-stage inverters by 1-stage inverter which behave as only reducing the current even after triggering.

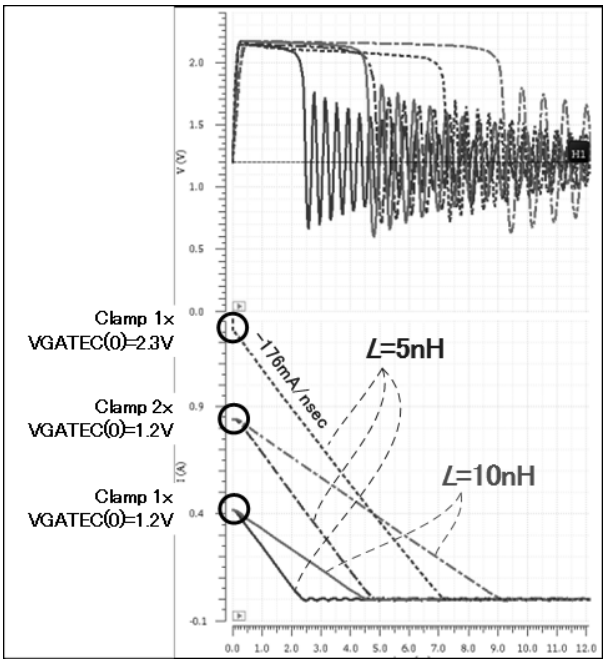

Figure 15: Single-stage Behavior Depending on Inductance
Top: V_{DDINT}, Bottom: I_{CLMP}

References

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