Workshop and Panel Discussions

Workshops Chair: Lorenzo Cerati, *STMicroelectronics*

A.1 EDA for Latch-up: Which are the Most Suitable Approaches?

Workshop Moderators: Michael Khazhinsky, *Silicon Laboratories, Inc.*;
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The verification of latch-up protection in modern integrated circuits is a difficult challenge. There are several factors including increasing design and process complexity, higher-pin counts, use of mixed voltages, power management, etc. that make latch-up analysis especially challenging.

EDA checking/verification tools to design for effective latchup protection are getting used more and more. This includes traditional DRC tools for latch-up geometrical rule checking as well as voltage awareness and resistance analysis checking tools.

Come share what your experiences are in the field. Do you feel you have the right tools to identify the most important potential failures? Is accurate verification for preventing conventional internal latch-up your main concern? Are special cases like biased/floating wells, grounded n-wells, transient latch-up, high voltage applications more important for you? Is information for running the EDA tools readily available throughout design flow? What more is needed to reduce/eliminate latch-up design escapes/failures? Bring your experiences and thoughts/innovations.