

Influence of self-heating on ESD current distribution in metal lines

David Alvarez (1), Nitesh J Trivedi (2), Michael Asam (1)

(1) Infineon Technologies, 85579-Neubiberg, Germany

tel.: +49-89-234-2555, fax: +49-89-234-1525190, e-mail: david.alvarez@infineon.

(2) Former employer: Infineon Technologies, Bangalore, India

Abstract – Copper metal lines from a 40nm CMOS technology are investigated by means of TLP, a static DC current-density-check tool and electro-thermal simulations. The role of self-heating during ESD in the current re-distribution across paths of different resistance is demonstrated. Conclusions are drawn for the proper interpretation of static electrical current-density-check results.

I. Introduction

EDA current density checks for ESD verification of metals and interconnects in ICs usually rely on static DC electrical simulations where thermal effects are not considered for simplicity [1], [2], [3]. This approach reduces the computation time and makes this type of current check practical for large designs, where many different pad combinations need to be verified. EDA tools typically check that the simulated current density in the metal lines does not exceed certain pre-defined maximum values, which have been previously determined by ESD measurements (e.g. TLP) on test structures [4]. In this way, it is possible to detect insufficient metal wiring of ESD devices (Figure 1). The minimum required metal width for a device is the ESD current target (ESD_{target}) divided by the maximum metal current density limit (CD_{limit}):

$$W_{eq} = ESD_{target}/CD_{limit}$$

Where W_{eq} is the total equivalent metal width, this is the sum of all widths of parallel metal paths.

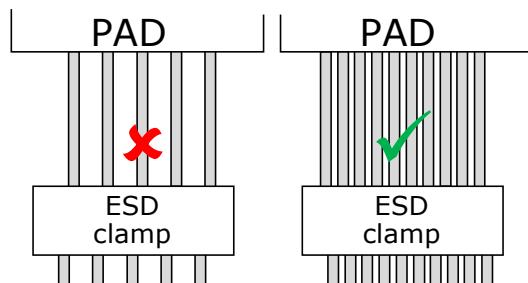


Figure 1. Schematic picture of an ESD clamp with insufficient metal connection (left) and improved design with larger metal width (right) after electrical check.

However, it is often experienced in real designs that despite having a sufficient equivalent metal width (W_{eq}), devices can still show violations if the simulated current over the total metal width is not uniform. The question then arises, since thermal behavior is not considered in the simulation, if self-heating can re-distribute the current across the total available metal width increasing the failure threshold. This would be supported by the observation in many designs where sufficient equivalent metal width is provided and such violations usually do not produce a real ESD failure.

In this work several metal structures were analyzed in order to understand the role of self-heating and to provide some insight for proper interpretation of static current density simulation results. The structures have been designed to reproduce typical constructions that can occur in the metallization of ESD devices in real designs that lead to a non-uniform current distribution. They have been simulated with a DC EDA tool and measured with TLP for comparison. To understand the discrepancy between them, 3D TCAD electro-thermal simulations were performed. The latter show a better agreement with the experimental TLP data and allow probing current vs. time in the different current paths of the structure: this enables a visualization of the current change over time caused by self-heating. With this information, conclusions are derived for a better interpretation of DC current density checks for ESD. An improved methodology which incorporates the use of electro-thermal simulations to the standard EDA flow in special cases is proposed.

II. Current simulator (EDA)

Pathfinder-S from Ansys was used for the current density analysis [5]. Point-to-point current density analysis feature of the tool was utilized: current was injected at one pad connecting the structure and the second one was grounded. The tool performs a pure DC simulation without considering thermal or dynamic effects. This is the typical approach also used by other state-of-the-art tools since it provides a way to check large designs without too much computing time. This was applied for different test structures: to determine the failure threshold, the injected current was sequentially increased until a certain current density limit was reached anywhere in the structure. This pre-defined current limit was set by measuring the failure point on reference structures stressed with 100ns TLP pulses. Each simulation took less than one minute. Large designs like microcontrollers involving several hundreds of pads and many different pads combinations typically require simulation times in the order of 20 to 40 hours.

III. Finite element solver (TCAD)

3D electro-thermal simulations were performed using the open source GetDP finite element solver [6]. The structures were meshed with a number of nodes in the order of ~10.000. The electrical and thermal parts were solved iteratively (fixed-point iterations) since the problem is not assumed to be strongly non-linear. For the thermal part the well-known heat equation

$$\rho c(T) \frac{\partial T}{\partial t} + \nabla \cdot (-k(T) \nabla T) = q_v$$

is solved, where ρ is the material density, T the temperature, $c(T)$ and $k(T)$ the temperature dependent specific heat capacity and thermal conductivity, respectively. The volumetric heat flux q_v corresponds to the electrical dissipated power:

$$q_v = \kappa(T) E^2 = \kappa(T) (\nabla V)^2$$

with $\kappa(T)$ being the temperature dependent electric conductivity, E the electric field and V the electrical potential.

For the electric part the stationary partial differential equation:

$$\nabla \cdot (-\kappa(T) \nabla V) = 0$$

is solved. Dynamic capacitance effects in the electrical part were neglected for simplicity. 100ns TLP current pulses were simulated. The pulse current was sequentially increased until failure was reached. As failure criterion the melting temperature of copper

(1085°C) was taken, whenever it was reached at any point in the structure. The thermal boundary conditions were 25°C set at the pads. The required simulation time for each structure was about ~1-3 minutes.

IV. Results

Four different copper metal test structures were investigated. The structures were coming from a 40nm CMOS technology. Two metal levels were used to construct the structures, namely 1x (minimum thickness) and 2x (double thickness). The structures had always a total metal width of 10μm. In the following the test structure and the cases they intend to address are described together with the TLP and simulation results.

Test structure 1

Figure 2 shows the simple case of straight metal lines directly connected to a metal plate. It addresses the connection of an ESD device to a large metal area like a pad or a power bus. The number of metal lines in the structure is 10, having each one a width of 1μm. The length of the metal line (d) was varied (5 and 30μm) to check the influence of this parameter.

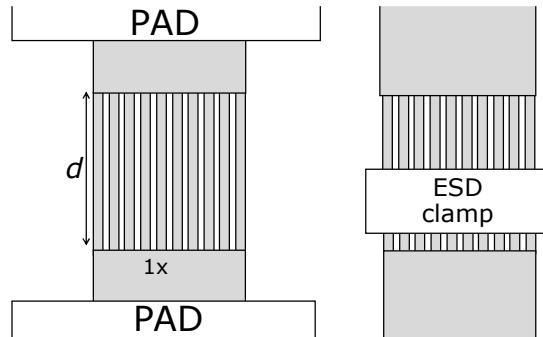


Figure 2. Test structure 1 (left) and case it addresses (right). The finger length d values tested were 5μm and 30μm.

Figure 3 shows the 100ns TLP curves for test structure 1 for the two different values of d . The structure with the shorter fingers has a higher It_2 and less self-heating. Figure 4 shows the TLP failure currents together with the values predicted by the EDA tool and the electro-thermal simulation (TCAD). One should note here the discrepancy between the TLP and the DC simulation for the structure with shorter d . The EDA tool shows no significant difference in It_2 between both structures, whereas the TLP measurement and the TCAD simulation show a higher failure level when reducing the finger length. When plotting the simulated temperature at a TLP

current of 1.9A (It2 of 30 μ m structure) the TCAD data show the reason for the higher failure current in the structure with shorter fingers (Figure 5). The shorter fingers show a much lower temperature profile due to the better heat dissipation to the nearby wide metal connections which act as a heat sink. This poses the question of what type of test structures to use when defining the current density limits for an EDA simulator. Since structures using very short fingers can overestimate the failure current for other constructions, the worst-case failure level of 190mA/ μ m corresponding to the longer finger structure was chosen as the current density limit for subsequent simulations.

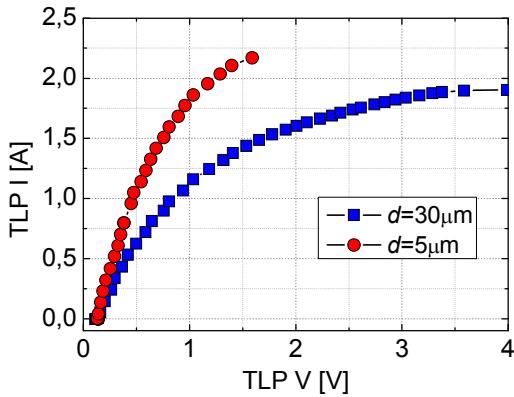


Figure 3: TLP I-Vs of test structure 1 for two finger lengths (d).

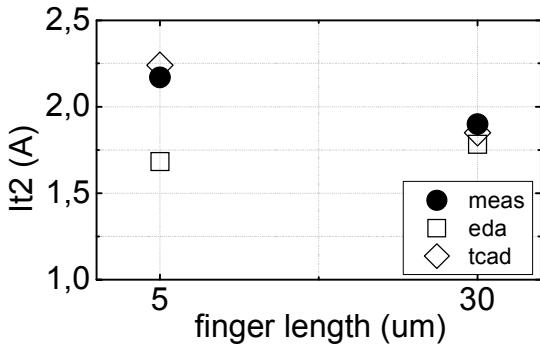


Figure 4: It2 comparison for test structure 1 as obtained by TLP, EDA and TCAD.

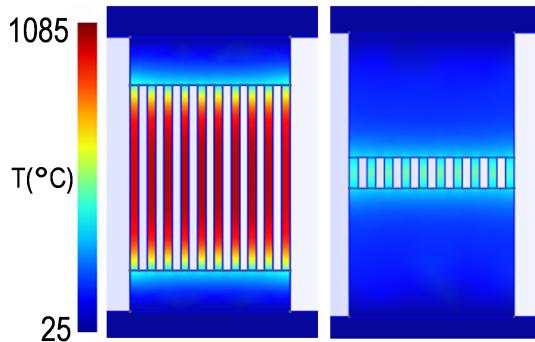


Figure 5: TCAD simulated temperature for test structure 1 variations at 1.85A TLP. Temperature scale: 25 – 1085°C.

Test structure 2

In test structure 2 ten metal lines of 1 μ m width were connected in a way that the current had to flow around two corner paths between the pads (Figure 6). This was aimed to investigate possible current inhomogeneities since the structure does not provide a straight path for the current. The finger length (d) was varied (5, 15 and 30 μ m) to check the influence of this parameter. The scenario intended to address is also depicted on the right-hand side of Figure 6. This could be for example an ESD clamp connected on the one side to an IO pad and on the other to a power bus running to a supply pad in the opposite direction.

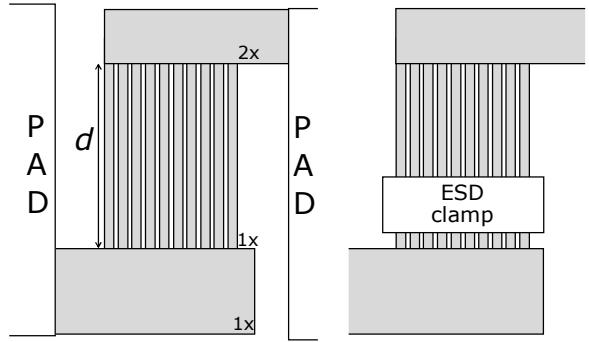


Figure 6: Test structure 2 (left) and corresponding case.

Figure 7 shows the measured It2 values together with the predicted ones by EDA and TCAD. For the shortest finger length (5 μ m) the EDA result shows a large discrepancy (35% lower It2) with TLP and TCAD. For the 15 μ m and 30 μ m finger lengths this difference is reduced to 20% and 10% respectively. EDA predicts also an opposite trend compared to the experimental results, with the shorter fingers having a decreased failure level compared to longer ones.

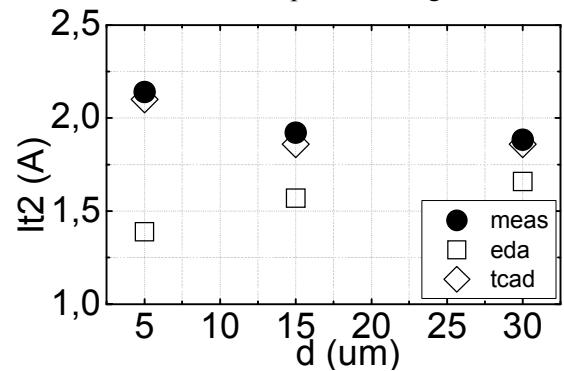


Figure 7: It2 comparison for test structure 2 variations as obtained by TLP, EDA and TCAD.

The EDA-simulated current at failure level (Figure 8) shows violations in the most outer fingers for all structures. Red parts correspond to current density violations (current values >100% of It2). The current

distribution across fingers is less uniform in the structures with short fingers. For longer fingers the differences in current among fingers is smaller and EDA shows a better agreement with the TLP data. Figure 9 shows the TCAD-simulated temperature profile (left) and the current over time for each finger (right) at failure level. A current re-distribution over time is observed in each finger due to self-heating.

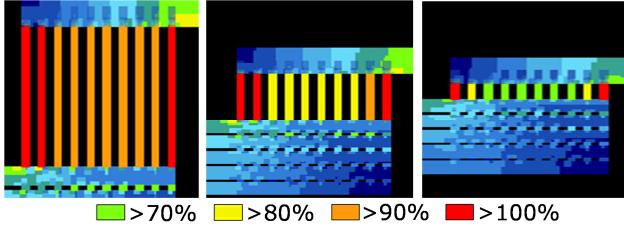


Figure 8: EDA-simulated current at failure for the 3 structures. The legend indicates the color coding for different current levels with respect to the failure current level I_{t2} (100%).

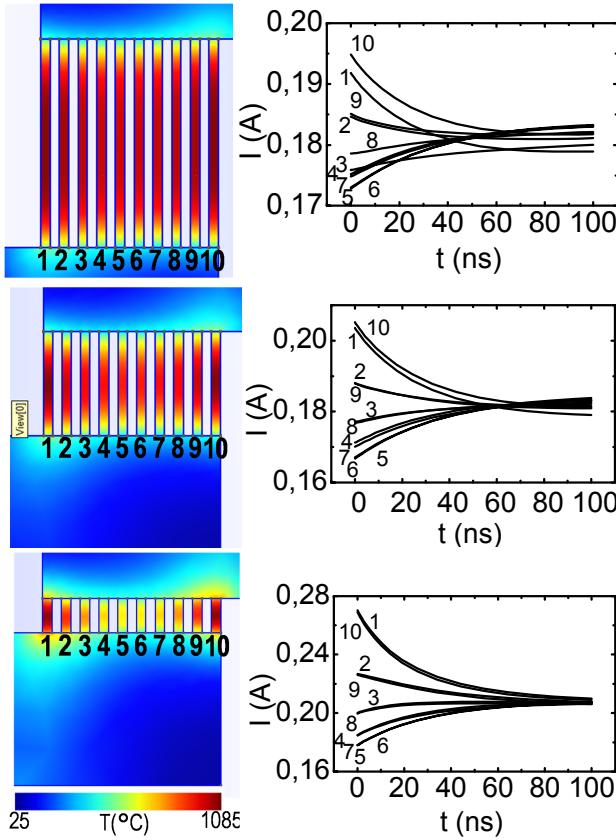


Figure 9: TCAD simulated temperature at failure level (left) and TLP current vs time through each finger (right) for structure 2.

The fingers on the outside take more current at the beginning of the pulse. As the pulse goes by and the resistance is increased due to thermal heating, they decrease their current level and the inner ones start to bring more current. For the 30 μm structure the effect is relatively small. In this case, the larger finger

resistance provides a more uniform current already at the beginning of the TLP pulse. This gives a better agreement with EDA. For the 5 μm structure, on the other hand, a large difference in current across fingers is observed (up to 40%) at the beginning of the pulse. The discrepancy of TLP with EDA is therefore the largest in this structure. The fact that the outer fingers take more current than the inner ones in all structures is related to the higher electric field occurring at the corners. This leads to larger current vectors at the sides (Figure 10). For illustration, the simulation of a single metal line is also shown in Figure 10 where the effect is more evident.

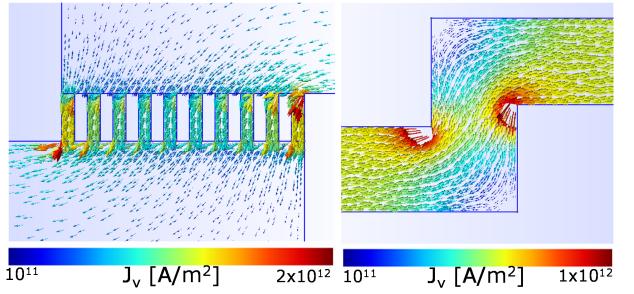


Figure 10: Current density vectors at failure level for the $d=5\mu\text{m}$ structure (left) and for single finger structure (right).

Test structure 3

This structure has two parallel paths of different length (d_1 and d_2) and same width, thus different resistance (Figure 11). This construction happens relatively often in designs with floorplan restrictions where a single connection of the ESD clamp to the next bond pad or bus is not possible and it has to be split into two. Each path in the structure has 5 metal lines of 1 μm width. The length of the metal lines in the upper part (d_1) was varied to provide different resistances (5, 15 and 30 μm). The lower branch of the structure had a fixed length d_2 of 5 μm . The resistance ratios between the upper and lower branches were 1, 3 and 6 respectively.

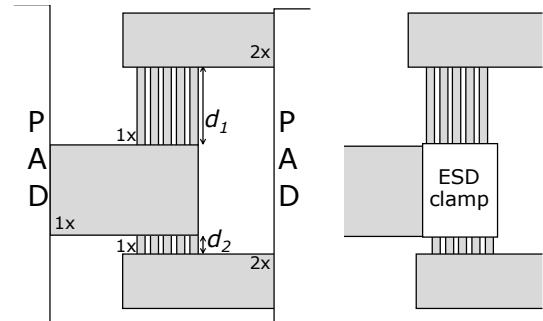


Figure 11. Test structure 3 (left) showing two parallel metal paths of different resistances and case it intends to address (right).

Figure 12 shows the EDA simulated current values at failure level. Violations (red parts) occur in the lower branch for the second and third structure, which corresponds to the least resistance path. The first structure, due to its symmetry, shows the same pattern in both the top and the bottom branches. The most outer fingers in all structures are taking more current than the inner ones, similarly as observed in the structures of the previous section.

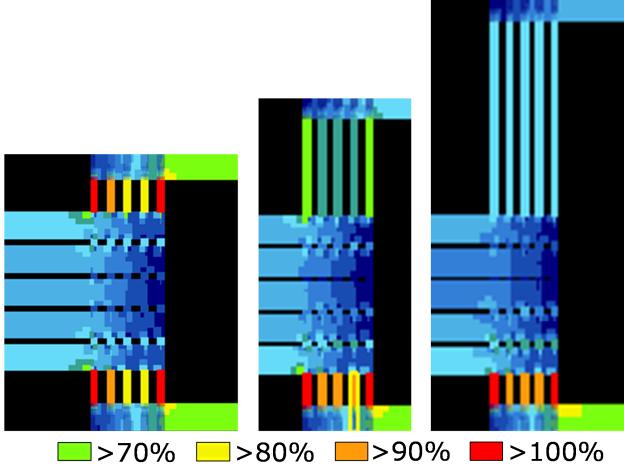


Figure 12: Current density simulation (EDA) at failure current level for the three variations of test structure 3 - $It_2 = 100\%$.

If compared with the TLP data (Figure 13), the EDA tool underestimates the It_2 by 25%, 28% and 30% respectively. One should note that the TLP data show a relatively small decrease in failure current in the asymmetric structures compared with the symmetric one. The decrease in the measured It_2 is only of 10% and 18% for the structures with resistance ratios of 3 and 6 respectively. On the other hand the failure levels produced by the EDA check are much lower. The TCAD results provide an explanation for this discrepancy. The electro-thermal simulations (Figure 14) show a similar pattern regarding current distribution as in the EDA case, but with higher failure levels, in better agreement with the TLP data of Figure 13. When the current through each finger is plotted as a function of time (Figure 15), a current re-distribution is observed over the TLP pulse length. The current within the fingers varies over time in the same way as observed in the previous section (metal corner case), with the outer fingers taking less current at the end of the pulse. In addition, the total current through the upper branch increases as the lower one heats up in the asymmetric structures. Figure 16 shows the thermal plot and the total current over time flowing through the upper and lower branches for the structure with resistance ratio 3. About 10% of the current is re-distributed from the lower branch to the

upper branch due to self-heating. The effect is even stronger (25%) for the structure with resistance ratio 6 (Figure 17). Both current re-distribution thermal effects result in an increased It_2 compared to the pure electrical analysis, where the current through the lower branch is overestimated.

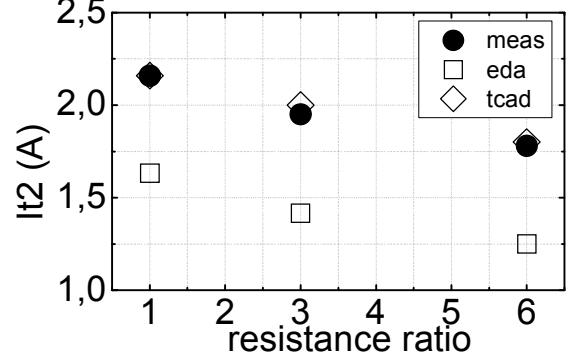


Figure 13: It_2 comparison for test structure 3 variations as obtained by TLP, EDA and TCAD.

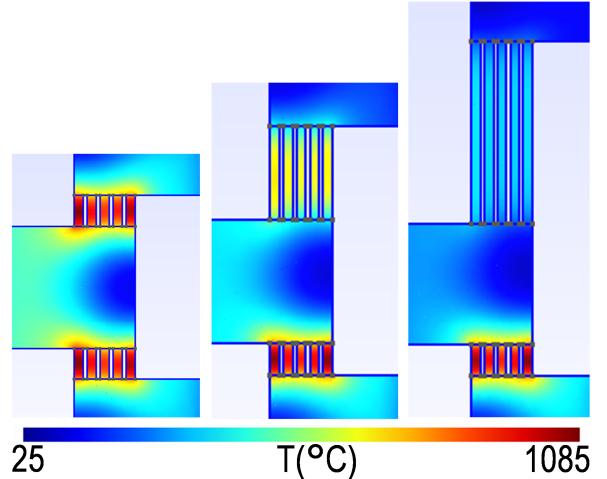


Figure 14: TCAD-simulated temperature plots at TLP failure current for the three variations of test structure 3.

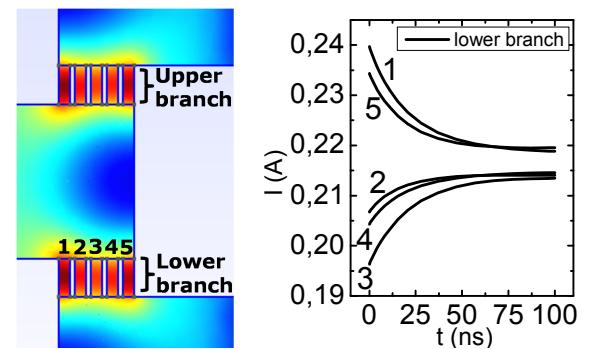


Figure 15: TCAD-simulated temperature (left) and current vs. time for each finger in the lower branch of the structure (right).

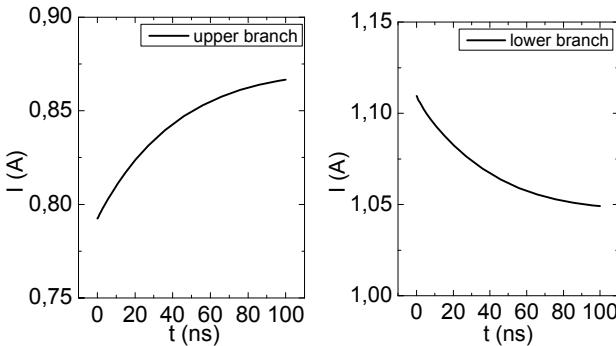


Figure 16: Total current vs time through upper branch (right) and through lower branch (right) of structure with resistance ratio 3.

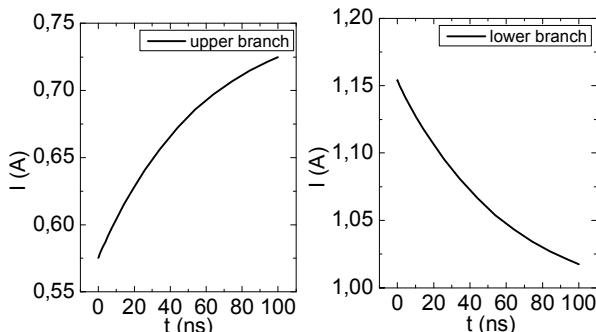


Figure 17: Total current vs time through upper branch (right) and through lower branch (right) of structure with resistance ratio 6.

Test structure 4

Test structure 4 is composed of 5 metal lines of $2\mu\text{m}$ width and $70\mu\text{m}$ length. In parallel to them, an additional metal line also $2\mu\text{m}$ wide has been added, connecting one of the outer fingers to the right pad (Figure 18). This additional connection provides a low resistive shortcut for the current. Such constructions can occur during top level layout design where a weak connection is unintendedly enabled parallel to a main ESD path. A reference structure without weak connection was also tested.

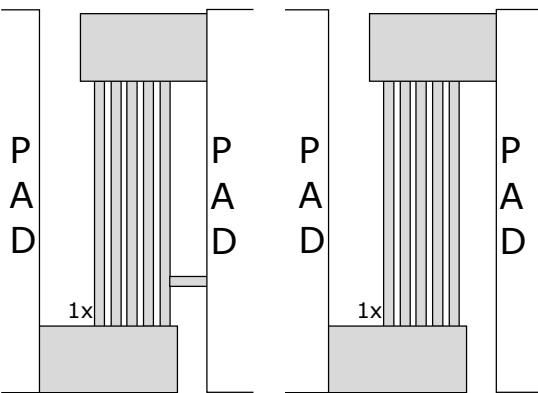


Figure 18: Test structure 4 with weak connection (left) and reference structure without weak connection (right).

Figure 19 shows the TLP curves for both test structures. The reference structure without weak connection has a failure current of 1.85A . The structure with the weak connection shows a significant decrease in failure current, having an $\text{It}2 = 1.04\text{A}$.

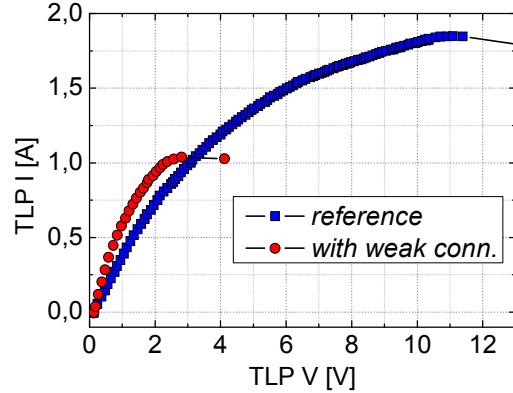


Figure 19: TLP I-V curves for test structure with weak connection and for reference structure.

When simulated with EDA, the reference structure shows a rather uniform current distribution, with differences of less than 10% across fingers (Figure 20).

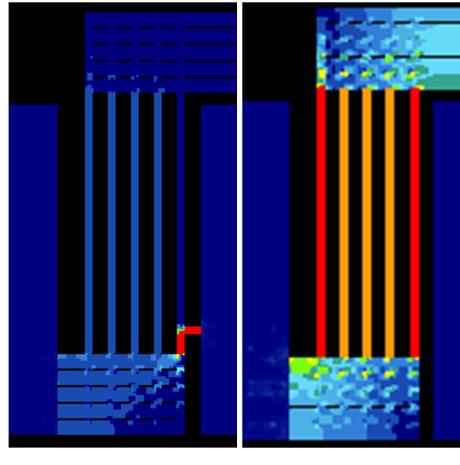


Figure 20: EDA simulated current at failure level for structure with weak connection (left) and for reference structure (right) – $\text{It}2 = 100\%$.

The EDA simulation is in good agreement with the TLP data (Figure 21). For the second structure with a weak connection, on the other hand, a large discrepancy of 50% in $\text{It}2$ is observed (Figure 21). The EDA current simulation shows a non-uniform current distribution where the weak connection takes more than 30% current than the rest of metal lines in parallel. Figure 22 shows the thermal plots for both structures at failure level as simulated by TCAD. When plotting the current over time in each metal line

of the reference structure a rather uniform current distribution across fingers is observed (Figure 23). For the structure with the weak connection, a large current (0.6A) flows through the shortcut at the beginning of the pulse (Figure 24). The parallel path on the contrary takes a minimum amount of current (~ 0.07 A). As the pulse goes by, the current through the weak connection is reduced by almost 50% at $t = 100$ ns due to self-heating. Correspondingly, the fingers in parallel increase their current by almost a factor of two by the end of the TLP pulse.

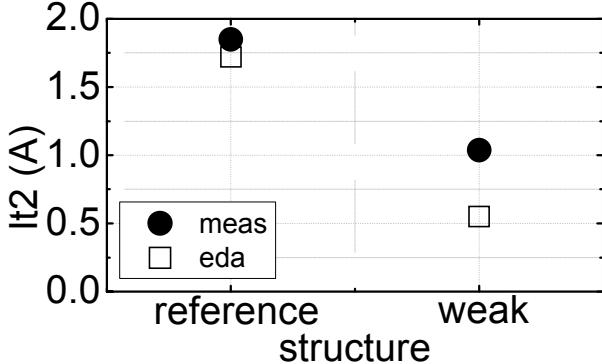


Figure 21: TLP and EDA failure currents for reference structure and for structure with weak connection.

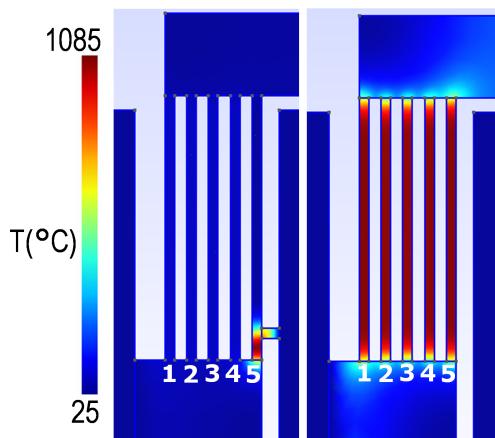


Figure 22: Simulated temperature at failure level for structure with weak connection (left) and for reference structure (right).

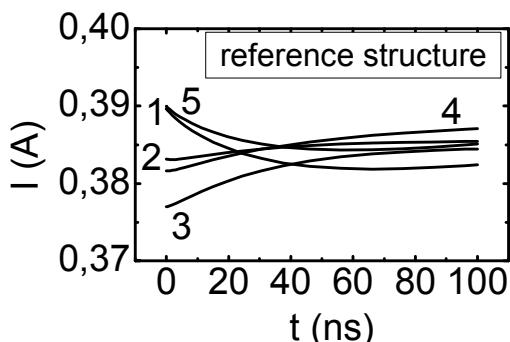


Figure 23: Current over time at failure level through each metal line of reference structure.

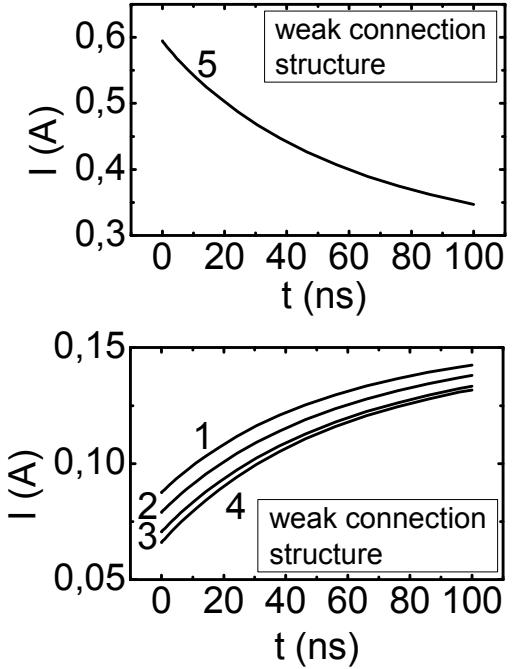


Figure 24: Current over time through weak connection (top) and through rest of metal lines (bottom) in the structure.

V. Application to a real design

A microcontroller design coming from a 65nm CMOS technology with embedded flash having more than 200 pads was checked using the Pathfinder-S current density tool in a first step. In a second step, violations showing non-uniform current distributions larger than 10% were analyzed using TCAD. The design had an HBM target of 2kV. A DC current of 1.33A was simulated for all pad combinations in the design. The total runtime for the current density check was 25 hours. Several violations showing not sufficient total equivalent metal width (W_{eq}) were detected, which in this design was 20 μ m, and fixed. The connection of an ESD diode to an IO pad having a total metal width of 32 μ m, larger than the minimum W_{eq} required, also showed a violation of 110% (Figure 25). The wiring was done in a way that two parallel metal paths of different resistance were connecting the diode to the IO pad. This led to a strong current non-uniformity (>30%) producing a violation in the left connection, which had a lower resistance to the IO pad compared to the right one. On the other hand, the Vss connection of the diode, with straight parallel metal lines and sufficient metal width, was clean and did not show any violation.

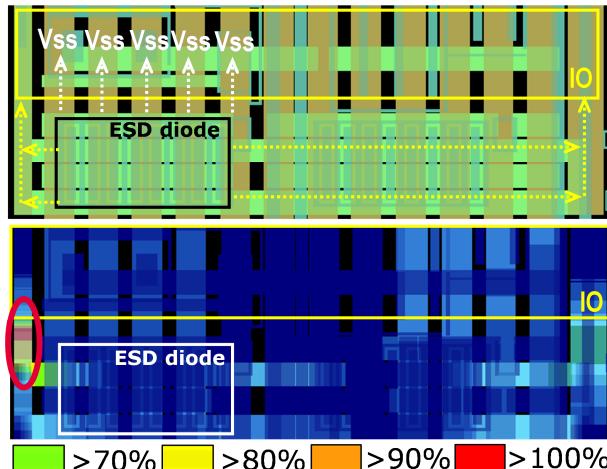


Figure 25. Metallization layout of an ESD diode (top) and 2kV current density simulation (bottom). The current density check shows a violation in the connection of the diode to the IO pad.

The diode metallization was simulated with TCAD in the same way as the previous structures in this work. Most of the effort was required in the structure generation (~1hour); the simulation time was of 3 minutes. TCAD predicted a failure current of 2.7A (Figure 26) which is much higher than the required TLP equivalent current for a 2kV HBM target (1.33A) [7], [8]. One should also note that the failure point is reached in the TCAD simulation further away from the IO pad than in the DC case due to the presence of the pad area which acts a heat sink. The current vs. time at failure level through the metal line where the failure takes place is shown in Figure 27. As expected, a large current re-distribution is observed due to self-heating, which explains the discrepancy with the static DC result. The decision was not to change the metallization for this device based on the TCAD result. When tested, the product showed an HBM pass level of 3kV (higher not tested) without any modification in the design.

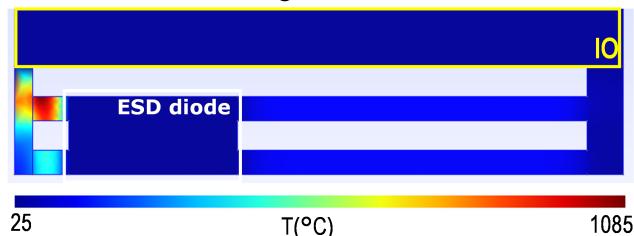


Figure 26: Simulated temperature at failure level ($I_{t2} = 2.7\text{A}$).

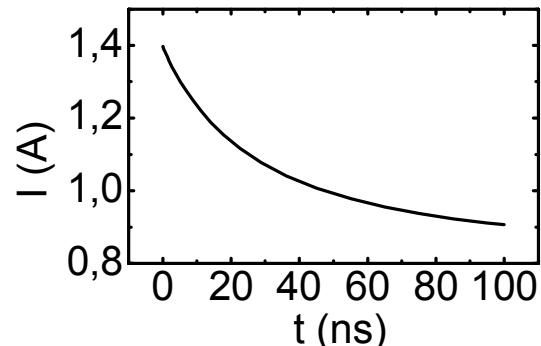


Figure 27: Simulated current vs. time for upper left connection of the diode to the IO pad (TCAD failure location).

VI. Conclusions

State-of-the-art ESD current density checks make use of DC simulations to detect metallization weaknesses in ICs without considering thermal effects. This approach provides realistic computation times to check large designs with many pad combinations. In this way, devices with insufficient metallization below a pre-defined minimum width can be easily detected. However, if current homogeneity in the metal is not ensured, violations can still occur even if sufficient metallization width is available. Proper assessment of such constructions needs to take thermal effects into account, as shown in several examples in this work. Self-heating can result in a re-distribution of the current which increases the failure level compared to the DC static case. This electro-thermal behavior can be simulated with TCAD tools which show a better agreement with the experimental data. In this work was found that for current differences larger than 10% across different metal lines, the DC simulation provides too pessimistic results and thermal analysis is required. Computing time for full chip verification of large designs would take unrealistically long with TCAD and therefore a mixed methodology is proposed where DC checks are used in a first run and TCAD analysis in a second one for specific pad combinations that show non-uniform current distributions larger than 10%. Typical runtimes for large microcontroller designs with more than 200 pads are in the order of ~30 hours for the EDA tool used in the work. TCAD for dedicated critical constructions results in an add-on of 1-2 hours per structure including structure generation and simulation time.

References

- [1] S. Mitra *et al.* “A Current Density Analysis Tool to identify BEOL fails under ESD Stress”, Proc. EOS/ESD Symp. 2011.

- [2] M. Ershov *et al.* “EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level”, Proc. EOS/ESD Symp. 2013.
- [3] E. Gevinti *et al.*, “Schematic-Level and Layout-Level ESD EDA Check Methodology Applied to Smart Power IC’s – Initialization and Implementation”, Proc. EOS/ESD Symp. 2015.
- [4] L. Di Biccari *et al.* “Thin Copper Metal Interconnections Thermomigration Analysis in ESD Regime”, Proc. EOS/ESD Symposium 2014.
- [5] <http://www.apache-da.com>, proprietary software
- [6] <http://getdp.info/>
- [7] A. Amerasekera *et al.*, “An analysis of low voltage ESD damage in advanced CMOS processes,” Proc. EOS/ESD Symp. 1990.
- [8] J. Barth *et al.*, “TLP calibration, correlation, standards, and new techniques,” Proc. EOS/ESD Symp. 2000.