An ESD Case Study with High-Speed Interface in Electronics Manufacturing and its Future Challenge

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Abstract – A networking semiconductor component with 25 Gbps high-speed interface experienced high manufacturing failure rate with CDM-like failure signature at contract manufacturer; design of experiment was performed and ESD source was located. Problem details, solution, future challenge and industry awareness are discussed in this paper.

I. Introduction

Nowadays Contract Manufacturers (CM), also known as Electronics Manufacturing Services (EMS) partners are required to establish an Electrostatic Protected Area (EPA) where susceptible electronic items are handled and assembled according to ANSI/ESD S20.20-2014 [1] or IEC 61340-5-1:2016 [2]. Both standards principally cover the requirements necessary to maintain a safe environment for handling electronic parts susceptible to damage by ≥100 V human body model (HBM), ≥200 V charged device model (CDM), and contact to isolated conductors with ≥35 V. Certification needs to be done by accredited certification bodies annually. It is commonly perceived that the certification guarantees that it is risk free to handle sensitive parts meeting 100 V HBM and 200 V CDM.

This paper will present a case that a networking semiconductor component, which is named as component "P" in this paper, that passes beyond the above-mentioned ESD test voltage, has experienced high number component failure in a S20.20-2014 certified factory. "P" is designed on 3 different boards, named A, B and C, consisting of 8, 2 and 6 instances of "P" respectively. Board failure rate varies from 2.23% up to 8.29% with (1), whereas component failure rate per board ranges from about 1 to 1.5% with (2), as summarized in Table 1. The calculation formula are as below:

$$\text{Board Failure rate} = \frac{[\text{Number of fail boards}]}{[\text{Total number of boards manufactured}]} \quad (1)$$

$$\text{Component Failure rate} = \frac{[\text{Number of P failure}]}{[\text{Total number of P required to assemble the same number of boards}]} \quad (2)$$

The high board failure rate severely impacted the manufacturing throughput and time-to-market. Plenty of design-related debugging work was done prior to isolating the root cause as Electrostatic Discharge (ESD), which will not be discussed in details.

Table 1. Aggregate Board and Component Failure Rate among Boards A, B & C.

	Boards		
	A	B	C
Aggregate Board Failure Rate	8.29%	2.23%	8.85%
Aggregate Component Failure Rate	1.04%	1.11%	1.48%
Number of "P" per Board	8	2	6

This paper will start from physical failure analysis (pFA), followed by the risk assessment of the manufacturing process. Potential ESD-risky processes were identified, a design-of-experiment (DoE) was then set up to isolate to a single manufacturing step. Corrective action was immediately implemented and validated by the manufacturing yield data, defective-part-per-million (DPPM).

We will discuss the issues that the current ESD control standard cannot detect or address. Technology road map forecasts that similar issue may happen more often and become worse in the future. ESD control is no longer a problem that could be solved solely by CMs, but the whole industry systematically including the factor of Design for Manufacturing (DfM).

II. Problem Statement

High DPPM was reported on "P" early during the Pilot build. "P" is a 19 mm × 19 mm BGA component which passes ESD qualification test with results of >|2000 V| HBM and >|200 V| CDM. The 25 Gbps high-speed interface I/O pins could pass |200 V| CDM only, whereas other pins could pass |250 V| CDM. It was not alerted to be a risky part during component qualification because:

1. The CDM passing voltage is well beyond the CDM level guaranteed by S20.20-2014
2. Past experience showed that CM could handle component passing as low as >|100 V| CDM without reporting any ESD related issue

All failed parts were sent to perform failure analysis (FA), functional failure was first confirmed by running final test program. However, the leakage could not be easily detected by external I-V sweep. The AC decoupling cap at the differential pairs prevent proper curve trace from the pad, as in Figure 1. Destructive failure analysis and fine probing are needed to find the leakage location. High leakage was measured at a transistor gate at the receiver side. Focus Ion Beam (FIB) and Transmission Electron Microscopy (TEM) result shows the gate oxide was damaged in Figure 2, resulting in I-V shift in Figure 3. The leakage of one transistor could hardly be detected by any current test except functional test. Other failure units all demonstrated different level of leakage at gate similar to Figure 3, a classic CDM failure signature. This is also confirmed that the same failure signature is observed through CDM qualification.

Given all the evidences proving ESD as high suspect, it was necessary to look for the root cause from different aspects including, but not limited to:

- Was a problematic lot of "P" shipped from supplier?
- Was component zapped after final test (FT) during delivery to CM?
- Does the CDM robustness degrade due to process variation?
- Was component zapped at CM?
- Was there an unwanted electrical stress to the component during electrical testing at CM leading to CDM-like damage signature?

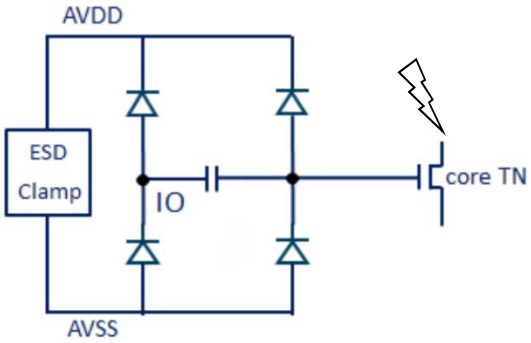

Figure 1. Standard ESD design with Dual Diodes and Coupling Cap for High-Speed Interface, Core TN was found to be damaged by ESD

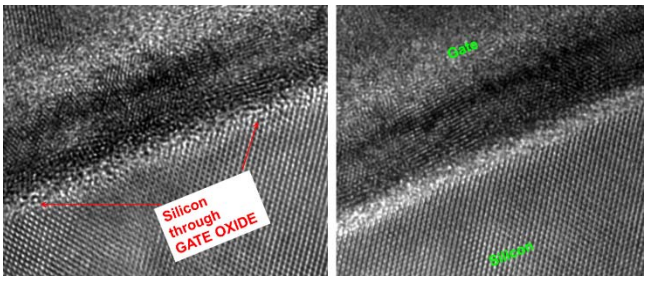

Figure 2. pFA shows gate rupture. Left is ESD damaged unit, right is good unit.

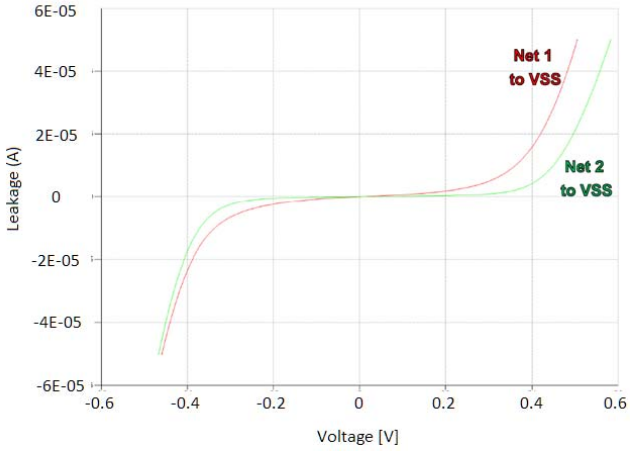

Figure 3. All failure unit demonstrates I-V drift that could hardly be detected by any current test except functional test

Answers to the first three questions were confirmed "No". Unused parts were shipped back to supplier for re-test, zero failure was reported. A few parts from the suspected lot were sent to perform CDM test, results were consistent with the qualification result. The board design and manufacturing process flow with "P" are very similar among boards A, B, and C. Board design

was reviewed thoroughly without anomaly found. Failure locations of "P" on boards are almost evenly distributed. Since the component failure rate is roughly about 1.1% for each board, the board design was ruled out to be the root cause. "P" was very likely damaged on the manufacturing floor.

III. Root Cause Analysis (RCA)

A. Risk Assessment of Assembly Process

Detailed inspection at each manufacturing process step was initiated. Since "P" is mounted on the top side of the printed circuit board (PCB), inspection on SMT process of the bottom side of PCB was skipped. ESD may happen anywhere after "P" is placed on the PCB. Several process steps were identified with different risk level.

The assessment aims to look for the following:

- Was the board charged up unexpectedly in any process?
- Was there any ESD event detected during the assembly?
- Was "P" charged up unexpectedly during handling?
- Was any object discharged through "P"?

A few manufacturing process steps, as shown in Figure 4, were identified where ESD may possibly happen to "P":

Scenario 1: When "P" is picked up from tray and placed on board by pick-and-place machine on the SMT line

Scenario 2: When a connector is press-fit (PF) onto board which causes a direct discharge to "P" through trace

Scenario 3: When a charged test module is inserted into front port connector and discharge to "P"

B. Design of Experiment (DoE)

In order to isolate the problematic area, design of experiment (DoE) was set up as in Table 2 with slightly modified process as shown in Figure 5. Additional test (DL Test) was added to facilitate validation of split B, which is a very simple functional test that could test the basic functionality of "P" without any press-fit connector as well as inserting any test module as required at the Electrical Test step.

Split A was the control lot running the same manufacturing process as usual, split B ran the same process as split A but the press-fit process was skipped. When splits A and B are completed, all boards were sent to run the DL test. If split A had failure whereas B did not have a failure, scenario 2 happened, otherwise, ESD happened somewhere other than press-fit process.

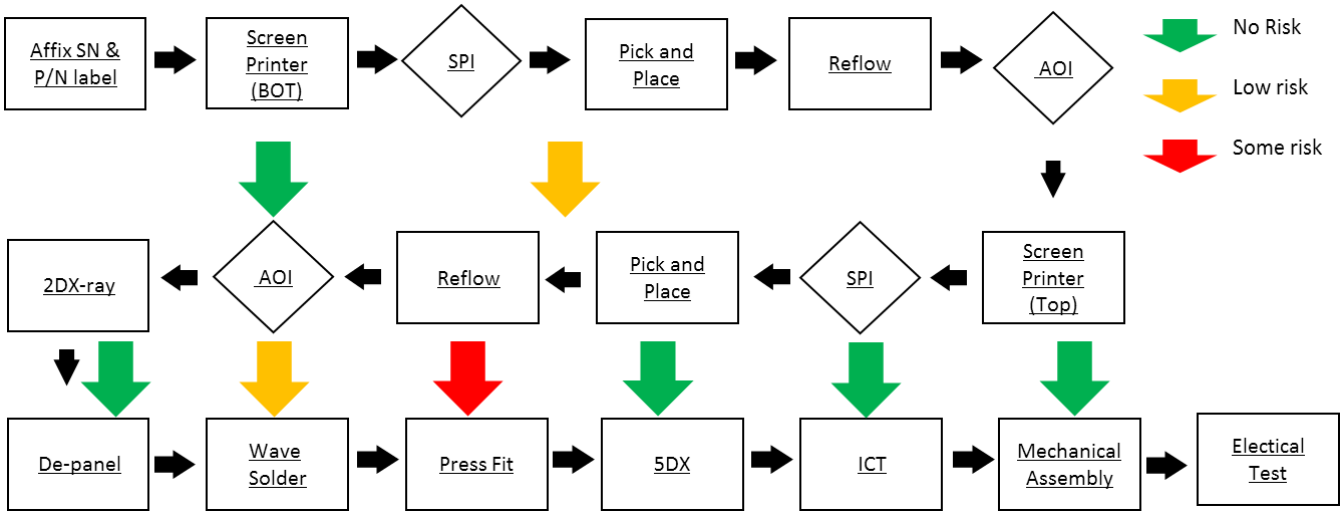

Figure 4. Assembly Process Flow with risk level

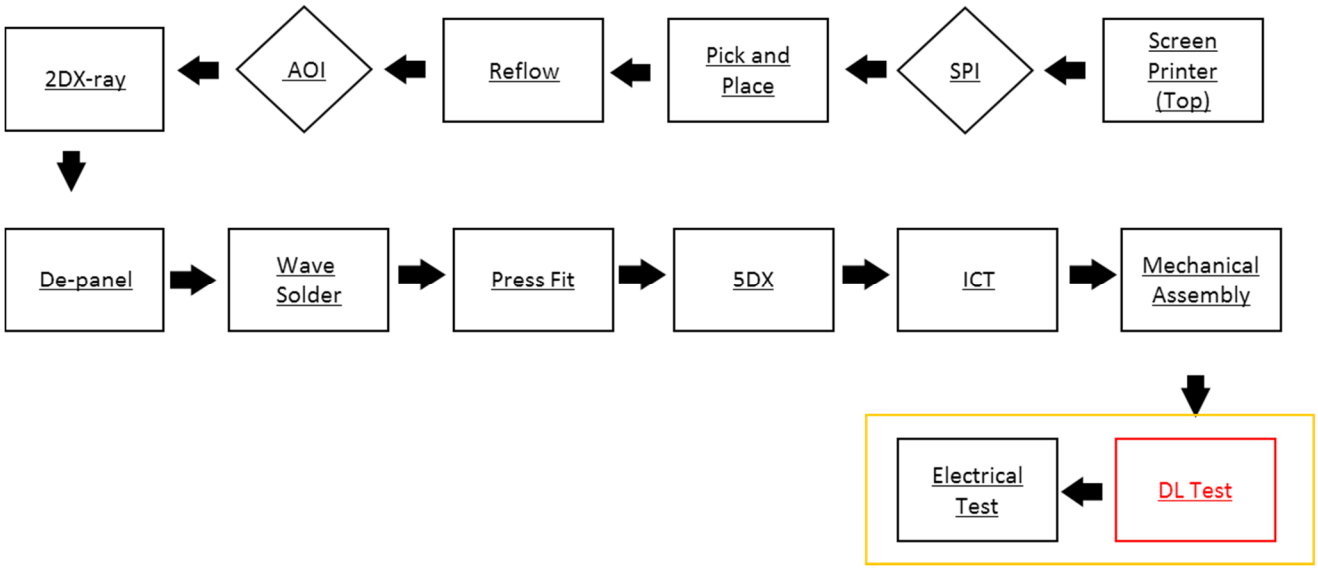

Figure 5. Modified assembly process with additional DL test

After split B went through the DL test, the passing boards resumed the press-fit process, then re-run the DL test again. Any new failure proved scenario 2 happened.

Split C was used to demonstrate if "P" was damaged during the pick and place process as scenario 1. "P" was taken out manually by ESD proved tweezers from the board after "P" was placed on board at the pick and place machine. They were immediately shipped and tested by supplier ATE test.

Table 2. Design of Experiment to isolate the problematic area

Split	Quantity of "P"	Split Detail	Purpose
A	480	Assemble as usual	Control Experiment
B	480	Same process as group A but skip the press-fit process. Resume the press-fit process after completing the DL test.	Any "P" failure means ESD happens in either scenarios 1 and 3 No "P" failure means ESD happens in scenario 2
C	103	"P" are taken out from board after pick and place	Any "P" failure means ESD happens in scenario 1

C. Results of Design of Experiment (DoE)

Table 3 lists the test results of splits A, B, B (PF) and C. Split A, as expected, had "P" damaged during the assembly, component failure rate of 1.46% that is a bit higher than the past. Split B had zero failure without the press-fit connector, however, one "P" failure was reported after the boards completed the press-fit process, failure rate was 0.21%, which is relatively low compared to previous, but the yield data in next few builds strongly prove the effectiveness of the mitigation. Another 103 parts of "P" from split C were tested by supplier final test program with 0 failure.

Press-fit station was highly suspicious where ESD event happens on "P". We re-visited the press-fit station and identified a few suspicious areas which require "more than S20.20" ESD control.

Table 3. Results of Split A, B (before and after press-fit) and C

Split	Quantity of "P"	# of Failure @ DL	# of Failure @ Electrical Test	"P" Failure Rate
A	480	7	7	1.46 %
B	480	0	NA	0 %
B (PF)		1	1	0.21%
C	103	All pass supplier's ATE test		0 %

D. Deep Dive of Press Fit Process

Press-fit is a process that presses a contact terminal, for example an external interface connector, into PCB. This technology was first introduced in the telecommunication industry in the 1970s [3]. It is a very common process used in networking products for years. This is a manual process that an operator takes a connector from its tray and placed onto PCB, connector is then pressed into PCB under a controlled target pressure.

Connectors are unavoidably required in the product design, which are defined as essential insulators in the EPA. They are usually designed with very "good" dielectric, thus it exhibits very high surface voltage. These connectors and their trays were sitting at least 50 cm (20 inch) away from any PCBA (PCB Assembly) and the press area, which is beyond the S20.20-2014 [1] requirement. Operators are well grounded by the ESD floor. All the PCBA are sitting inside grounded ESD-compliant trays. Press-fit table is grounded. Technically, the working area is compliant to the S20.20-2014 requirement.

The connector used in the product has a metal cage holding a block of dielectric embedded with an array of small signal pins, which are used for high-speed signal connection. Plenty of measurement were conducted at the area to look for any possible sources of ESD in terms of surface voltage, ESD event count and charges with tools such as non-contacting electrostatic voltmeter, surface resistivity meter, ESD event detector, contact-type voltmeter and coulombmeter. Since measurement results vary from device to device, maximum data is reported in this paper. Observations are described as below.

a. Connector tray had a word "Antistatic" printed on the tray but it shows off-scale surface voltage, beyond 2000 V (Figure 6). Supplier was later found not to have any proper and effective outgoing inspection test to verify the "Antistatic" properties.
b. Connector inside the tray is charged, the electrostatic voltage can have several hundred volts (Figure 7).
c. Connector signal pin area exhibits tens of surface voltage when connector is held by a grounded operator.
d. Charges with maximum value of 2.9 nC was measured on signal pins when connector is sitting inside tray (Figure 8).
e. Charges with maximum value of 1.7 nC was measured on signal pins when connector is held by a grounded operator (Figure 9).
f. Charges with maximum value of 0.40 nC was measured from the other end of trace when connector is pressed into PCB demonstrating that there is a direct charge transfer from the connector signal pin to the networking chip (Figure 10), there was no alternate path.

Figure 6. Surface field >2000 V was measured on tray marked with 'Antistatic'

Figure 7. Surface voltage of -411 V on connector metal cage

Figure 8. At maximum 2.9 nC charges were measured from connectors sitting inside tray

Figure 9. At maximum 1.7 nC charges were measured on signal pins held by grounded operator

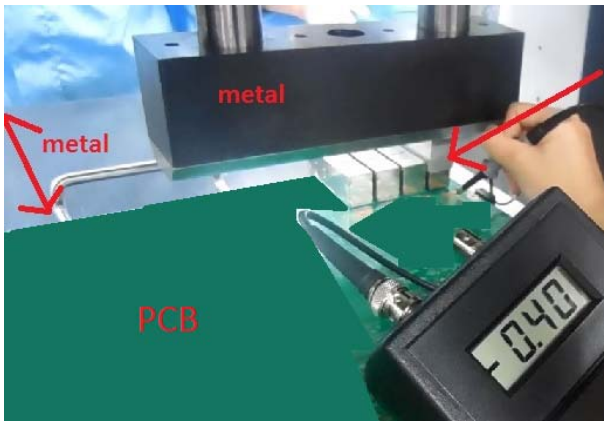

Figure 10. 0.40 nC charges were measured from the other end of trace when connector is pressed into PCB

E. Analysis

Connectors have been sitting inside a high charging tray with high surface voltage for many days and hours, a lot of vibration and friction happened on the connector, lots of charges were induced on the signal pins. Non-contacting voltmeter meter was used to measure the voltage of signal pins area of connectors immediately out of the box, as high as 324 V was measured as shown in Table 4. Due to the limitation and capability of the non-contactor voltmeter, the actual voltage of the signal pin could be much higher than 324 V.

Table 4. Surface voltage of connector varies from connector to connector, voltage >80 V is reported.

	#1	#2	#3	#4	#5	#6	#7	#8
Volt (V)	136	118	187	117	91	236	324	204

First of all, when a grounded operator holds the connector metal case, it grounds the external case, but the signal pins or ground pins are isolated by the connector dielectric with volume resistivity of 10^{14} ohm-cm. Grounding the case does not neutralize charges on the signal pins.

Secondly, the PCB trace connecting the connector pins and "P" is a very short trace without any extra components or test point for testing purpose. If the signal pins carry charges and come into contact to the trace connected to "P" with solder. The current path would be GND→ "P" → Trace → Connector signal pins or vice versa depending on the polarity of the charges on the connector pins.

Thirdly, the Vias on PCB for the signal pins are back-drilled for better signal integrity, when the board is sitting on a grounded fixture, the Vias do not have physical contact to the fixture. There is no alternate path to shunt the discharge current. All the charges go through "P" to ground as Figure 11.

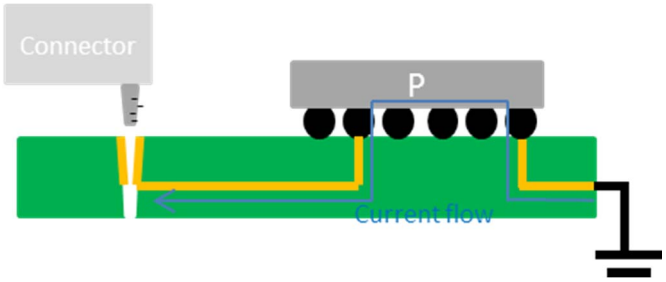

Figure 11. Direct discharge from the connector through P to the ground. If the positive charges are accumulated on the connector, the current flow will be in an opposite direction.

IV. Corrective Action and Validation

Due to unwanted charges induced on the connector signal pins, process changes were immediately implemented:

i. Connectors are taken from the tray and placed on ESD grounded table map with ionizer air blowing towards signal pins of connectors

ii. All connectors have to be sitting under ionized environment for over 5 seconds

iii. Unused standby materials have to be placed at least 1 meter away from the ionized area where connectors sitting

Another build was started immediately to validate the corrective action under the normal manufacturing process flow and speed. It was reported zero failure out of 960 pieces of "P". The result proved that the corrective action was effective. Table 5 shows the aggregate component failure of boards A, B and C before and after ionizer is implemented.

Table 5. Aggregate Component Failure Rate among Boards A, B & C without and with ionizer

	Boards		
	A	B	C
Without Ionizer	1.04%	1.11%	1.48%
With Ionizer	0.11%	0.00%	0.86%

V. Further Discussion

A. CDM vs S20.20

Both S20.20-2014 and IEC 61340-5-1:2016 state that the ESD qualification test is to establish a baseline of susceptibility data for device comparison. The ESD withstand voltage determined by these tests does not necessarily represent the ability of the device to withstand ESD from real sources at that voltage level. [1] [2] The CDM level qualified per component becomes a meaningless value to the factory or system design company because it cannot be used for the process assessment before project starts or until the issue is discovered.

At the same time, both IEC61340-5-1:2016 and ANSI S20.20-2014 state that activities compliant to the standards could handle parts over 200 V CDM. [1] [2] However, the case reported in this paper is about a component passing 200 V CDM in a S20.20-2014 certified factory having high component failure rate with classic CDM failure signature, which disagrees with the statement. Unfortunately, CM generally like to take this statement as a reason to push back for any further ESD improvement or investigation.

It is necessary to understand the real CDM discharge at the factory to setup a correct CDM testing environment for component qualification as well as clarify the relationship between CDM passing level of a component and S20.20-2014.

B. Definition of "Antistatic" or "Low Charging"

"Antistatic", also known as "Low Charging", is commonly used in ESD products. However, there is no clear definition of properties and testing methodology of "Antistatic" materials. In this case, the supplier measures surface resistivity instead of surface field potential. Per the Packaging standard ANSI/ESD S541, it is stated that there is no correlation between resistance measurements and the ability of a material to be antistatic. Apparently, this is not fully understood by the industry.

Also, there is no standard of the shelf-life of ESD-coated material which may become an ESD threat if the coating material deteriorates and wears off. The lack of traceability in packaging creates quality control problem since it is impossible for CMs to know the actual life usage of the ESD packaging for immediate ESD risk mitigation.

C. Future Challenges

Technology roadmap shows that the speed of high-speed I/O almost doubles for each generation, meaning that the CDM level is dropping. [4] This ESD case study already pre-alerts the industry this issue may be getting serious. Connector is considered as non-sensitive component, which does not have any ESD concern. Technically it does not violate any ESD standard. However, it becomes a risk when it is assembled with other highly sensitive component in CMs. ESD packaging should also be applied to non-sensitive components. CMs are no longer be able to manage this problem alone by being compliant to S20.20 standard, system design companies should jointly solve this systematically along the supply chain from the design for both sensitive and non-sensitive components like connector, manufacturing process step and more than S20.20 ESD control. New technology should be explored together to look for holistic solution.

VI. Conclusion

This paper reports an ESD issue with a networking component passing 200 V CDM having high manufacturing failure in a S20.20-2014 certified manufacturing floor. Root case is a direct discharge from connector to the high-speed interface signal pin of a networking chip at the press-fit assembly process. Ionizer and packaging improvement implemented has proved that it could dramatically reduce the number of failure in the manufacturing process.

It is suggested that S20.20 or IEC61340 standards to address the challenges reported in the paper. Further work is needed to investigate the gap of real ESD event at factory floor versus component-level ESD test as well as clear definition and test methodology of "antistatic" material.

References

[1] ANSI/ESDA, S20.20-2014

[2] IEC 61340-5-1, Edition 2.0 2016-05

[3] Joakim Mattsson et. al., "Press-fit Technology", White Paper, TE Automotive, July 2014

[4] R. Wong, R. Fung, and S.-J. Wen, *"Networking industry trends in ESD protection for high speed IOs,"* in Proc. IEEE ASIC Conf., 2013, pp. 1–1