Window Effects in HBM and TLP Testing

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Abstract – We present a study of products showing systematic window effects during HBM and TLP testing. It is shown that the window effects are mainly the consequence of race conditions between different ESD current paths. Window effects are sometimes difficult to detect, but are in principle relatively easy to prevent.

I. Introduction

Window effects are often mentioned in discussions about ESD qualifications and ESD problems [1]-[9]. Such claimed effects are often not documented. [7]-[9] show one actual window effect each, in HBM, TLP and System Level ESD, respectively. Often the reason for the window effect is not discussed.

In the context of this paper a device exhibits a window effect, if ESD qualification and/or characterization results show a failure window. We use the definition of failure window as given in [4], with the addition that, mutatis mutandis, it can also be applied to TLP data: An intermediate range of stress voltages that can induce failure in a particular device type, when the device type can pass some stress voltages both higher and lower than this range. For example, a component with a failure window may pass a 500 V test, fail a 1000 V test and pass a 2000 V test. Hence, the failure window of the device is between 500 V and 2000 V.

Often window effects are suggested when, in a series of passing results, there is a single failing sample. Single fails are very difficult to analyze. In such cases, 'window effect' is possibly a description of the data, but not an explanation. In this paper, we only discuss repeatable window effects. This implies that for all cases many more than the minimum number of samples have been used and more than 1 failure was observed. After the presentation of four different case studies, the cases will be compared and generalized. This leads to a discussion of risk of missing an existing ESD failure window and possible actions to avoid the occurrence of ESD window effects. The paper finishes with conclusions of this study.

II. Case studies

A. Product A (90 nm)

A regular HBM qualification showed one sample failing at 500 V. A second round of stresses on fresh parts again produced a fail, only at 500 V. Statistics of further experiments, illustrated in Figure 1, show a very narrow failure window, having the highest probability to fail at 450 V and a quite low failure rate at 500 V. As illustrated by the number of samples used there is no doubt that there is a real window effect in these results.

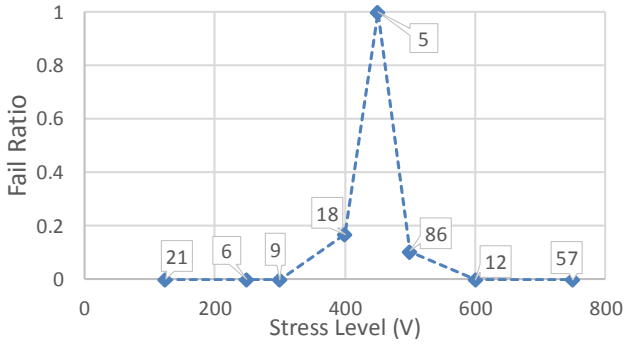


Figure 1: Failure rate at different HBM stress levels. Data labels indicate the number of stressed samples at a specific level.

As shown in Figure 2, FA reveals a classical drain-source filament in a device connected to the bond pad.

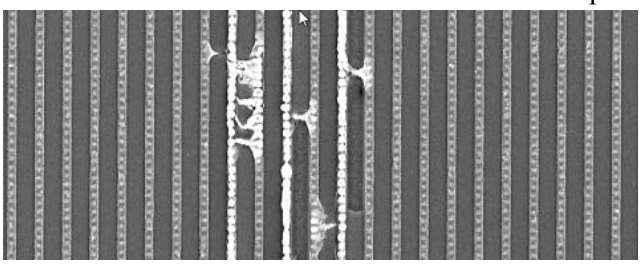


Figure 2: SEM photograph of HBM induced damage.

With 100 ns TLP (T_r = 10 ns), the problem could not be reproduced, but long pulse TLP (pulses longer than 200 ns) replicates the misbehavior at each investigated device. Furthermore, TLP in the reverse stress direction, i.e. starting from high level and decreasing to lower levels, clearly confirmed a window effect at low stress level. This is shown in Figure 3, where the TLP curve for increasing stress shows the window to start at 0.22 A and the TLP curve for decreasing stress shows the window to end at 0.36 A.

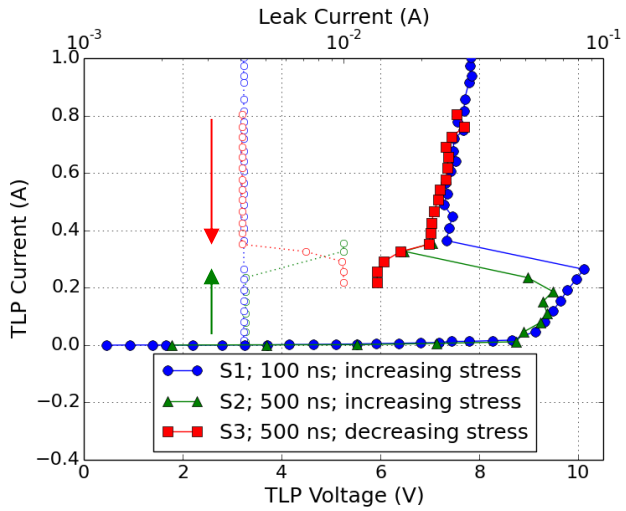


Figure 3: TLP results, illustrating the window effect.

The fact that 100 ns TLP does not reproduce the fail, while longer pulse TLP does, clearly shows that the problem is related to the duration of the stress. Note that the full HBM stress lasts longer than 100 ns, even when most of the energy is dissipated within this time. Transient voltage waveforms from the decremental TLP, shown in Figure 4, just before fail and at the fail level show the triggering of the primary protection and the parallel, weak ESD path. Note that the parallel path triggers at ~ 150 ns and is fully conducting after ~ 200 ns, and thus is not visible in regular TLP.

Further experiments with a 2-pin HBM tester also reproduced the issue. Thus, (known) tester artefacts [4] can be excluded as a root cause. Just as with TLP, a window effect was demonstrated by starting HBM stressing at a high level and decreasing the level until a failure was observed. Using 20 V steps the 2-pin HBM tester results demonstrated that the failure window was between 420 V and 520 V HBM.

The 2-pin HBM system allows to measure the voltage and current as function of time during the HBM pulses. Two stresses, at the edges of the HBM window, are shown in Figure 5. The 420 V HBM waveform shows the same decrease around 200 ns as the long pulse TLP. The 520 V waveform shows the same correct triggering as the corresponding long pulse TLP. The voltage response also shows that the turn-off of the primary protection, approximately at 450 ns, does not lead to a voltage that triggers the destructive path.

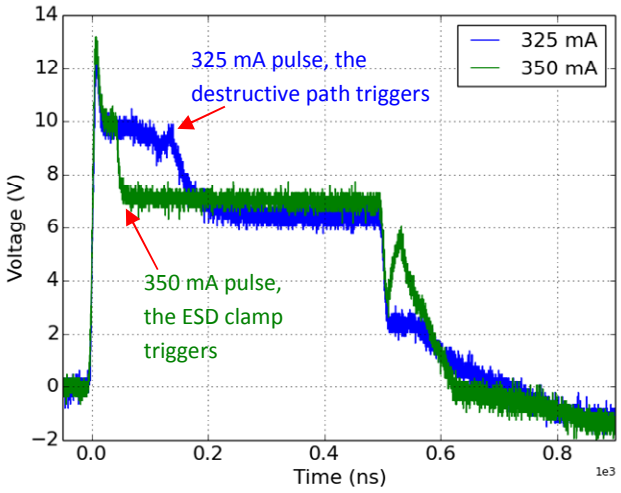


Figure 4: decremental TLP: waveforms just before and at failure.

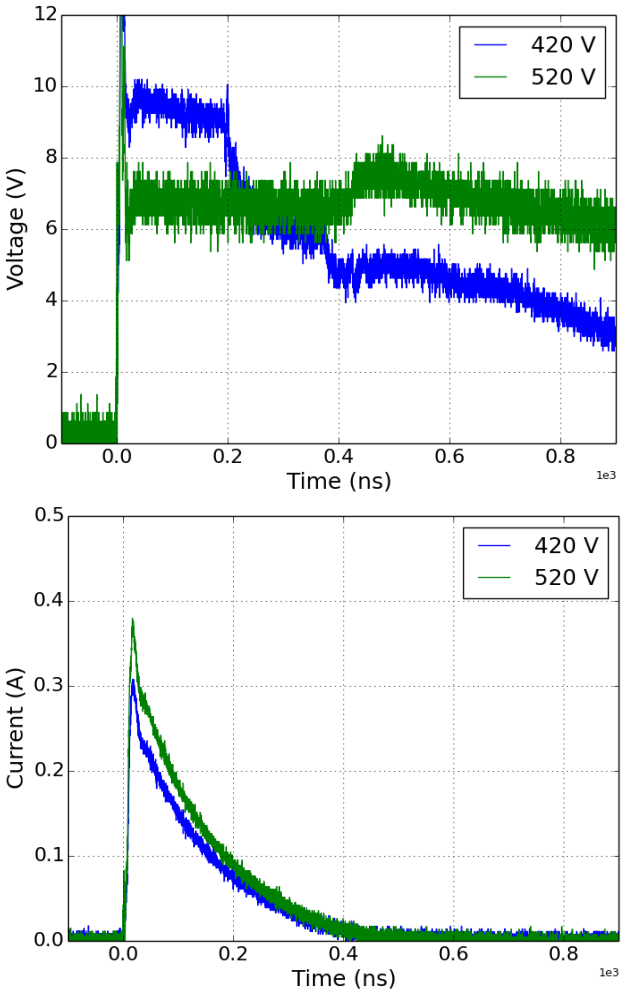


Figure 5: Voltage (top) and Current (bottom) as function of time for HBM stresses at the low and high boundaries of the window.

Data shows that the destructive path is obviously slower and has a slightly lower trigger voltage than the dedicated ESD protection. There is a competition between these two paths and, as the HBM data shows, there is a statistical distribution on which path triggers first. Such a competition between two different paths for the ESD current will be called a race in the remainder of this paper.

Even knowing the failing devices, the destructive ESD path is not completely understood. Figure 7 presents the simplified schematic by pointing to the damaged NMOS devices, as well as showing the critical stress-combination. It is important to notice that stress to the Vss pin or other pins do not show a window effect. This means that the decoupling capacitors at the internal nodes can be excluded to be the main part of the destructive ESD path.

Four improvement measures were implemented:

1. Decrease of the trigger voltage of the main ESD protection
2. Limitation of the ESD current through a single finger of the damaged NMOS devices
3. Reduction of substrate current injection by
   (a) changed guard ring connection and
   (b) changed substrate connections
4. Active charging of the internal nodes behind the damaged NMOS devices

Obviously the first measure addresses the primary protection, while measures 2-4 aim at making the circuitry to be protected less sensitive. Measure 2 is an implementation of the technique described in [10]. Measure 3 consists of 2 ways to limit local substrate voltage differences near the failing devices. Measure 4 effectively limits the voltage across the failing devices during an ESD event.

HBM ESD qualification and long pulse TLP proved that the implemented measures solve the window issue. TLP data, shown in Figure 6, demonstrates that lowering the trigger voltage was clearly achieved and most likely prevents triggering of the destructive path.

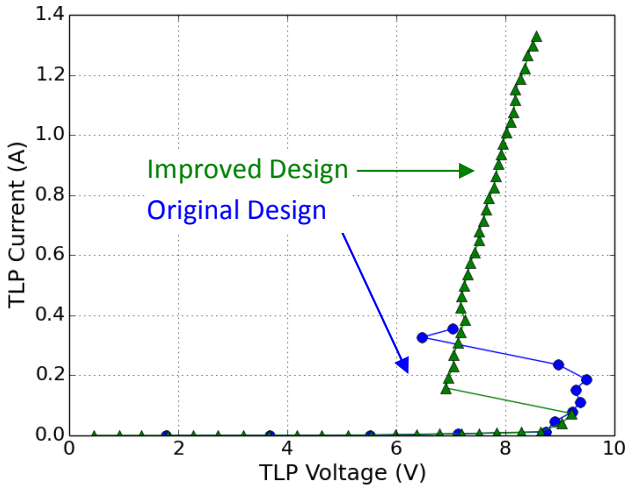


Figure 6: 500 ns TLP of weak and improved design.

To investigate which of the improvement measures was the most relevant one, additional experiments were carried out. In a series of experiments several of the measures were removed. This was done by several FIB circuit modifications. All experimental versions were stressed up to failure with 500 ns TLP. The results are collected in Figure 8, which shows the full curves and a zoom in for the critical region around the trigger condition. The redesign with all 4 measures included fails at 4A (500ns TLP). An important finding is that also without the reduced trigger voltage, the product now survives the snapback and reaches relatively high failure levels. Nevertheless, it is also clear that the robustness decreases if one or more of the other measures is inactivated.

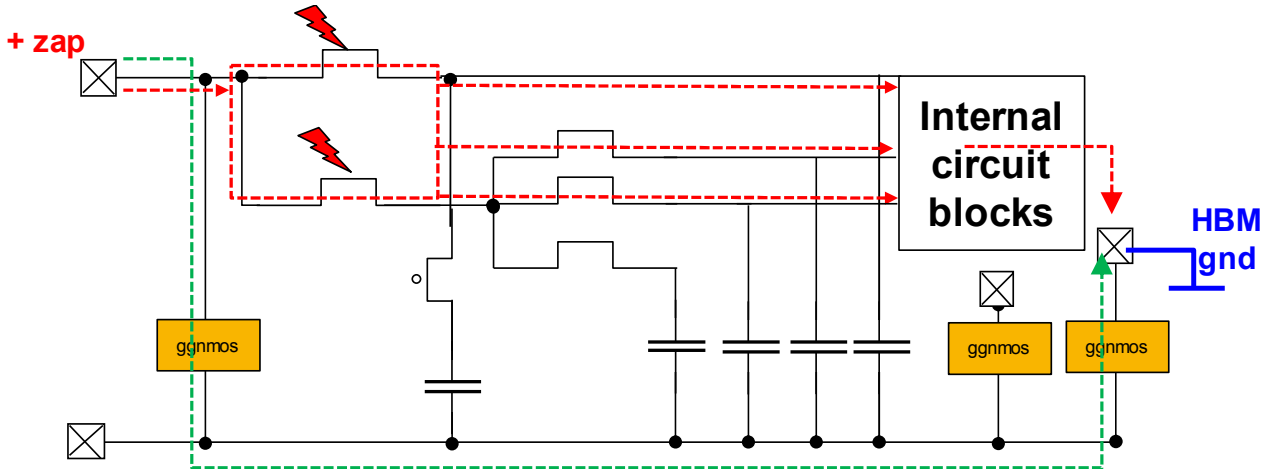


Figure 7: Simplified schematic pointing to the damaged NMOS devices and the critical stress setup. Green line represents the designed ESD path, the red line points to the destructive path. Decoupling Capacitors of the internal nodes to gnd are shown.

Apparently, improving the substrate connection and limiting the voltage across the victim device are the most effective. However, only together they are sufficiently effective. Since the reduced trigger voltage is a more general solution, clearly this one must be implemented in every new design.

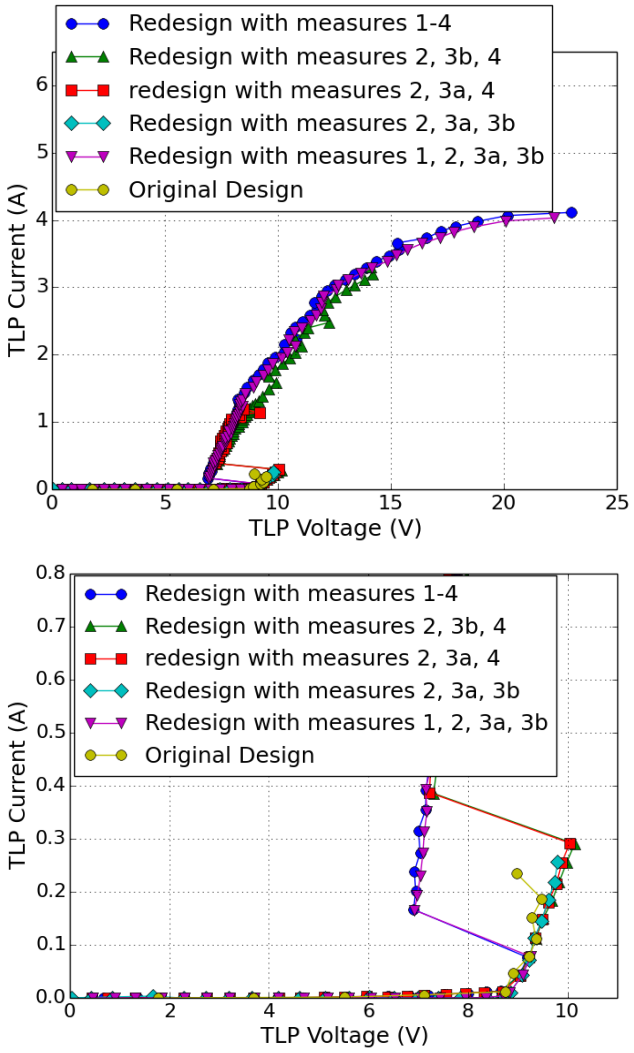


Figure 8: 500 ns TLP results of experiments, all shown up to last good point (top) and zoom in for trigger regime (bottom).

This example illustrates that window effects can occur and can be difficult to analyze, even if the failure is reproducible. For the analysis, it was of key importance to find a simple way to reproduce the failure mode. Without the 500 ns TLP the analysis would have taken much more time and effort.

B. Product B (180 nm)

A mixed signal chip was HBM stressed at 0.5, 1.0, 1.5, 2.0 and 2.5 kV. All samples passed, except 1 sample stressed at 1.5 kV. To exclude incidents, more samples were stressed at 1.0, 1.5 and 2.0 kV. Fails were observed for samples stressed at 1.5 kV. In total 4/10 failed, all with increased leakage in a certain power domain. Four new parts were stressed on only that domain: two failed for positive stress.

Figure 9 shows TLP results of a good and a bad sample. A distribution that seems to depend on the voltage needed to trigger all fingers of the protection appears to exist. If the protection does not trigger correctly, the core circuitry experiences a high voltage (~8 V) for 100 ns and fails. A TLP characterization was started at high current level (2 A) and with steps decreased to just above 1 A. No fails were observed. The same sample was stressed again, now starting from low levels. The product failed at 0.7 A, which clearly demonstrates a window effect.

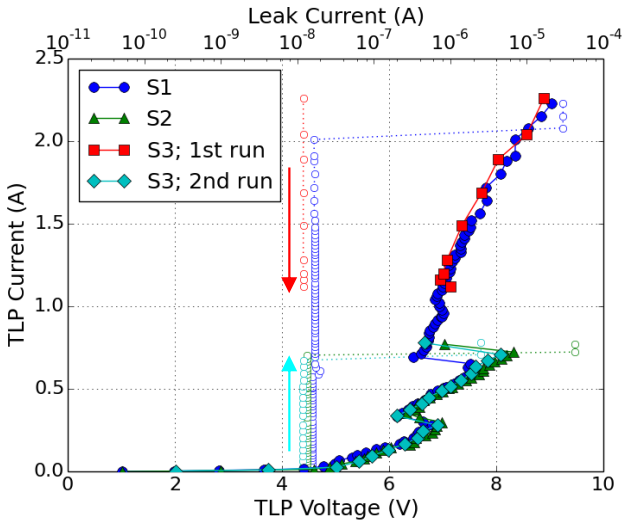
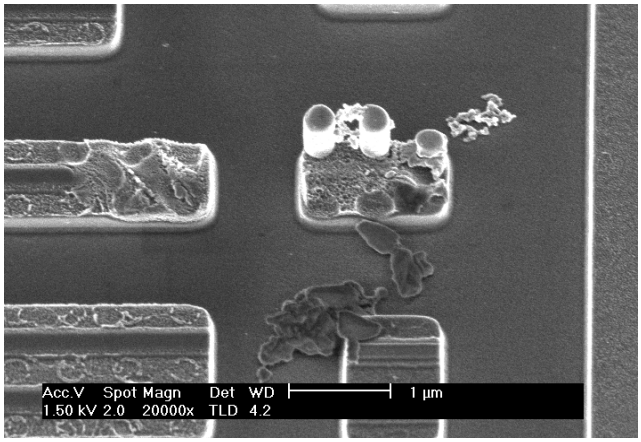


Figure 9: TLP characteristics, illustrating the window effect.

Figure 10 shows FA results of a sample stressed by HBM and a sample stressed with TLP. Both samples showed damage on the same internal buffer, suggesting that a parasitic thyristor between supply and ground had triggered.

It can be concluded that the window effect is due to a competition between complete triggering of the multi-finger supply protection and triggering of the core circuitry. The multi-finger behavior is clearly visible in the TLP curves of Figure 9. If the supply protection does not turn on completely, the trigger voltage of the internal circuitry is reached for HBM voltages around 1.5 kV and the product fails. At lower stresses, the voltage does not reach the internal trigger level and at higher stresses the chance of uniform supply clamp triggering is higher, because of the dV/dt reduced clamp trigger voltage. Because of time-to-market and the relatively high failure level, the performance was accepted as is. The datasheet was adapted. The product was used for years without customer returns related to this issue.



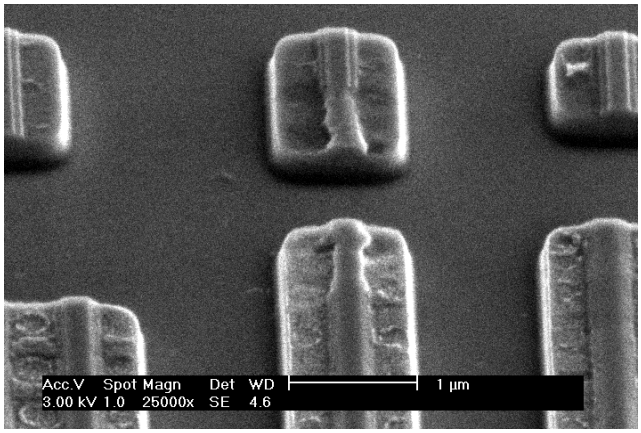


Figure 10: SEM photograph of damage due to HBM stress (top) and TLP stress (bottom).

C. Product C (55 nm)

This case study has similarities with the previous one. This design contained a mix of third party IP and in-house custom design. The original HBM qualification run only showed fails at 1750 V and not at other levels. Further investigations were done to understand the problem. This resulted in 16/16 fails at 1750V and 1/9 fails at 2000 V. The critical stress was positive stress on 2 identical IO pins versus GND. All stresses at other levels and for negative polarity showed passing results (at least 9/9 pass per condition). The FA result in Figure 11 shows a very clear filament in an output driver NMOS.

Subsequent TLP characterization, shown in Figure 12, demonstrated a very similar race as in the previous example. The region around 0.7 A is the most critical, since the quasi-static voltage is equal to the junction breakdown voltage. A 100 ns TLP current of 0.7 A corresponds to ~1 kV for a voltage driven failure and to ~1.4 kV HBM, for a dissipation based failure [11]. Since the 'snapback' around 0.7 A occurs gradually, it is likely that a second conduction path starts to conduct more and more with increasing stress.

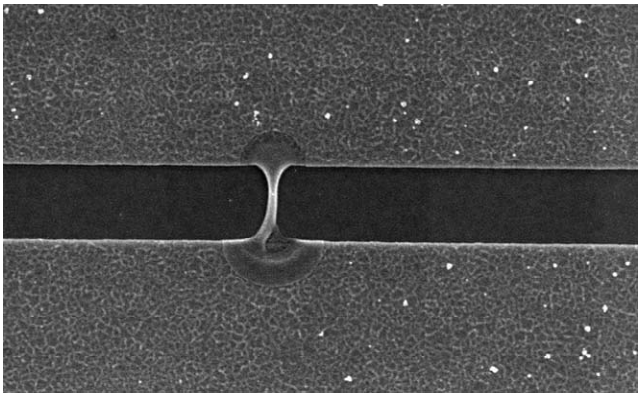


Figure 11: Backside SEM photograph of damaged NMOS.

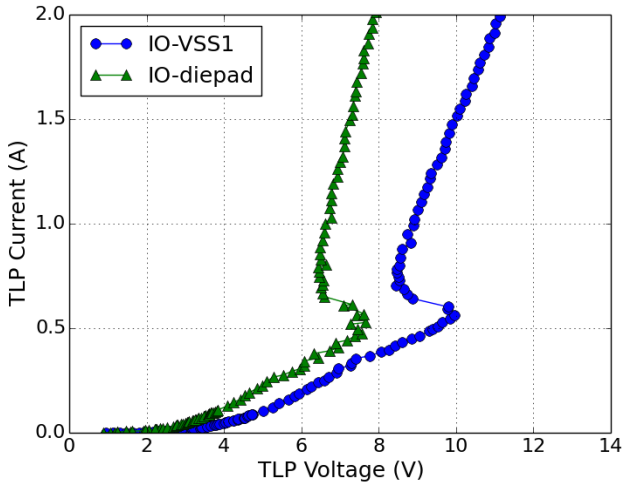


Figure 12: TLP characteristics of failing IO to 2 different GNDs.

A basic schematic of the relevant part of the circuit is shown in Figure 13. Analysis of the circuit design clearly shows that a race condition is possible. The competing paths are indicated by the colored lines in Figure 13. The intended protection path is highlighted in dashed green, while the problematic path is indicated in dotted red. Similar paths that could have been critical had been made robust by using silicide blocked NMOS's (indicated by the lightning bolt symbol). This explains why this output driver fails and others do not. Clearly this indicates that this path, which multiplexed third party and in-house IP, was overlooked by the design team.

Interestingly, similar investigations on a more modern HBM tester and on a 2-pin HBM tester did not reproduce the fail. It is not fully understood why the first tester consistently produced such damage. The HBM standard [4] allows choosing the favorable result. Nevertheless, the root cause is that the design is not optimal and can be improved by a relatively easy change. It was decided to implement such a change.

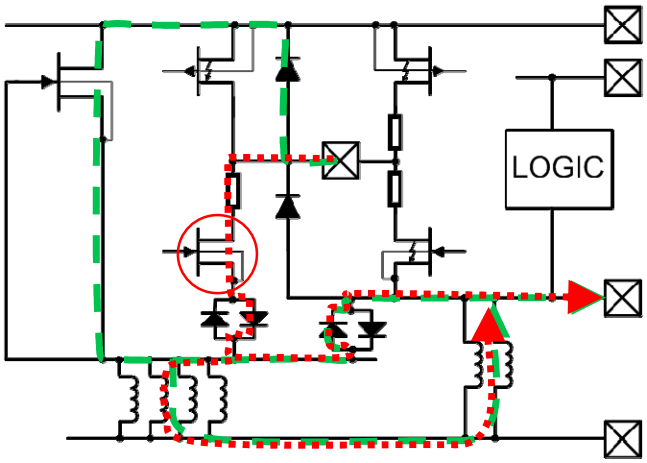


Figure 13: ESD network with indication of current paths. Red circle indicates damaged transistor. The dashed green path indicates the primary protection path, while the dotted red path indicates the ESD current flow that causes the damage.

D. Product D (140 nm)

A product with a rail-based protection strategy, using an RC triggered active NMOS clamp, failed product qualification at 500 V HBM. All higher levels to 2 kV HBM showed no problems. Analysis of the ATE results showed that all fails were on the same domain. The ATE data indicated increased current consumption in that domain. Failure analysis, illustrated in Figure 14, showed that the damage was in the large NMOS of the active clamp, which agrees with the electrical failure signature. This is typically an indication of a trigger problem, especially when this happens at normal stress levels.

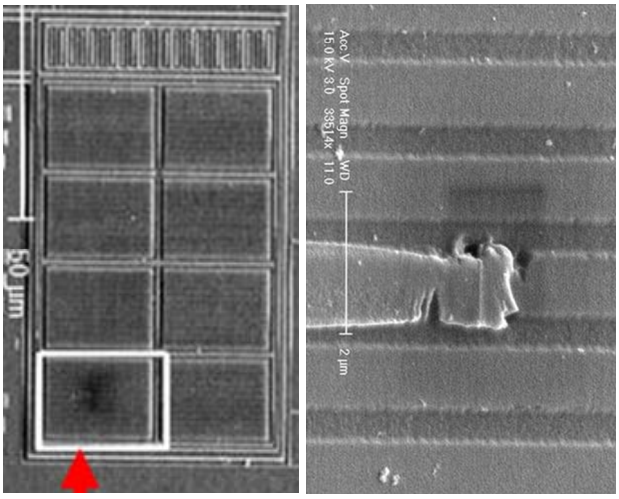


Figure 14: Failure analysis of a damaged supply clamp.

It is well known that trigger problems can be related to HBM tester artefacts [4]. However, since also TLP produces the failure, as can be seen in Figure 15, it can be concluded that this behavior is not caused by the parasitic capacitance tester artefact of the HBM tester. The results clearly indicate that for a certain stress, the active clamp does not trigger and the voltage increases to the trigger voltage for bipolar action. The device most likely to trigger will be the NMOST rail clamp.

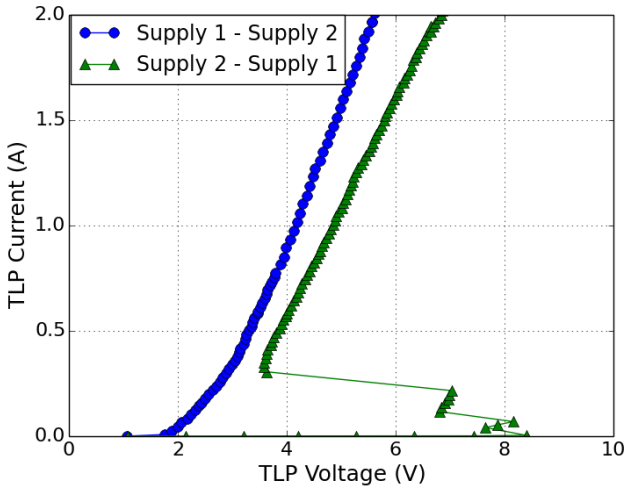


Figure 15: TLP characteristics in both current directions between two supply pins.

The clamp used a slew-rate controlled trigger circuit. Simulation on a stand-alone clamp, with and without inclusion of layout extracted parasitic capacitances, showed the problem was due to capacitive loading. Figure 16 shows that for low current stress the clamp does not trigger correctly and consequently the voltage increases to dangerous levels.

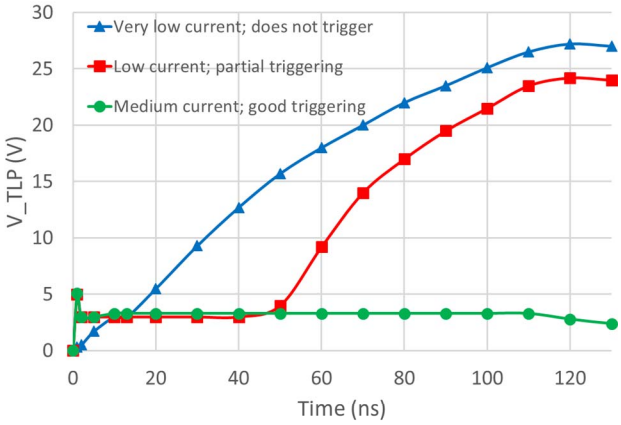


Figure 16: Spice simulation results of the supply clamp.

The trigger circuit was improved by increasing the RC time of the slew-rate detector. This makes the design less sensitive for capacitive loading. Figure 17 shows the simulation results of the improved design, for the

same conditions as those in Figure 16. Clearly the clamp now also reacts at the low current stress levels.

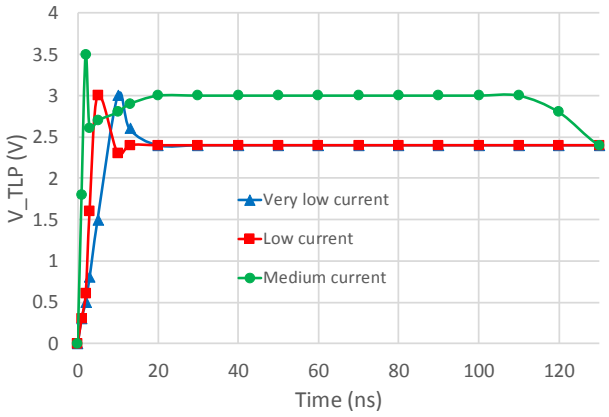


Figure 17: Spice simulation results of the improved supply clamp.

HBM qualification on a next version of the product did not reveal any issue. The improved clamp design has been used in multiple products of varying size without any problems.

III. Discussion

All presented cases of window effects were discovered by further analysis of regular qualification fails. As demonstrated one of the cases had a fail window width of just 100 V. However, in most cases the window is larger than that. Thus, the chance that an extremely small window is completely missed is relatively small.

Nevertheless, window effects of less than a step size wide have a chance to be overlooked. Since the standards [4] suggest a progressive step size towards higher qualification levels, the chance of failing to detect a small window increases at those levels. Evidently the risk of failing to detect windows in general is reduced by using smaller step sizes.

Rather than detecting a window during product qualification, it is better to minimize the chance that a window effect is present. For this pre-qualification of IO libraries and IP blocks on test chips can be very useful. In addition, TLP characterization can yield very useful insight in potential window effects.

The presented cases all indicate that window effects are related to some form of a race condition between ESD protection network and device or circuit to be protected. The race condition can be either voltage driven or timing driven.

Since the trigger condition of snapback-based protection often is governed by the same avalanche mechanism as the damage condition for the protected circuitry, such race conditions occur more often in snapback ESD protection strategies.

Based on the analysis in many cases window effects can be prevented by careful design of the ESD strategy. For snapback-based protections, it must be ensured that the trigger voltage of the primary protection is clearly less than the trigger voltage of the circuitry to be protected. A design strategy should focus on comparison of potential parallel paths with the primary protection discharge path. Netlist inspection tools can be used to compare the type and number of elements in competing paths. As an example, the primary protection path for case C contains two diodes and an *ESD robust* thick oxide transistor. One of the parallel paths contains 2 diodes and a *regular* thick oxide transistor. This should flag a warning in the verification tool. If snap back device models are available, it is also possible to simulate such race conditions. However, models including all details associated with dynamic triggering effects are quite rare and often not physics based, implying that they may not work well in situations that differ from the calibration structures. It is e.g. difficult to include layout aspects, such as the distance to substrate contacts (case B) and the delayed triggering (case A).

Since rail-based strategies can be simulated in more detail, it is easier to guarantee the absence of critical races for these types of strategies. For rail-based RC-triggered protections, it can be ensured, by extensive simulations, that the trigger circuit will be activated under all relevant conditions with respect to slew-rate, process corners and capacitive loads. Furthermore, it is possible to simulate HBM events on relevant pin combinations to verify if the total voltage over all circuitry to be protected remains sufficiently low.

IV. Conclusion

For the first time, case studies of window effects in ESD qualifications are presented and analyzed. It is shown that typically window effects are related to critical race conditions in the ESD current paths.

The windows can be as small as 100V, which makes it difficult to guarantee absence of pass/fail windows in regular ESD qualifications. Based on the experience of the authors the chance of occurrence of such windows is small. The best indication for presence of a window effect is one or more fails at a single default stress level. A single fail should never be classified as a window effect without further analysis. Obviously, classification as a window effect does not change the pass/fail conclusion.

ESD testing and TLP characterization at and around that level gives insight into the nature of the window effect. Increased confidence in the absence of windows is obtained by applying a qualification strategy with finer steps.

Very refined versions of simulation and EDA tools are needed to cover all demonstrated forms of window effects, but some may be caught by existing methodologies. With these the risk of introducing ESD windows can at least be minimized before first silicon is made.

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References

[1] K.T. Kaschani and R. Gaertner, 'The Impact of Electrical Overstress on the Design, Handling, and Application of Integrated Circuits', Proceedings EOS/ESD Symposium, 2011, pp. 220-229.

[2] A. Amerasekera and C. Duvvury, 'ESD in silicon integrated circuits', Wiley, 2002.

[3] C. Duvvury and H. Gossner, 'System Level ESD Co-design', Wiley, 2015.

[4] ANSI/ESDA/JEDEC JS-001, Human Body Model (HBM) - Component Level.

[5] R. Steinhoff et al., 'Current Filament Movement and Silicon Melting in an ESD-Robust DENMOS Transistor', Proceedings EOS/ESD Symposium, 2003, pp. 98-107.

[6] B. Keppens and G. Wybo, 'Using the Voltage and Current Waveforms from VFTLP systems to study transient device behavior', Proceedings RCJ Symposium, 2006, pp. 173-182.

[7] J. Lebon et al., 'IEC vs. HBM: How to Optimize On-Chip Protections to Handle Both Requirements', Proceedings EOS/ESD Symposium, 2009, pp. 358-363.

[8] G. Boselli et al., 'The Relevance of Long-Duration TLP Stress on System Level ESD Design', Proceedings EOS/ESD Symposium, 2010, pp. 31-39.

[9] A. Salman et al., 'Mutual Ballasting: A Novel Technique for Improved Inductive System Level IEC ESD Stress Performance for Automotive Applications', Proceedings EOS/ESD Symposium, 2013, pp. 133-13.

[10] A.J. Huitsing, et al., 'A Simple Design Methodology for Increased ESD Robustness of CMOS Core Cells', Proceedings ESSCIRC, 2003, pp. 481-484.

[11] G. Notermans, et al., 'Pitfalls when Correlating TLP, HBM and MM Testing', Proceedings EOS/ESD Symposium, 1998, pp. 170-176.