Implementation Methodology of Industrial and Automotive ESD, EFT and Surge Generator Models which Predict EMC Robustness on ICs and Systems

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Abstract - This paper presents a novel methodology to develop and validate disturbance generator models for a virtual EMC lab. New simulation models for ESD, EFT and Surge stimuli have been created and verified on a wide range of load conditions.

I. Introduction

Prior to chip manufacturing and testing, designers want simulation models to evaluate circuit robustness to electromagnetic disturbances. Prediction by simulation is key to avoid costly chip re-design and associated time to market constraints. Prediction by simulation also allows IC designers and their customers to ascertain full system EMC robustness. With this in mind, novel disturbance generator models were developed to form part of a virtual EMC lab. The underlying circuit model topologies rely on a comprehensive characterization methodology. The suite of EMC tests reviewed includes Electrostatic Discharges (ESD), Electrical Fast Transients (EFT), and Surge industrial and automotive stimuli specified in IEC61000-4-2/4-4/4-5, ISO10605 and ISO7637-2/3 [1-5]. Existing publications on simulation models focus mainly on the IEC61000-4-2 discharge [6-11]. Their scope varies and their main focus is to replay the disturbance as specified in the specification only. In this work, comprehensive and accurate models have been implemented and verified over a wide range of load conditions. The analysis also highlights some of the standards' imprecisions, showing that the use of different test equipment may result in different pass/fail EMC results. Section II of this paper explains the methodology used in the model creation and validation. Sections III, IV and V concentrate on the ESD, EFT, and Surge stimuli. Each section details the model topologies, and shows the excellent correlation between simulation and measurement for a wide range of loads. Full system simulation and coupling-decoupling mechanisms are also considered. The focus is on the model topology definition but does not claim detailed implementation of the widely varying equipment design.

II. Model Implementation and Validation Methodology

Accurate disturbance models for SPICE simulation should give reliable predictions independent of the load conditions. The model topology validation methodology developed in this work is described here after:

1) Preliminary generator models based on specifications and prior art were developed and combined with a SPICE simulation test bench.
2) Evaluation circuit boards with components of different values were designed and manufactured. The suite of load components used in this study is summarized in Tables 1 and 2. The boards were modeled using different methods to ensure that the simulation results are independent of the board parasitics. These methods include the definition of a lumped board element equivalent circuit as well as the extraction of an EM model with EMPro [12].

Resistive loads
2.2 Ω
10 Ω
47 Ω
100 Ω
330 Ω
470 Ω
1 kΩ

Capacitive loads
10 pF
100 pF
150 pF
470 pF
4.7 nF

Table 1 & Table 2: Evaluation board load components.

3) A lab measurement phase followed. EMC transients were injected into the boards with different resistive and capacitive impedances. To account for measurement variations, envelope waveforms were recorded for each load/voltage-discharge configuration. In this study, over 15 test variations and 37 test voltages were used; over 10000 individual measurements were performed. Currents were measured using a CT1 current probe from Tektronix and a TESEQ [13] MD300 for the surge analysis. Different current probes were evaluated for the current measurement of the ESD events, many were unsuitable due to their frequency range or their current saturation limit; as an example, the CT6, also from Tektronix, entered current saturation during the ESD current measurement, reporting lower than expected current values after 30ns. Voltages were recorded via a 4kV LeCroy voltage probe.
4) The measured current and voltage waveforms were overlapped with the simulated data. A good overlap for all loads studied either validated the models or indicated the scope for enhancements and iteration of the generator models.

III. ESD Models as per IEC61000-4-2 and ISO10605

A. Standards Considerations

The IEC61000-4-2 and ISO10605 specifications describe system-level ESD immunity tests. IEC61000-4-2 defines the industrial test. ISO10605 is the automotive specification that details four discharge scenarios dependent on the injection location and coupling method. In this study, measurements were taken using two pieces of equipment, both aiming to reproduce the ESD pulse according to IEC61000-4-2: a TESEQ NSG438 gun [13] and an IC test system, a Langer P331 probe hooked to a BPS203 burst power station [14]. Both test set-ups are shown in Figures 1 and 2.

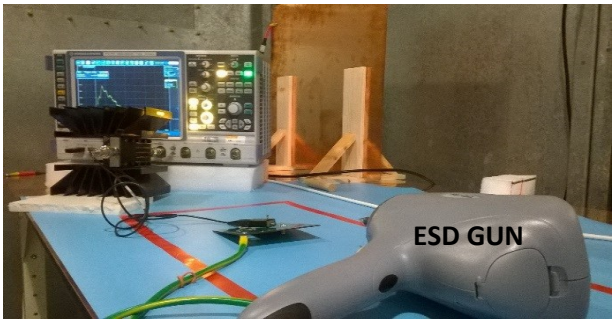

Figure 1. ESD gun test set-up.

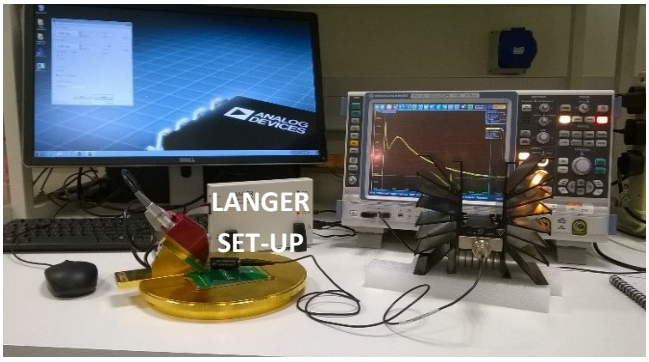

Figure 2. Langer probe test set-up.

The specifications definition and characteristics of the discharge current waveform are limited to a load ≤2.1Ω. Figures 3 and 4 show the comparison between a TESEQ NSG438 discharge and a Langer P331 discharge. One can observe good agreement between the critical waveform parameters of IEC61000-4-2, i.e. rise time, I_{peak}, I_{30ns} and I_{60ns}, delivered by the gun and the probe into a 2.2Ω load. However, for high resistive loads, one can see a large discrepancy in the I_{peak} values supplied by the two systems as shown in Figure 4 for a 1kΩ load. This rules out any assumption that system-level test equipment and IC-level test equipment deliver the same current waveforms, whatever the load condition. If one translates this finding to the simulation arena, one can understand that while many models do re-create the current waveform given in the standards for loads R≤2.1Ω, these same models may not reproduce the ESD gun discharges for different load conditions. The specifications need to be more "specific". Only a measurement-to-simulation correlation study on a broader spectrum of resistive and capacitive loads can close the gap and allow for more accurate current and voltage predictions.

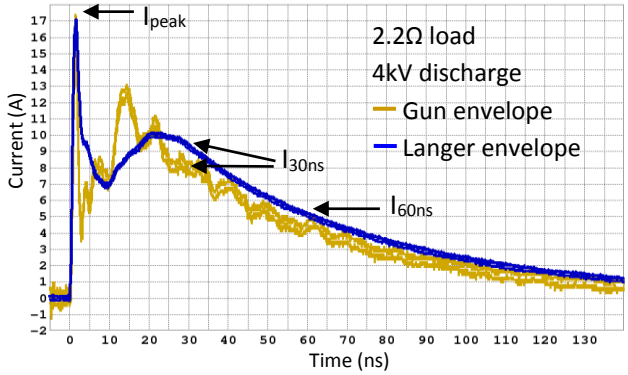

Figure 3: Comparison of current waveforms for a 4kV discharge from a TESEQ NSG438 gun and a Langer P331 probe into a 2.2Ω load.

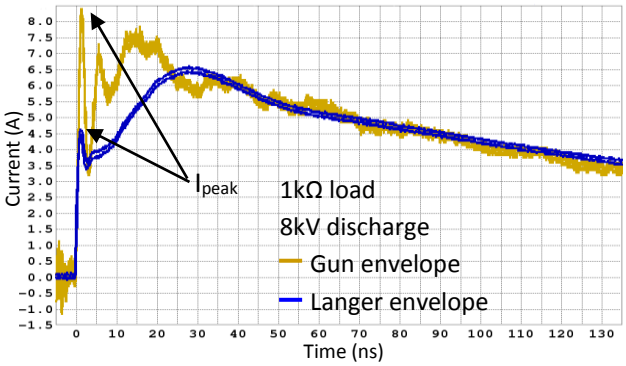

Figure 4: Comparison of current waveforms for an 8kV discharge from a TESEQ NSG438 gun and a Langer P331 probe into a 1kΩ load.

B. Model Internals

Models were implemented for both the TESEQ NSG438 gun and the Langer P331 probe. The model for the gun is captured in the simplified gun schematic displayed in Figure 5. The model consists of a slow network, which houses the 150pF and 330Ω network described in IEC61000-4-2 [1], a fast network to re-create the first peak and a tip parasitics network inspired by [7]. The waveforms from the four networks presented in ISO10605 [2] can be modeled as follows: the capacitor C can be changed from 150pF to 330pF, for discharges occurring inside the vehicle; the resistor R can be varied from 330Ω to 2kΩ where the discharges occur directly through the human skin.

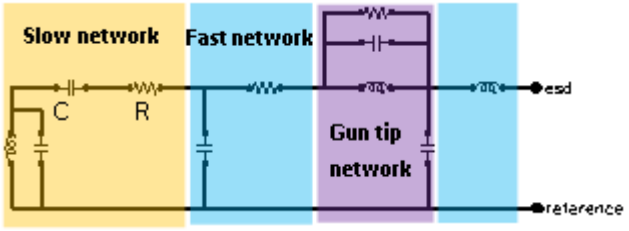

Figure 5: Simplified ESD TESEQ NSG438 gun model schematic.

The Langer probe model is shown in Figure 6.

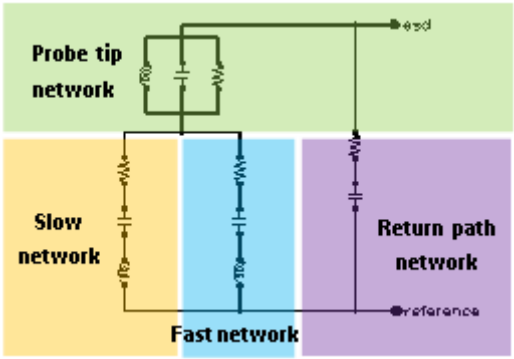

Figure 6: Simplified ESD Langer P331 probe model schematic.

C. Model-to-Measurement Agreement

Figures 7 to 9 demonstrate the good agreement between the gun measurement and the proposed gun model. One can see that the peak rise times and current values, I_{peak}, I_{30ns} and I_{60ns} are well matched between measurement and simulation for the different load conditions. The gold curves represent the envelope waveforms of the measurements, the dark blue curves are the simulated data. Reasonable agreement is not limited to the presented data set but extend to the entire test range.

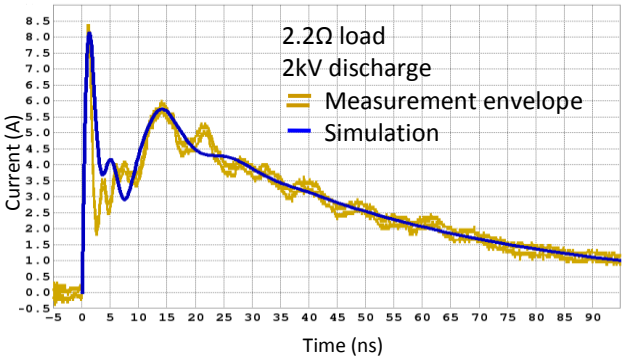

Figure 7: Measured current from the TESEQ NSG438 gun discharges compared to simulation data into 2.2Ω for a 2kV discharge.

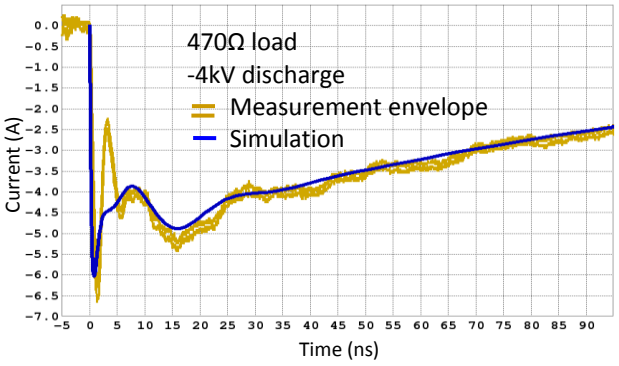

Figure 8: Measured current from the TESEQ NSG438 gun discharges compared to simulation data into 470Ω for a -4kV discharge.

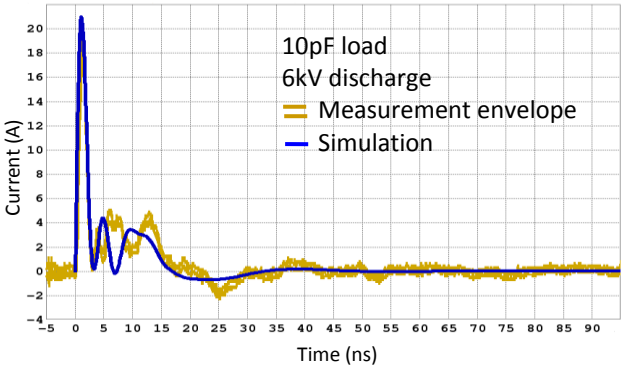

Figure 9: Measured current from the TESEQ NSG438 gun discharges compared to simulation data into 10pF for a 6kV discharge.

While evaluating the IEC61000-4-2 model-to-measurement correlation for a 330Ω load, the model seemed to under-estimate the current for this load (green and dark blue curves in Figure 10). Discharges were also recorded with a second TESEQ NSG438 gun (gold envelope curves in Figure 10), the modeled data overlaps very well with the measured data from this second gun. Any small deviation of the 330Ω network resistor from its expected 330Ω value will show up as the largest model-to-measurement discrepancy when performing the discharge into a load match of 330Ω. One should however note that the two guns tested are well within specification for the 2.1Ω calibration load, as the tolerances for I_{30ns} and I_{60ns} values are very wide, i.e. ±30%.

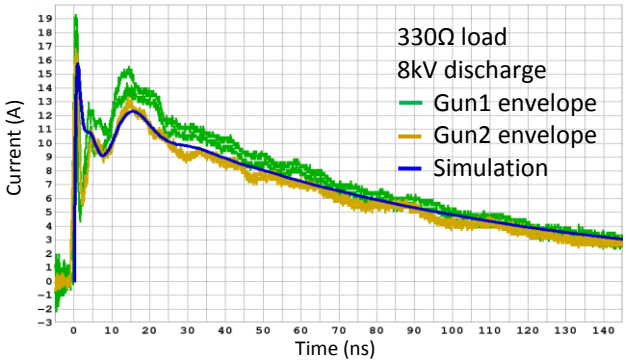

Figure 10. Comparison of IEC61000-4-2 discharge measurements from two TESEQ NSG438 guns and simulated data into a 330Ω load.

Figures 11 to 13 display measured current ESD waveforms from the Langer P331 probe, overlaid with the Langer simulated data for different load conditions. Good agreement between measurements and model data can be observed.

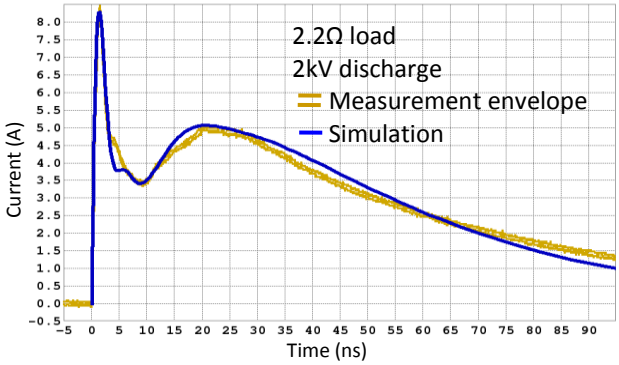

Figure 11. Measured current from the Langer P331 probe discharges compared to simulation data into 2.2Ω for a 2kV discharge.

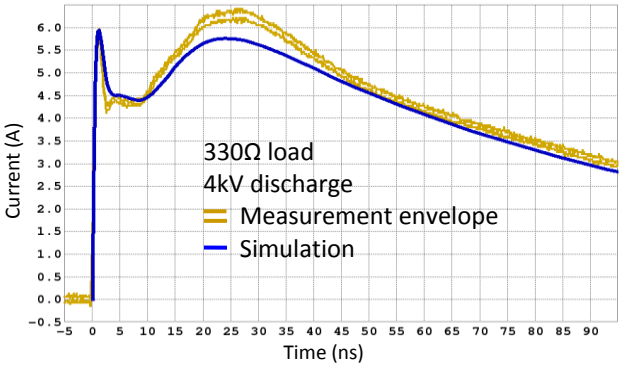

Figure 12. Measured current from the Langer P331 probe discharges compared to simulation data into 330Ω for a 4kV discharge.

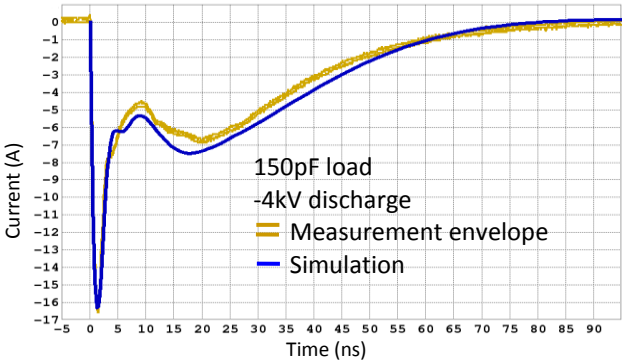

Figure 13. Measured current from the Langer P331 probe discharges compared to simulation data into 150pF for a -4kV discharge.

D. Comparison with Other Existing Models

The accuracy of the proposed model over existing models, is particularly demonstrated in the case of high resistive loads and low capacitive loads. These situations can arise, for example:

- When the equipment under test (EUT) is very small, giving a small coupling capacitance to the ESD table set-up, this capacitance will dominate the capacitive load of the EUT.
- If the ESD protection scheme chosen is to be of very small area (which can be the case when a size constraint exists for the total chip/board area).
- If the ESD protection scheme chosen is slow to turn-on (which can be the case when the protection device is large).

In many cases, the impedance of an EUT at the location where the IEC discharge is to be delivered is not known; therefore a model accurate for any load condition is necessary to enable system robustness prediction. Figures 14 and 15 display measured IEC discharges on a high resistive load and a low capacitive load, comparing the proposed model with

other available ESD gun models. Only the proposed model agrees with the measured data.

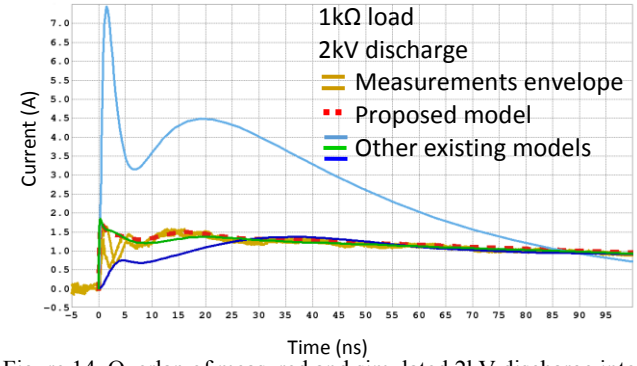

Figure 14. Overlap of measured and simulated 2kV discharge into a victim circuit of 1kΩ.

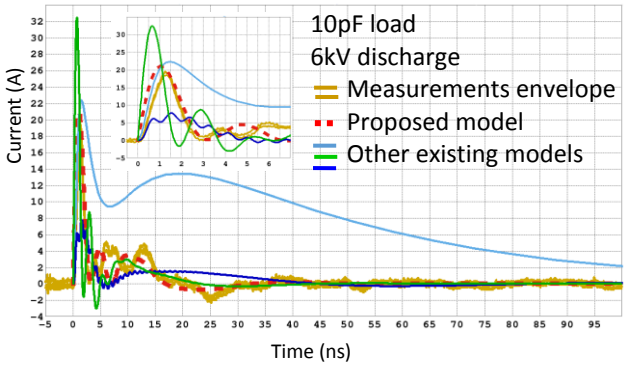

Figure 15. Overlap of measured and simulated 6kV discharge into a victim circuit of 10pF. Inset: zoom on 1st ESD peak.

IV. EFT Models as per IEC61000-4-4 and ISO7637-2/3

A. Standards Considerations

Voltage transient events are often the result of contact arcing that occurs during mechanical or electromechanical switching of an inductive load as shown in Figure 16.

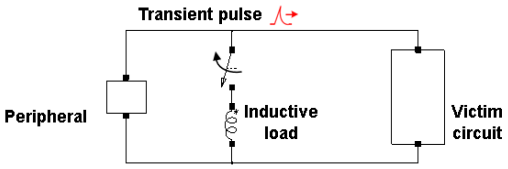

Figure 16. EFT source [15].

The industrial standard, IEC61000-4-4 [3], describes a fast pulse (5ns rise time, 50ns duration time). The automotive specifications ISO7637-2 and ISO7637-3 [4] give different pulses depending on the surrounding circuitry and on whether the EFT strikes a supply line or a signal line; these pulses have rise times ranging from the nano-second to the milli-second. Similar to the ESD standards, a too limited number of calibration loads are offered for each of the EFT pulses.

B. Test Set-up and Model Internals

1. Test Set-up

TESEQ NSG5500, NSG5600, FT5531 and MT5511 pulse generators [13] were used to stress the components described in Tables 1 and 2. The set-up is shown in Figure 17.

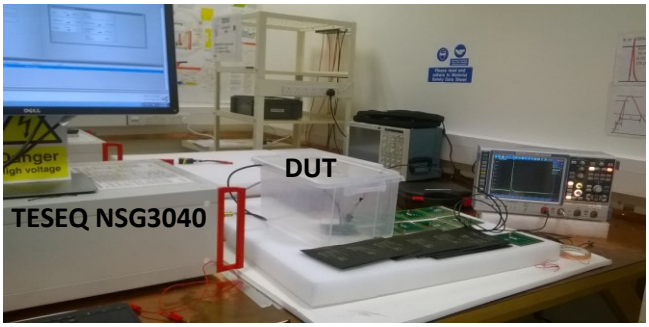

Figure 17. EFT test set-up for IEC61000-4-4.

TESEQ supplied pulse waveform verification loads with their pulse generator; EFT voltages were measured on these loads and are presented in Figure 18. One can observe two regimes in these voltage waveforms, differing from the smooth waveform displayed in the specification [3]. The simulation model has to replicate this behaviour, so as to reproduce the exact frequency contents of the EFT delivered to the evaluation board.

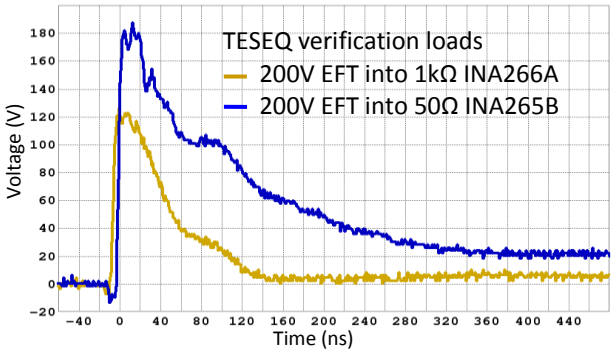

Figure 18. EFT voltage waveforms from the TESEQ NSG3040 into TESEQ INA266A/265B burst verification loads.

2. Model Internals

Eight different generator models were created to cover the full spectrum of EFTs mentioned in the IEC and ISO specifications. The IEC model, the fast pulse from ISO7637-3 and Pulse 1 from the ISO7637-2 are presented in this paper. The model topologies

developed for the three pulse generators are displayed in Figures 19 to 21. The models consist of a charging block, a shaping block to reproduce the given waveforms and a matching block to comply with the generator output impedance given in the specifications. A blocking sub-circuit is added to the IEC model as per specification; an undershoot block was necessary to replicate the ISO7637-3 voltage waveforms; and a decoupling block was required for the ISO7637-2 pulses as these EFTs are applied directly to power lines.

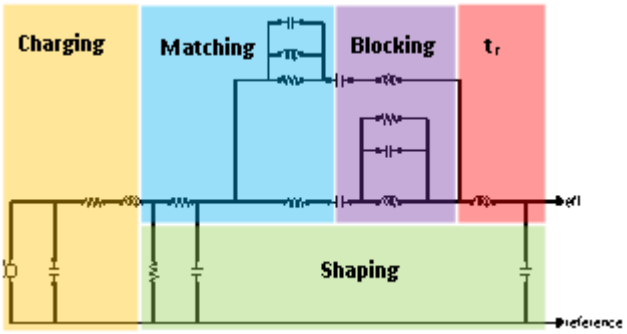

Figure 19. Simplified IEC61000-4-4 EFT generator model schematic.

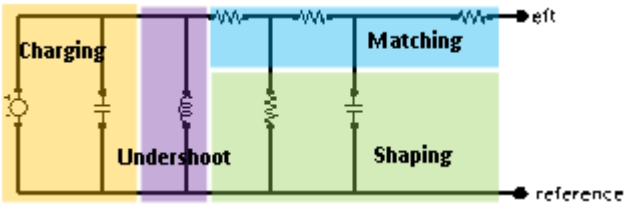

Figure 20: Simplified ISO7637-3 Fast EFT generator model schematic.

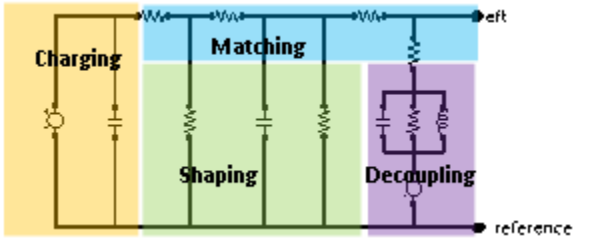

Figure 21. Simplified ISO7637-2 Pulse 1 EFT generator model schematic.

C. Model-to-Measurements Agreement

IEC61000-4-4 offers two calibration points, 50Ω and 1kΩ, while ISO7637-2 and ISO7637-3 merely give one calibration point for each of the eight pulses they specify. In this study, all loads mentioned in Tables 1 and 2 were tested, and good agreement between all measurements and the model data was observed, a representative set is shown in Figures 22 to 26.

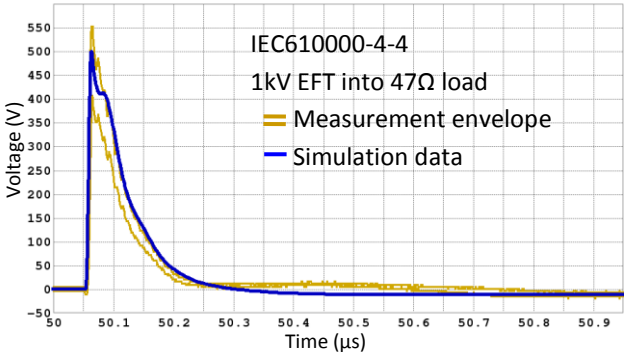

Figure 22. IEC61000-4-4 EFT measured voltage waveforms from the TESEQ NSG3040 compared to simulation data, EFT of 1kV into 47Ω.

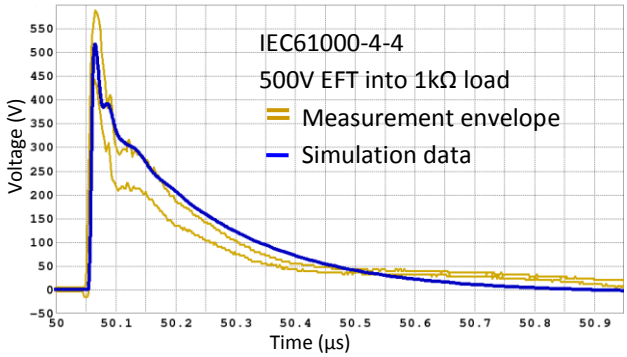

Figure 23. IEC61000-4-4 EFT measured voltage waveforms from the TESEQ NSG3040 compared to simulation data, EFT of 500V into 1kΩ.

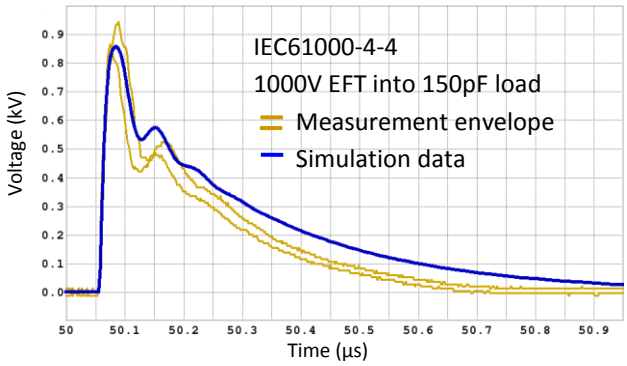

Figure 24. IEC61000-4-4 EFT measured voltage waveforms from the TESEQ NSG3040 compared to simulation data, EFT of 1kV into 150pF.

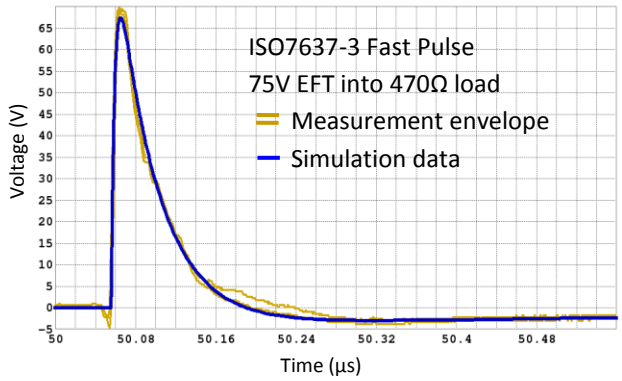

Figure 25. ISO7637-3 Fast EFT measured voltage waveforms from the TESEQ NSG5500 option FT5531 compared to simulation data, EFT of 75V into 470Ω.

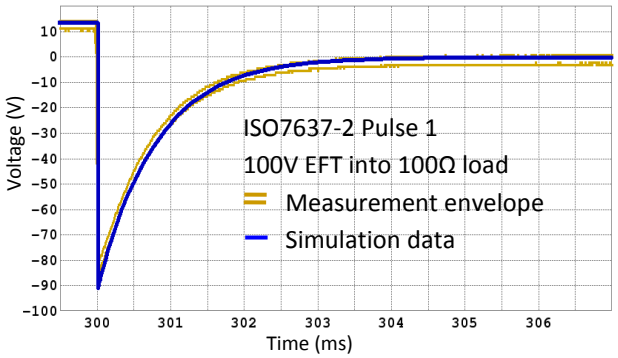

Figure 26. ISO7637-2 Pulse 1 EFT measured voltage waveforms from the TESEQ NSG5500 option MT5511 compared to simulation data, EFT of 100V into 100Ω.

D. Coupling Considerations

Different coupling techniques are proposed in the ISO and IEC standards [3,4]: direct capacitance coupling (DCC), capacitive coupling clamp (CCC) and inductive coupling clamp (ICC). The TESEQ CDN500 CCC and the TESEQ CIP9136A current probe used in the automotive test-bench, were modeled with the aim of simulating the full lab set-up. The objective is to model all test set-up ingredients accurately to provide exact final system predictions. The clamp models were extracted using EM solver solutions from EMCoS [16], the clamp layouts for the extractions are shown in Figures 27 and 28.

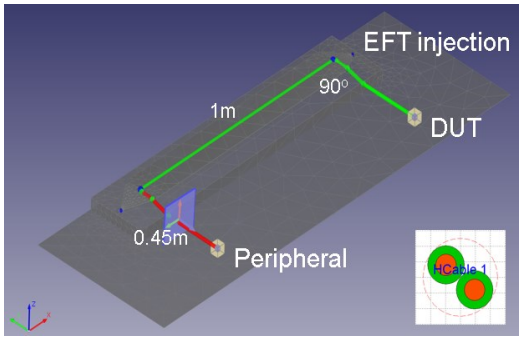

Figure 27. TESEQ CDN500 CCC model – inset: DUT to peripheral cable model.

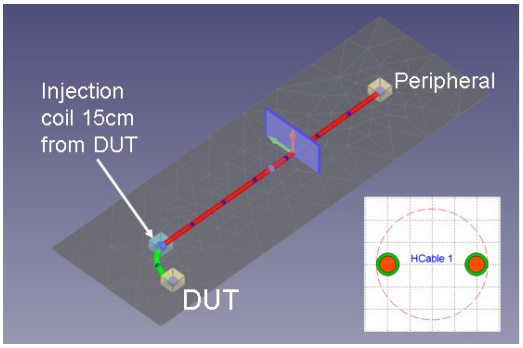

Figure 28. TESEQ CIP9136A ICC model – inset: DUT to peripheral cable model.

V. Surge Model as per IEC61000-4-5

A. Standard Considerations

The EMC IEC61000-4-5 [5] specification addresses the most severe transient conditions on both power and data lines. These are transients of high energy, with durations in the micro-second range, characterized by a rapid rise time followed by a slower fall time [17]. This modeling work reports on the 1.2/50µs combination wave generator (CWG). Different test configurations are detailed in the IEC61000-4-5 standard: open-circuit; short-circuit; 18µF coupling line-to-line; and 9µF + 10Ω coupling line-to-ground were investigated. One should note that this surge standard is by far the most detailed of the EMC transient specifications. It provides voltage and current waveform rise times, duration times and undershoots for different load conditions and different coupling/decoupling schemes.

B. Test Set-up and Model Internals

1. Test Set-up

The measurements were performed using a TESEQ multifunction generator system NSG3040 [13], the currents were measured using a TESEQ MD300 current probe. The test set-up is presented in Figure 29.

Figure 29. Surge test set-up.

2. Models Internals

Figure 30 displays the internal topology of the surge simulation model. Similarly to the EFT models, the surge transients can be modeled using charging, matching and shaping blocks. An undershoot functionality block is added to reproduce the current undershoot for low resistive load conditions.

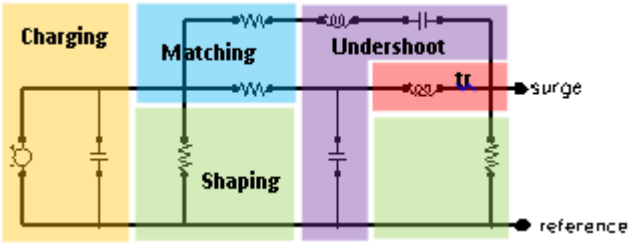

Figure 30: Simplified surge generator model schematic.

C. Model-to-Measurement Agreement

All voltages comparison between the measurements and the model data resulted in very good agreement between both set of data, for any load condition studied. An example for a 100Ω load is shown in Figure 31. Measured and simulated current overlay very well, with an exception for the short circuit condition where the model over-predicts the current undershoot as displayed in Figure 32. The model predicts a current undershoot of 19.4% of the current peak, the standard specifies $I_{undershoot}$ to be between 0% and 30% of the peak current. A literature research demonstrated that the model predicts an $I_{undershoot}$ closer to measured data when compared to other models [18,19].

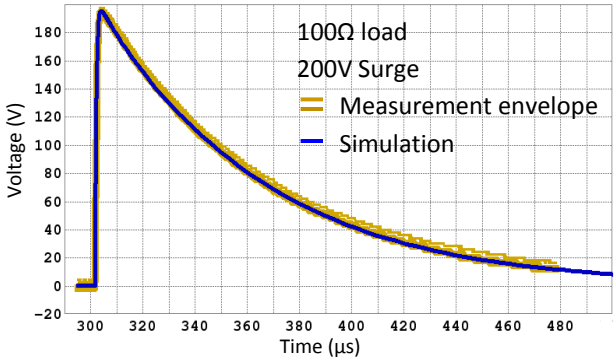

Figure 31: Measured voltage from the TESEQ NSG3040 compared to simulation data, surge of 200V into 100Ω.

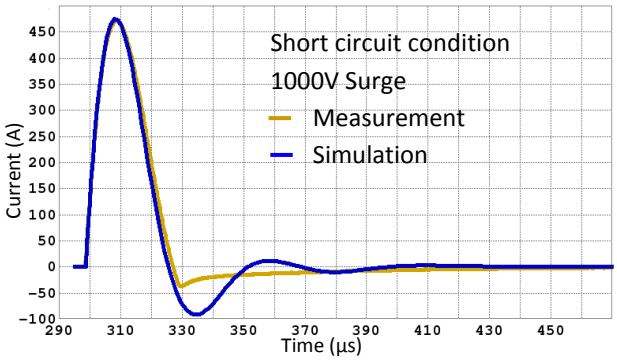

Figure 32. : Measured current waveform from the TESEQ NSG3040 compared to simulation data, surge of 1000V in short circuit condition.

Conclusions

A new EMC virtual lab has been created through the development of accurate transient simulation models. These models are being used in production and allow for system issue debugging, system layout and EMC protection scheme correction prior to tape out. In combination with the existing ESD IC-modeling solutions [20] and the development of package and board models, IC and system EMC robustness can be predicted.

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