High-Performance Bi-directional SCR Developed on a 0.13um SOI-based Smart Power Technology for Automotive Applications

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Abstract - Novel bi-directional SCRs have been developed on an advanced 0.13um SOI-based smart power technology. Leveraging the benefits of the SOI, the SCRs achieved high and adjustable Vh with new NBL/collector and base engineering techniques. Outstanding DC, TLP, IEC61000-4-2, and EMC performance were achieved for automotive applications.

I. Introduction

ESD protection for automotive application is usually required to provide high holding voltage (Vh) for latch-up immunity and reliability, in addition to high ESD robustness [1].

Bi-directional silicon controlled rectifiers (SCR) [2, 3, 4] are very attractive devices. They provide bi-directional ESD protection in a single compact device.

HV SCRs Vh is usually dependent on base doping concentration, Epi thickness, and collector/NBL doping concentration. These are not easily adjustable in bulk technologies [3, 4].

Developed on the latest 0.13um Smart Power technology [5] from NXP/Freescale, this work proposed bi-directional SCRs with high and adjustable Vh. The Vh-adjusting techniques include collector/NBL and base engineering of the bipolar(s) in SCR.

The reported Vh improving techniques include adding floating N+ diffusion in Nwell [6], and segmented emitter layout [7]. These techniques largely improved Vh, however at sacrifice of significantly reduced It2 and increased clamping voltage. [8] demonstrated a single-polarity SCR with a floating P+ region implemented on Anode side (in Nwell) of the device. Its Vh was improved by introducing avalanche breakdown between base and emitter junction of PNP inside SCR. While the concept is innovative, it could be challenging to be implemented in processes with shallow and abrupt P+/Nwell junction, prone to damages under stress.

NBL engineering in HV NPN and SCR has been discussed by a few articles [1], [9]. [1] described the Vh engineering of vertical NPN with diluted NBL. But the doping concentrations of mask layers are usually determined by the platform devices on a technology. And adjusting the doping is not always a feasible solution for ESD development in ICs. [9] presented good investigation work of NBL experiments on single-polarity SCRs. It covered single-polarity SCRs with NBL, with no NBL, with half-blocked NBL, or NBL at center of the devices. And it found single-polarity SCRs with no NBL or half-blocked NBL provided better It2 than the device with NBL.

Following the concept of NBL engineering, comprehensive study of bi-directional SCR has been conducted on SOI technology. It is realized, unlike single-polarity SCR, NBL is an integral part of bi-directional SCR even in SOI technology. NBL engineering is to be implemented with understanding of both bi-directional SCR and the SOI process, which will be detailed in chapter II and IV. With NBL partially removed in device to eliminate vertical operation of the device, about 20% Vh increase has been observed. The increase is

limited. However, it opens the door for further effective Vh improvement by adjusting lateral current flow with base engineering. By combining the NBL and base engineering technique(s), Vh can be doubled from the baseline design. Moreover, the proposed techniques only need layout change and do not consume additional die area as presented by some other works.

II. Novel Bi-directional SCRs

A. Device Architecture

We first built a baseline bi-directional SCR based on our development work [3, 4] on Freescale's previous generations of bulk smart power technologies. As shown in Figure 1, the device includes NPN transistors using Pwell as base regions. It has full NBL coverage connected to N-sinker, acting as the shared collector for them.

On either IO or GND side, there is a lateral NPN ($NPNL_F$ or $NPNL_R$) using Nsinker as the collector, and a vertical NPN ($NPNV_F$ or $NPNV_R$) using NBL as the collector. The device is laterally triggered by spacing Sp between Pwell and Nsinker in forward, and spacing Spr in reverse. Each NPN's base region (Pwell) encloses a P+ region as the base terminal, and an N+ region as the emitter. The base and emitter terminals are shorted, providing either the GND or the IO electrode. The parasitic PNP transistor would form SCR with the NPNs providing good ESD robustness.

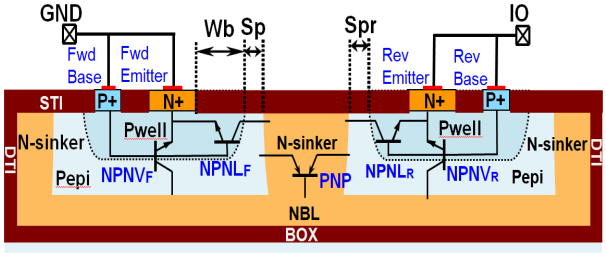
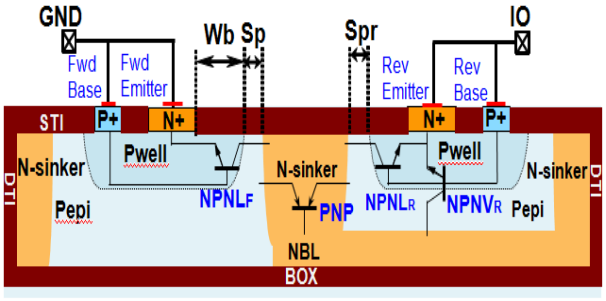


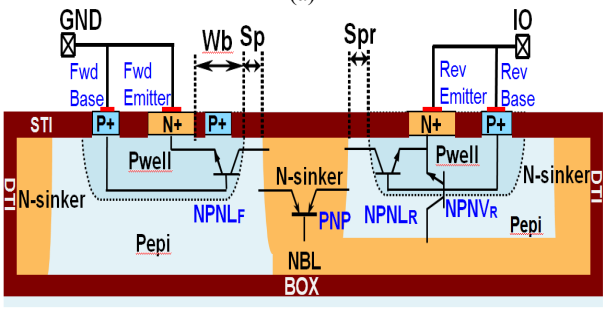
Figure 1: Baseline Bi-directional SCR with Full NBL on SOI Technology

While in bulk technologies, the devices rely on NBL to isolate them from P-substrate. SOI technology provides isolation with BOX (buried oxide), DTI (deep trench isolation) and STI (shallow trench isolation). This allows opportunity for NBL engineering to improve SCR's performance with the device still isolated from substrate.

Figure 2 shows the new bi-directional SCRs proposed in this work. Figure 2(a) demonstrated a new SCR with NBL partially formed only on IO side. Figure2 (b) shows further a new SCR with partial NBL, and a floating P+ region inserted in Pwell, between N+ and edge of Pwell at GND side.



(a)



(b)

Figure 2: New Bi-directional SCRs Developed on SOI Technology (a) with Partial NBL, (b) with Partial NBL and Floating P+ Region

B. Device Working Mechanism

It is well known that SCRs Vh is dependent on product of NPNs and PNPs current gains. PNP is a low current gain device. NPN(s) then becomes the focus for Vh engineering, with much larger room to reduce current gain than PNP.

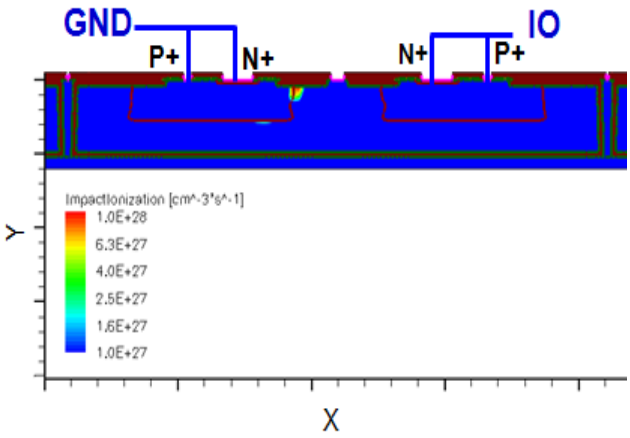
1. Collector/NBL Engineering

To get insight into the behavior of the device, TCAD simulations has been performed on the baseline SCR with the full NBL. When IO is applied with positive pulses vs. GND, the device will be triggered by reverse-biased blocking junction N-sinker/Pwell controlled by Sp in $NPNL_F$ as shown in Figure 3(a).

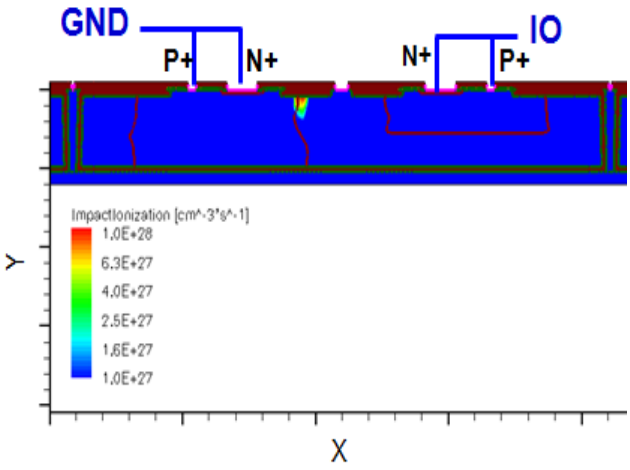
As the avalanche breakdown increases, the holes flow to Fwd Base of NPN(s) creating voltage drop to forward bias base-emitter junction. Eventually both vertical and lateral NPNs would turn on, making the device snap back. TCAD simulation showed the post-snapback impact ionization is

highly concentrated on the upper edge of NBL in Figure 4(a). This suggested that vertical NPN is the main contributor of the device's post-snapback behavior. The vertical NPN limits Vh of the device in 2 ways: 1) low collector resistance from heavy-doped NBL leading to a highly conductive vertical current path with lower Vh, 2) high current gain due to intermediate EPI thickness between Pwell and NBL offered by the technology [5].

The new SCR shown in Figure 2(a), has NBL removed partially, thus vertical NPN no longer present, at GND side. It has the same triggering mechanism as the baseline device, as shown in Figure 3(b). But its post-snapback is clearly only dependent on the lateral NPN as in Figure 4(b) which leads to improved Vh.

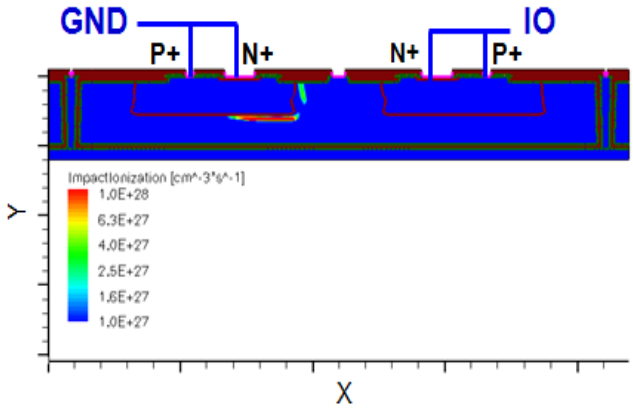


(a)



(b)

Figure 3: TCAD-simulated Impact Ionization before Triggering of Baseline SCR with Full NBL (a), and New SCR with Partial NBL (b)



(a)

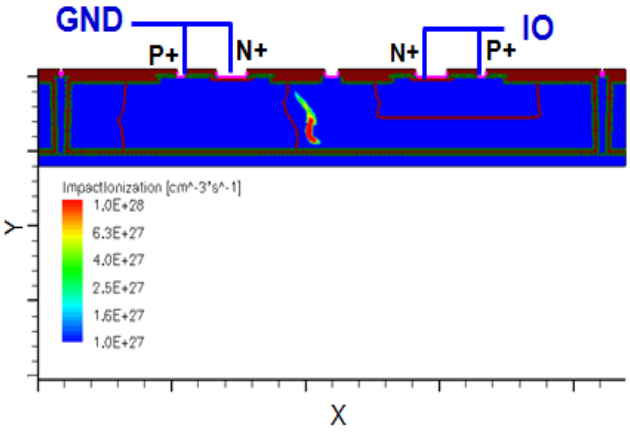
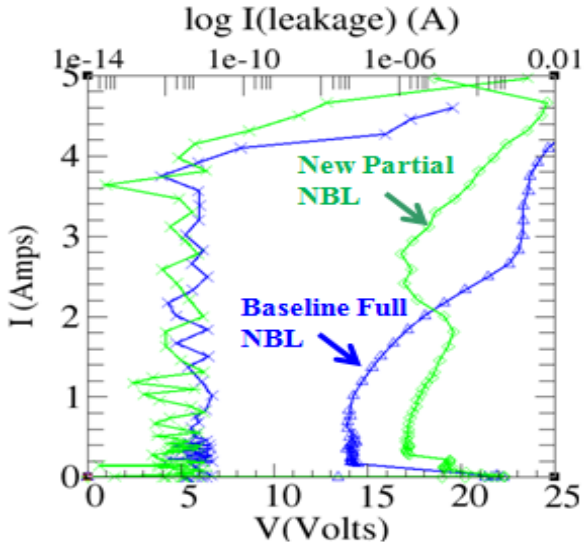


Figure 4: TCAD-simulated Post-snapback Impact Ionization of Baseline SCR with Full NBL (a), and New SCR with Partial NBL (b)

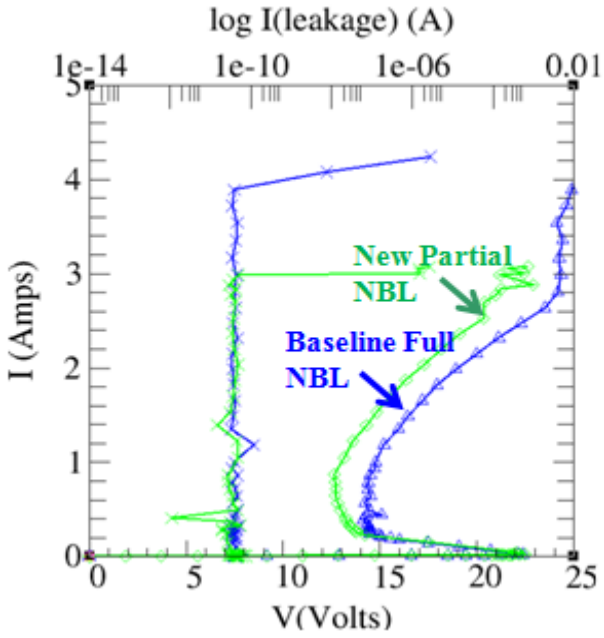
A baseline and a new bi-directional SCR have been implemented as +15V/-15V ESD protection, with emitter length (Le) 57um. The TLP data is shown in Figure 5. In forward, the new device showed improved Vh = 17V, vs. Vh=14V for baseline device. A 20% Vh increase was achieved without increasing the die area. Moreover, the new device also showed improved It2 and Ron due to changed field distribution.

In reverse polarity, 2 devices showed similar Vh, as it is dominated by vertical NPN at IO side as expected. The reason to keep vertical NPN at IO side will be detailed in Section IV.

TLP data also indicated same Vt1 for the new device as compared to the baseline device in both forward and reverse polarities. This verified that the partial NBL scheme does not change the triggering mechanism as expected by the TCAD simulations in Figure 3.



(a)

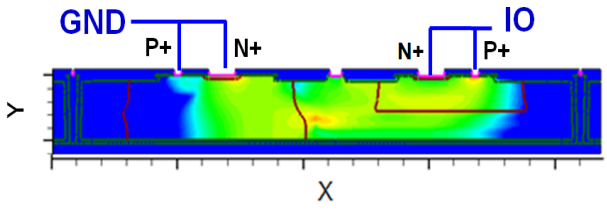


(b)

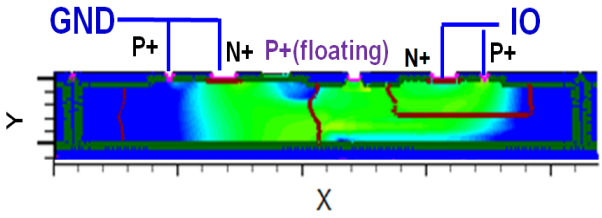
Figure 5: Forward (a) and Reverse (b) TLP of 15V/-15V ESD Clamps Based on Baseline SCR, and SCR with Partial NBL.

2. Base Engineering

On top of the partial NBL scheme, Vh can be further increased by engineering the Pwell base. While increasing the base width (Wb) of the NPN is commonly seen in publications to reduce current gain, we propose a more effective technique – to insert a floating P+ region in the Pwell base with cross-section shown in Figure 2(b). Under positive ESD transient, the floating P+ region has similar potential as GND as it sits in the same Pwell as the base terminal(P+). It will block surface part of electron current flowing from emitter (N+) to collector (N-sinker in the center of the device) of $NPNL_F$. This makes the current diverted deeper into the silicon, leading to a longer current path thus higher Vh. It can be seen by TCAD simulation in Figure 6.



(a)



(b)

Figure 6: TCAD Post-snapback Current Density of Bi-directional SCR with Partial NBL (a), Partial NBL & Floating P+ (b).

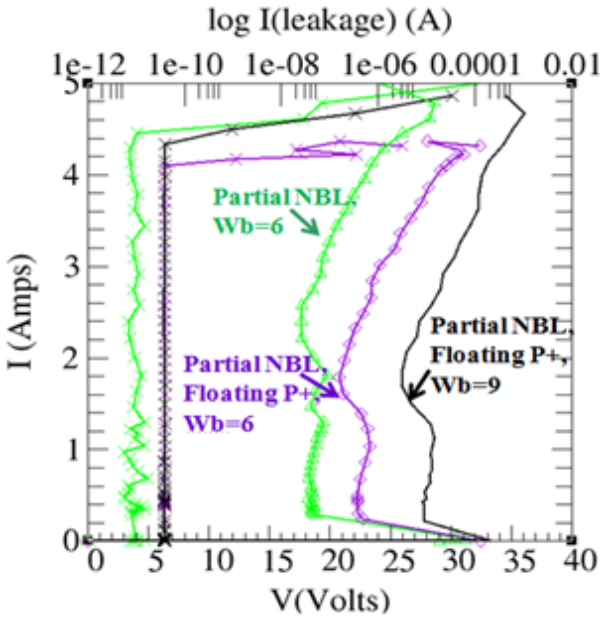


Figure 7: TLP of 25V ESD Clamps Showed Good Control of Vh with Partial NBL and Base Engineering Techniques.

This technique can be demonstrated by experiments targeting as 25V ESD clamps, with TLP data in Figure 7. With increased Wb and floating P+ tie inserted, 28V Vh has been achieved, about double of baseline device's Vh.

It is to be noted that, although floating P+ technique was described in [8]. Our work is based on completely different mechanism. [8] proposed a single-polarity SCR with floating P+ on Anode side (in Nwell). This makes the PNP in SCR got emitter floating. With only base of PNP connected to Anode, its emitter-base junction (P+ to Nwell) could breakdown under ESD stress causing reliability concern for the shallow junction. In this work, a floating P+ was inserted at GND (Cathode) side in Pwell. It increases Vh by modulating current flow of $NPNL_F$, with no reverse-biased junction introduced.

III. Qualification Results

In this section, we demonstrate qualification data of 40V/-40V ESD clamps built with 2-stack of new bi-directional SCRs for automotive.

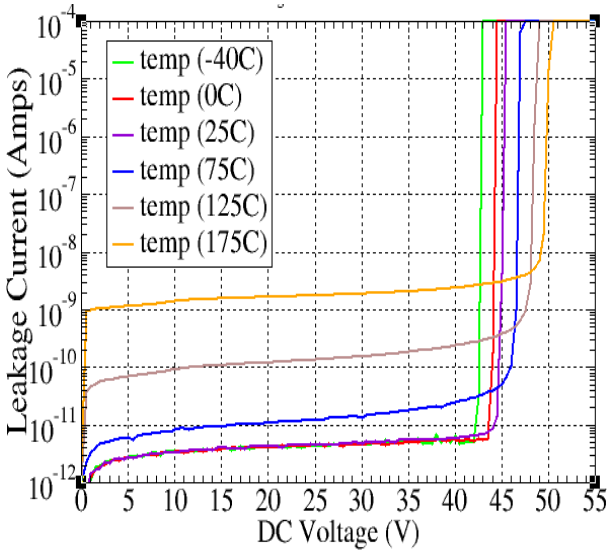


Figure 8: DC Sweeps of 40V/-40V ESD Clamp with Temperature Varied from -40℃ to 175℃.

A. DC Test Results

Extensive DC test has been done to make sure the ESD clamps DC BV above maximum rating with temperature varied from -40℃ to 175℃ per automotive requirements. The data showed typical avalanche breakdown behavior and low leakage with varied temperatures as in Figure 8.

B. TLP Test Results JEDEC Clamp

As shown in Figure 9, 40V/-40V JEDEC clamp achieved high Vh by combining NBL and base engineering techniques. With emitter length (Le) =57um, 4A It2 has been demonstrated. Forward Vh=~38V and reverse Vh=~30V is on target for most automotive applications such as CAN and LIN transceivers [1].

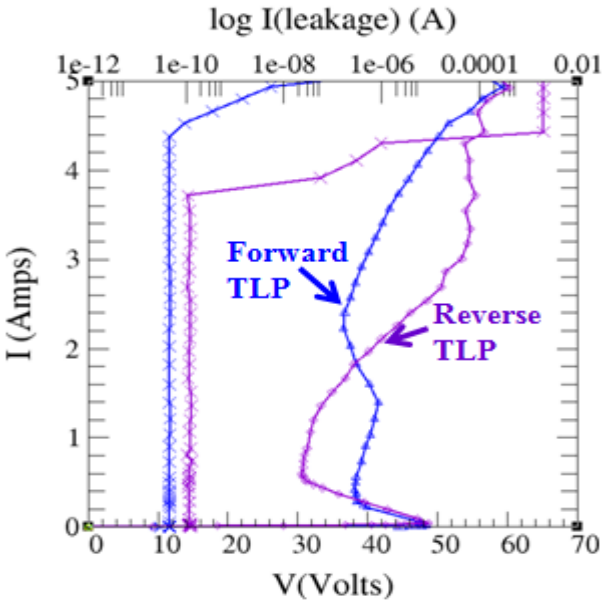


Figure 9: TLP of 40V/-40V JEDEC Clamp

C. System-Level IEC61000-4-2 Test Results

Using same device configuration, but larger emitter length (Le), we have built on-chip 40V/-40V ESD protection for system-level IEC61000-4-2 stress. TLP It2 scaling data is shown in Table 1. For clamps with Le>=250um, It2/Le=~60mA/um.

Table 1: TLP It2 vs. Emitter Length of 40V/-40V ESD Clamps

Emitter Length(um)	Forward It2 (A)	Reverse It2 (A)
57	4.4	3.7
250	15.3	14.9
350	21.5	20.4
700	>30*	>30*

*It2 exceeded TLP tester current limit

System-level test results in Figure 10 suggested 40V/-40V clamps IEC robustness scales with the emitter length. Without external components, the clamp with Le=250um passed 8KV test. And at Le=700um, it passed 17KV IEC test.

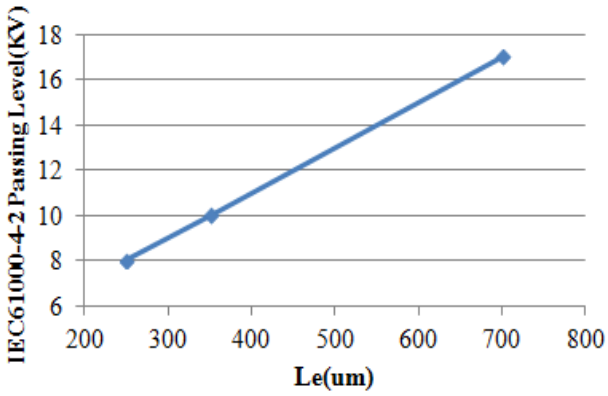


Figure 10: IEC61000-4-2 Test Results of 40V/-40V ESD Clamps with Varied Le

D. EMC Test Results

EMC immunity is essential to automotive applications [10]. The measurements on 40V/-40V clamp suggests it is compatible with EMC immunity requirement described in IEC62132-4 DPI (direct power injection), until 36dBm. Rectification phenomenon was not observed during the EMC tests.

IV. Discussion

In section II, it has been discussed that vertical NPN limits Vh of bi-directional SCRs. It is due to its highly conductive vertical current path and the high current gain, from heavy NBL doping concentration and intermediate Epi thickness. By removing vertical NPN with NBL engineering, Vh was increased. In addition, with Vh only dependent on lateral current flow, it is more controllable. Increasing Wb and inserting floating P+ tie are both effective base engineering techniques to further improve Vh.

While partial-NBL scheme can be used in bi-directional SCRs on bulk technologies, it leaves devices non-isolated from P substrate thus limits its usage.

With the partial-NBL bi-directional SCR well-implemented on SOI technology, we could face the question why NBL can't be removed on IO side to improve reverse Vh?

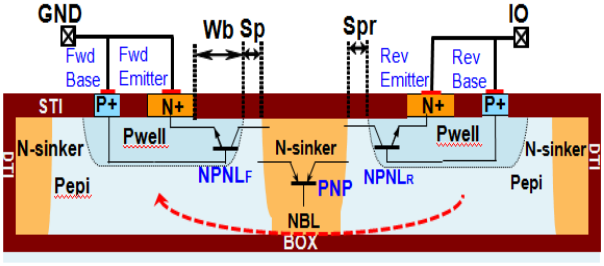
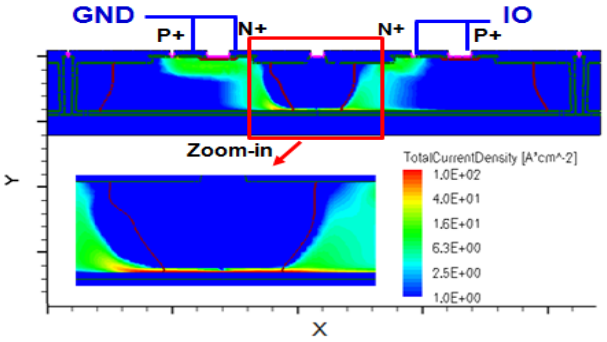
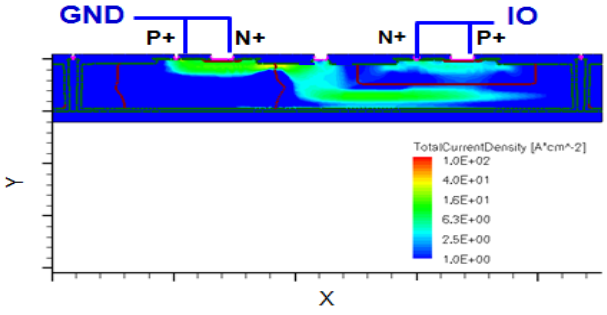


Figure 11: Removing NBL on Both IO and GND Sides Causes High Leakage Current

Unlike single-polarity SCRs [9], NBL can't be removed freely in bi-directional SCRs. Since there are Pwell/Pepi regions on both IO and GND sides, NBL and N-sinker are essential to isolate $NPNL_F$ from $NPNL_R$. If NBL were removed on both sides as in Figure 11, parasitic PMOS would be formed by Pwells, and BOX acting as the gate. The bottom diffusion of NBL would be inversed, causing high leakage current as shown by TCAD simulation in Figure 12(a). The proposed device simulated proper leakage current in Figure 12(b).



(a)



(b)

Figure 12: TCAD-simulated Current Density under DC Bias Showed Parasitic PMOS Turns on Causing High Leakage Current if NBL Removed on Both IO and GND Sides (a), the Proposed Partial-NBL Device Simulated Proper Current Distribution (b).

V. Applications

The new bi-directional SCRs have been successfully integrated in a number of automotive and industrial products with HBM, CDM, and system-level ESD requirements.

VI. Conclusion

Novel bi-directional SCRs have been developed on an advanced 0.13um SOI-based smart power technology. TCAD simulations have been performed to study contribution of vertical NPN and lateral NPN to post-snapback behavior of the device. It has found that vertical NPN limits Vh of bi-directional SCRs. It is due to its highly conductive vertical current path coming from heavy-doped NBL, as well as the high current gain from intermediate EPI thickness of the technology. By NBL engineering, the vertical NPN was removed from the device to increase Vh. Inserting P+ tie in Pwell base of NPN modulates the ESD current flow for further Vh improvement. With NBL engineering and floating P+ tie technique combined, 28V Vh has been achieved, doubled from that of baseline design. Outstanding DC, TLP, IEC61000-4-2, and EMC performance were achieved for automotive applications.

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