Correlation Limits between Capacitively Coupled Transmission Line Pulsing (CC-TLP) and CDM for a Large Chip-on-Flex Assembly

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Abstract - For the first time this correlation study compares air discharge CDM and contact-mode Capacitively Coupled Transmission Line Pulsing (CC-TLP) for a large chip-on-flex assembly e.g. for the Internet of Things (IOT) applications. Both ground planes overlap only part of the flexible substrate with long traces. Correlation can be established according to impulse energy and multi-zap wear-out effects rather than peak current. Circuit simulation supports the experiment. A new scanning method yields the potential distribution across the substrate.

I. Introduction

The development of a process to enable fabrication and integration of ultra-thin silicon in foils is one of the milestones in flexible electronics, which has opened the door for various applications like flexible displays, wearables and foldable electronics in recent years. Specific advantages like light weight, flexibility and foldability, lower costs, potential transparency and new application opportunities [1] have attracted the interest of numerous electronics manufacturers. However, flexible electronics also implies an increased and specific demand for reliability, both mechanical as well as electrical. While several groups are investigating the mechanical reliability of Chip-on-Flex (COF) samples [2], the attention received by Electrostatic Discharge (ESD) analysis of COFs is rather minimal. To our knowledge, this work is the first to analyze the specific ESD issues of COFs, which should be applicable for very large scale packages exceeding the size of the Ground Plane (GP) in CDM.

The bendability of these components requires mechanical support for processing and as such yields a higher risk of triboelectric charging. Electrically insulating substrate materials like polyimide (PI) enable the storage of a significant amount of charge on their surface and may easily charge up to hundreds of volts. The paper describes an innovative method of scanning the surface potential across the polymer substrate with its copper traces.

Flexible electronics with substrates that may exceed the size of standard packages significantly brings up new aspects of Charged-Device-Model (CDM) testing. We report our investigations dealing with COF samples, consisting of a few cm long narrow traces on a passivated PI foil substrate. One key question in this case is the feasibility of CDM and Capacitively Coupled Transmission Line Pulsing model (CC-TLP) stress tests on the COF assembly, as the GP does not overlap the sensitive chip. For this purpose, we analyzed the current waveforms and studied the entire discharge environment, including the chip, by means of simplified circuit simulations. For verification of our results, we examined their correlation with CC-TLP at wafer level regarding peak current, other stress parameters and their failure thresholds together with the failure signatures. This work discusses the ESD challenges of testing COF assemblies and thereby investigates expected limits of the CC-TLP method as an alternative to the well-established CDM test method. COF results may also apply to the testing of large scale packages.

II. Chargeability of the Foil Substrate

Before starting the stress tests, the charging of the foil as a critical aspect concerning ESD on COFs was analyzed [3]. Employing a Monroe non-contacting electrostatic voltmeter with a chopper sensor in combination with a wafer prober a lateral resolution of a few millimeters and a potential resolution of 1 V was achieved. After scanning the foil line-by-line, the data was processed to generate a contour plot, which shows the charge contribution on the foil (see Figure 1). In its later application as a flexible and bendable substrate, the charging of the foil can hardly be avoided. The same applies to the handling of the COFs during ESD tests. Even if we assume a non-charged foil after its roll-to-roll production process, the challenge arises when the entire roll must be cut into individual foils afterwards. The PI foil is extremely sensitive to triboelectric effects. Only when all necessary ESD precautions, such as ionization, are precisely applied, is it possible to keep the surface potential of the foil down to levels in the region of some tens of Volts (see Figure 1, Unstressed foil). For example, to demonstrate this effect, sticking and pulling off an adhesive strip (see Figure 1, Foil 1) or by applying electrical stress on the left side of the foil (see Figure 1, Foil 2), voltages below - 800 V can be produced on this side. According to the triboelectric series [4], PI has a charge affinity of about -70 nC/K. This explains why it accumulates a strong negative charge when it is rubbed against most other materials.

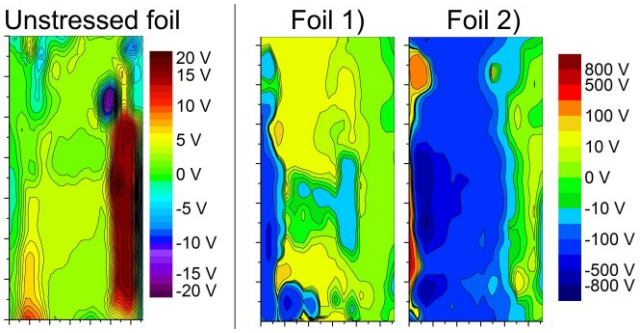

Figure 1: Surface potential on foil measured by an electrostatic voltmeter. The automated scanning of 34 vertical lines per picture generates the picture.

Once the foil is charged, the trapped charge remains, and decays very slowly unless an air ionizer is used. In the meantime, the foil is surrounded by electrostatic fields, which may influence or separate charge carriers in other parts. This further complicates the prevention of ESD-events. The electric fields might also lead to a charge displacement in the copper traces on foil, which would likely have an effect on ESD testing, as the pulse may be distorted by crossing different potential levels on its way to or from the die yielding miscorrelation. Overall, the high chargeability of the foil is one main aspect that shows the risk to COFs concerning ESD as well as the difficulty of performing ESD tests on it.

III. Measurement Techniques

The full-custom modular ATIS MCDM test system with the ATIS JEDEC test head free of ferrites and tuning cavities was employed to test the susceptibility of the electronic devices on flex with respect to the JEDEC standard JESD22-C101. Its 3 dB-S_{11} bandwidth well exceeds 19 GHz [5]. For reference, Figure 2 shows the 200 V discharge waveform of a large standard calibration module captured on a high bandwidth oscilloscope at 12 GHz.

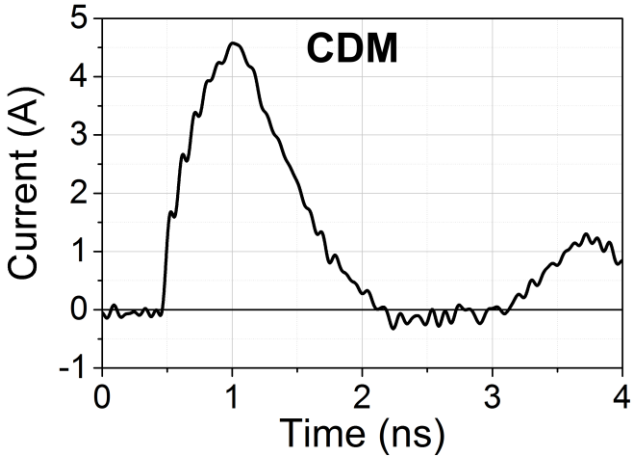

Figure 2: CDM discharge current measured on a large JEDEC calibration module using a precharge voltage of 200 V on a high bandwidth oscilloscope at 12 GHz.

We measured the resulting CDM stress waveforms using both a 4 GHz and a 33 GHz oscilloscope and compared them with the waveforms generated using the alternative contact-mode test method CC-TLP (see Figure 3), with waveforms measured using a 33 GHz oscilloscope. The latter was developed to eliminate CDM's peak current variation resulting from air discharge [6]. CC-TLP provides the reproducibility of two-pin Very Fast Transmission-Line Pulsing (VF-TLP) while making just a single connection between the hot pulse terminal and a floating device under test (DUT). Furthermore, it can replicate narrow-pulse high current CDM events. The floating DUT is capacitively coupled to both the GP positioned above and the chuck underneath the DUT. The resulting background capacitance (C_b) corresponds to the distributed capacitance of a

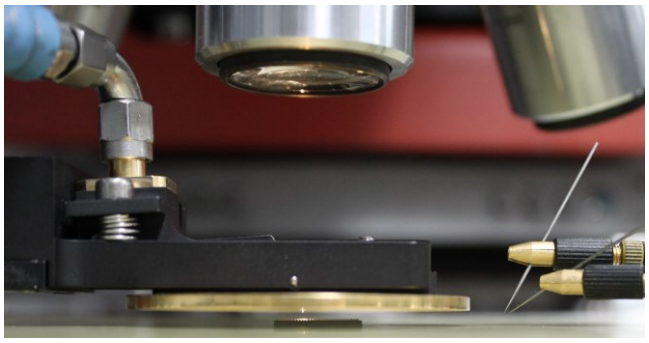

Figure 3: CC-TLP probing set up during stress testing at package level.

packaged device in CDM and establishes the ground return path. The background capacitance charges up via the DUT during the VF-TLP square pulse and discharges after the pulse's falling edge. The output of a 10:1 voltage pick-off, separated by a 1 m long cable from the CC-TLP probe head, is connected to the oscilloscope to sample the incident and reflected pulses in a single shot. By time shifting and superposing the two signals, the stress current I_{TLP} through a DUT can be determined by:

$$I_{TLP} = \frac{V_{inc} - V_{ref}}{50\,\Omega} \quad (1)$$

In the last decade, several correlation studies [5]-[10] have shown that CC-TLP is capable of reproducing gate oxide related field failures equivalent to the CDM test. The results correlate well regarding electrical and physical failure signatures for distinct peak threshold currents at package and CC-TLP at wafer level. In its objective to identify limitations of the CC-TLP correlation with CDM this paper is the first to examine the correlation for a large COF assembly and even a pn-junction failure.

Figure 4 depicts the principle of the probing setup for the CC-TLP investigations. The probe needle contacts one of the pads at the edge of the flex, which has a number of passivated traces connecting to the

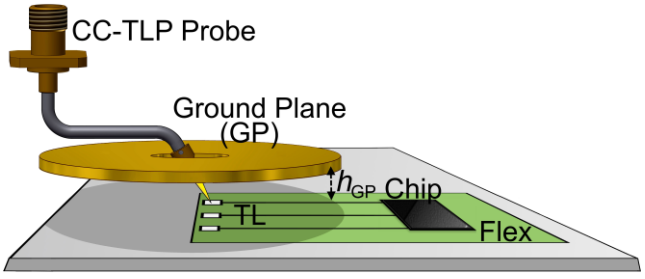

Figure 4: CC-TLP probing set up during stress testing on flex. The probe needle is in contact with the pad of one trace, which leads to the COF. For reasons of clarity, only three of many traces are illustrated.

pads/bumps of the flip chip. The particular challenge involved here is that the traces are longer than half the side length of the square CDM GP (32 mm) and the radius of the CC-TLP GP (25 mm). Thus, in both methods the GP and the chip do not overlap (see Figure 4), which implies that their capacitive coupling is very low and can only be induced by fringing fields. Hence, the configuration provides an unconventional way of performing CDM and especially CC-TLP tests, which could lead to irregular results. Nevertheless, the extreme case should also allow some generic insight into the probing of large scale packages.

IV. Circuit Simulations

In order to gain a better understanding of ESD tests on a COF technology, it is advantageous to initially create a simulation model of the ESD event, which was performed by means of the Keysight (Agilent) ADS circuit simulation tool.

A. Simulation Models

Figure 5 illustrates the key components of the schematic CC-TLP simulation model on flex.

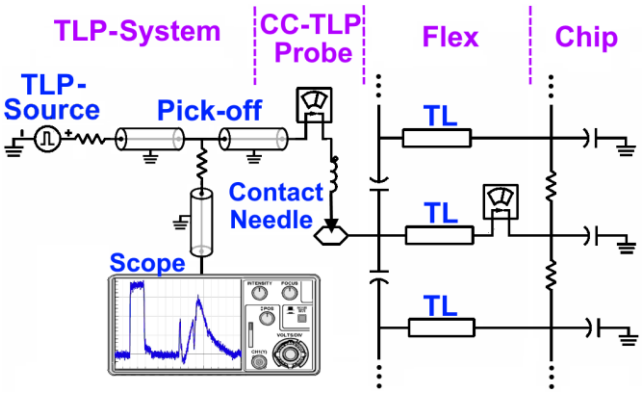

Figure 5: Applied lumped element model of the CC-TLP simulation setup on flex. The probe needle is in contact with one of the electrically and inductively coupled TLs of the COF assembly (Inductive coupling is left out to simplify the diagram).

In the CC-TLP simulation, the dataset of a real measured voltage pulse was imported and assigned to the Transmission Line Pulsing (TLP) source for the incident pulse. In the measurement as well as in the simulation, an attenuator behind the TLP source can optionally be used to reduce reflections. On the right side, a generic RC network models the complex integrated circuit (IC) with many inputs and narrow traces on flex that - in combination with the tester setup - can be looked at as transmission lines (TLs). Optionally, some inductive elements can also be added in series. In addition, each of these TLs is

capacitively and inductively coupled with two adjacent neighbors. For both stress methods, the pad to be contacted is positioned at the end of one of the TLs which extend for several cm (see Figure 4). The TLs all lead in parallel to the flip-chip-on-flex interconnections.

The CDM simulation setup contains the same model for the COF. The model of the CDM tester is equivalent to the one in [11]. In the CDM simulation the whole chip, including all the TLs, is charged up before it is discharged through a 1-Ohm disk resistor to the GP. After making some measurements, it turned out that the COF circuit chosen for this study is highly sensitive to CDM and that the precharge voltage required to generate CDM failures is well below 100 V. A good fit between the simulation and the measurement was obtained, when we chose an average resistance of 10 Ω [12] for the air discharge in a nitrogen atmosphere.

B. Impedance Extraction of the TLs

A significant difference between the CDM and CC-TLP setup is the characteristic impedance of the TLs. In CC-TLP, the round GP establishes the return path and is positioned directly above the TLs at a distance of h_{GP} = 500 µm by default (see Figure 4). In CDM, the square GP is, due to the length of the pogo pin, much further away at a distance of around 3.5 mm. Here, the main coupling is formed by the Field Charge Plate (FP) below the foil, which forms a capacitance with the GP [13]. The characteristic impedance of the TL was quantified by a Time-domain Reflectometry (TDR) step response measurement using a TDS8000 sampling oscilloscope. Together with the sampling rate, the rise time of the step generator determines the geometric resolution, which was 30 ps. During the TDR-measurement, the CDM and CC-TLP probe was in direct contact with the input pad of a TL on the flex from which the chip was removed to generate an open termination at the end of the TL. In order to allow the measurement of the characteristics impedance change from the pogo pin to the TL, we removed the 1-Ohm disk resistor of the CDM probe. Figure 6 illustrates the analysis of the TDR traces resulting in characteristic impedances of the TLs of 190 Ω for CDM and of around {100, 150, 160, 170} Ω, for CC-TLP with separation heights of h_{GP} = {100, 300, 500, 1000} µm between GP and flex. This dependency can be explained by the fact that the characteristic impedance of a TL depends inversely on the capacitance per length. Because of the low capacitive coupling between the DUT and the GP in CDM, a decrease of the GP-foil distance from around 3.5 mm to 2.7 mm, through a stronger tension of the spring-loaded pogo pin does not lead to any impedance change.

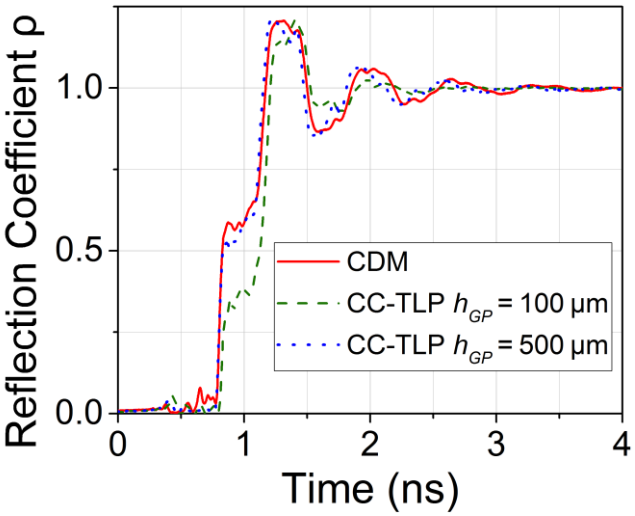

Figure 6: Reflection coefficients of copper strips on flex without chip measured by the TDS8000. The first step arises due to the impedance rise at the transition from the CDM pogo pin or the CC-TLP contact needle to the TL. The results were used to determine the characteristic impedances of the TLs for the simulation model. (The curves for separation heights h_{GP} of 300 µm and 800 µm were left out to simplify the diagram)

C. Transient Simulation Results

The TDR measurement provided the necessary parameters for the simulations models. In Figure 7, the simulated (red) and measured (blue) waveforms are compared. Generally, the simulated curves match the measured ones, which is an indication that the model and the choice of its parameters describes the system in a proper way. The wave-shaped curve of the CDM transient shows the characteristic impact of the TLs on foil. The discharge current oscillates between the chip and the 1-Ohm resistance of the CDM head, which leads to a ringing of the current transient. The period of one of these steps is around 0.3 ns, which is consistent with the TDR analysis as well as with the theoretical calculation of the signal propagation time.

In general, the current I_{TLP} flowing from the CC-TLP contact needle into a DUT can be calculated by the superposition of the measured incident voltage pulse V_{inc} and the reflected voltage pulse V_{refl} (1). In the case of a non-COF technology, where the contact needle is directly connected to the pin or pad of the DUT without additional TLs between, I_{TLP} corresponds to the stress current seen by the DUT. In the case of the investigated COF technology, the TLs may have an impact on the stress current seen by the IC as well as

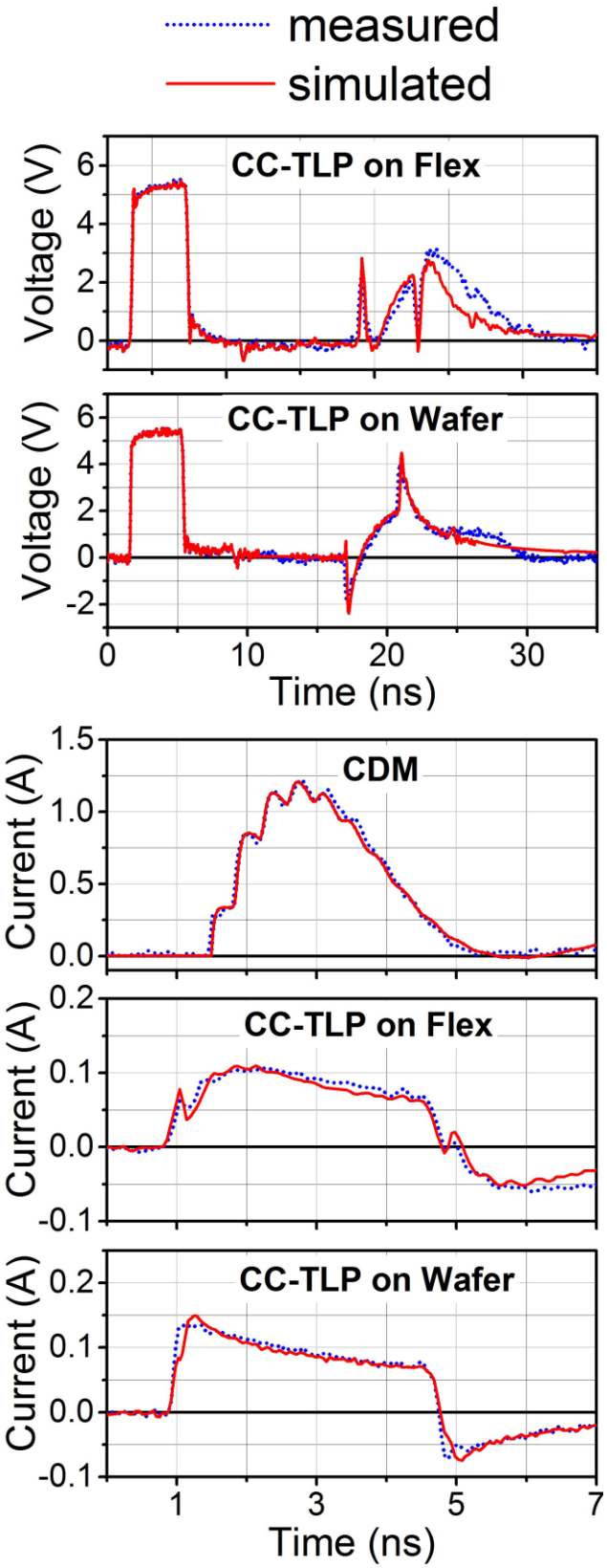

Figure 7: Comparison of measured and simulated transients of CDM and CC-TLP on flex and on wafer. The two curves on top are voltage transients of the incident and the reflected CC-TLP pulse. The three lower curves are the corresponding current transients plus the discharge current of a typical CDM pulse.

on the measured signal. This impact depends strongly on the capacitive and inductive coupling between the TLs and cannot directly be extracted from the measured data. However, the simulation provides an instrument to evaluate the influence of the TLs on the stress current. Since the capacitive and inductive coupling are adaptable parameters in the simulation model, they can be estimated and optimized by fitting the simulated curve (see Figure 7, red curve) to the measured current transient (see Figure 7, blue curve). For a wide variation of the coupling parameters around their optimized value, the simulated stress current at the end of the TL, reaching the chip, is only a few percent higher than the peak current at the end of the CC-TLP probe needle (see Figure 8). This means that the measured current I_{TLP} (1) is a good measure for the real stress current that reaches the IC.

The verified simulation model allows the investigation of waveforms at various locations, helping to distinguish between different influences and parameters. The shape of the reflected pulse in CC-TLP on flex is basically created by the following three impedance discontinuities or mismatches: the inductance of the contact needle, the impedance rise from the contact needle to the TL and the impedance fall from the TL to the chip during its capacitive charging. The superposition of these three reflections creates the original reflected pulse measured in CC-TLP (see Figure 7, first plot). Removing the TL, the inductance of the needle is followed directly by the impedance fall from the transition to the chip. Consequently, this corresponds to the measured and simulated CC-TLP waveform on a wafer (see Figure 7, second plot).

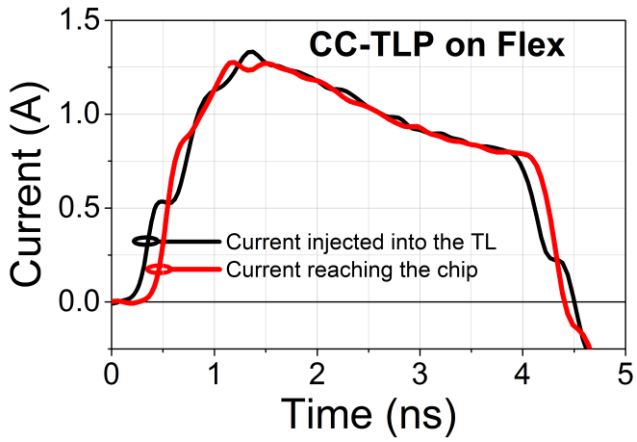

Figure 8: The reconstructed current from the oscilloscope data (1) equals the current at the end of the CC-TLP needle, which was injected into the TL (black). This simulation shows that its peak current, is only 5 percent higher than the peak current at the end of the TL, seen by the chip (red). Figure 5 shows the measuring positions of the two current probes.

V. Failure threshold analysis

Having investigated the basic operating principles of CDM and CC-TLP applied to the COF assembly and having demonstrated their theoretical feasibility, we proceed to analyze the correlation between CDM and CC-TLP regarding their current threshold. To reduce measurement differences within the metrology chains, the 33 GHz oscilloscope was used for both methods. The CDM test was performed following the JEDEC specification JESD22-C101 [14] with three positive and negative pulses per pad. As CC-TLP is a contact-mode test model with no air discharge, there is no lack of reproducibility as it is in CDM [5]. Therefore, only one positive stress pulse per pad was used. In preliminary investigations, the positive polarity was determined as being more sensitive one for the IC. In this polarity, the current flows through the reverse biased junction, eventually causing its failure. In this configuration, the CDM test provides a failure current threshold of around 0.7 A, while the failure current threshold of CC-TLP on flex was higher, with around 1.2 A.

However, by reducing the CDM stress sequence from three positive pulses to one positive and one negative pulse per pad, the failure current rises to around 1.1 A and thus aligns with CC-TLP on flex. To exclude any polarity effects, CDM was also performed with just a single pulse of the most sensitive polarity, reproducing the same result. We conclude that, unlike gate oxide rupture typical for CDM, in this case cumulative damage increases the leakage in the junction until the failure criterion is met, thereby defining the failure threshold of the DUT. This was a first indication that beyond peak current the dissipated energy could be an alternative failure criterion of this IC.

For additional verification of the correlation, we performed CC-TLP at wafer level. This test yielded the same failure signature at the same peak current failure threshold of 1.2 A.

In this context, we found another hint on an energy dependent failure mechanism. As expected, by changing the height h_{GP} of the GP above the flex (see Figure 4) the waveform of the current transient changes. This is explained by the fact that the characteristic impedance of the TLs depends inversely on the capacitance per length. This means that for a defined peak current, the higher the separation h_{GP}, the higher pulse voltage is needed to generate an equivalent current. However, besides that, we measured that also the failure current threshold increases with height. Figure 9 shows the lowest current transients of CC-TLP on flex which lead to a failure of the IC. This effect was observed by increasing stepwise the pulse amplitude of the TLP system and watching the leakage current after each stress pulse. The currents failure thresholds were specified to {1.1, 1.2, 1.4} A, for separation heights of h_{GP} = {300, 500, 1000} µm. In addition to that, Figure 9 depicts the lowest failure current waveform of CC-TLP on wafer which amounts to 1.2 A (green hatched area).

A variation of the GP-foil distance results in a small deviation from the initial measured threshold level of 1.2 A. However, as expected from Figure 9, the integration of the current curves over the charging period as well as the integration of the square of the curves yields to a very similar value. This clearly indicates that the total transferred charge and as such the energy dissipated in the junction have a dominant influence on triggering the failure.

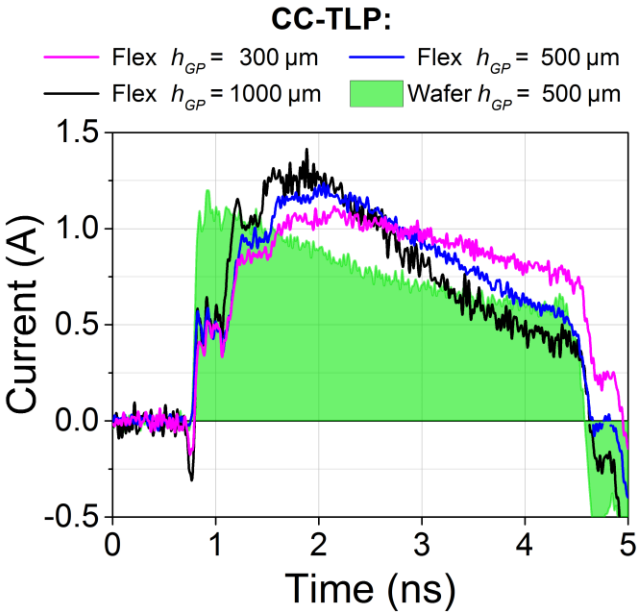

Figure 9: Lowest failure current waveforms of CC-TLP on wafer and on flex. For the default distance between GP and flex of h_{GP} = 500 µm, the peak current of CC-TLP on flex and on wafer correlate. Besides, all the waveforms and the square of the waveforms show a very similar area under the curve.

VI. Conclusion and Outlook

This work highlights emerging challenges for ESD testing on large flexible electronic assemblies e.g. for IOT applications. Clearly, the strong tendency for charging and slow decay of the stored charge on the substrate foil complicates the prevention of ESD-events and is a risk for ESD testing. Contour plots, generated by an innovative automated scanning setup, provide a quantitative understanding of the origin and

location of the mobile and immobile charge on DUTs and in particular on large chip on foil.

Our study demonstrates the feasibility of CDM testing on a COF assembly that significantly exceeds the size of standard packages. This has been verified by correlation of the CDM failure current threshold with its alternative contact method, CC-TLP, at wafer level. These results have also been reproduced by CC-TLP on the flex circuit, even though there is no direct overlap between the GP and the chip. Instead, the GP couples with the long interconnect traces on the polyimide film. The CC-TLP method gives a reduced characteristic impedance for the traces, compared to CDM, resulting from the reduced GP height above the circuit. The correlation of CC-TLP with CDM in this unconventional case gives further justification for the establishment of the CC-TLP stress test method in the industrial environment.

Our simulations provide a deeper insight into the ESD event on the COF itself. As the simulated and measured waveforms match very well, we were able to investigate the impact of the electrically coupled traces on foil and demonstrate that the reconstructed current in CC-TLP is an appropriate measure for the stress current that flows directly into the chip.

Unlike gate oxide related leakage, for this stressed chip with a sensitive pn-junction in the direct discharge path, the number of stress pulses obviously has an influence on the degradation and ultimately the level at which the failure threshold is reached, if the failure criterion is not checked after each impulse. This requires a clear specification of the number of stress pulses for a reliable correlation. In this context, we pointed out that even for the adiabatic conditions of CDM and CC-TLP the pn-junction failure result is more closely related to the dissipated energy than the peak current.

Looking at the CC-TLP in this study the single, very repeatable, impulse simulates typical CDM failure mechanisms, here a pn-junction, very well and in a highly controllable way.

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