Chip-level ESD-induced Noise on Internally and Externally Regulated Power Supplies

Yang Xiu, Nicholas Thomson, Robert Mertens*, Collin Reiman, and Elyse Rosenbaum
Dept. of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA
*Now with NXP Semiconductor, 6501 W. William Cannon Dr., Austin, TX 78735 USA

Abstract –Power integrity during system-level ESD is studied on two test chips that have different integrated voltage regulator designs. On-chip voltage regulation can provide increased immunity to ESD-induced noise, especially if the internally-generated power supply does not utilize any off-chip decoupling capacitors.

I. Introduction

A large current may enter an integrated circuit (IC) through one of its pins as the result of a system-level electrostatic discharge. If the IC is in the power-on state, the ESD current with its large time-derivatives will generate noise on the on-chip power supply nets [1]. The resulting supply voltage fluctuations, if large, may lead to malfunctioning of the IC and loss of data [2]. The amount of noise added onto the chip supply during ESD depends on the system power delivery network (PDN), which extends from the IC and its package to the PCB.

On-chip low-dropout (LDO) voltage regulators are used to provide a higher level of integration as well as to improve noise immunity and power efficiency. However, it should be considered whether an internally-generated power supply is isolated from the ESD-induced noise on the IO supply and whether the LDO will continue to operate properly during a power-on ESD event. Refs. [3] and [4] showed that LDOs can be compromised by the large substrate currents generated during ESD and latch-up tests. This paper focuses on the propagation of supply noise from the IO supply to an internally regulated supply; it will be shown that for a well-designed LDO, it is the presence or absence of decoupling capacitors (decaps) on the circuit board that may determine the ESD robustness.

II. ESD-induced on-chip supply noise

The ESD current that enters an IC through an IO pin gets shunted to the chip's PDN, where it generates noise, especially for wire-bonded packages. The induced noise on the supply has commonalities to "simultaneous switching noise" [5, 6, 7], but the amplitude of the supply noise caused by ESD is much larger [1, 8]. If the on-chip portion of the current return path includes the IO circuit's ground bus, the noise propagates to all the other on-chip supply domains, even if the IO circuits have a separate ground bus. This assertion may be understood with the aid of Figure 1, which illustrates the case of a negative discharge to an IO pin. When the ESD current is decreasing from its peak magnitude, the on-chip VSSIO is lifted above the system (board) ground potential, due to the "$L\frac{di}{dt}$ effect." The amplitude of the on-chip ground bounce is determined primarily by the package-level inductance, and it can be several volts for wire-bonded components during system-level ESD. The disturbance on VSSIO propagates to VSS through the antiparallel diodes (APD) used for ESD protection. This produces an under-voltage transient on the core power supply VDD, i.e., $\left(\mathrm{VDD(t)\text{-}VSS(t)}\right) < \mathrm{VDD_{nominal}}$.

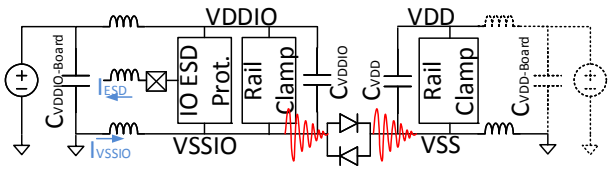


Figure 1. ESD-induced noise can propagate between power domains. "Core" power supply voltage VDD may be generated either off-chip or on-chip. In the latter case, VDD might not have any package pins connected to it.

In Figure 1, the "core" (low voltage) power supply, VDD, may be generated by an external voltage regulator or by an on-chip ("integrated")

voltage regulator. When VDD is generated on-chip, it is subject to noise transmitted from the supply domain that provides power to the regulator, which may be the VDDIO domain.

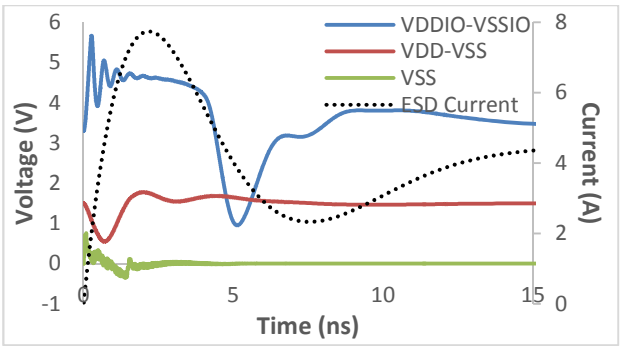
The ESD-induced noise on VDD was simulated for the specific case of the 130-nm CMOS test chip described in [9]. In the simulations, an IEC 61000-4-2 [10] ESD gun discharges into a self-protected IO pin; VDD is an externally-generated 1.5 V supply and VDDIO is 3.3 V. Figures 2(a) and (b) show the simulated waveforms for a +2 kV and a -2 kV discharge, respectively, to an IO pin with dual-diode protection; Figure 2(c) shows the simulated waveforms for a +2 kV discharge into an IO protected by a local clamp—a DTSCR in parallel with a reverse diode. It is observed that, regardless of the discharge polarity and the type of ESD protection at the IO, the on-chip VDD supply experiences bipolar voltage fluctuations (noise).

Additional simulations indicate that, in the case of this particular test chip, an on-chip decap in the range of 1-2 nF would be sufficient to limit the amplitude of the supply voltage fluctuations to a range in which digital circuits are not affected; however, not all commercial ICs have area available to accommodate that amount of decap on-chip. Since the on-chip decap will usually be too small to eliminate ESD-induced supply noise, it is worthwhile to further examine the phenomenon. Circuit simulations indicate that the amount of the supply voltage overshoot and undershoot mainly depends on the characteristics of the rail clamp and the bond-wire inductances, as well as the decap size, and it may not monotonically increase with the ESD level.

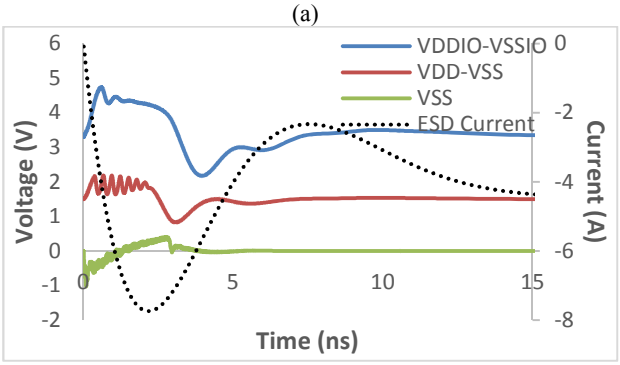
If the ESD current is injected into an IO pin, the on-chip protection will shunt the current to VDDIO or VSSIO. For the case of a chip with just a single power domain, one can easily derive the condition for no fluctuations of the on-chip supply voltage; this is given in Eq. (1) for the (usual) case that the board-level supply voltage is well-maintained by the (large) decaps on the circuit board.

$$L_{VDDIO}\frac{di_{VDDIO}(t)}{dt} = L_{VSSIO}\frac{di_{VSSIO}(t)}{dt}, \quad (1)$$

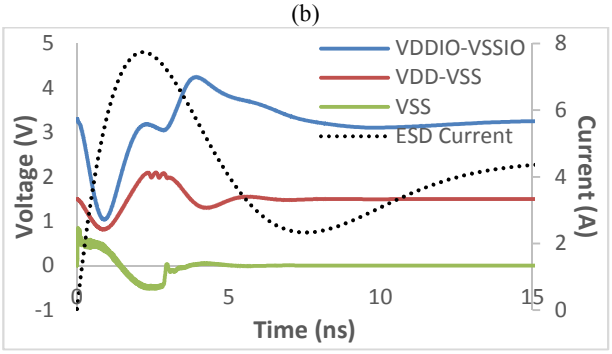
where L_{VDDIO} is the equivalent inductance of the bond-wires connected to VDDIO, L_{VSSIO} is the equivalent inductance of the bond-wires connected to VSSIO, and i_{VDDIO} and i_{VSSIO} are the currents



(a)



(b)



(c)

Figure 2. Simulated on-chip waveforms for (a) +2 kV and (b) -2 kV IEC 61000-4-2 ESD injection to a dual-diode protected IO, and for (c) +2 kV ESD injection to an IO protected by a local clamp. VSSIO and VSS are connected by APDs. VDDIO (3.3V) and VDD (1.5V) are supplied to the chip through package pins. Bond-wires connect the die to the package.

returning to the board via the VDDIO and VSSIO nets, respectively. Since the magnitude of the ESD current can be much larger than the chip's normal current consumption, it follows that

$$i_{VDDIO}(t) + i_{VSSIO}(t) \cong i_{ESD}(t), \quad (2)$$

where $i_{ESD}(t)$ is the total ESD current injected into the IO. Eqs. (1) and (2) suggest that the on-chip decap and the rail clamp could help to distribute the ESD current evenly between the two nets so that comparable voltages are induced across L_{VDDIO} and L_{VSSIO}. This will especially benefit the power integrity in the case that it is infeasible to use a low-

inductance package that minimizes L_{VDDIO} and L_{VSSIO}.

The rail clamp is a non-linear device which turns on only when the on-chip supply voltage is higher than normal. The equivalent resistance of the rail clamp is a decreasing function of the current through it, and thus it directs an increasing fraction of the ESD current to the VSSIO net as the ESD level is increased. This leads to a non-monotonic relation between supply noise and the ESD level.

As noted earlier, ESD noise is transmitted from the IO supply to any other on-chip supplies through the APD or a shared ground net. The label VDD is used to denote the non-IO supply; its power integrity during ESD may be understood with the aid of the simplified circuit schematic in Figure 3. I'_{ESD} is the current that flows through the APD to the VSS net; the resulting noise on VDD is proportional to the transfer impedance, Z_{Tapd}.

$$Z_{Tapd} = \frac{vdd - vss}{i'_{esd}} = \frac{sL_{VSS}}{1 + \frac{Z_{off-chip}}{Z_{on-chip}}}, \qquad (3)$$

where

$$Z_{off-chip} = \frac{1}{sC_{off-chip}} + s(L_{VDD} + L_{VSS}) + R_{off-chip} \qquad (4)$$

$$Z_{on-chip} = R_{load} || \frac{1}{sC_{on-chip}} \qquad (5)$$

Above, $C_{on-chip}$ is the on-chip decap connected to VDD. R_{load} represents the circuitry between VDD and VSS; this resistance is usually large (e.g., hundreds of Ohms) under normal operating conditions. L_{VDD} is the sum of the supply bond-wire inductance and the ESL of the off-chip decap, $C_{off-chip}$, and L_{VSS} is the ground bond-wire inductance. For wire-bonded packages, the bond-wire inductances usually dominate the package inductances. $R_{off-chip}$ is the sum of the ESR of the off-chip decap and the resistance of the trace connecting the power pin to the off-chip decap, and is usually negligible compared to the other terms in $Z_{off-chip}$ in the frequency range of interest, which is typically above the series resonant frequency of L_{VDD}, L_{VSS} and $C_{off-chip}$.

The magnitude of the transfer impedance must be small to achieve good power integrity during ESD; (3) indicates that the desired result occurs if the impedance of the on-chip path between VDD and VSS, $Z_{on-chip}$, is much smaller than that of the off-chip path, $Z_{off-chip}$, over the frequencies of interest, or if L_{VSS} is small. For IEC 61000-4-2 compliant discharges into a self-protected IO, the first current peak primarily consists of components in the hundreds of MHz range [11]. For chips in wire-bonded packages, L_{VSS} and L_{VDD} are several nH, and the magnitude of sL_{VSS} in Eq. (3) is on the order of Ohms. For moderate ESD levels, I'_{ESD} is several Amperes. Circuit boards typically contain a large amount of decoupling capacitance; for $C_{off-chip}$ of at least a few hundred nF, $Z_{off-chip}$ is dominated by the term $s(L_{VDD} + L_{VSS})$. For the magnitude of the transfer impedance in (3) to be small, it is required that

$$2\pi f \frac{L_{VDD} + L_{VSS}}{L_{VSS}} C_{on-chip} \gg 1\,, \qquad (6)$$

at frequencies f in the range of several hundred MHz. The design guideline in (6) is consistent with circuit simulations showing that nF-scale $C_{on-chip}$ is needed to limit the fluctuations of VDD to a tolerable few hundred mV on the wire-bonded test chip of [9].

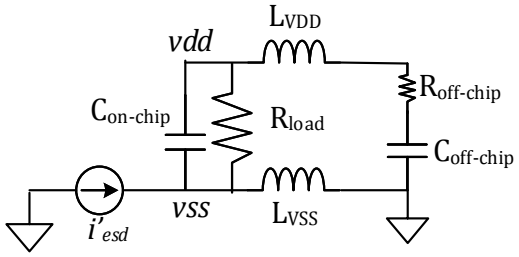


Figure 3. Circuit used to analyze the noise susceptibility of the on-chip supply to the ESD-induced ground current.

R_{load} was not considered in the derivation of (6) because the requirements on L_{VSS} and/or $C_{on-chip}$ need to be formulated for the worst-case ESD zap. R_{load} decreases significantly if the ESD protection circuit between the power and ground nets turns on; otherwise, $C_{on-chip}$ is the dominant term in $Z_{on-chip}$, as is assumed in (6). As shown in Figure 2, for the case of a positive discharge to an IO pin, VDD first experiences an under-voltage transient and the rail clamp will not yet have turned on, regardless of the ESD protection at the IO; thus, R_{load} is large. Of course, the reverse diode between *VSS* and *VDD* becomes forward biased if the under-voltage is sufficiently large, but at this point the supply polarity has been reversed and that is precisely the type of very large amplitude disturbance one tries to avoid with the aid of (6).

III. Integrated voltage regulator

Figure 4 shows a typical LDO used for on-chip voltage regulation. A well-designed LDO will have a large power-supply rejection ratio (PSRR); this will prevent ESD noise on VDDIO from propagating to VDD. Stability is a major concern when designing an LDO; it is achieved by ensuring that the dominant pole lies at a significantly lower frequency than do the others. An LDO cannot respond instantly to a rapid change of load, due to its limited bandwidth. Therefore, decoupling capacitance C_{DD} is placed on VDD to minimize voltage fluctuations when the load changes, e.g., when the current being drawn from VDD changes due to logic activity. If the required decoupling capacitance is large, it is reasonable to place the dominant pole at the LDO output. Otherwise, it is placed at the gate of the pass transistor; capacitor C_0 is added–usually in a Miller configuration–to obtain the desired frequency response.

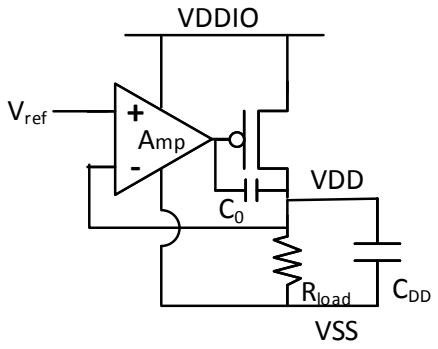


Figure 4. Typical on-chip LDO design. R_{load} represents the LDO load, which consists of the circuitry in the VDD domain.

Two separate test chips, each containing an integrated voltage regulator, underwent IEC 61000-4-2 testing. Each test chip contained supply noise monitor circuits. On one test chip, the internally-generated supply domain experienced much less ESD-induced noise than did the supply domains with external voltage regulators; however, the internal supply domain on the other test chip had a great deal of ESD noise. In both cases, the LDO had a high PSRR and was stable. The experimental details and analysis of results are provided in the following sections.

IV. Experiment

Figure 5 shows Regulator Design A, which was used on a 65-nm CMOS test chip. This LDO uses an NMOS pass transistor. The dominant pole of this design is placed at the gate of the NMOS pass transistor by adding C_0. For simplicity, the 1.2 V reference for the comparator was generated externally, but it passes through an on-chip low-pass filter that removes noise of the type shown in Figure 2. The chip contains a single VSS bus that is common to the IO and core supply domains.

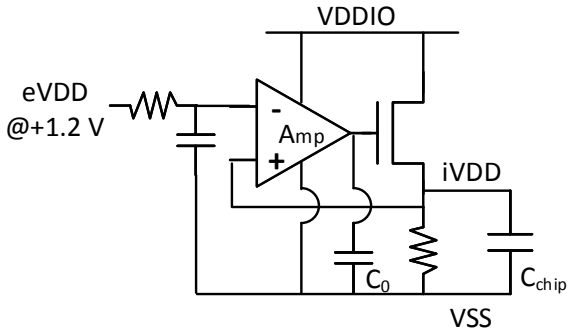


Figure 5. Voltage regulator design A. C_0 is added to the gate of the NMOS driver for stability. The body of the NMOS is tied to VSS.

The test chip with Design A contains a noise monitor circuit that signals the presence of large-amplitude differential-mode noise on the supply; the schematic is shown in Figure 6 [12]. The circuit is initially reset to $OUT = 0$. RST is an external signal that is filtered on-chip by an RC filter with a 100-ns time constant. As shown in Figure 2, ESD may cause the net supply voltage ($VDD - VSS$) to decrease briefly, which causes the two capacitors in the circuit to partially discharge through the cross-coupled inverters. If the supply voltage falls below a certain level, the output of those inverters becomes indeterminate; once the supply starts to recover, the displacement current through the capacitors will cause the stored bit to be flipped relative to its original value and thus $OUT = 1$. Circuit simulation may be used to find the minimum supply voltage undershoot that will cause the monitor output to flip states. The supply voltage waveform used in the simulations is shown in Figure 7. The simulation results are shown in Figure 8; it is observed that ΔV, the minimum magnitude under-voltage that causes the output to change states, depends on the time duration of the under-voltage event as well as the parameter t_r, which measures the speed of the recovery.

The monitor's output is trustworthy only if the *RST* signal is undisturbed from its logic-low state by the ESD-induced supply fluctuations. As shown in Figure 6, *RST* is connected to an NMOS transistor

whose gate-to-source capacitance causes *RST* to be more strongly coupled to VSS than to VDD. Unless there is a very large over-voltage transient, RST cannot be pulled high enough to reset the latch to 0. The supply voltage overshoot, $\Delta V'$, in this test chip is limited by its efficient rail clamp, and *RST* appears to stay low.

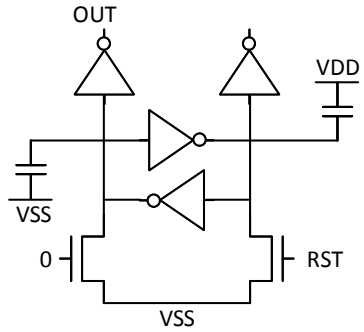


Figure 6. Noise monitor circuit consisting of cross-coupled inverters with asymmetric capacitive loads. The output flips from low to high if there is a large amplitude under-voltage transient on the supply.

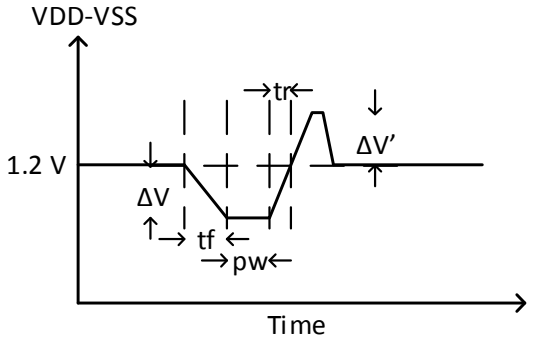


Figure 7. The noisy supply voltage waveform used to simulate output bit flips for the noise monitor circuit.

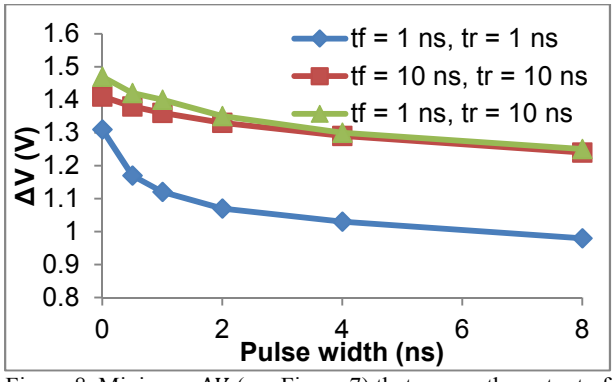


Figure 8. Minimum ΔV (see Figure 7) that causes the output of the noise monitor circuit shown in Figure 6 to change states.

The simulation results in Figure 8 indicate that the noise monitor is quite robust against supply voltage fluctuations unless the supply voltage drops to about zero; that is, the noise monitor will detect only a severe under-voltage transient.

Table 1. IEC 61000-4-2 discharges to an IO pin cause the monitor of Figure 6 to upset at the threshold levels indicated in the table. The monitor is instantiated in both the eVDD and the iVDD power domains. The upset threshold is insensitive to the choice of the zap pin. The ESD gun pre-charge voltage was increased in 1 kV steps.

	Positive		Negative	
	Sim.	Meas.	Sim.	Meas.
eVDD	**1 kV**	**2 kV**	**1 kV**	**2 kV**
iVDD	> 6 kV	6 kV	> 6 kV	> 6 kV

The test chip contains two instantiations of the noise monitor circuit. One is connected to the internally generated 1.2 V supply, iVDD. The other is connected to an externally generated 1.2 V supply, eVDD. The chip was mounted on a battery-powered circuit board and ESD gun discharges were performed. There is no low-impedance DC current return path back to the ESD gun from the battery-powered board. The noise monitor circuit connected to eVDD triggers when the ESD amplitude reaches ±2 kV. In contrast, the noise monitors on iVDD do not trigger up to ±6 kV, as shown in Table 1. Clearly, iVDD is quieter than eVDD during ESD. Notably, based on the simulation results of Figure 8, it is concluded that eVDD briefly collapses to zero following a moderate intensity (2 kV) static discharge to a self-protected IO.

The simulated values of the minimum ESD level needed to trigger the noise monitor are also shown in Table 1. The simulation results show reasonable agreement with the measurements. The simulation netlist includes the ESD tester, ESD protection devices at the IO pin, the package bond-wire inductances for the IO and all power and ground pins, the rail clamps for all the power domains, the on-chip and off-chip decaps, the power and ground buses, and the on-chip LDO.

Figure 9 shows Regulator Design B, which was used on a 130-nm CMOS test chip [9]. This regulator achieves stability if the decoupling capacitance at its output node, C_{chip}, is 60 pF. However, to minimize the voltage fluctuations associated with load changes, a larger decoupling capacitance is needed. For example, for a 1 mA step in the output current, 90 pF is needed to limit the voltage fluctuation to 10%. For simplicity, the 1.5 V reference for the regulator was generated externally (eVDD). The reference voltage eVDD is unfiltered and will become noisy during system-level ESD

but, since the bandwidth of the regulator is 120 kHz, the noise at the reference will have minimal effect on iVDD. The test chip contains two separate ground nets; VSSIO and VSS are connected through APDs. Due to area limitations, the decap on iVDD was only partially placed on-chip. The test chip contains C_{chip} = 16 pF and there was an additional 10 nF of off-chip decoupling capacitance, C_{board}; C_{board} is more than two orders of magnitude larger than the calculated minimum but it was assumed that a larger decap would serve only to further improve the power integrity in the iVDD domain. Placing part of the iVDD decap on the board requires that there is a pin connected to iVDD, and therefore a rail clamp is placed on iVDD. In contrast, the iVDD supply on the previous (65-nm) test chip, which was isolated from the outside world, did not have a rail clamp.

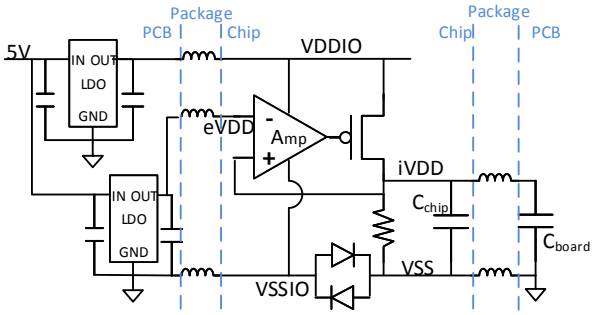


Figure 9. Voltage regulator Design B. C_{board} = 10 nF.

The test chip with Design B contains power supply under-voltage and over-voltage monitor circuits in its eVDD and iVDD supply domains. The monitor circuits can detect and measure nanosecond-scale transient supply disturbances and record the maximum and minimum supply voltages, as illustrated in Figure 10 and Table 2. The details of the supply voltage monitor circuits are given in [9]. The monitor circuit's outputs are read-out after the system-level ESD test.

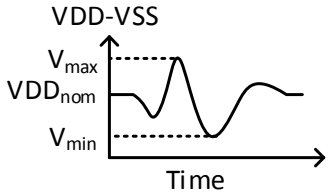


Figure 10. Supply voltage monitor circuits record V_{max} and V_{min}.

ESD gun discharges were made to two IO pins with different ESD protection circuits and the measurement results are shown in Table 3.

Table 2. The supply voltage monitor output levels were calibrated using pulse measurements (pulse-width = 4 ns, rise-time = 200 ps) [9]. The nominal supply voltage is 1.5 V. V_{min} and V_{max} are defined in Figure 10.

	Under-voltage monitor	Over-voltage monitor
Level 0	$V_{min} > 1.15$ V	$V_{max} < 2.1\ V$
Level 1	$0.54\ V < V_{min} \leq 1.15$ V	$2.1\ V \leq V_{max} < 2.29$ V
Level 2	$0.13\ V < V_{min} \leq 0.54$ V	$V_{max} \geq 2.29\ V$
Level 3	$V_{min} \leq 0.13$ V	Not applicable

Table 3. Monitor output readings as a function of the ESD level. IO_A is an IO protected by dual-diodes. IO_B has local clamp protection—a DTSCR in parallel with a reverse diode.

(a) **Under-voltage** monitor readings after system-level ESD.

	eVDD		iVDD	
Vpre (kV)	Zapped IO			
	IO_A	IO_B	IO_A	IO_B
-5	2	2	3	3
-4	1	2	3	3
-3	1	1	3	3
-2	1	1	2	3
-1.5	1	1	1	2
-1	1	1	1	2
-0.5	0	0	1	1
0	0	0	0	0
0.5	0	0	1	1
1	1	0	1	1
1.5	1	1	3	2
2	1	2	3	3
3	2	3	3	3
4	3	3	3	3
5	3	3	3	3

(b) **Over-voltage** monitor readings after system-level ESD.

	eVDD		iVDD	
Vpre (kV)	Zapped IO			
	IO_A	IO_B	IO_A	IO_B
-5	2	2	2	2
-4	2	2	2	2
-3	1	2	2	2
-2	1	1	2	2
-1.5	1	1	1	1
-1	1	1	1	1
-0.5	0	0	1	1
0	0	0	0	0
0.5	0	0	1	1
1	1	0	1	1
1.5	1	1	2	1
2	1	1	2	2
3	1	1	2	2
4	2	2	2	2
5	2	2	2	2

Evidently, iVDD is subject to even more noise than eVDD. This finding is in marked contrast to that for Design A (see Table 1). Design B had not been expected to have worse ESD robustness than Design A. It had been expected to have somewhat

better noise isolation between its power supply domains than did Design A, because it uses separate VSSIO and VSS buses.

V. Analysis of the results

There are three possible sources of the noise on iVDD: differential noise on VDDIO with respect to VSS, differential noise on eVDD, and noise on VSS. To separate the contribution of each, the simulation setup of Figure 11 is used to inject noise from just one of the sources at a time. The voltage waveform used for each noise source is obtained from the -2 kV ESD simulation results.

Figure 12 and Figure 13 show the effect of each noise source on the power integrity of iVDD. For Design A, none of the sources generate a strong disturbance on iVDD. For Design B, VSS noise generates supply noise, i.e., fluctuations of $(iVDD - VSS)$. Design B is sensitive to VSS noise because its iVDD was connected to a large off-chip decap.

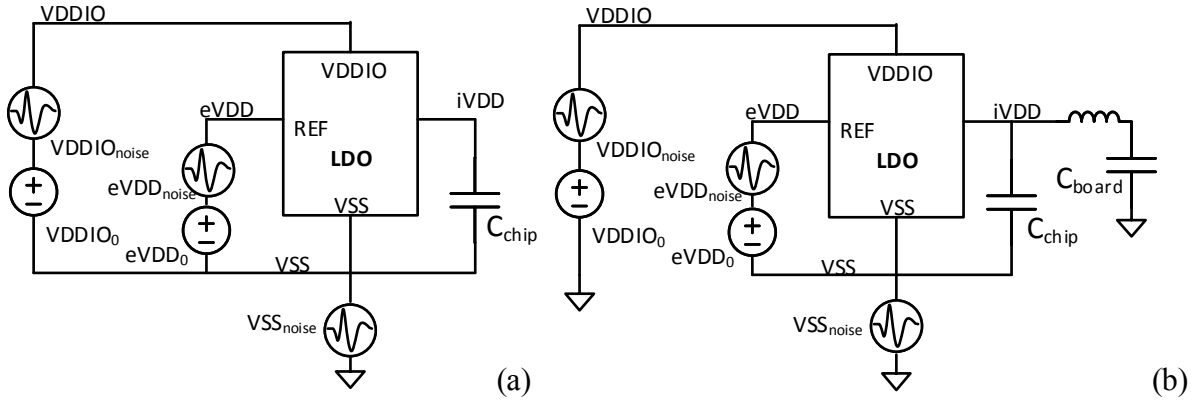


Figure 11. Supply noise simulation setup for (a) Design A, (b) Design B. Only one noise source is active in a single simulation.

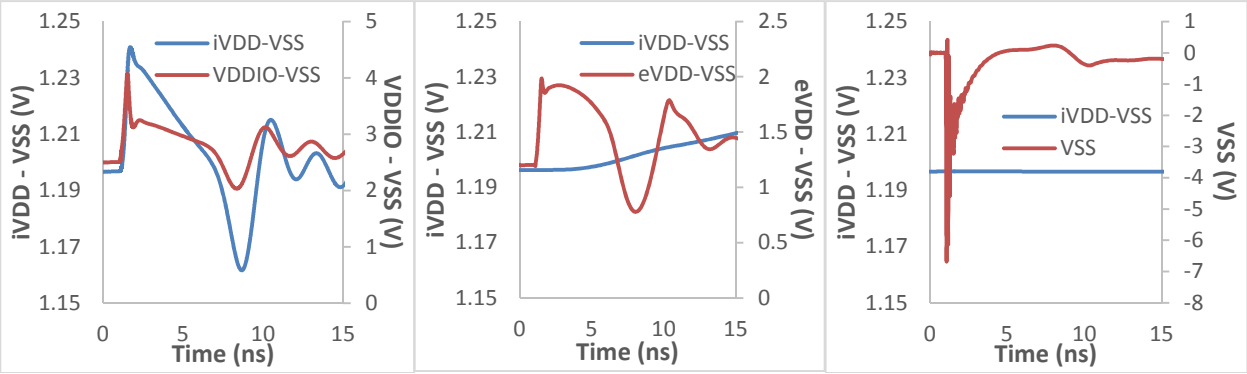


Figure 12. Design A. Simulated response of iVDD (in blue) to various noise sources (in red). (a) Noise source is on VDDIO (w.r.t. VSS) (b) Noise source is on eVDD (w.r.t. VSS). (c) Noise source is on VSS (w.r.t. board ground).

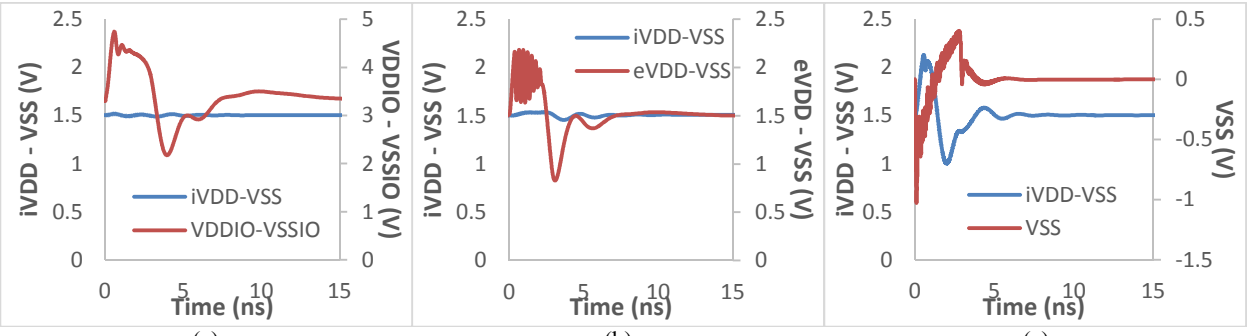


Figure 13. Design B. Simulated response of iVDD (in blue) to various noise sources (in red). (a) Noise source is on VDDIO (w.r.t. board ground) (b) Noise source is on eVDD (w.r.t. VSS). (c) Noise source is on VSS (w.r.t. board ground).

Figure 14(a) shows the schematic used to explain the results of those simulations. ESD induces voltage fluctuations on both VDDIO and VSS. The voltage fluctuations may be separated into the common-mode noise on VDDIO and VSS, $v_c(t)$, and the differential-mode noise, $v_d(t)$. The total effect is approximated by the linear superposition of the individual contributions from the two sources of noise. Figure 14(b) is used to analyze the effect of $v_d(t)$; it suggests that if the LDO has a large power supply rejection ratio, PSRR, the effect of the differential-mode noise will be small. However, in the actual design, the amplifier of Figure 9 is connected to VSSIO. This detail does not change the conclusion regarding the effect of $v_d(t)$, in part because the noise waveforms on VSSIO and VSS are very similar. The PSRR of Design B is 40 dB at 10 MHz, which is sufficiently large such that the differential-mode noise between VDDIO and VSSIO (or, equivalently, between VDDIO and VSS) is rejected.

The circuit used to analyze the effect of the common-mode noise between VDDIO and VSS is shown in Figure 14(c) and this can be transformed to the equivalent schematic shown in Figure 14(d). The common-mode noise $v_c(t)$ in Figures 14(a) and (c) is the ESD-current-induced voltage difference between on-chip VSS and board ground. It is given by

$$v_c(t) = L_{VSS}\frac{di_{LVSS}}{dt}, \qquad (7)$$

where i_{LVSS} is the ESD current exiting the chip through the bond-wires connected to VSS

The magnitude of this noise increases with increasing L_{VSS} and $\frac{di_{LVSS}}{dt}$. Therefore, having a smaller bond-wire inductance connected to VSS or a smaller ESD current directed to VSS will improve the power integrity of the iVDD domain, consistent with the previous analysis of power integrity in a supply domain without an integrated voltage regulator.

Figure 15(a) includes more details of the LDO circuit shown in Figure 14(d). C_1 represents the sum of the decap in the iVDD domain and the parasitic capacitance of the pass transistor, M_p, connected to $ivdd$. M_p is driven by an amplifier with a transfer function $A(s)$; this amplifier is comprised of an error amplifier and the buffer stage that drives the PMOS pass transistor. The loop in the LDO is

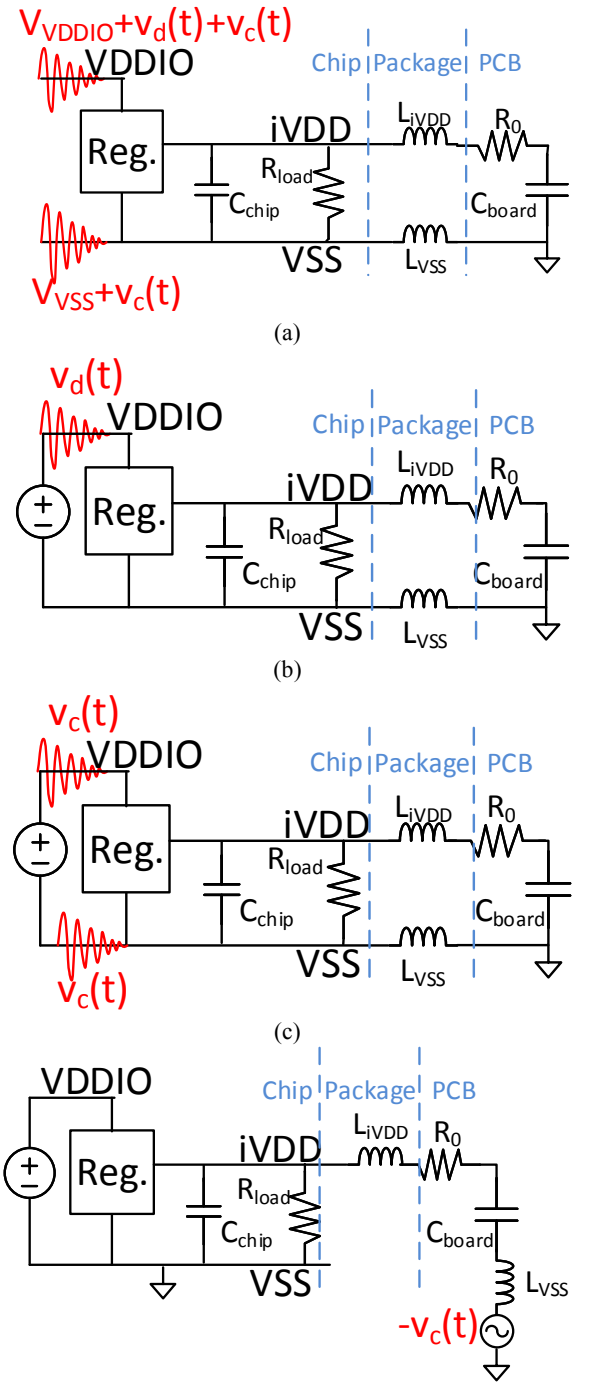


Figure 14. (a) The ESD current induces noise voltages on both VDDIO and VSS. $v_d(t)$ is the differential noise voltage between VDDIO and VSS. $v_c(t)$ is the common noise voltage between VDDIO and VSS. For linear circuits, the total effect is a superposition of the effect of $v_d(t)$ and $v_c(t)$ separately, as shown in (b) and (c). The circuit shown in (d) is equivalent to the one in (c) for studying the noise on $(iVDD - VSS)$.

closed by a feedback stage with a transfer function $f(s)$. In this analysis, it is assumed that the

reference voltage, REF, is quiet with respect to VSS, which is the ground in Figure 15. A quiet reference can be provided by a reference voltage generator, such as a bandgap reference, if low-pass filtering is applied at the output of the reference. The product $A(s)f(s)$ is approximated as

$$A(s)f(s) \approx \frac{A_{DC}f_{DC}}{1 + s/p_1}, \qquad (8)$$

where p_1 is the dominant pole in this product and the term $A_{DC}f_{DC}$ is large.

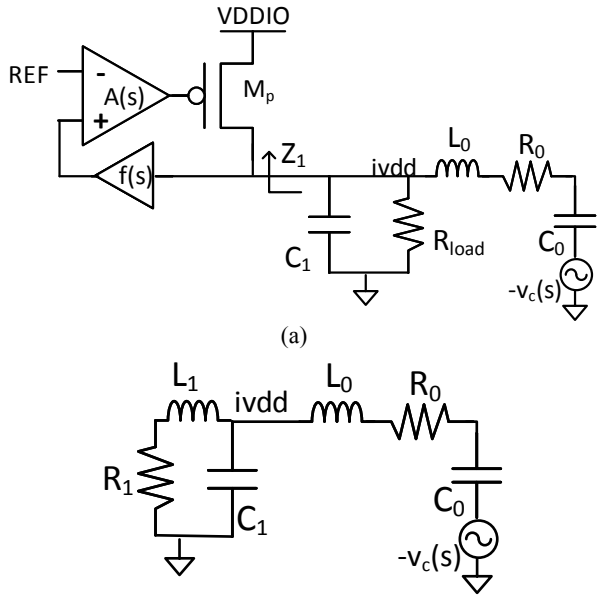


Figure 15. (a) Internally generated power supply subjected to ESD-induced noise $v_c(s)$, including a representation of a generic LDO. L_0 is the sum of the inductance of the bond-wire connected to $ivdd$ and the ESL of the off-chip decap C_0. R_0 is the ESR of the off-chip decap. R_{load} represents the power-consuming circuits in the iVDD domain. (b) Equivalent circuit of the one shown in (a). Since R_{load} is large (several hundred Ohms with several mA of operating current), it is neglected in the analysis.

Eq. (8) is used to formulate LDO design guidelines such that the supply voltage fluctuation during ESD will be limited. The impedance looking into the output of the LDO, Z_l, is given by

$$Z_1 = \frac{1 + s/p_1}{A_{DC}f_{DC}g_{mp}} = sL_1 + R_1, \qquad (9)$$

where

$$L_1 = \frac{1}{A_{DC}f_{DC}g_{mp}p_1}, \qquad (10)$$

$$R_1 = \frac{1}{A_{DC}f_{DC}g_{mp}}, \qquad (11)$$

and g_{mp} is the transconductance of the PMOS pass transistor. Eq. (8) indicates that the LDO may be modeled by an inductor in series with a resistor, as shown in Figure 15(b).

To minimize the voltage fluctuations on $ivdd$ with respect to ground (vss), the voltage gain from v_c to $ivdd$ must be small.

$$\left|\frac{ivdd(s)}{-v_c(s)}\right| = \left|\frac{Z_{on-chip}}{Z_{off-chip} + Z_{on-chip}}\right| \ll 1, \qquad (12)$$

where

$$Z_{on-chip} = \frac{sL_1 + R_1}{s^2L_1C_1 + sC_1R_1 + 1} \qquad (13)$$

$$Z_{off-chip} = R_0 + sL_0 + \frac{1}{sC_0} \qquad (14)$$

A sufficient condition to satisfy the inequality of (12) is given in (15) and an alternative sufficient condition is given in (16).

$$C_1\left(4\pi^2f^2L_0 + \frac{1}{C_0}\right) \gg 1 \qquad (15)$$

where f is in the range of several hundred MHz. Alternatively,

$$\begin{cases} L_1 \ll L_0 \\ R_1 \ll R_0 \end{cases} \Rightarrow \begin{cases} A_{DC}f_{DC}g_{mp}p_1L_0 \gg 1 \\ A_{DC}f_{DC}g_{mp}R_0 \gg 1 \end{cases} \qquad (16)$$

In essence, the inequalities of (15) and (16) indicate that the impedance of the on-chip path from $ivdd$ to vss is much smaller than that of the off-chip path. The inequalities given in (16) suggest that the gain and bandwidth of the LDO be made large, since the gain is in proportion to $A_{DC}f_{DC}g_{mp}$, and the bandwidth may increase with increasing p_1. The test chip with Design B had poor power integrity during ESD because $C_{on-chip}$ does not satisfy the inequality of (15) and the LDO does not have a sufficiently high gain and bandwidth to compensate; additionally, the iVDD bus routing in Design B uses a more resistive metal layer than does eVDD, which tends to make iVDD relatively noisier.

VI. Conclusion

Internally-generated power domains can isolate sensitive circuits from ESD-generated supply noise if the ESD response is considered as part of the design process. If the chip ground will be decoupled from the system ground during system-level ESD events due to the package-level inductance, the use

of LDO designs that require off-chip decaps is inadvisable, unless special care is taken in the design. If an off-chip decap is required, the impedance between the on-chip power and ground nets should be small at frequencies that contribute to the first peak of the system-level ESD current. A small impedance can be achieved either by a sufficient amount of the on-chip decap or by an LDO with a large gain and a high bandwidth.

Acknowledgements

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