High Blocking Voltage ESD Timer Clamp With Mis-Trigger Protection

Sirui Luo, Srivatsan Parthasarathy, Javier A. Salcedo, Jean-Jacques Hajjar

Analog Devices Inc., 804 Woburn St, MS-613, Wilmington, MA 01887 USA
tel.: 781-937-2963, fax: 781-927-2008, e-mail: Sirui.luo@analog.com

50 Words Abstract – A supply clamp architecture is presented which ensure a reliable low leakage performance at the higher supply voltage. An active feedback network designed into the supply clamp architecture ensures uniform clamping through the duration of the ESD event. Mis-trigger immunity is additionally incorporated to ensure reliable functionality up to 5V.

I. Introduction

Complementary SiGe BiCMOS process technologies have become key for the development of RF and high speed analog integrated circuits (ICs). These technologies combine core and I/O CMOS devices operating in the range of 1.8V to 3.3V with higher performance (f_T ~ 15 to 60GHz) and higher voltage (2.5V to 8V) SiGe Bipolar Junction Transistors (BJT) [1]. To achieve these desired electrical characteristics, circuits operate near or at the breakdown voltage ($BV_{CE)}$ in particular) of the bipolar transistors. Consequently, protecting these circuits against electro-static discharges (ESD) becomes very challenging.

One solution to this is using the low voltage CMOS cells to build the high voltage tolerance clamp. There are couple of designs has shown promising data on that. However, it is extremely risky to using those low voltage cells on the high voltage domain. The voltage drop on the gate will varies depending on the different operating conditions. If one of the transistor used are overstressed during any possible situation, the ESD clamp will facing unstable reliability issue which can potentially causing the whole chip latching at the normal operation.

To overcome this issue and adopting the benefit of high voltage SiGe bipolar junction transistors, a bipolar-based transient-triggered power supply clamp has been demonstrated [2]. However, in regards of the RF and high speed analog applications, such timer clamps are susceptible to trigger during fault conditions resulting from any switching event at the power supply. Such event during the circuit's normal operation will cause the timer clamp to turn on, and the amount of energy is usually too high for the ESD clamp to handle compared the normal ESD event. This work introduces an improved Higher Voltage tolerant clamp circuit utilizing SiGe bipolar junction transistor in the BiCMOS SiGe applications and which also addresses some of the timer clamp limitation described above.

II. Supply Clamp Design

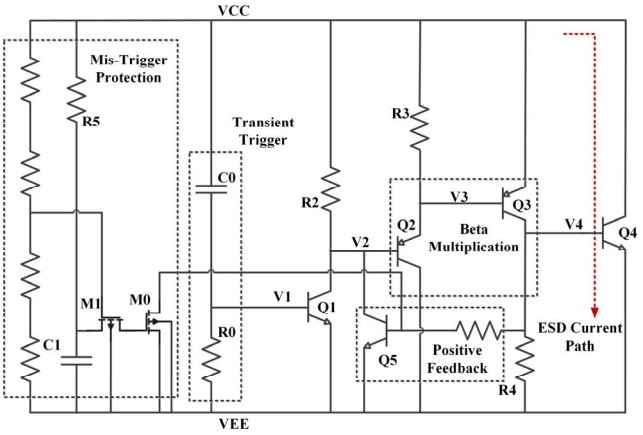

Figure 1: Active bipolar ESD timer clamp with Mis-trigger protection

Figure 1 shows the schematic of the transient triggered bipolar clamp [3] incorporate with the design improvement about the mis-trigger protection and positive feedback to have better transient performance and also help avoid unexpected latching condition from the previous design.

The transient bipolar clamp is implemented on an Analog Devices proprietary 0.18 μm high-performance complementary SiGe BiCMOS process. Deep oxide trenches and a buried SOI (silicon-on-

insulator) substrate are used to isolate the devices from each other and also from the substrate [1].

Traditionally active clamps [5]-[7] employ a RC detection/timing network with a 1 μs time constant to activate and keep them in the on-state during the ESD event. The latter vary between 10ns and 0.7us for the CDM (Charged Device Model) and HBM (Human Body Model) ESD classification tests, respectively. The detection/timing circuit for the clamp comprised of a capacitor resistor network (C0, R0) and a NPN (Q1) transistor. During the ESD event, characterized by current rise times ranging from 0.2 to 10 ns, the capacitor resistor network couples a portion of the ESD signal in the form of a voltage developed across the emitter-base junction of the NPN (Q1) and turns it on. Since node V2 is being pulled to ground it forces Q1 into the saturation region of operation.

The second stage consists of PNP transistors Q2/Q3 configured as a Darlington-pair. The primary function of this block is to provide current gain (β) multiplication. This stage is activated in two steps: 1) Q1 turns on and pulls the base of the Q2 to GND resulting in its activation and 2) once Q2 is turned on, it pulls the base of Q3 to a voltage that is a diode drop above GND. As the second β multiplication stage is activated, it results in the triggering of the main current handling PNP (Q4). The built-in beta multiplication helps optimizing the size required for the final stage PNP by maximizing its current handling capability. The clamp footprint in general is dominated by the discharge path stage, as this stage takes most of the stress.

By making use of the V2 note are pull to the ground and keep Q1 in the saturation mode, Q5 turns on due to the connector of Q3 were pulled up. This positive feedback keeps clamp on, resulting in a smaller RC network. A R0 (25KΩ)*C0(500fF) were used here to make sure clamp won't shut down during the ESD current conduction. Comparing with the previous data [4] where a R0 (25KΩ)*C0(2pF) time constant of 50ns will causing clamp shuts off after 250ns.

The mis-trigger protection was built using a NMOS (M0) devices to pull the node (V4) down to the ground during the power-on normal operation condition. When there is constant supply voltage, the voltage on the middle of the resistor chain will turns on the M1, which will help the M0 keep in the "on" state. A second RC network were used in this clamp to help to pull the gate of M0 to high during the normal DC operation. And during the ESD current conduction, this RC network will act faster than the resistor chain, so that the M0 transistor won't turn on during the initial stage of the ESD current.

The mis-trigger protection block will behave like a negative feedback while there is any voltage drop on the supply after some amount of time when the M0 turns on. In order to make sure the full conduction of the ESD current, a positive feedback was also been added using another bipolar transistor (Q5). While the node V4 was pulled high during ESD event, it will also help turn on the Q5, which helped to ensure the node V2 is at low state. And that eventually helped the longer ESD current conduction.

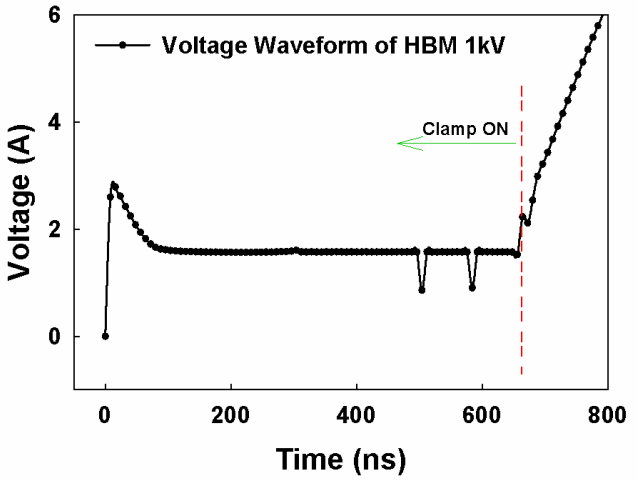

Figure 2. Voltage waveform of 1kV HBM simulation

During the clamp designing, a transient HBM simulation has been used to understand the clamping voltage capability on this clamp. Figure 2 shows the simulated voltage waveform of 1kV HBM stress. The clamp remains ON for around 700ns, which is close to a standard HBM stress event duration (600ns). A long on-state time ensures that most of the ESD transient is dissipated in that duration. In this case simulation indicated that the clamp was ON for the major portion of the ESD signal. To clarify a clamp is defined to be "ON" as long as the voltage across it remains linear. Noted the voltage increases after the clamp shuts off in the simulation. This is due to the ideal HBM generator was used, and the little amount of the current after clamp in the off state will result in the voltage going up.

The layout of the bipolar device in the discharge path stage is also required to use uniform and wide low impedance metallization to properly handle the stress current. On the 5V supply clamp, another area-intensive component is the capacitor. Because only MIMCAP or MOMCAP are able to sustain 5V reliably other than the area efficient MOS capacitor. Relatively small capacitor value used in this clamp helps minimize the extra area that is required. Metal-insulator-metal (MIM) were choose to be utilize here

within a relatively small area, for instance using high-level metal 4 and metal 5. Thereby, a good portion of the capacitor can be placed above the bipolar control circuit layout without impacting the total clamp footprint. For the rest of the components in the bipolar control circuit stages, the layout arrangement and aspect ratio can be relaxed without risk of compromising the transient-triggered bipolar clamp performance. The supply clamp has a total area of ~ 105 x 127 μm^2.

A. Clamp Mis-trigger analysis via SPICE simulation

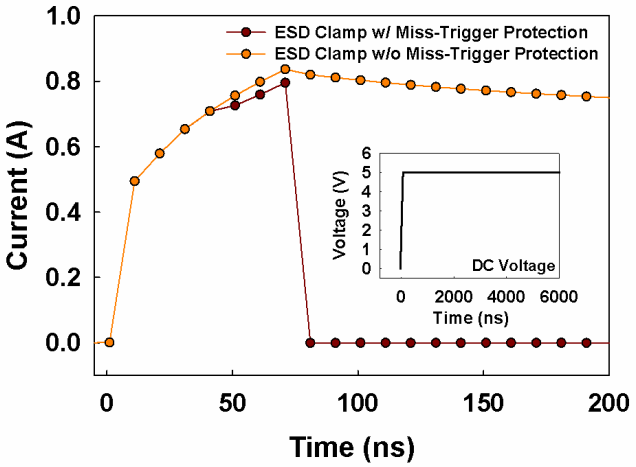

Figure 3: Voltage ramp from 0V to 5V on the supply

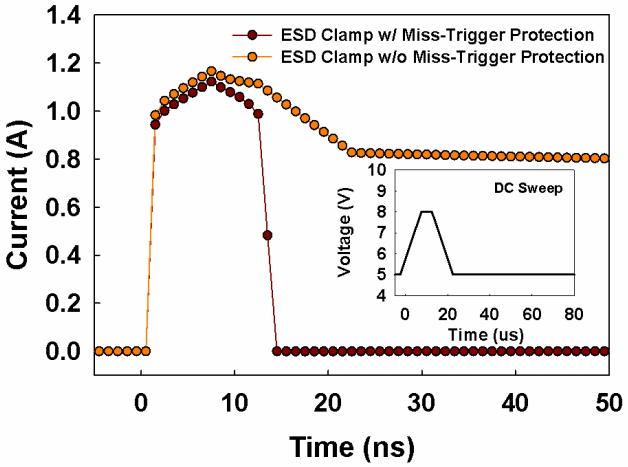

Figure 4: Noise during the circuit operation

Analysis from the previous bipolar ESD clamp design [4] has been demonstrated the potential mis-trigger condition for sub 500ns ramp rates. To compare the performance of this timer clamp with or without mis-trigger protection, we did voltage ramp simulation in the SPICE. Shown in the Figure 3, depicts first voltage ramp condition: from 0V to the operation voltage (5V) within 100ns. The clamp current start latching after subject to such fast event as shown in the orange curve. This is a limitation associated with any transient triggered clamp. Once the ramp rate is in the vicinity of the R*C time constant of the clamp, there is a potential to activate the clamp and trigger it. This is due to the introduction of the positive feedback loop where the internal node V2 if forced to go to a low potential, which result continues latching. Current will only end when there is thermal failure of the junction at the main current conduction bipolar Q4.

However, with the mis-trigger protection, the clamps conduct limited amount of current and shut itself down as shown in the dark brown curve.

Another possible condition happens when the circuit are during the power on condition while the supply is subjected to the fast rise noise event, as shown in Figure 4, or internal node V2 is pulled up by some coupling effect on the power rail. Similar to the previous condition, the clamp without the mis-trigger protection immediately started to latch at 1A current level and stays on subsequently, but the one with the mis-trigger protection only conduct 10nA current during the noise spike. It shuts off after the noise dissipates.

III. Measurement Data

A. DC-Analysis

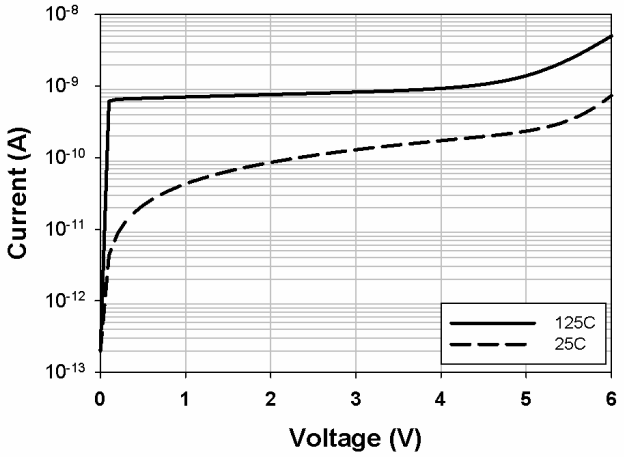

Figure 5: DC leakage characterization

To reduce leakage during standard circuit operation resistors R2, R3 and R4 are incorporated. Additionally, the long channel MOS devices were using as the resistor voltage divider and optimized for low leakage. Since there is very little current flow

through the resistors during regular circuit operation the effective voltage drop across them is negligible. This ensures nodes V2 and V3 are pulled to VCC, effectively turning off the transistors and minimizing any form of leakage during regular circuit operation. Figure 5 shows the DC current-voltage (I-V) characteristics of the clamp at 25°C and 125°C. The low standing leakage current level obtained in this clamp is also critical to maximize energy efficiency for battery-powered RF systems.

B. Quasi-static-Analysis [TLP Characterization]

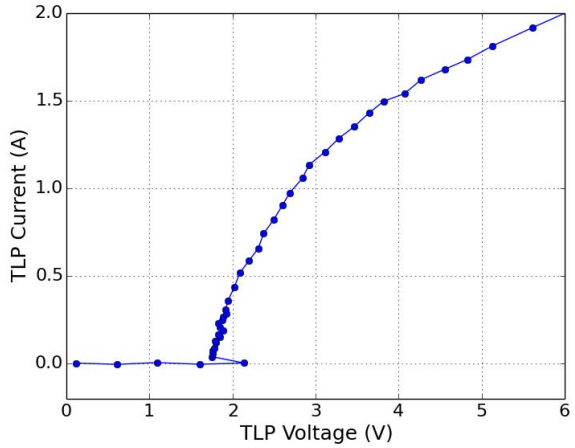

Figure 6: 100ns TLP of mis-trigger timer clamp

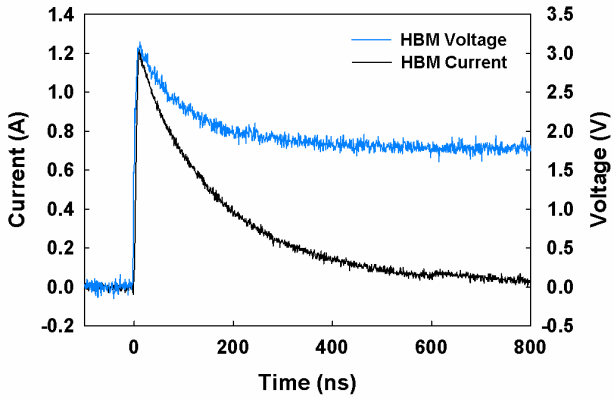

Figure 7: HBM results of mis-trigger timer clamp

To investigate the ESD robustness of the bipolar clamp, transmission line pulse (TLP) measurements are performed. The measurements are performed using a 100ns current pulse with a 10ns rise time, which helps us understanding the ESD current clamping capability. Figure 6 shows the measured quasi-static current vs. voltage TLP characteristics. The transient activation helps to achieve this low trigger voltage (2v), where in normal operation condition it will have blocking voltage higher than 6V as DC shown in the Figure 5. Similarly to the MOSFET based timer clamp cell, there is low risk of latch up. Besides this is built in a trench isolated process, so there is no latch-up.

The clamp itself will be able to take 3A+ TLP current. But it is to be noted that high f_T bipolar transistors in this process have a collector to emitter breakdown of 7 to 9V. In consideration of the IO protection devices, the proper design window for the clamp is to have a holding voltage lower than 6V. And as shown in the figure 6, the clamp is able to take 2A TLP current which is equal to roughly 2.5kV HBM without leakage change. We believe it is possible to handle more than 2kV HBM Stress in the applications.

To future verify the HBM performance, a HBM stress is also investigated for this clamp, and Figure 7 shows the transient current and voltage waveform from a 2kV HBM stress. No leakage changes were detected after stress. The clamp itself are able to clamping the current without any problem.

Conclusion

An improved transient triggered bipolar clamp architecture has been demonstrated in a 0.18-μm SiGe BiCMOS process. The clamp is formed using five stages: the detection and timer; the current gain multiplication; the positive feedback; the negative feedback and the discharge path stages. The negative feedback, as part of the mis-trigger network, provides false-trigger immunity against fast voltage ramps or noise spike during the normal operation of the circuit. The simulation and measurement results has demonstrated the robustness of this clamp and its performance during the ESD events.

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