Correlation study of different CDM testers and CC-TLP

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Abstract – This paper analyzes the correlation between test results of three different CDM testers and corresponding results of Capacitively Coupled Transmission Line Pulsing (CC-TLP). Furthermore, it discusses the significance of the current slew rate as an additional failure threshold and the reasons for a poor reproducibility of CDM failures.

I. Introduction

The Charged Device Model (CDM) is the primary cause for electrostatic discharge (ESD) failures in manufacturing and automatic handling. There is a wide range of possibilities of characterizing the susceptibility of a device to damage from ESD under CDM conditions. Apart from the choice of the ESD standards, e.g. JESD22-C101 [1] or ANSI/ESD S5.3.1 [2], which have recently been replaced by the joint standard ANSI/ESDA/JEDEC JS-002-2014 [3], one can choose between a handful of different CDM testers and test equipment.

The weakness of CDM is its limited reproducibility and repeatability caused by the strong variation of the spark resistance during the air discharge [4]. To increase the repeatability, the contact-mode test method Capacitively Coupled Transmission Line Pulsing (CC-TLP) [5],[6] was developed.

Like the CDM testers, CC-TLP needs to reproduce the failure locations and failure signatures of field failures in order to meet the requirements of a real-world CDM test. Furthermore, CDM and CC-TLP should replicate the same failure threshold level. Starting with an "ancient" 3 µm NMOS technology, this correlation was demonstrated for 130 nm and 90 nm CMOS technologies, at package and at wafer level as well as on a 0.35 µm Chip-on-flex (COF) technology in several studies in the last decade [7]-[12].

This paper extends these studies by investigating the correlation between CC-TLP and three different CDM testers regarding the reproducibility of the test results and the failure threshold, signature and location of an IC designed in a 0.25 µm BCD technology. In addition, the reasons for a poor reproducibility of the CDM test results are discussed.

II. Measurement equipment and device-under-test

A. CDM testers

To characterize the correlation between the different CDM testers, we performed field induced CDM stress tests according to JESD22-C101F [1]. This standard requires an oscilloscope with single shot bandwidth of 1 GHz for calibration. The qualification test itself requires at least one positive and one negative stress pulse per pin. The stress currents are recorded, however, there is no upper limitation on the bandwidth, which makes the comparison of the different CDM tests more difficult (see Table 1).

	CDM			CC-TLP
Test Equipment	A	B	C	
Scope Bandwidth (GHz)	6	4	8	33
Number of Pulses	1	3	1	multiple (step stress)

Table 1: Used test and measurement equipment as well as the number of pulses per pin and stress polarity.

B. CC-TLP equipment

CC-TLP is a contact-mode test method alternative to CDM. It combines the narrow-pulse high current stress pulses known from CDM with the reproducibility of Very-Fast Transmission-Line Pulsing (VF-TLP) [13], by directly connecting only one pin or pad of the device-under-test (DUT). In contrast to CDM, CC-TLP can be applied both on package level and on wafer level. While the contact needle of the CC-TLP probe is connected to a single pin of the floating DUT, a highly reproducible fast rising rectangular voltage pulse is created by the VF-TLP generator and transmitted through a coaxial cable and the contact needle of the probe to the DUT (see Figure 1). The CC-TLP probe contains a round, gold-plated brass plane called Ground Plane (GP), which is connected to the outer conductor of the coaxial cable. It is positioned above the DUT to form a background capacitance (C_b), which corresponds to the distributed capacitance of a packaged device in the CDM test. Thereby, it establishes the ground return path. During a CC-TLP pulse, the background capacitance C_b charges up during the rising edge of the pulse and discharges during the falling edge of the pulse. Identical to the VF-TLP the obtained data from

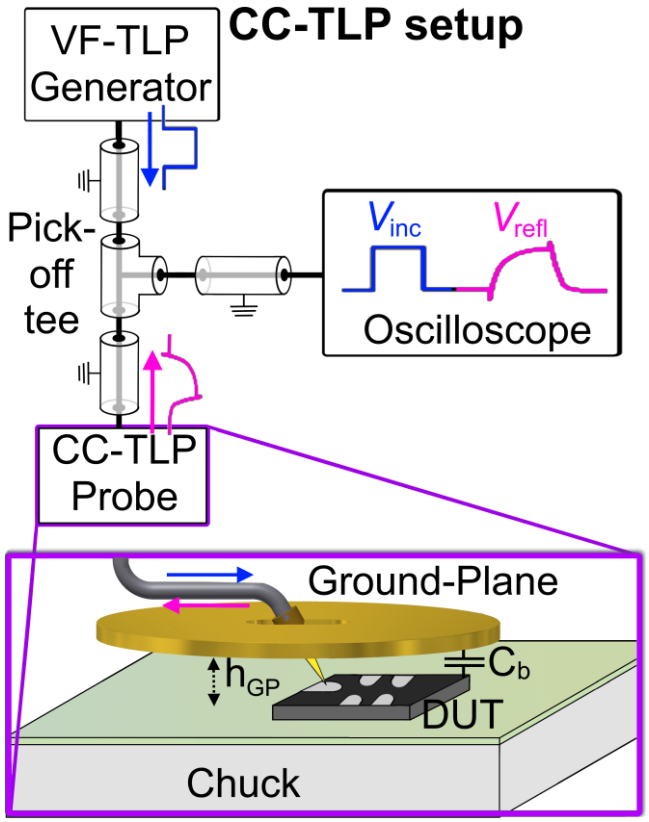

Figure 1: Principle probe set-up for CC-TLP testing on package level.

a CC-TLP stress consists of an incident voltage pulse $V_{inc}(t)$ and the voltage pulse that is reflected from the DUT $V_{refl}(t)$. The stress current $I_{TLP}(t)$ through the DUT is the superposition of these two pulses:

$$I_{TLP}(t) = \frac{V_{inc}(t) - V_{ref}(t)}{50\,\Omega} \qquad (1)$$

To measure a part of both signals, the voltage pulse is separated and fed into the oscilloscope by means of a voltage pick-off tee between the VF-TLP generator and the CC-TLP probe. The reconstruction of the peak current depends on the exact superposition of the fast rising edges of the measured voltage pulses. Therefore, we used an oscilloscope with a bandwidth of 33 GHz (see Table 1).

C. CC-TLP calibration

Following JESD22-C101F [1] the ESD sensitivity is qualified in terms of voltage levels, which for an ideal CDM tester represent the precharge voltage that is applied to the Field Charge Plate (FCP) of the tester. This voltage is the primary parameter that defines the CDM discharge current. In contrast, the primary parameter of CC-TLP is the stress current. This raises the question how the CC-TLP stress current can be practically reconstructed from the voltages captured by the oscilloscope (1) and how this current can be aligned to the CDM stress levels. The following paragraphs outline the main aspects of CC-TLP calibration and point to possible error sources that could influence the correlation between CDM and CC-TLP.

Similar to CDM, the first step before starting a CC-TLP measurement is the mechanical alignment of the system. This includes the parallel orientation of the GP with respect to the working surface, the compensation of any tilt angles and the adjustment of the GP height with respect to the contact needle tip. The latter specifies the length of the contact needle that protrudes from the GP and thus defines the capacitive coupling between the DUT and the GP [12]. In our measurements, the separation height h_{GP} was set to 0.3 mm. The procedure was performed with the help of an adjustment plate with milled slots of different depths [9].

Another essential point in the calibration procedure refers to the reconstruction of the stress current. By means of the time domain reflectometer principle, it equals the superposition of the incident current pulse and its reflection at the DUT (1). Propagating through a 50 Ω system the incident and the corresponding reflected voltage pulse can be measured time-

separated at the oscilloscope output of the pick-off tee. To reconstruct the pulses at the location of interest, resistive losses of the transmission lines (TLs), especially of the pick-off tee and the impact of resistances in series and parallel to the DUT are removed by calibration and de-embedding. This process corresponds more or less to the calibration in VF-TLP and is principally based on a short calibration [9]. In order to overlap both pulses numerically, the final step is to shift the later arriving reflected pulse by the time step of its additional path towards the earlier arrived incident pulse.

The most straightforward method to determine this time shift is to take the time difference between the rising edge of the incident and the reflected pulse. Depending on the specification of the edges (e.g. the point in time with the highest slope or at zero crossing), the time shift may spread in the range of some tens of picoseconds. That may not seem to be much, however, since the peak current of the stress is achieved in the range of these superposed rising edges, this has a significant influence on the peak current. Figure 2 illustrates how sensitive the peak value of the reconstructed current responds to the time shift.

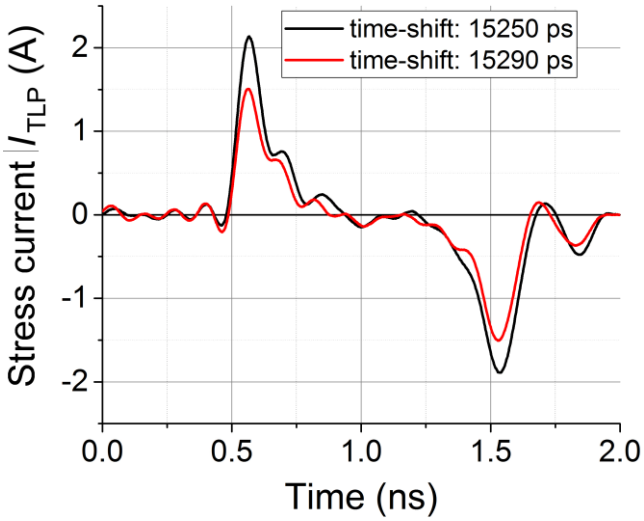

Figure 2: A deviation of the time shift of only 40 ps, which can already result from the selection of the determination method, leads to a peak current variation around 30%.

A more sophisticated technique to determine the necessary time shift is to minimize the residual current, while measuring an open. Figure 3 shows the dependency of the residual current on the time shift calculated by an optimization routine. Note, that the optimum time shift in contact with the DUT may need a small re-adjustment against the time shift measuring an open. A possible error indication for a miscalibrated time shift is a significant undershoot before the rising edge of the stress current. In this case, the reflected pulse was shifted too much in time.

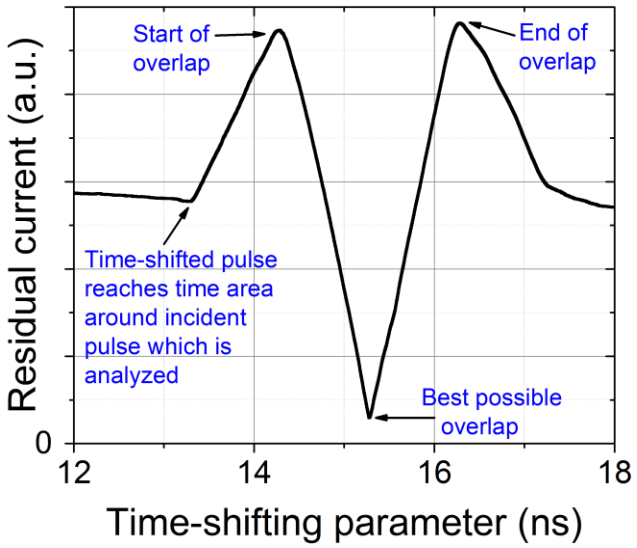

Figure 3: Dependency of the mean residual current on the time shift obtained by the reconstruction routine while measuring an open. Since only the time interval around the superposition is investigated, the residual current rises when the reflected pulse is shifted into this integration area and almost vanishes for the optimum overlap.

Having calibrated the parameters of the reconstruction process, the obtained peak currents have to be compared with the CDM peak currents of CDM reference voltage pulses. This requires that CDM current waveforms are recorded which also allow to monitor their variations caused by the air discharge.

For tester B three stress pulses were used in order to be less sensitive to outliers that do not reach the nominal peak current level and to increase the possibility to reach 100% failure rate. In this case (assuming a hard limit for the CDM robustness), the highest peak current in each set of three stress pulses should be considered. As in the case of no DUT failure, this was the highest stress current of the set below the current failure threshold and in the case of a DUT failure, it was definitively above the current failure threshold.

We can assume in a first approximation that the single CDM peak currents follow a normal distribution [11] (superimposed with unknown distribution due to field emissions). Our calculations have shown that the maxima of each set of three pulses are also normally distributed, of course around their higher means. However, the benefit of using the maximum of three pulses instead of all single pulses is that the standard deviation of this distribution reduces by 25% against the standard deviation of the distribution of single

pulses. This "highest peak current" criterion does not hold, if the failure mechanism is subject to accumulation effects as some junctions display [12]. If this is not the case and if more devices with the same precharge voltage are tested, the maximum peak currents (one for each device) form the relevant dataset of the CDM voltage level.

We refer to a correlation, if the CC-TLP failure threshold current matches the mean peak current of this dataset or in the case of a single stress pulse (as for tester A and C) the mean of all peak currents of one voltage level.

D. Device-under-test (DUT)

The correlation of CDM and CC-TLP according to the failure threshold and failure signature of certain devices has already been shown in some earlier studies [7]-[12]. This paper examines the correlation between four systems, one CC-TLP system and three different CDM testers. The device-under-test (DUT) is an IC manufactured in a 0.25 µm BCD technology and assembled in a package with a footprint of 7.5 mm². Note, since the CC-TLP probe needle is (significantly) smaller than a CDM pogo-pin, even packaged devices with very small pins and pin pitches can be accurately contacted with the CC-TLP probe needle. The response of three pins of this DUT to CDM and CC-TLP stress is investigated.

III. Measurement results

A. Waveform analysis

We started the correlation study by characterizing the waveforms of the four test systems by stressing the ground pin of the DUT. The ground pin was chosen, because it has the least impedance which results in the largest discharge currents. The results are shown in Figure 4. Since the package of the DUT has a very small footprint, the duration of the measured current waveforms is fairly small. To induce the same failures, CC-TLP has to generate a current waveform similar to CDM discharge currents. The pulse width of the stress current I_{TLP} in CC-TLP is determined by the background capacitance C_b, which can be controlled by the distance of the GP h_{GP} above the DUT (see Figure 1) and the pulse width of the VF-TLP generator [9]. By setting the separation height to h_{GP} = 0.3 mm, a 1 ns voltage pulse triggers a stress current waveform with a pulse width of around 300 ps. This resulting current waveform at the interface of the DUT matches the current waveforms of CDM (see Figure 4).

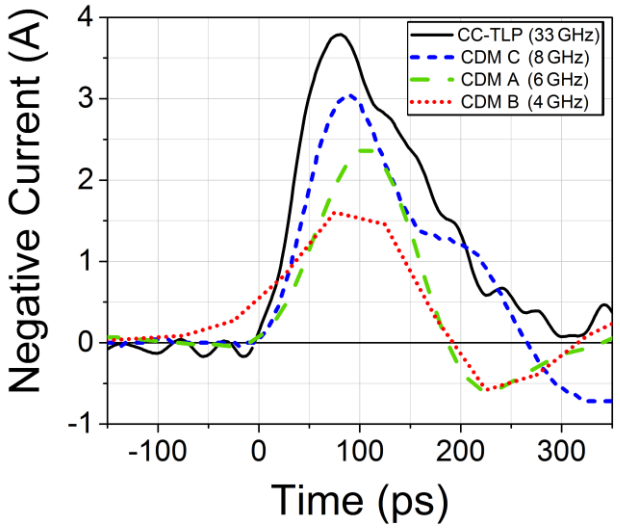

Figure 4: Current waveforms of CDM testers A, B and C for +500 V CDM stress of the ground pin and CC-TLP with a higher current level.

The difference in amplitudes of the CDM curves is due to the variation arising from the air discharge and to the difference in the bandwidths of the oscilloscopes used (see Table 2).

	CDM			CC-TLP
Tester	A	B	C	
Scope bandwidth (GHz)	6	4	8	33
Signal rise time t_r (ps)	72	128	55	49
Signal bandwidth BW (GHz)	5.9	3.3	7.7	8.7
Current slew rate SR (A/ns)	26	10	44	60

Table 2: Reconstruction and comparison of the rise time, bandwidth and current slew rate of the signals (Figure 4), measured by the respective oscilloscopes of the CC-TLP and the CDM testers.

The rise time t_r of the measured output signal indicates how well the system preserves a fast transition of the input signal. For the relation between the rise time and the bandwidth BW of a signal, we use the following common rule of thumb [14]:

$$t_r \cong \frac{k}{BW},\ k \approx \begin{cases} 0.35 & \text{if } f_{Scope} < 1\,\text{GHz} \\ 0.40 - 0.45 & \text{if } f_{Scope} \geq 1\,\text{GHz} \end{cases} \quad (2)$$

Table 2 compares the 10% - 90% rise times of the waveforms shown in Figure 4. Note, the signal bandwidths BW reconstructed from the rise times of the CDM waveforms match the bandwidths of the

used oscilloscopes very well. These bandwidths seem to represent the limiting factor of the given CDM systems.

For CC-TLP, the highest measured bandwidth is only 8.7 GHz which is much lower than the bandwidth of the oscilloscope (33 GHz). Obviously, the rise time of the system is limited by the rise time of the cables, the CC-TLP probe and the pick-off tee which can be estimated by:

$$t_{\mathrm{rSystem}} \cong \sqrt{t_{\mathrm{rCables}}^2 + t_{\mathrm{rPickoff}}^2 + t_{\mathrm{rScope}}^2} \qquad (3)$$

To better understand the CC-TLP lower than expected bandwidth, the high frequency properties of the pick-off tee were closely examined. Figure 5 shows the transmission coefficient S_{21} that characterizes the stress path, from the VF-TLP generator through the pick-off tee to the DUT. The transmission coefficient S_{21} of the pick-off tee from the stress path to the metrology path has a similar behavior and bandwidth. Both 3 dB bandwidths amount to 12.5 GHz and are only a little bit higher than the signal bandwidth derived from the signal rise time (see Figure 4).

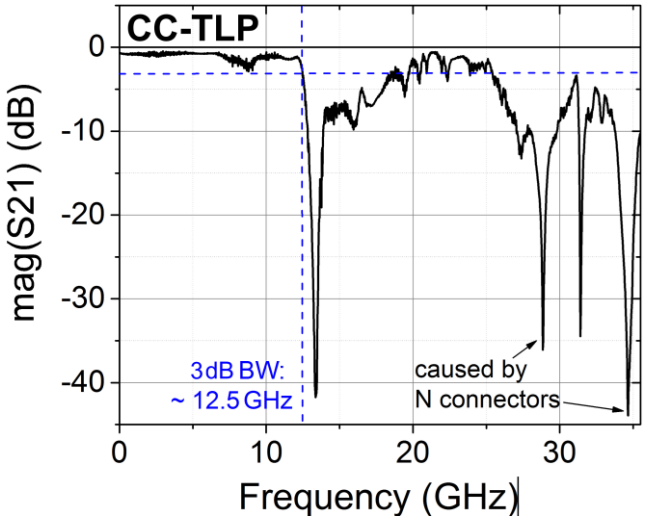

Figure 5: Measurement of the transmission coefficient S21 of the pick-off tee along the stress path. The 3 dB bandwidth is around 12.5 GHz.

Independent of the signal amplitude and a key factor in ESD for the susceptibility of some components or structures to fail is the slew rate *SR*, which is defined as the mean change of voltage or current per unit of time. Hence, it is also limited by the bandwidth of the given oscilloscope, as can be seen in Table 2.

B. Failure threshold analysis

The CDM results obtained with the different CDM testers are summarized in Table 3.

	CDM (testers and failing pins)					
Tester	A		B		C	
Pulses	1 (pos. & neg.)		3 (pos. & neg.)		1 (pos. & neg.)	
< 500 V	27/0		12/0		6/0	
500 V	18/4	(1,2)	6/0		3/0	
625 V	9/5	(1,2)	6/0		3/0	
750 V	18/5	(1,2,3)	6/3	(2)	3/3	(1,2)
875 V	-	-	6/3	(1,2)	-	
1000 V	18/8	(1,2,3)	6/2	(1,2)	3/3	(1,2)
1500 V	18/8	(1,2,3)	-		3/2	(1,2)

Table 3: CDM test results reporting the ratio of the total sample size (left number) and the number of failing samples (right number). The number of the failing pins is denoted in brackets on the right of the corresponding test result.

By polarity split tests we found that the failing pins are sensitive to negative CDM stress, i.e. positive CDM currents. In all tests, CDM stress levels between 250 V and 1.5 kV were used. First device failures were found at 500 V for tester A. Tester B and C started to generate failures at 750 V. Note, in most of the cases, at least half of the tested devices passed the test, even for 1.5 kV. Even for single CDM testers, the threshold voltage was not reproducible. Obviously, pin 3 only failed for tester A.

For deeper analyses, the stress currents for tester B were recorded during the CDM test. Due to the air discharge, the CDM peaks reveal a relative deviation of up to ±20% of the mean value. This is consistent with former statistical analysis of CDM current variations [4]. Although tester C provided the most stringent results, in-situ measurements of its peak current variation showed a spread of up to ± 65% for some stress levels and pins. Measured peak currents at pin 1 and pin 2 are shown in Figure 6.

Still the failure thresholds of testers B and C are in good agreement. This indicates that a failure dependency on the number of pulses per pin can be ruled out for the tested device. In addition, it was verified by means of pre/post CDM stress drift analyses that no passing unit suffered from any degradation or wear-out effect after the stress. Nevertheless, the soft transition from PASS to FAIL of testers A and B and the <100% failure rates of all CDM testers suggest that the reproducibility of the CDM testers is limited.

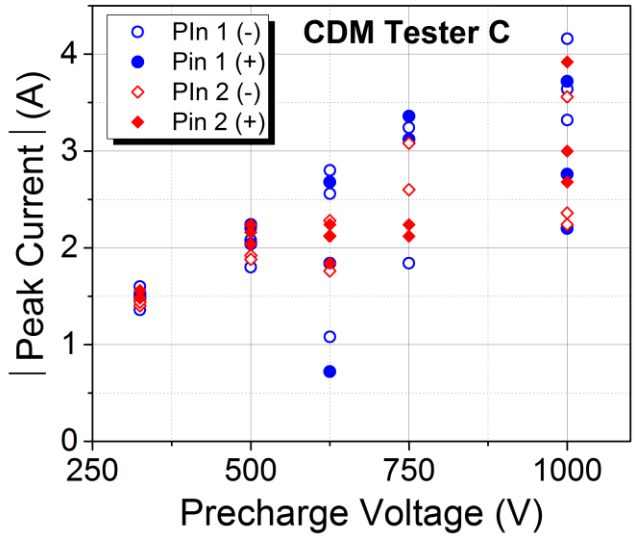

Figure 6: Example of peak currents measured with tester C at pin 1 and pin 2 for three units stressed with one positive and one negative pulse.

For CC-TLP, the failure threshold was determined by a step stress. It was measured by increasing stepwise the pulse amplitude of the TLP system and monitoring the leakage current after each stress pulse. The evolution of the leakage currents is shown in Figure 7.

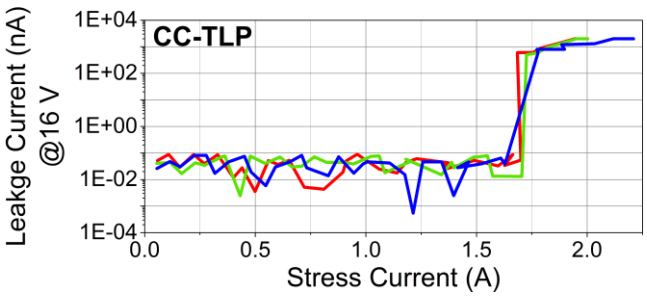

Figure 7: DC leakage current evolution at pin 2 of three different DUTs as function of the CC-TLP stress current.

Figure 8 illustrates the electrical DC characteristic before and after the CC-TLP measurement. This failure signature was found to match the electrical failure signature of the failing units after CDM stress perfectly well (see Figure 9).

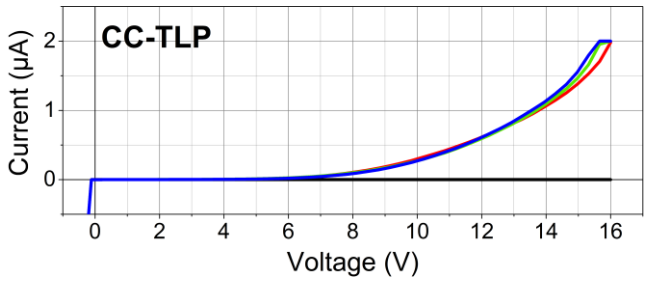

Figure 8: DC curve-traces before (black curve) and after CC-TLP stress at pin 2 of three different DUTs (blue, green, red curves).

For CC-TLP, all pins that were stressed above the failure threshold show a clear leakage current. The CC-TLP failure currents are depicted in Table 4.

Pin	1	2	3
CC-TLP failure threshold current	2.1 A	1.7 A	2.6 A

Table 4: Failure threshold current of CC-TLP. Measured thresholds show a high reproducibility.

In contrast to CDM, the failure thresholds determined by CC-TLP are very reproducible. Single CC-TLP stress pulses as well as multiple CDM discharges gave the same test results, which shows that step stressing has no impact on the failure current. Pin 2, for instance, has a threshold limit around 1.7 A (see Figure 7). Compared to the CDM peak current of pin 2, measured at tester B, this corresponds to a CDM voltage of around 625 V. The same applies to pin 1. The threshold current of pin 3 is around 2.6 A, which matches the failure threshold level listed in Table 3 for tester A quite well. So overall, the failure thresholds determined with CC-TLP match those of the CDM testers. A possible reason why pin 3 shows no fail for tester B is that pin 3 fails at around 50% larger stress levels than pins 1 and that for tester B such a high stress level (1.125kV) was not tested. Tester C shows a <100% failure rate at 1.5kV, which may be caused by partial discharges as shown in [14] and may have prevented a failure of pin 3.

C. Correlation of failure signatures and failure locations

In the course of the physical failure analyses, the damaged DUTs have first been investigated for their electrical failure signatures by means of DC curve-traces of the damaged pins. All three device pins damaged by CDM or CC-TLP stress showed very similar failure signatures as shown in Figure 8 and 9.

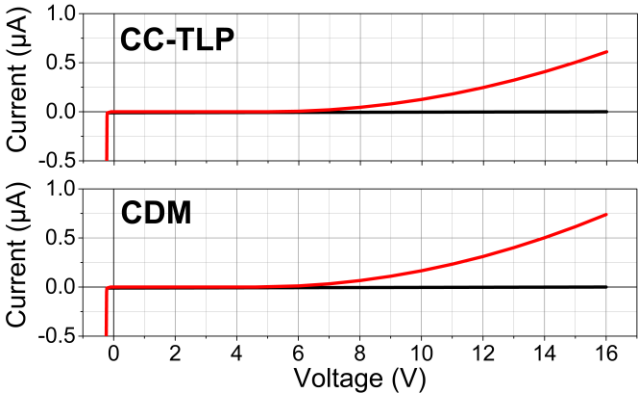

Figure 9: DC curve-traces of failing device pins after CC-TLP stress (top) and CDM stress (bottom).

Afterwards, the failure location was narrowed down by backside photon emission microscopy (EMMI). Two corresponding EMMI images of DUTs damaged by CDM and CC-TLP stress are shown in Figure 10. As can be seen, both images show emission spots at the same location. Note, unfortunately the contrast of backside images is limited.

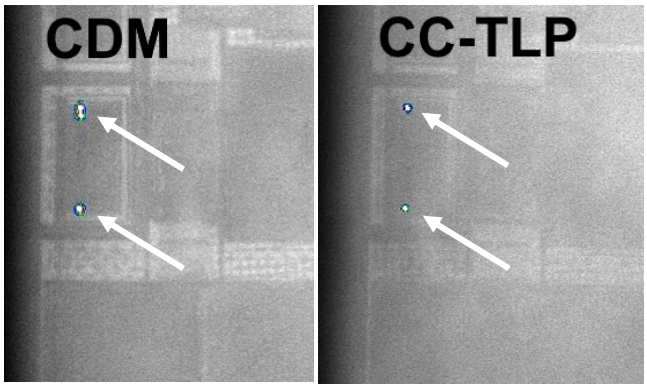

Figure 10: Backside photon emission microscopy (EMMI) images of DUTs with pin 2 failures. The spots indicate the failure locations after CDM stress (left) and CC-TLP stress (right).

Finally, the devices were deprocessed in order to investigate the detailed failure location and microscopic failure signature. After polysilicon etching scanning electron microscope (SEM) images were taken of a CDM stressed device (see Figure 11) and of a corresponding CC-TLP stressed device (see Figure 12). They show the damaged gate oxide of a transistor connected to the stressed pin. Obviously, the CC-TLP measurement has caused the same failure signatures in the same location as the CDM stress.

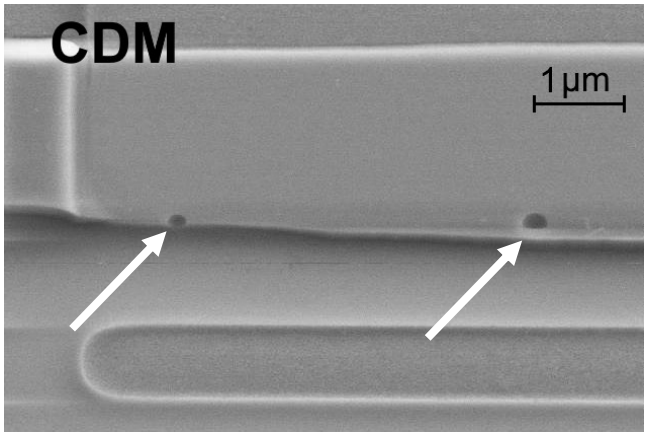

Figure 11: Scanning electron microscope (SEM) image of a gate oxide damaged by CDM stress.

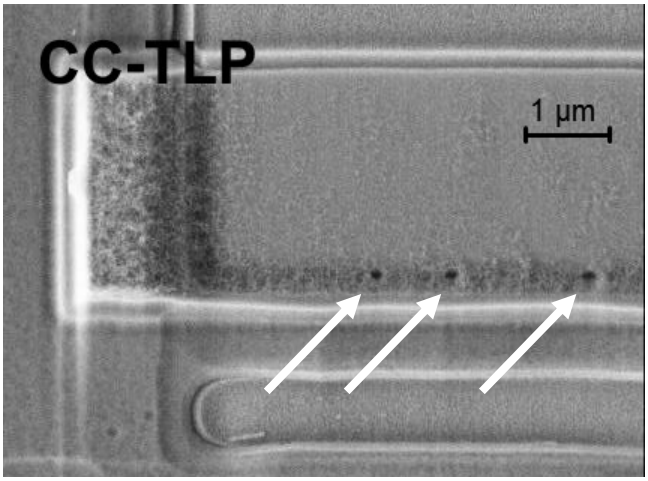

Figure 12: Scanning electron microscope (SEM) image of a gate oxide damaged by CC-TLP stress.

Consequently, all aforementioned figures in this section demonstrate the excellent correlation between CDM and CC-TLP stress.

Figure 13 shows a corresponding schematic of the 20 V transistor MN1, the gate oxide of which was damaged by negative CDM (positive CC-TLP) stress.

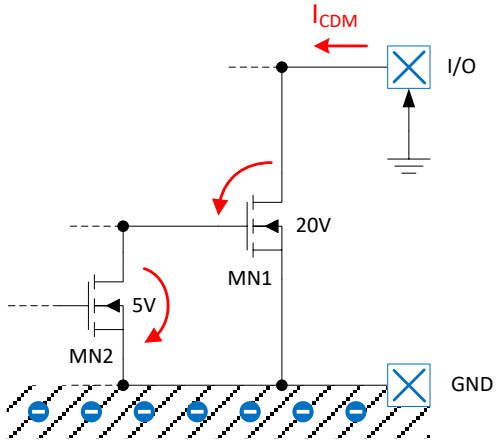

Figure 13: Conceptual schematic showing the transistor MN1 with damaged gate oxide and the transistor MN2 with a damaged drain-to-source junction as a result of negative CDM stress.

This damage represents the primary effect of the given stress. As a secondary effect, it was found in a deeper analysis of some damaged devices that the drain-to-source junction of the driving 5 V transistor MN2 suffered from a melt filament. A corresponding SEM image is shown in Figure 14. Based on this circuit topology and the given failure locations and signatures the failure mechanism can be derived as follows: In the course of the negative CDM (positive CC-TLP) stress event, a large voltage was induced at the I/O pin with respect to the substrate ground (GND). By design, MN2 is turned off during this

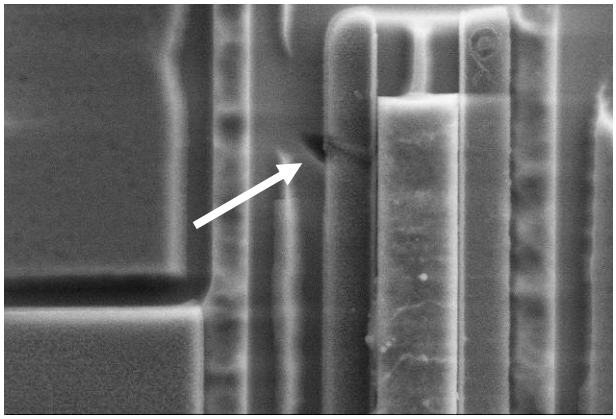

Figure 14: Scanning electron microscope (SEM) image of the drain-to-source melt filament of the 5 V transistor MN2.

event. When the induced overvoltage exceeded the sum of the transient gate-oxide breakdown voltage of MN1 and the drain-to-source breakdown voltage of MN2, first the gate oxide of MN1 was damaged. The resulting current flow across the damaged gate oxide increased the voltage drop across MN2 until second breakdown occurred leading to a melt filament between its drain and source. As a result, a leakage path was established between the given I/O pin and the substrate ground.

IV. Reproducibility issues of CDM failure thresholds

All CDM testers were calibrated according to JESD22-C101F [1]. The results of the CDM tests in Table 3 show a poor reproducibility of the threshold voltages between 500 V and 700 V with no hard limit (i.e. 100% failure rate) for the CDM robustness. In contrast, the failure threshold determined by CC-TLP is highly reproducible and lies within this range.

In this investigation, the most sensitive pin (pin 2) was stressed. The rise time of the CC-TLP setup was varied by rise time filters that were inserted into the stress path. The stress currents and corresponding slew rates are plotted in Figure 15 for the different rise time configurations. In the default setup without any filter, pin 2 was found to fail for currents above 1.7 A (Figure 15, black curve). The corresponding slew rate amounted to 41 A/ns (Figure 15, vertical black dotted line). Having inserted a 100 ps rise time filter, a higher pulse voltage was required in order to cause a failure. This is because the high-frequency part of the waveform and thus a contributing to its amplitude in time-domain was cut off by the filter. Nevertheless, the threshold current remained at 1.7 A, whereas the corresponding slew rate dropped to only 15 A/ns (Figure 15, blue curve). However, employing a 200 ps rise time filter, the failure threshold current increased to slightly less than 2.8 A, whereas the slew rate remained at 16 A/ns (see Figure 15, red curve).

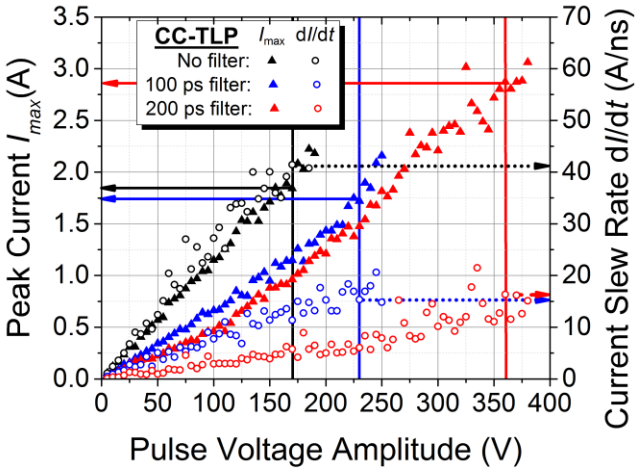

Figure 15: Peak currents (▲) and corresponding slew rates (O) for a CC-TLP step stress of pin 2 without (black), with 100 ps (blue) and with 200 ps (red) rise time filter in the stress path. The vertical lines mark the respective failure thresholds.

For confirmation, these tests were repeated several times but always gave the same results. This indicates that both a threshold current and a threshold slew rate have to be exceeded in order to cause a failure, which is absolutely plausible given the naturally limited triggering speed of any ESD protection structure. A corresponding diagram visualizing these three data pairs is shown in Figure 16.

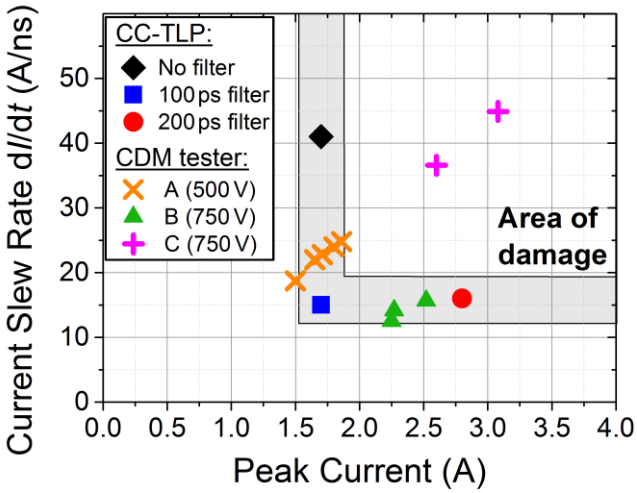

Figure 16: Threshold currents and threshold slew rates derived from CC-TLP step stress of pin 2 with different rise time filters (black, blue and red symbol) and corresponding data measured at CDM tester A (orange symbols), B (green symbols) and C (pink symbols).

The evaluation of the current slew rate of pin 2 stressed by tester B resulted in a threshold slew rate

around 10 A/ns (see Figure 16, green symbols). Note, the difference to the threshold slew rate determined by CC-TLP (15 A/ns) is assumed to be due to the different bandwidths of the different test systems (see Table 2). The CDM slew rate variation caused by the air discharge (see Figure 17) may explain the low failure rates above 625 V for tester B in Table 3.

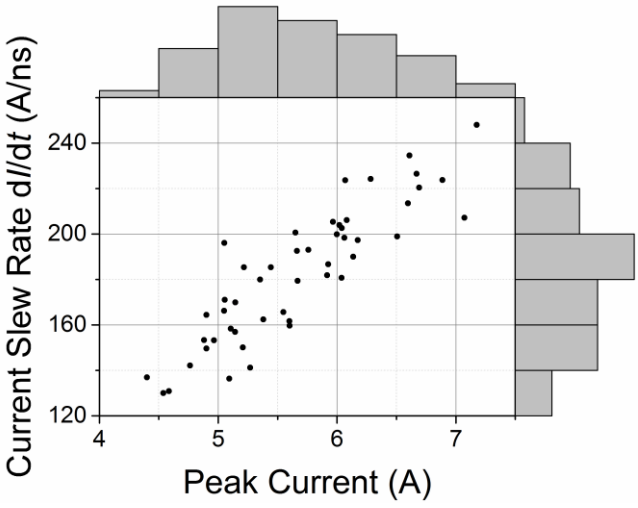

Figure 17: Peak current - slew rate distribution of 50 positive stress pulses obtained with tester B on pin 2 under test condition TC 1000 of JS-002-2014 [3], measured by a 33 GHz oscilloscope.

However, the threshold slew rate is clearly exceeded by testers A and C, even if a typical CDM slew rate spread of ± 30% as indicated in Figure 17 is assumed. Since the data of tester A is distributed around the peak current threshold in Figure 16, its peak current variation might be the limiting factor for its low failure rate at 500V. However, this variation cannot explain the low failure rates of tester A and tester C at higher stress levels. This leaves parasitic effects as a possible explanation for the poor reproducibility of tester A and C. As explained in [14] CDM tester discharges can be divided into a reproducible discharge regime and a non-reproducible discharge regime. The latter is reported to be facilitated by a high charging voltage, a spiky pogo pin, a curved device pin, a slow contact velocity, an inaccurate alignment and a high humidity. From these contributing factors, a curved device pin and a high humidity can be ruled out for the given CDM tests, since the given IC is assembled in a QFN-like package and the humidity is controlled by air conditioning. Unfortunately, none of the other factors can be ruled out as well. Hence, in particular the passing devices at 1.5 kV could be explained by partial discharges while operating tester A and C in the non-reproducible discharge regime.

Unfortunately, the root cause of the 500 V failure threshold obtained with tester A is still unknown. However, it should be noted that the 500 V and 625 V fails of tester A could not be repeated with the same tester in subsequent CDM tests of the same DUT, which opens the door for speculations on a temporarily miscalibrated or defective tester.

V. Summary and conclusions

Three different CDM test systems and a CC-TLP system were compared regarding their mode of operation, their discharge waveforms, the reproducibility of their measurement results and the resulting failure thresholds, failure locations and failure signatures of a small device-under-test. Special attention was paid to the calibration of the CC-TLP system, the characteristics of the metrology chain and the failure thresholds of devices-under-test.

We found that the failure thresholds and failure locations as well as the electrical and microscopical failure signatures obtained with CC-TLP measurements matched those obtained with the CDM testers very well. Hence, these results demonstrate an excellent correlation between CDM tests and CC-TLP measurements. At the same, it became obvious that the major weakness of the CDM test is its limited reproducibility and repeatability, which is not an issue at all for CC-TLP measurements thanks to its contact-based mode of operation.

In addition, it was found that differences of the measurement chain become especially important for the extremely narrow discharge pulses of small devices. By means of a special investigation of the current slew rate it was shown that both a threshold current and a threshold slew rate have to be exceeded in order to cause a failure.

This work points out clearly the advantages of CC-TLP over CDM testing, particularly its minimal parasitic influences which enable highly reproducible and repeatable stress pulses and test results as well as its ability to control and tune the rise time and pulse width of its pulses for special investigations. Considering previous work and publications in addition to the findings of the given paper, we believe that CC-TLP has reached a level of maturity that calls standardized CDM stress testing to be replaced by corresponding CC-TLP tests.

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