Wafer Level Test Methodology for HV Latch-up Spacing Rules Development in BCD Process Technologies

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Abstract – A wafer-level latch-up test methodology was developed to address latch-up spacing rules complexity in HV Bipolar CMOS DMOS (BCD) process. The proposed approach is validated by multi-point comparison of the component level experimental results with JEDEC-compliant standard industrial tester and against a number of process technology variations.

I. Introduction to HV Latch-up

Conventional Latch-Up (LU) in Low Voltage (LV) CMOS processes up to 5V [1] includes the CMOS *I/O* and *Core* latch-up scenarios. Both create conditions for a permanent turn-on of a parasitic SCR structure formed in IC layout by either current injection or overvoltage test regimes. In *Core* circuit latch-up cases the parasitic SCR structure can be formed by a High Side (HS) electrical potential connected PMOS device with the source as p+-emitter and a Low Side (LS) connected NMOS with the source as n+-emitter. Inverters are an example of this case.

A forward biased junction in the I/O circuit can become an injection source. In the case of I/O LU, the parasitic p-n-p-n SCR structure is already present in the I/O circuit. During the LU test the carriers are injected directly into the structure drift regions. The typical LV LU spacing rules for *I/O* are mainly focused on disabling the victim SCR with better isolation of emitters by bases (with well ties). Essentially, the spacing rules aim at reducing the gain of the npn and pnp BJTs forming the SCR. For *Core* LU, a typical approach is to space apart the core circuit from the injectors.

The spacing rules are different in principle in High Voltage (HV) BCD processes (starting from 12V up to 80V and above). Since both *I/O* components and the *Core* circuits are typically isolated in separate N-pockets the focus of the spacing rules is N-pocket to N-pocket isolation and corresponding collection rings placement. The physical semiconductor structure that represents the LU scenario in HV BCD processes is an NPN formed by the LS pocket (acting as n-emitter), p-isolation (acting as p-base) and the HS pocket (acting as n-collector). At the minimum layout spacing rules, such NPN structure cannot sustain high blocking voltage in the LU injection conditions due to achieving the critical thermo-electrical regimes for conductivity modulation. Therefore, some spacing rules must be followed as a function of the injection current, latch-up test temperature, pocket-to-pocket voltage as well as the injector and victim structure specifics.

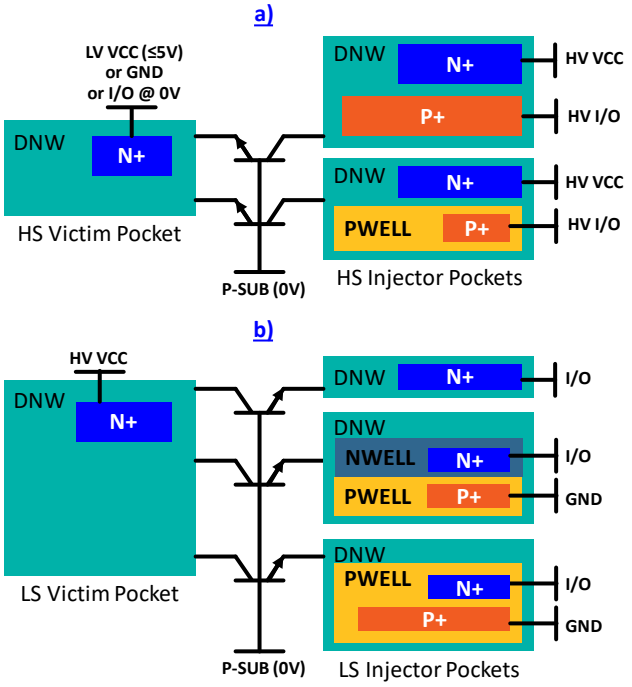

Figure 1: a) High Side Hole Injectors and Victims
b) Low Side Electron Injectors and Victims.

There are two major scenarios for LU in HV BCD processes: HS LU when the holes are injected by the junction forward biased above the HV supply (Figure 1a) and LS LU where electrons are injected by a

forward biased junction biased below the substrate (Figure 1b).

Typical circuit regimes leading to HS injection are for example, a positive ESD strike on an IO pin protected by a rail diode with a cathode connected to a supply. In this case, the ESD diode within a Deep N+ Well (DNW) pocket connected to the supply is forward biased, with the I/O node at a potential above the supply. Holes are injected into the substrate, and then drift away toward victim structures biased at a lower potential. Another potential condition would be the high side transistor of a push-pull output power stage. During switching, an inductive load may force current through the forward-biased body diode of the MOS transistor, elevating the output node above supply and injecting holes into the substrate.

Conversely, LS circuit conditions may appear when a negative ESD strike brings the I/O node below substrate potential and injects electrons into the substrate via a forward-biased ESD diode. Similarly, the low-side power transistor in a power converter's output stage can inject electrons into the substrate during inductive load switching. These electrons then may drift toward a victim structure biased at an elevated potential, which may trigger a latch-up condition or generate excessive detection current and power dissipation in the injector and/or the victim.

Design rules are usually created to address both potential LU conditions separately, identifying the HS and LS injector and victim structures based on the circuit configuration, and mandating minimum spacing requirements based on the node voltages. In addition to pocket-to pocket spacing the LU rules may specify N+ Channel Stop (NCS) rings, N-pocket moat rings placed around LS injectors and connected to a supply; and primary, directly grounded substrate rings around HS injectors and HS victims.

This reasoning drives spacing rules that are substantially more complex compared to the aforementioned LV CMOS LU rules. Substantial experimental data collection and analysis are required due to multiple HV voltage domains, collection ring structures and self-heating effects due to high detection current during injection. Establishing LU layout rules becomes an increasingly crucial task to achieve a LU-immune power analog integrated circuit design. Meantime, the traditional LU testing at package level per JEDEC standard [2] is not an efficient approach for HV LU rule acquisition testing because irreversible LU burnout events typically destroy the entire sample, and the substantial number of tests required would consume many packaged units, increasing the costs.

In this study, the proposed Wafer-Level Latch-up (WLL) test setup and methodology are not a substitute for the industrial IC tester, but an efficient approach to acquire solid data and derive the HV LU spacing rules for new power analog process technologies. The approach enables dealing with diverse structures and devices, multiple wafer lots and splits, and evolutions of the process of record during the development cycle.

Thus, *the purpose of this work* is to establish a test method to characterize LU at the wafer-level, yielding qualitative and quantitative results correlating with standard-compliant [2] package-level LU tests, rather than TLP based approaches [3, 4] which stress the devices within a much shorter time domain.

II. WLL Test Methodology

The JEDEC JESD78E standard [2] specifies a broad range of current injection pulse durations that are approved for testing IC LU. The range specified is anywhere from 10 microseconds up to 1 second. A typical injection pulse setup used for IC compliance testing on the MK2 instrument used to test the packaged samples was 3 milliseconds injection pulse and 10 milliseconds wait time. This setup was retained for the HV LU packaged sample tests, and matching waveforms were used on the WLL setup. The injector to victim transient voltage is also applied in accordance with the standard, being set-up a certain time before the injection current begins and maintained for a time after. In the proposed methodology source-meter units (SMUs) were chosen as pulse sources for the ease of programming precisely synchronized pulses and the ability to collect measurement data.

A Keithley 2636B dual SMU was used to generate simultaneous synchronized pulses of either voltage or current, up to 20V and 1A on both SMUs. For the characterization of HV BCD structures, voltages higher than 20V are obtained using an additional DC power supply (A computer controlled 60V/1A supply) in series with the injector-victim voltage source SMU. A standard probe station is used to connect this equipment to the test structure at the wafer-level. Voltages and currents are monitored by an oscilloscope; with the actual data collected by the SMUs.

A schematic representation of the test setup with a cross-sectional view of the typical HV LU test structure for HS LU is shown in Figure 2. In this setup, the I_{pulse} source is provided by SMU1, the V_{pulse} source is provided by SMU2, and the *VDC* offset is used if testing is conducted with $V_{pp} = V_{pulse} + VDC$

(pocket to pocket voltage) above the maximum of 20V supplied by SMU2. HS injection conditions (Figure 2) are created when a junction is forward biased inside the DNW at high potential. An optional P+ ring shorted to the cathode may be used to enhance hole collection by the cathode during HS injection, as depicted in Figures 2 and 3.

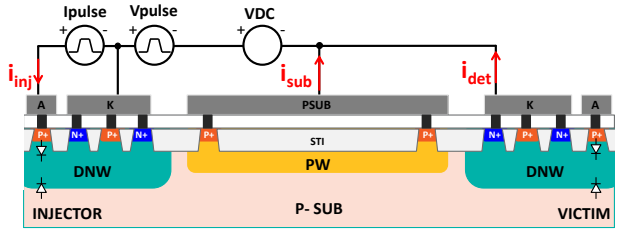

Figure 2: Cross-sectional view of the High Side latch-up test structure with WLL test setup components.

The scenario for LS injection (Figure 3) is realized when the DNW to substrate junction of an injector pocket is driven below the substrate potential, injecting electron current into the substrate and turning on parasitic devices formed by a nearby, HV biased DNW pocket (the victim). An n-moat ring biased to some power supply potential may be used to collect some of the electron current and reduce LU susceptibility.

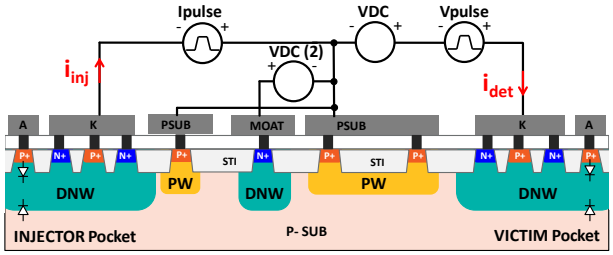

Figure 3: Cross-sectional view of the Low Side latch-up test structure with n-moat and WLL test setup components.

The SMUs are capable of sourcing voltages and currents in a pulsed mode, accurately timed and synchronized by the instrument and triggered by the control computer. Simultaneously, the SMUs can sample current multiple times during the pulse, effectively acting as a high accuracy, low sampling rate oscilloscope with current probes. This allows the setup to record the current waveforms on both the injector device and the victim device. The typical waveforms for the HS setup (Figure 4) are programmed to match the typical setup used in accordance with the standard [2]. The measurement window overlaps the injection pulse and represents the interval of time sampled for current by both SMUs.

Prior to initiating a LU injection pulse sequence, the same SMUs are programmed to perform a low current DC test of the structures, to obtain a pre-test status of the device. The breakdown voltage of the junctions, and leakage current levels at specified bias voltages can be collected and used as references.

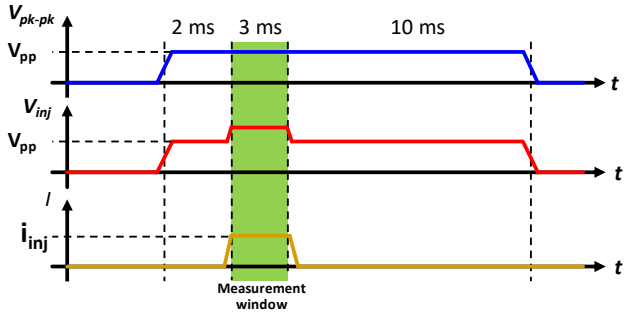

Figure 4: HS injection latch-up test waveform in the WLL setup for the pocket to pocket voltage, and injector voltage and current.

When the parasitic structures turn on because of a LU event occurring during the injection, the current drawn by the injector and victim structures sharply increases. The SMUs then attempts to regulate the current back to the target value. Since the device behavior under these conditions is strongly non-linear and has a negative resistance characteristic, this interferes with the regulation and causes an oscillation. This is detected by analyzing the waveforms using criteria such as: difference between injection target and measured, a threshold in detection current, or a jump of the detection current (indicating a parasitic device turn-on).

Once LU is detected for a given (V_{pp}, I_{inj}) pair, the program will perform a post-test DC test of the structure and assess its integrity by comparing to the saved pre-test reference data. If the device is damaged, the test sequence ends otherwise the LU test sequence proceeds further. Typically, the next test pulse would be programmed to decrease either V_{pp} or I_{inj} by a small amount, and apply the next injection pulse. If no LU is detected after that, the program may increase either V_{pp} or I_{inj}. allowing for an automatic characterization of the curve formed by the lowest (V_{pp}, I_{inj}) pairs that triggered LU on the structure. A strong advantage of the method is that the high sensitivity of the algorithm to LU via the waveform analysis, combined with the current limiting functions of the SMUs allows multiple LU tests to be performed on the same device automatically, collecting many data points quickly and automatically.

III. WLL Experimental Validation

To validate the proposed WLL methodology, a set of test structures were packaged and tested using an industrial MK2 tester from ThermoFisher Scientific.

Package level data were collected for two identical ESD diodes at various distances, one configured as an injector and the other as a victim. The victim diode only has its DNW pocket connected, with its anode left floating (as depicted in Figure 2). Data were collected in both HS and LS configurations at 25°C and 125°C. The test structures were assembled in side-brazed DIP packages and connected to the MK2 tester via a standard test card. The tests were conducted with injection current I_{inj} stepped up to 250mA in 25mA increments until LU was detected. V_{pp} voltages were set at a limited number of fixed levels, due to the limited number of samples available.

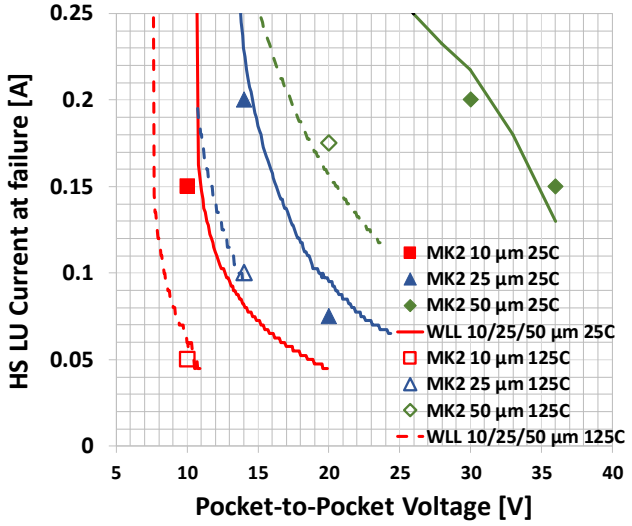

Figure 5: WLL and Industrial MK2 critical HS LU current at 25°C and 125°C as a function of applied V_{pp} for different spacing.

The JEDEC standard specifies that latch-up is detected when the supply current after the injection pulse has increased by 10mA or 40%, whichever is the greatest [2]. In the case of the structures tested in this work, there is no initial supply current (only leakage level currents) since there is no active circuitry operating. There was also no preliminary biasing required and the parking condition was to float the pins prior to the injection test. The supply compliance during the injection testing was set between 200mA and 1A (maximum system capability) depending on the test being performed. During the injection test, SCR triggering or current multiplication by parasitic bipolar transistors typically caused excessive power dissipation in the structure beyond a critical current level. The result was that in most cases, a latch-up condition was coincident with permanent device damage during MK2 testing.

Identical test structures were then tested at the wafer level using the proposed WLL methodology. The automatic stepping program was used, yielding a high-resolution characteristic curve with I_{inj} stepped at 2.5mA or 5mA increments, and V_{pp} stepped at 50mV or 100mV increments for HS and 0.5V for LS. Figure 5 shows the curves of the (V_{pp}, I_{inj}) points which induced HS LU on the same pair of ESD diodes at spacing of 10, 25 and 50µm, at 25°C and 125°C. The symbols denote the MK2 LU data points. The agreement is reasonably good, since the accuracy of the MK2 data is 25mA in current, and since some small voltage differences can be expected between both methods due to the probe contact resistance.

LS injection LU test results obtained on similar silicon structures at 125°C with both methods are shown on Figure 6. Note that in the HV BCD process of interest, the structures are immune to LS injection up to 250mA at 36V. Instead of a LU condition, the detection current induced in the victim pocket was used as a figure of merit. The agreement is good, with both methods showing the same trend of reduction of the detection current with increasing spacing. Similar results and agreement were also seen at 25°C.

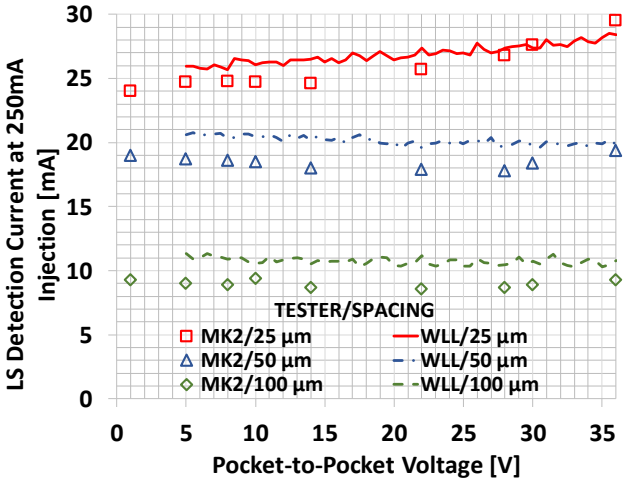

Figure 6: WLL and Industrial MK2 results at 125°C: LS LU detection current as a function of applied V_{pp} for different spacing.

IV. WLL for Process Development

Some of the main advantages of the proposed WLL method are overcoming the limitation in the number of testable structures, and preserving wafer integrity since there is no need for packaging. It becomes extremely useful for new technology process development due to lower cost, faster data acquisition, possible statistical data collection across the wafer and split lots comparisons. Additional benefits also

include design validation of ESD devices optimized for reduced LU injection, for example by adding a specially designed PW tap hole collection rings within the device. Successful design requires the evaluation of many test structures, which is effectively enabled by the proposed WLL method.

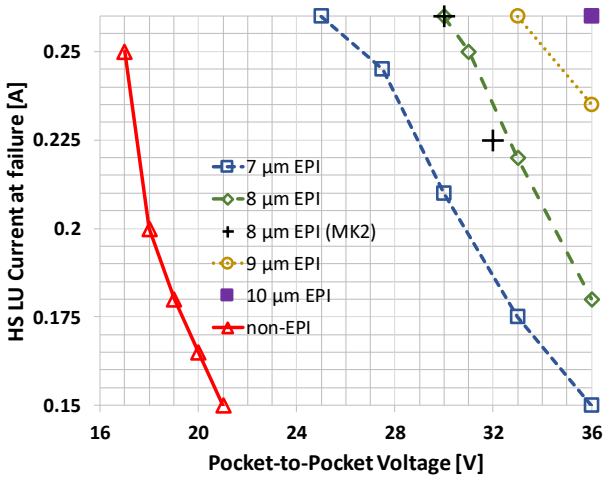

Figure 7: High Side latch-up test results of a 50 µm spaced diode test structure on various epi and non-epi wafers at 125°C.

To demonstrate this a study of various P+/P- epi wafers and non-epi (P-) wafers for HS LU immunity at 125°C was done using the WLL approach (Figure 7). It shows the immunity of a structure is much greater on the P+/P- epi wafers than on the non-epi material. Among the epi wafers, a dependency with epi thickness is observed. Further testing demonstrated that the failure mode of the thinner epi wafer structures was found to be excessive power dissipation in the vertical PNP transistor formed under the injecting structure, which collector efficiency is enhanced in thinner epi wafers. However, the wafer with 10 µm epi layer thickness showed complete immunity for HS LU up to 250 mA, demonstrating that a trade-off exists between enhancing the vertical PNP efficiency and inhibiting of the lateral NPN gain. Note that points on the chart at 260 mA denote that the structure survived the HS LU test at 250 mA. Limited packaged structure data collected on the industrial MK2 tester was available for the 8 µm epi wafer only, and is also shown on Figure 7. It matches closely the WLL results.

V. Conclusions

An experimental setup for a new Wafer-Level Latch-up test methodology was proposed and implemented for the first time. It "mimics" with good accuracy the JEDEC [2] industrial LU tests. Although this new approach is not intended to replace the quality assurance testing of the final packaged products with industrial equipment, it provides substantial packaging cost reduction and test time savings while enabling much greater analysis flexibility for the latch-up rules development data acquisition.

The method was fully validated by comparison of the HS and LS injection cases for HV LU spacing rules acquisition based on 4-terminal experimental test structures. An adequate matching between the packaged and wafer level is demonstrated for the regimes with low detection current (HS LU cases presented). For the regimes with high detection current (LS LU cases) small discrepancies exist, likely due to the difference in heat dissipation between a wafer and a packaged unit.

While adapting the industrial tester for wafer-level testing is theoretically possible, such a setup would be much more complex and expensive compared to the proposed approach. Besides, the HV LU rules development requires does not require the multiple supplies, pin biasing networks and monitoring systems provided by the industrial tester.

However, despite its pin count limitations, this method can be effectively applied to improve not only the granularity and accuracy of the latch-up design rules (by allowing LU data collection on many more structures spacing configurations), but also to simplify partition tests of analog product cases when a few pins can reproduce a particular latch-up failure event. Another application is scanning the latch-up response for wide variation of the pulse duration, including system level surge pulse-induced latch-up.

Acknowledgements

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