Circuit under Pad Active Bipolar ESD Clamp for RF Applications

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Abstract - With the rapidly increasing RF Complexity of RF BiCMOS designs for key Mobile and Internet of Things (IoT) applications, achieving both extreme RF performance and ESD reliability requirements has become a big challenge. In this paper, a novel active bipolar clamp is proposed featuring Circuit under Pad for RF applications.

I. Introduction

Leading edge RF products for key mobile and Internet of Things applications require high RF performance with high integration level and low cost in terms of die area. In this context, achieving both extreme RF performance and proper ESD reliability (typically 2kV HBM and 500V CDM) requirements has become a big challenge for the products.

Several active bipolar ESD power clamps solutions are described in literature for RF applications. The bandgap regulated supply clamp [1] is vulnerable to high temperature operational life (HTOL) and latchup tests due to a strong temperature dependency of the diode-string trigger mechanism. Transient triggered bipolar clamps for ESD protection have been also reported in prior works with reduced leakage [2, 3], with reduced temperature dependency [4] and with adjustable trigger voltage showing a snapback trigger mechanism [5]. Prior art publications [6, 7] reported diode-based and snapback ESD structures placed under the metal stack of an integrated circuit wire-bonding pad in CMOS processes.

In this paper, a novel compact 5V ESD active bipolar ESD power clamp is presented with superior ESD performance (It2~9.5A, Vt2~10.9V), low leakage at high temperature (1µA at 150°C) and low capacitance (0.6pF) in an NXP Semiconductors proprietary 0.25µm 180GHz F_T RF BiCMOS process. Furthermore, this ESD clamp is silicon validated for Circuit under Pad technology in a wafer level chip scale package (WLCSP). An overall die area reduction higher than 10% is observed for the RF medium power amplifier products by placing the digital devices and all ESD protections underneath the bumppads.

II. Active Bipolar Clamp

A. Design Aspects

Figure 1 represents the schematic of the active bipolar clamp for RF applications. It is composed of an RC-trigger stage for fast dV/dt transient detection, a holding stage setting the ON-time of the clamp during an ESD event and finally the power stage to dissipate the ESD energy. The cascoded Darlington NPN's are meant to accommodate for the 5V application. Furthermore, an explicit ESD diode (not shown in below schematic) is typically implemented between VCC and VSS in the application for the negative zap combination VCC/VSS.

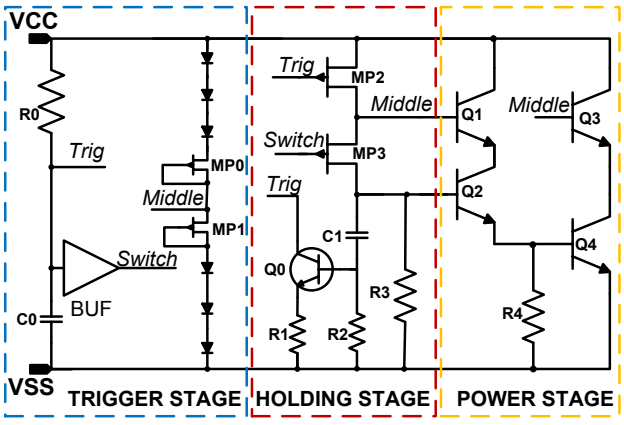

Figure 1: Schematic of the active bipolar CUP power supply ESD clamp.

1. The Trigger Stage

When an ESD stress with fast dV/dt transient event is detected, there is an increase of the current in the trigger resistor R0 and charges the trigger capacitor C0. Both the *Trig* and *Switch* nodes are pulled low making therefore both MP2 and MP3 PMOSTs to conduct. This leads to turn on the Darlington NPN's bipolar Q1 and Q2 and then the power NPN's Q3 and Q4 short-circuit Vcc to Vss with a low ohmic dynamic resistance. When the trigger capacitor is fully charged, the V_{GS} voltages of the PMOSTs decrease to 0V (there is no current in the trigger resistor) and the power stage of the ESD clamp is switched off. To reduce the leakage of the ESD clamp during normal operation, the RC trigger constant has been decreased and a dedicated holding stage has been implemented.

2. The Holding Stage

The holding stage sets the ON-time of the ESD clamp during an ESD event. The main role of the holding stage circuit extension is to maintain the sink current through the trigger resistor R0 beyond the ESD step dV/dt detection, thus to extend the ON-time of the power stage. This action is achieved by setting the high voltage NPN bipolar Q0 in saturation mode. Its base is fed with the discharge current of the capacitor C1. ESD and design optimization requirements set the RC trigger time constant to 3µs with C1= 2pF and R2= 150 kΩ.

3. The Darlington Power Stage

The power stage makes use of power NPN transistors Q3 and Q4. During an ESD event, the Darlington bipolar transistors Q1 and Q2 are driven by the cascoded PMOSTs in a common source configuration. To keep the ESD clamp off during normal operation, a DC biased *Middle* node is defined by a 6-diodes string and PMOSTs MP0 and MP1.

B. Circuit under Pad Layout Aspects

The layout 150.9µm x 113.5µm of the ESD clamp has been designed and optimized following all design rules from the BiCMOS process. From ESD perspective, a silicon calibrated commercial ESD layout check tool was used. This ESD layout check tool provides full chip and IP level ESD analysis for HBM and CDM events. The purpose of the tool is to verify that the ESD design guidelines are fulfilled and met. In addition, it can highlight weak areas of the design and report current density violations and high resistance paths.

The ESD simulations were performed on the layout of the 5V CUP power supply ESD clamp allowing quick iterations for possible and required design corrections before tape-out of the ESD testchip module. As an example, Figure 2 shows a homogeneous ESD current distribution not exceeding the current density limits at HBM simulations with peak current of Ipeak~9.5A.

Furthermore, deep trench isolation (DTI) ring and PTAP ring is used to improve the substrate noise isolation and the latchup immunity of the design.

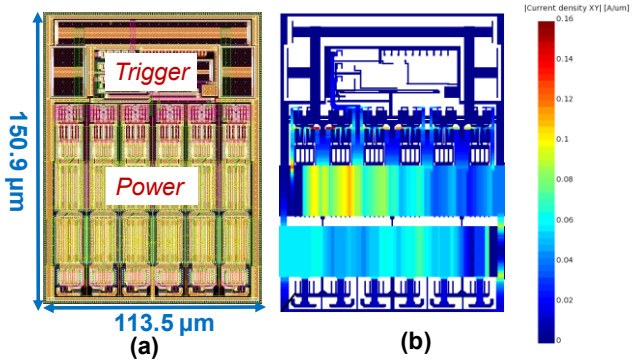

Figure 2: Layout view (a) and ESD current distribution of the CUP power supply ESD clamp (b).

III. Silicon Validation Results

A dedicated ESD testchip was designed and the active bipolar clamps were placed under bumppads. This was required to validate the circuit under pad (CUP) concept for the ESD clamp in the BiCMOS process including WLCSP product level reliability tests (notably the Al-TMCL).

A. RF Module Board Design

The ESD teschip module was mounted on a dedicated RF board for ESD measurements purpose. The goal was to check the impact of the bump and board mechanical stress on the ESD behavior of the ESD clamp, as indicated in Figure 3.

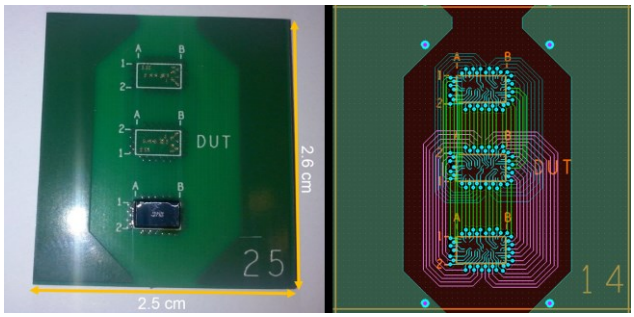

Figure 3: ESD testchip module mounted on an RF board (photography and layout view).

B. TLP Characterization Results

Similar ESD robustness is found for bare wafer, bumped wafer and mounted board measurements especially for its ESD robustness with It2~9.5A with a dynamic resistance Ron~1.1Ω for the 100ns-TLP measurements (Figure 4). The results of the ESD clamp mounted board shows a slightly higher dynamic resistance due to the routing of the RF board. At about 7.5A TLP current, a bipolar action at the power stage of the ESD clamp is triggered. This current is reached at the latchback breakdown voltage of the power NPN transistor Q4 BV_{CER}~10V. Note that the BV_{CER} voltage is strongly base-emitter resistance dependent. In the case of the CUP power supply ESD clamp, the BV_{CER} voltage is influenced by the R4 resistor. This triggering mechanism is however not harmful to the CUP power supply ESD clamp.

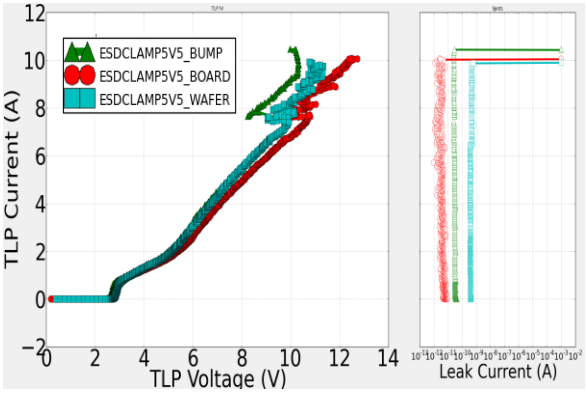

Figure 4: TLP results of the CUP ESD clamp on bare wafer, bumped wafer and mounted RF board.

C. VF-TLP Characterization Results

The VF-TLP measurement of the ESD clamp was performed with 100ps rise time and 2.5ns pulse width to mimic the CDM time domain. Figure 5 indicates a turn on voltage Von~2.9V, a dynamic resistance Ron~0.7Ω and the failure parameters were not evaluated (It2>28A) due to tester limitation.

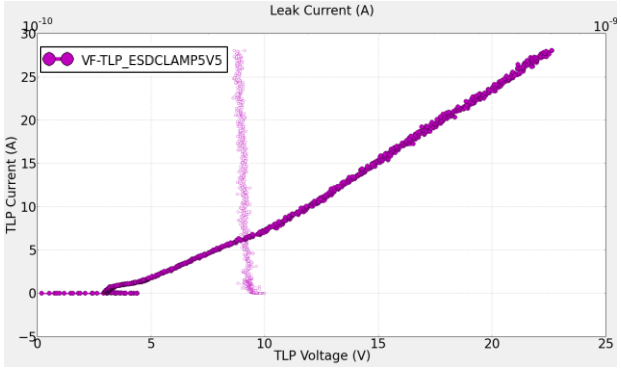

Figure 5: VF-TLP measurements of the CUP power supply ESD clamp.

A little snapback mechanism is observed during the trigger of with Vt1~4.5V due to a very fast transient.

The supply ESD clamp exhibits a very moderate voltage overshoot as shown in Figure 6, with a differential voltage overshoot (difference between the peak voltage and the quasi-static voltage) of about 3.0V at 5.0A.

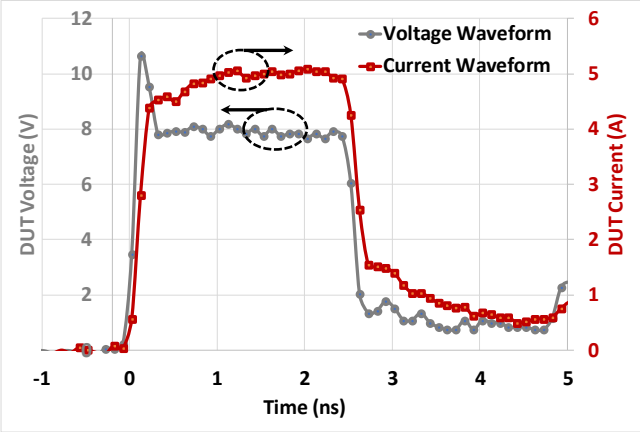

Figure 6: VF-TLP current and voltage waveforms of the CUP power supply ESD clamp.

D. Electrical Characterization vs. Temperature

The Figure 7 shows the leakage current and the capacitance of the ESD clamp at different temperatures as a function of the supply voltage. The leakage current increases with the temperature but remains however below 1µA for 5V at 150°C. The capacitance has a good linearity and is low, about 0.6pF, especially around 5V operational voltage. The good linearity and the low capacitance of the ESD clamp are key features for RF medium power amplifier designs, especially for special RF output pins [8].

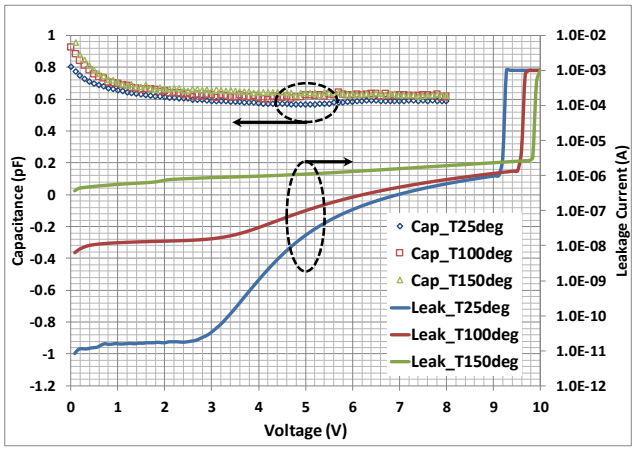

Figure 7: Electrical characterization of the CUP power supply ESD clamp at different temperatures.

E. EOS Like Stress

The powered device TLP measurement demonstrates that the RC-trigger mechanism is disabled, with a higher turn on voltage Von~6.5V. This represents the voltage trigger mechanism of the ESD clamp power stage. Its ESD robustness remains however It2~9.0A (Figure 8).

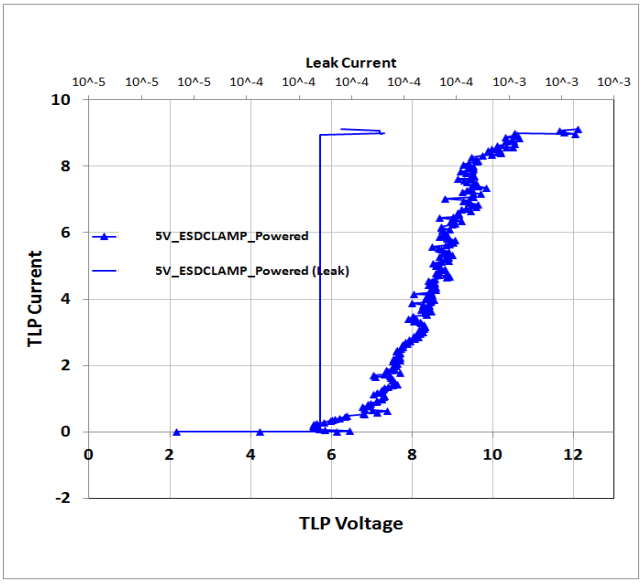

Figure 8: Powered CUP power supply ESD clamp TLP characterization.

Furthermore, long-pulse TLP stress (Tr=10ns and a pulse width=1.2µs) was applied to the ESD clamp. The characterization results show that the failure current It2 reduces to ~2.8A and the voltage at the failure Vt2~5.8V with a turn on voltage Von~4.0V. The long-pulse TLP I-V chart of the CUP power supply ESD clamp is plotted in Figure 9.

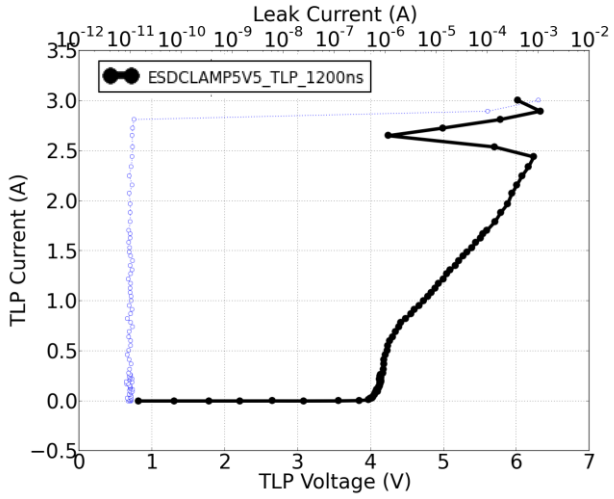

Figure 9: Long pulse characterization of the CUP power supply ESD clamp (I-V chart of 1200ns-TLP).

An example waveform, shown in Figure 10, clearly demonstrates the clamp remains ON for more than the 1.0µs of the IC level ESD time domain.

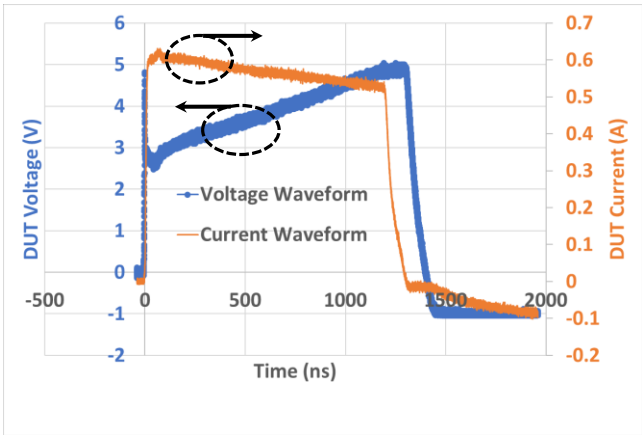

Figure 10: Long pulse characterization of the CUP power supply ESD clamp (DUT voltage and current waveforms of 1200ns-TLP).

Below Table 1 reports the failure current, the voltage at the failure and the power to fail parameters of the CUP power supply ESD clamp at various TLP pulse widths stress. For all measurements below, the rise time of the TLP system is Tr~10ns. Note that TLP pulse widths stress shorter than 25ns could not bring the CUP power supply ESD clamp to fail and the maximum pulse width allowable by the TLP setup used for the electrical characterization is 1600ns.

Table 1: Failure parameters of the CUP power supply ESD clamp at various TLP pulse widths

TLP Pulse (ns)	It2 (A)	Vt2 (V)	P_{FAIL} (W)
25	17.5	16.8	294.0
50	11.9	14.3	170.1
100	9.5	10.9	103.6
300	6.9	7.6	52.4
600	5.7	7.7	43.8
1200	2.8	5.8	16.2
1600	2.1	5.8	12.1

Interestingly, the power-to-fail versus pulse duration of the CUP power supply ESD clamp of Figure 11 corresponds to the 1D and 2D heat diffusions of the

Wunsch-Bell and Dwyer experimental range models [9, 10].

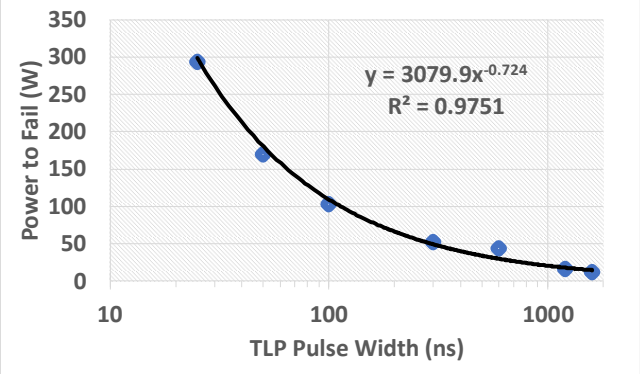

Figure 11: Power-to-fail versus pulse duration of the CUP power supply ESD clamp.

The typical failure mechanism of the ESD clamp under EOS-like circumstances is the collector-emitter breakdown of the power NPN transistor due to thermal effect and leading to a high leakage as revealed by Obirch spot in Figure 12.

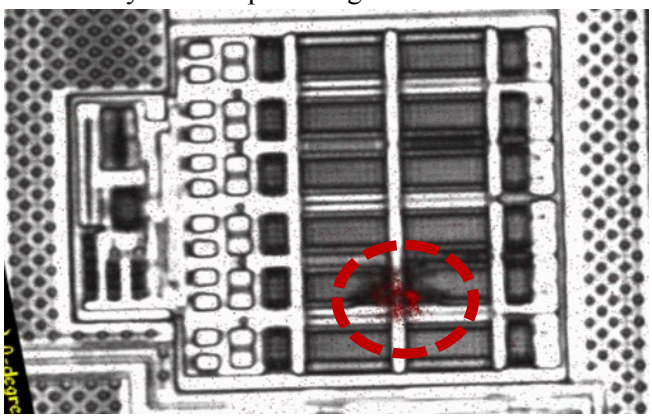

Figure 12: Failure analysis picture of the CUP power supply ESD clamp.

IV. Application to an RF Medium Power Amplifier

The RF medium power amplifier is a Single Pole Double Throw (SPDT) switch that only has a single input and can connect to and switch between two outputs. This means that it has one input terminal and two output terminals. It also has an embedded low noise amplifier (LNA) and power amplifier (PA) module for the IEEE802.11ac wireless local area network (WLAN) applications. When interfaced with highly integrated transceiver and controller IC on a WLAN card, the module will help to enhance RF sensitivity and transmit power of the overall solution. The WLAN cards are intended to serve the electronic consumer and mobile markets by providing wireless functionality.

A function diagram for the module may appear as depicted in Figure 13. By implementing the CUP power supply ESD clamp along with the ESD protection network and digital devices under the bump pads, a significant area reduction higher than 10% of the chip was achieved.

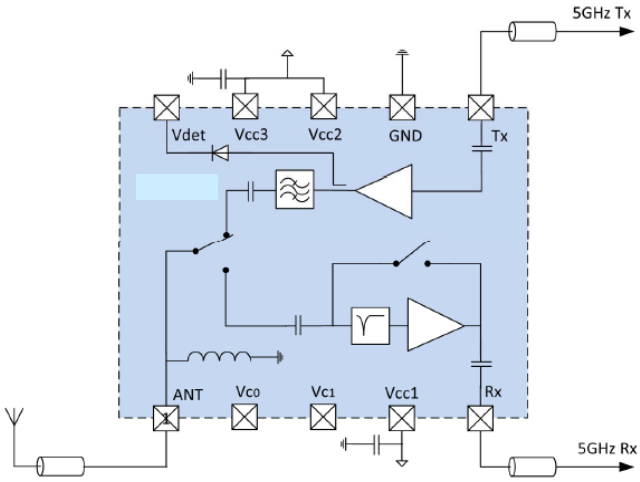

Figure 13: Principle of operation for the RF medium power amplifier.

A 3D view of the padring layout of the RF medium power amplifier is presented in Figure 14 with top metals stack, it shows that the CUP power supply ESD clamp can be placed under the bump pads and therefore reduces the chip area occupied by the ESD protection network. The module was housed in a small RF IC package with height less than 0.33mm (HX2SON10).

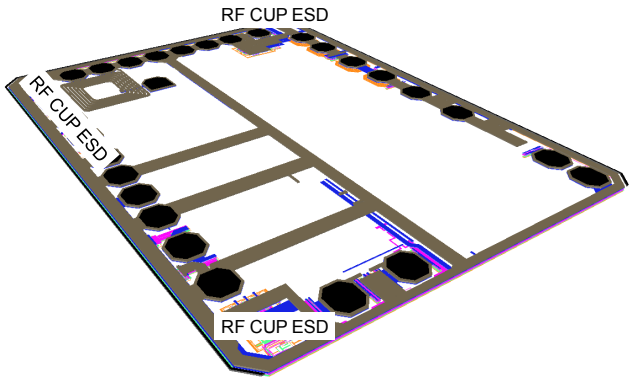

Figure 14: 3D view of the RF medium power amplifier IC.

A very high RF performance of the amplification gain is achieved at 5.0 GHz, 5.4 GHz and 5.8GHz for the AM/AM and AM/PM high power receiver RX mode (Figure 15) and transmission TX mode (Figure 16). It is very remarkable to notice that the CUP power supply ESD clamp has a very limited impact on the RF performance of the RF medium power amplifier. In accordance with the design target, the highest RX and TX gains are indeed achieved in the 5.0GHz,

5.4GHz and 5.8GHz operational RF frequencies range of the application.

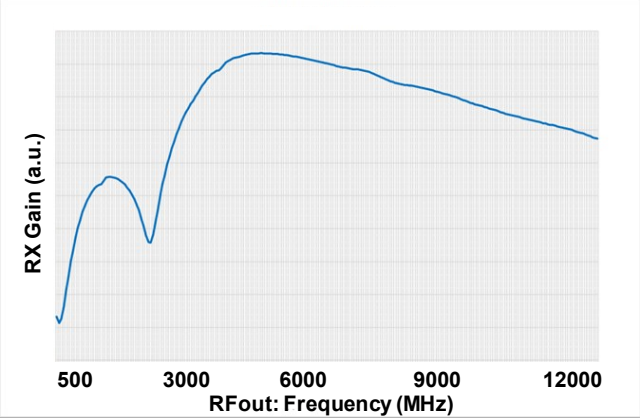

Figure 15: RF performance of the RF medium power amplifier (RX gain mode), a.u.= arbitrary unit.

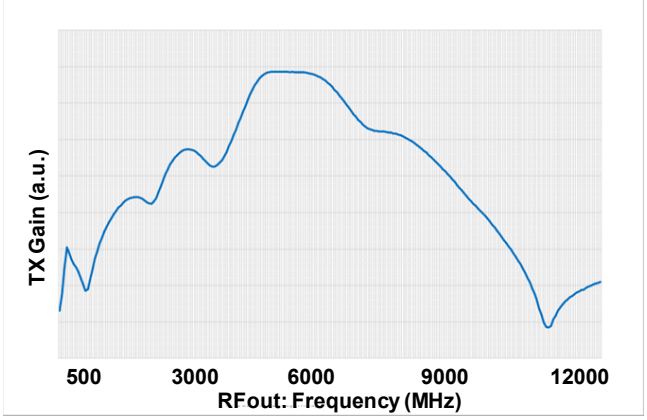

Figure 16: RF performance of the RF medium power amplifier (TX gain mode), a.u.= arbitrary unit.

A rail-based ESD protection strategy was implemented using the active bipolar CUP clamp for all pins and an RF ESD co-design for sensitive RF pins like Antenna (Ant), Receiver (Rx) and Transmission (Tx). The product successfully passed 2.5kV HBM based on the ANSI/ESDA/JEDEC JS-001 specification [11] and 650V CDM using the ANSI/ESDA/JEDEC JS-002 specification [12]. Also, a latchup testing of the product showed an electrical robustness of +/-100mA current injection at 85°C and 150°C according to the JESD78 Standard [13]. Both ESD and latchup results were above and in accordance with the requirements respectively.

V. Discussions

The power-rail ESD clamp circuits for RF applications in bulk CMOS technologies using Cladded diode string, Boosted diode string, or Cantilever diode string still exhibit high leakage current (~mA) at high temperature 125°C [14]. In comparison, the CUP active bipolar ESD clamp described in this paper has a low leakage (1µA at 150°C).

Interestingly, the transient stress measurements performed on the ESD clamp in HBM, CDM and EOS like time domains showed a power-to-fail results fully in line with the Wunsch-Bell and Dwyer theory. This further explains the thermal collector-emitter breakdown of the power NPN transistor as typical failure mechanism of the clamp.

VI. Conclusions

The RF circuit under pad active bipolar ESD clamp presented in this paper is a novel power-rail ESD clamp circuit. It exhibits a high ESD performance (It2~9.5A and Vt2~10.9V), a low leakage for 5V operational voltage (1µA at 150°C) and superior RF performance with low capacitance (0.6pF).

The good linearity and the low capacitance of the ESD clamp are required for RF products like the medium power amplifier with high RF swing signals at the RF output pins and high linearity requirements.

The application of the 5V CUP power supply ESD clamp to the RF medium power amplifier IC design has shown a very limited impact on the RF performance of the product. A superior RF performance was achieved especially in both RX gain mode and TX gain mode at operational RF output frequencies of 5.0GHz, 5.4GHz and 5.8GHz. Furthermore, the product passed the ESD qualifications (2.5kV HBM and 650V CDM) and other reliability tests including high temperature operational life (HTOL) and latchup testing of +/-100mA current injection at 85°C and 150°C successfully.

Finally, the implementation of the 5V CUP power supply ESD clamp along with the ESD protection network and digital devices under the bump pads allowed to achieve a significant area reduction (more than 10%) of the medium power amplifier chip compared to preceding series of similar IC's.

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