How to build a Generic Model of complete ICs for System ESD and Electrical Stress Simulation?

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Abstract - For precise system ESD simulation the transient chip behavior needs to be modeled accurately. As there are several typical characteristics possible (e.g. diode breakdown, snapback-element or forward diode) a straight forward methodology to build a generic model for transient behavior with destruction limits in SPICE is presented. This enables full-system transient ESD and electrical stress simulation for system robustness evaluation.

I. Introduction

For development and characterization of ESD protection elements transmission line pulsing (TLP [1]) is more or less a standard tool. Failure levels of TLP with a length of 100 ns are a good indicator for the component ESD test "human body model" (HBM) [2] failure level in most cases. Simulation models of ESD protection devices are usually generated out of these quasi-static I-V-characteristics obtained by 100ns TLP measurements [3] [4]. But ESD pulses on system level [5] and more in general, transient electrical stress pulses are not correlating with 100ns TLP pulses any longer. This is especially valid when different discharge networks of ISO10605 are used. The first peak of the system-level ESD (hereafter so-called GUN) pulse is in the range of a few ns and goes up to high current levels (3.75A/kV) while the second peak is in the range of 2A/kV to .275A/kV at 30 ns respectively 400 ns depending on the discharge network. An overview of the current waveforms from different ESD test methods and 100 ns TLP is given in Figure 1. Additionally the external components on the PCB can shape the pulse and some arbitrary pulse comes to the integrated circuit (IC). The methodology of SEED [6] addresses this topic. The SEED methodology proposes to measure the behavior of the external protection element and determine out of it the residual pulse which is coming to the IC. Instead of quantifying the pulse coming to the IC and measure the robustness of the IC against this pulse, it would be more convenient to model the IC behavior at arbitrary pulses and do a system simulation to see what is happening in the real system.

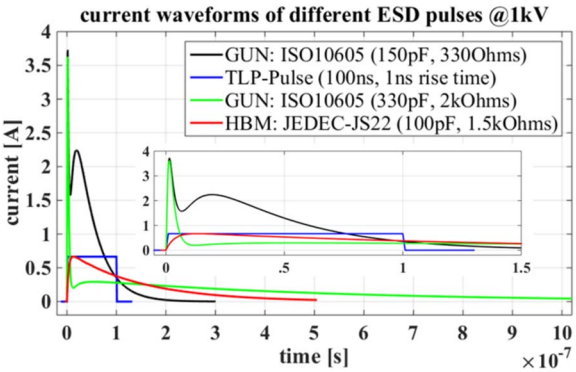

Figure 1: Overview of current waveforms for different ESD test methods and 100ns TLP pulse

To get accurate system simulations the quasi-static characteristic of the IC, obtained by 100ns TLP, is not enough. The complete transient behavior of the IC needs to be modeled in order to get reasonable results [7] [8].

In order to model the more realistic transient behavior instead of only taking the quasi-static 100

ns-behavior the measurement effort is inevitable higher, but the results show advantages over the quasi-static approach. Not only the systems robustness against ESD tests, no matter which discharge network is chosen, but also the robustness against disturbance pulses in a different time domain can be obtained by simulation. For example the robustness against ISO7637-2 pulse 2a [9] [10], with pulse length up to a few tens of microseconds, can be simulated in good accuracy. This work will present a generic transient behavior model (TBM) in SPCIE which is adjustable with a set of parameters introduced in Section II. The generic model can be used to model behaviors of different ESD device concepts e.g. high voltage breakdown diode, snapback based ESD protection or forward diode by only changing the setting of model parameters (Section III). In Section IV modeling of a complete IC product for system level simulation is described. In Section V the simulated robustness for GUN tests and ISO7637-2 pulse 2a are compared to measured robustness values followed by a short summary.

II. Generic transient behavioral model in SPICE

Like a simple switch, an ESD protection element is high resistive during the normal operation. Above a certain voltage level V_{TR} the switch S_1 is closed and provides a low resistive path to ground and conducts ESD current. The methodology to model the behavior of ESD protection elements with switches in SPICE [11] [12] was found to be well applicable for snapback elements.

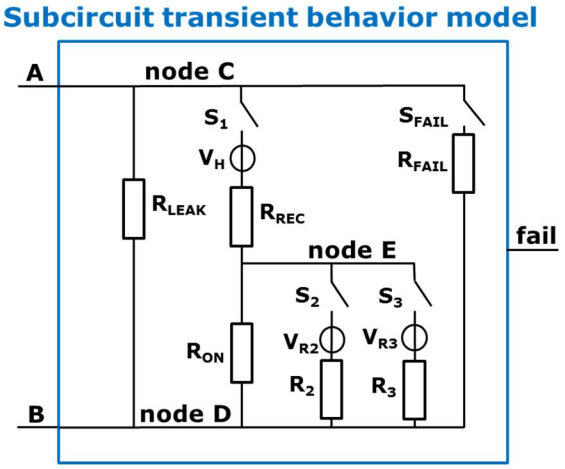

Figure 2: Schematic implementation of a subcircuit to model the transient behavior of an IC

If the model is extended with a few more elements the behavior of complex ESD networks can be modeled with a good accuracy. With an additional switch S_{FAIL} and a low-ohmic series-resistor R_{FAIL}, e.g. 0.1 Ω, a failure indication of the model is built-in.

Figure 2 shows the general schematic of the presented subcircuit to model the transient behavior between *Pin A* and *Pin B* for one polarity. Beginning at low voltages there is only a very low current flowing through the device which is modeled with the resistor R_{LEAK}. At the turn-on voltage the switch S_1 is closed and activates the current path through the voltage source V_H and the resistor R_{ON}. When V_{TR} and V_H are set to the same value the model gives the behavior of a breakdown diode. With a V_H smaller than V_{TR} a snapback behavior is modeled. As the core of the modelling methodology, the resistance R_{ON} varies with the pulse energy that is dissipated in the element. Since R_{on} depends on temperature, it also depends indirectly on pulse energy. The detailed coherences and dependencies of the resistance with temperature and pulse energy are not investigated and established here. Physically the dynamic resistance is directly coupled with the temperature of the device itself. With the temperature-raise of the silicon the internal resistance of the device in silicon increases. As the temperature is in first order linked to the energy due to Joule-heating within the device, the dynamic resistance is linked to the energy absorbed by the element. Correctly, the temperature of the device depends on the power (Joule-heating), the geometry of the device and the thermal properties of the material (thermal capacity and thermal resistance). As these parameters contain a lot of information about the manufacturing technology and the device design the resistance dependency is reduced to pulse energy in order to protect the intellectual property (IP) of the IC vendor. With experimental data the equation (1) with the fitting-parameters R_A, R_B and R_C was found to be well suited for modeling the R_{ON} dependent on the pulse energy E_P.

To model the conductivity modulation during the forward recovery effect of diodes [13] the resistor R_{REC} is included. As described in [13] the resistance during conductivity modulation R_S (equation (2)) has a constant contribution R_{s0}. R_{sM} is the modulated portion of the resistance, while

Q_M is the modulated charge coupled with the diffusion current of the diode I_D as $Q_M = \tau * I_D$ (τ is defined as the transit time of the diode). The parameter Q_0 is the threshold charge for the onset of conductivity modulation. In the model a similar equation is chosen to describe these effects with R_{REC}, see equation (3). As the constant resistance (*better: not-conductivity modulated resistance*) is modeled with R_{ON}, the part of R_{s0} is set to 1 mΩ not to disturb the simulation and improve convergence of the simulation. The parameters R_{sM} and Q_0 are the fitting parameters to adapt the model to the measured data. The pulse duration *tp* and current through the device *I* are obtained from the simulation.

$$R_{ON} = R_A * E_P^{(R_B)} + R_C \quad (1)$$

$$R_S = R_{s0} + R_{SM}/(1 + Q_M/Q_0) \quad (2)$$

$$R_{REC} = 1m\Omega + R_{SM}/(1 + (I * tp)/Q_0) \quad (3)$$

$$P_{FAIL} = P_A * tp^{-1} + P_B * tp^{-0.5} + P_C \quad (4)$$

$$E_{FAIL} = E_A * tp + E_B * tp^{0.5} + E_C \quad (5)$$

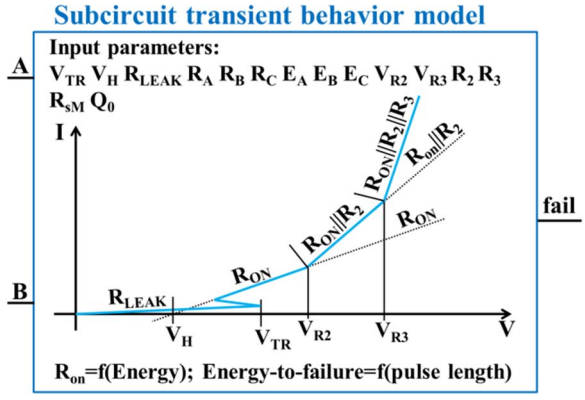

Figure 3: Schematic behavior of the generic modeling methodology for transient disturbances

The dependence of power-to-failure P_{FAIL} on the pulse length *tp* is well investigated [14] [15]. Based on the results of Wunsch & Bell [14] and Dwyer [15] equation (4) is chosen to describe the thermal destruction limit P_{FAIL} depending on the pulse length *tp*. The parameters P_A, P_B and P_C are used as fitting parameters to fit measured values. As found out in [16] energy-to-failure E_{FAIL} as failure criterion is better suited for energy based fails (thermal fails). As energy is just the integration of power over time equation (5) is derived from equation (4). Here the parameters E_A, E_B and E_C are also used as fitting parameters. In the model both failure borders E_{FAIL} and P_{FAIL} can be integrated. As some pin-combinations showed one or more kinks in the measured I-V-curves two paths parallel to the on-resistance R_{ON} are integrated in the model. These parallel paths are activated at a certain voltage V_{R2} or V_{R3} with the resistances R_2 or R_3 respectively.

The presented subcircuit is able to simulate most of the available ESD protection devices, e.g. forward diode, breakdown diode (reverse mode), snapback elements and power clamp (with static triggering). A schematic I-V-curve is depicted in Figure 3.

In a basic version the triggering of the switches can be done only by node voltages. To improve the model quality the triggering of the switches can be done by a separate, dedicated circuit with some small logical functions. With a behavioral source that compares the voltage between *node C* and *node D* (V_{CD}) with the trigger-voltage V_{TR}, the turn-on of the element is detected. This information can be saved in a voltage node, e.g. $V_{trigger}$ = 1 V. If the voltage V_{CD} goes below the holding voltage V_H, the voltage $V_{trigger}$ is set to 0 V again. $V_{trigger}$ can directly control S_1. With a behavioral source that integrates 1 over time while $V_{trigger}$ = 1 V the pulse duration *tp* can be quantified. As E_{FAIL} is modeled depending on the pulse length *tp*, this voltage *tp* together with the parameters E_A, E_B and E_C is used in another behavioral source to produce E_{FAIL} at the current pulse time *tp*. With an additional source which is showing the energy which was already absorbed by the device as $E_P = \int V_{DC} * I_{S1}\, dt$, it is possible to check if the energy is below the destruction E_{FAIL} at each time point in simulation. If this border is exceeded the node V_{FAIL} can be set to 1 V which indicates a physical destruction of the device.

III. Parameter derivation for different elements

To demonstrate the setting of the parameters an application specific integrated circuit (ASIC) is modeled. The ASIC contains a magnetic sensor for automotive applications. The sensor measures the magnetic field and switches the output signal if a certain threshold is reached. A related, but more complex ASIC was investigated in [17]. Details on the ASIC-core are not necessary in this study and therefore not described here. To protect the IP of

the IC vendor the IC-model shall contain as little as possible information about the manufacturing technology and the chip design, ideally no information at all. Therefore a "black-box" behavior modeling methodology is chosen. The modeling is only based on the characterization measurements with the complete product.

The ASIC has three pins and was measured in each Pin-combination and polarity with different pulse lengths (5, 10, 20, 50, 100, 250, 500, 1000 and 1540 ns). The measurements were done with a TLP-system up to the destruction limit for each combination. The first pin-combination was characterized with $V_{TR} \approx 50.3V$ showing no snapback i.e. $V_H = V_{TR}$. The measured I-V-curves with TLP (pulse lengths: 5 ns, 100 ns and 1540 ns) are shown in Figure 4. The matching of the model and the real TLP I-V-curves with three pulse lengths and simulated I-V-curves are also shown in this figure.

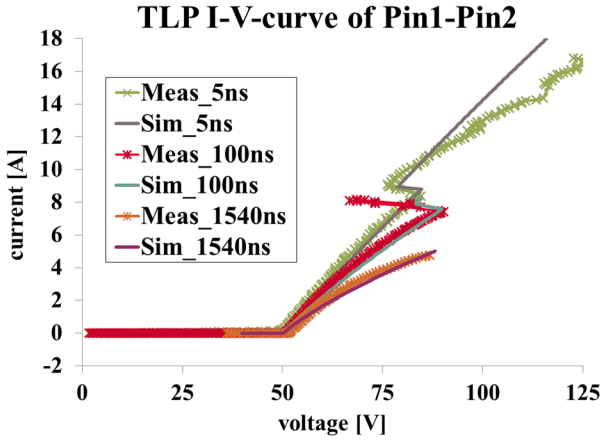

Figure 4: TLP-I-V-curves with three different pulse lengths of the HV-breakdown diode at Pin1-Pin2

The effect of self-heating and the related change in R_{ON} is modeled with an energy dependent resistance. To find out the relation between resistance and energy long TLP pulses (1 µs or 1.5 µs) are evaluated with different average windows, see Figure 5. A short average window is chosen (e.g. 15 ns length) and the current I and voltage V are evaluated at different times of one pulse. With V and I the resistance $R = U/I$ can be calculated. With the power $P = U * I$ and the elapsed time the energy which was already absorbed by the Element can be calculated $E = \int P\, dt = U * I * tp$.

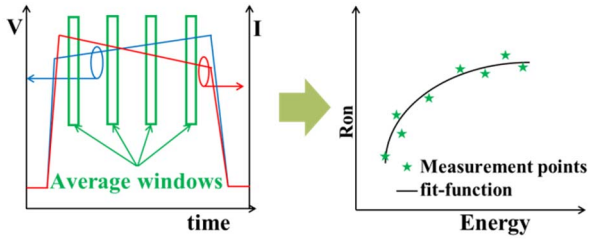

Figure 5: Basic principle for getting the dependence of R_{on} on E with averaging V and I at different time points

This procedure is done with different TLP pulse voltages to get a broad range of pulse energies. The parameters of equation (1) are chosen to fit the measured values best.

Furthermore Figure 6 shows the matching of measurement and simulation for one pin–combination showing a snapback behavior. The trigger voltage of this combination is $V_{TR} \approx 41V$ and the holding voltage is modeled with $V_H \approx 30.3V$. Additionally the 5 ns TLP I-V-curve shows a kink at $V_{R2} \approx 50.5V$ which is also included in the model.

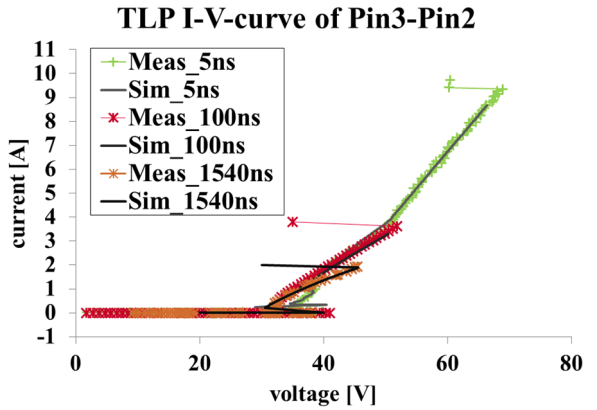

Figure 6: TLP-I-V-curves with three different pulse lengths of the snapback element at Pin3-Pin2

The combination Pin1-Pin2 in negative polarity shows a breakdown behavior at $V_{TR} \approx 22V$ and a first kink at $V_{R2} \approx 78V$ and a second kink at roughly $V_{R3} \approx 100V$, see Figure 7.

The kinks indicate that at this voltage an additional element in parallel to the original one gets into breakdown and conducts a part of the current. This is why it looks like the on-resistance is reduced at this point. The self-heating respectively the increasing resistance is modeled only for the first resistor called R_{on} in the model.

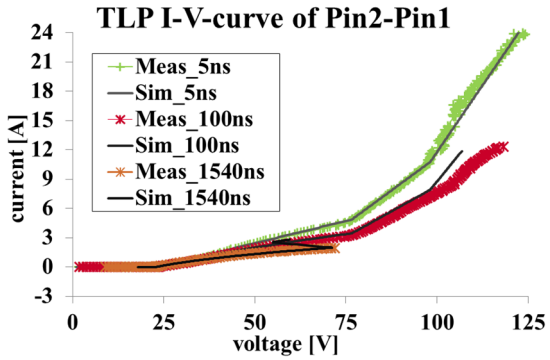

Figure 7: TLP-I-V-curves with three different pulse lengths of several parallel elements between Pin2-Pin1

The characteristic of a forward diode was measured at Pin2-Pin3. This behavior is modeled with a $V_{TR} = V_H \approx 0.8V$. As Figure 8 shows no real self-heating effects, the R_{ON} is modeled with a constant value.

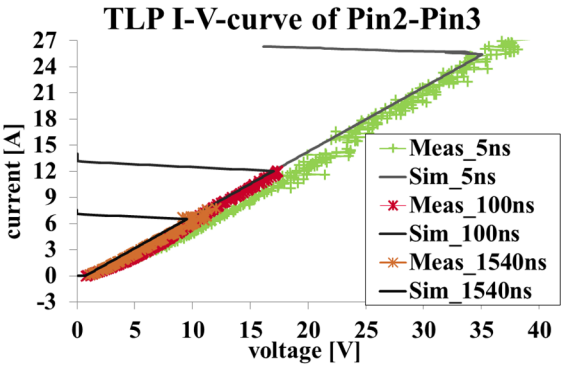

Figure 8: TLP-I-V-curves with three different pulse lengths of a forward diode at Pin2-Pin3

In contrast to the presented transient behavior modeling technique (TBM) modeling is usually done with the quasi-static 100ns-TLP I-V-curve. Only the correlation of voltage to current which was measured with TLP pulses of 100 ns length is reproduced by the IC model. The threshold for a physical failure is usually set to the failure current I_{t2} measured with the TLP. This modeling technique is widely used and therefore taken as a reference for the presented TBM and referenced to as *100ns-model* or *quasi-static-model*.

IV. Complete full-chip model of an ASIC

With the above described methodology a transient behavior model was generated for all relevant Pin-combinations of the investigated ASIC. To get a complete model of the IC all subcircuits were connected. The measurements showed that the combination Pin1-Pin3 is equal to Pin1-Pin2 + Pin2-Pin3. For this reason modeling for Pin1-Pin3 was skipped and assumed that simulation will work with Pin1-Pin2 + Pin2-Pin3. Figure 9 shows schematically the structure of the complete IC model.

Pin1-Pin2 shows a snapback of a presumably parallel element at roughly 90V. For short pulses (5 ns) this snapback is not immediately destructive, see Figure 4. For longer pulses like 100 ns or 1.5 µs this snapback causes immediate destruction. To reproduce this behavior an element *U5* was added in parallel to *U1* in the full-chip model of the ASIC. *U5* models a snapback element with a trigger voltage V_{TR}=*90V* and a very low destruction limit. This construction is capable to indicate the failure condition when a short pulse goes above the trigger voltage V_{TR}=*90V* and afterwards a significantly lower pulse destroys the device at a level below the failure voltage and current of only a single pulse.

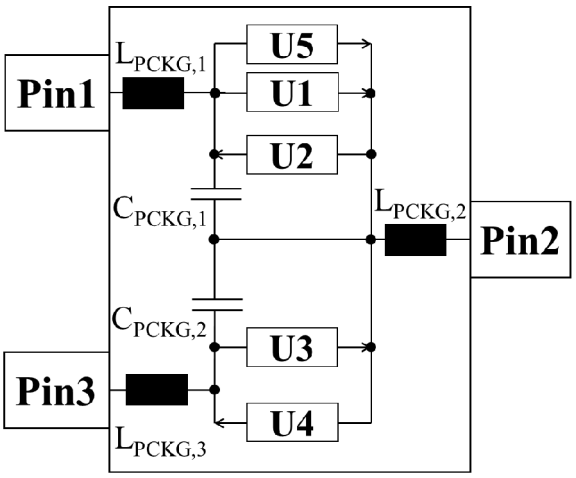

Figure 9: Overview how the model for the complete IC is constructed

The shape of an ESD generator pulse on system level is a combination of a short but high current peak combined with a second pulse at lower current levels which contains the most of the energy. In HMM-TLP-measurements the failure occurred exactly when the first peak was above 90V. Then the voltage drop at the second peak was significantly lower than at the previous pulse, which indicates the snapback of the parallel element.

The parameters for the subcircuits *U2* to *U4* are extracted as described in the section before. To

validate the accuracy of the model in terms of transient behavior, TLP-simulations were performed with a simulation setup identical to the one described in [18]. The pulse voltage of the TLP was varied within a certain range and at each voltage step a complete transient simulation was performed. Within the transient simulation the current and voltage levels were evaluated between 70-90% of the pulse duration, like in the TLP-measurements, exemplary in Figure 10 to Figure 12. The resulting quasi-static TLP-I-V-curves are depicted in Figure 4 and Figure 6 to Figure 8.

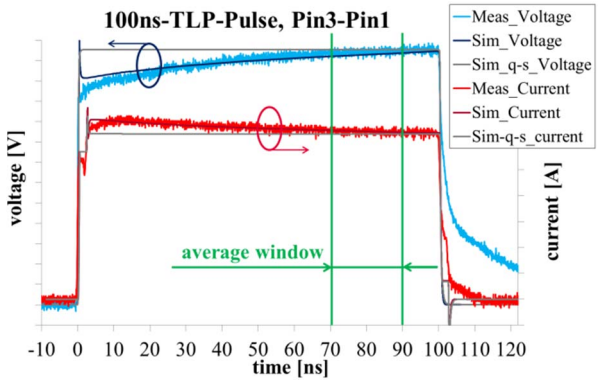

Figure 10: Voltage and current waveforms of a 100ns TLP-pulse obtained by measurement and simulation

Figure 10 to Figure 12 show the transient current and voltage waveforms from TLP measurement (*Meas_Current, Meas_Voltage*) in red respectively blue. Additionally the simulated waveforms with the presented IC-model are shown (*Sim_Current, Sim_Voltage*) in dark red respectively dark blue. To see the advantages of TBM compared to 100 ns quasi-static modeling these simulated waveforms are also included in grey (*Sim_q-s_Current, Sim_q-s_Voltage*).

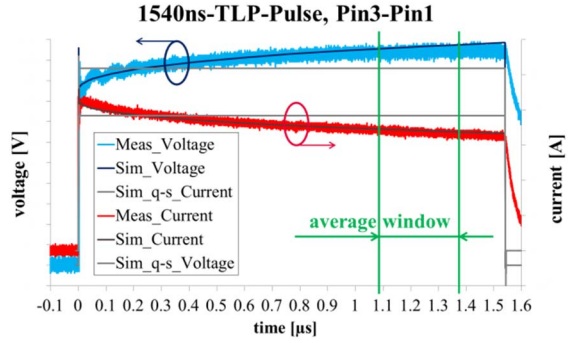

Figure 11: Voltage and current waveforms of a 1.54µs TLP-pulse obtained by measurement and simulation

The impact of the package on the transient behavior of an IC is included in the model by parasitic inductance L_{pckg} and capacitance C_{pckg}. The inductance and capacitance values of the package were extracted from an S-parameter measurement with a vector network analyzer (VNA) at small signal conditions (sinus with 1 V_{PP}).

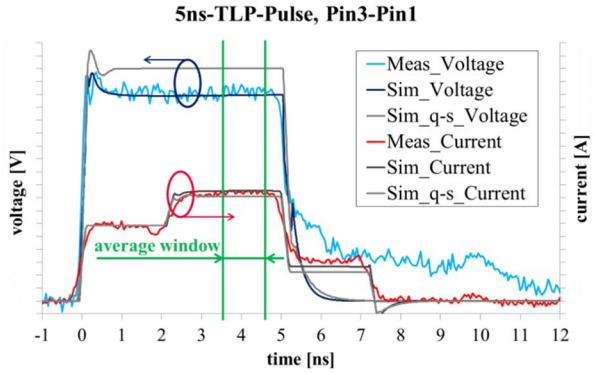

Figure 12: Voltage and current waveforms of a 5ns TLP-pulse obtained by measurement and simulation

All TLP-measurements where done with very short RF-probes directly on package to eliminate influences of the setup on the measurements.

V. Simulation vs. Measurement

An adequate way to prove the quality of a modeling approach is to compare simulation results with measurements. To get comparable results the simulation setup must consider all details which have an influence on the results. This work focuses on modeling of ICs therefore the details of the surrounding simulation setup are not always described in every detail.

A. GUN-Robustness on bare IC

Together with a GUN simulation model of [19] and the transient behavior model (TBM) of the investigated ASIC transient ESD simulations were performed. The ESD voltage in the GUN was raised in steps of 0.5kV or 1kV similar to the measurement until the simulation model indicated a physical failure. In the measurement a physical failure was assumed when the DC I-V-curve changed after the GUN stress.

The TLP-HMM system has the advantage of very good controllable and reproducible pulses in the shape of GUN pulses [20]. The waveforms of current and voltage at the DUT during the pulses

can be easily recorded. The good matching of the HMM waveforms obtained from measurement and simulation is shown in Figure 13. The shift between voltage and current waveforms is intended to show both first peaks of voltage and current separately.

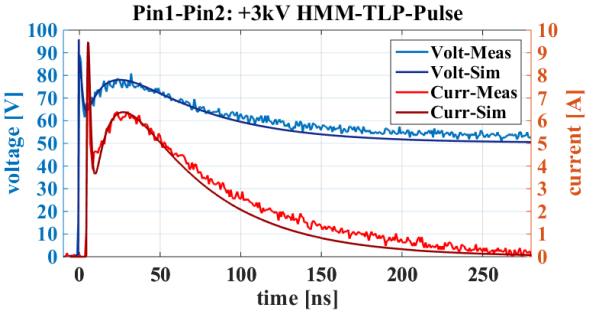

Figure 13: Comparison of HMM waveforms from measurement and simulation for +3kV on Pin1-Pin2

To characterize only the GUN robustness of the IC alone, the measurements were done directly on the IC pins without a dedicated PCB. One pin was directly contacted with the discharge tip of the GUN while the other pin was low-inductively connected to the ground reference plane. All GUN measurements where performed with a robotic system to minimize influences of the manual handling.

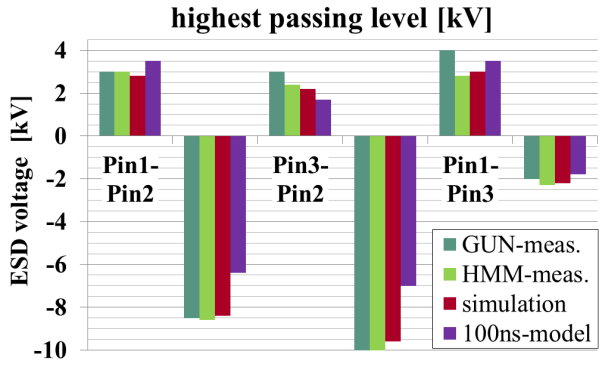

Figure 14: GUN robustness of investigated ASIC, comparison of simulation and measurement

Measurements were done with a NoiseKen TC-815R ESD generator (150pF/330Ω) and the HMM extension of a TLP system. The results for GUN-, HMM-TLP-measurements [20] and simulations are illustrated in Figure 14. The results of GUN- (dark green) and HMM-TLP-measurements (light green) show a good agreement except combination Pin1-Pin3 in positive polarity. This is assumed to be originated from the big variations of GUN-measurements which are well known in the industry. The dark red bars indicate the robustness levels obtained by simulation with the presented transient behavior modeling (TBM) methodology which are in good agreement with the measurements.

To compare TBM with 100ns-quasi-static IC modeling (100 ns-model) the failure levels of 100 ns-model are also included (purple). If the robustness levels of both simulations are compared to HMM-TLP results the TBM shows an accuracy of ±10% while the 100ns-model is only in the range of ±30%. This indicates that the TBM has a higher accuracy in predicting GUN robustness levels than the 100 ns-model.

B. GUN-Robustness on PCB with external components

It is expected that the advantages of TBM over the 100ns-model is more prominent on a printed circuit board (PCB) with external components. Therefore combination Pin1-Pin2 in positive polarity was investigated with an external protection capacitor. With the IC alone a GUN robustness of 3kV can be reached. An investigation was done to see how the capacitance value influences the GUN-robustness. For this purpose a very simple PCB was used. The PCB-layout in principle is shown in Figure 15.

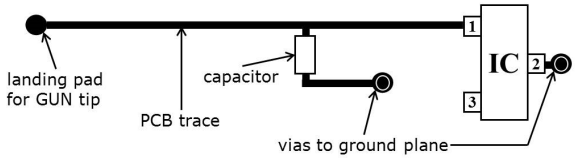

Figure 15: PCB-layout for GUN-measurements with ext. capacitor (schematically, not to scale)

In order to make precise simulations and to get meaningful results the L-, R- and C-parasitic values of the PCB-traces were included in the simulation. Also the parasitics of PCB vias were considered. The values of the parasitic elements were extracted with the geometrical values of the PCB with the software *PCB Toolkit V7.02* [21] at 500MHz and 1GHz. As the differences between the frequencies were negligible the values were assumed to be constant over frequency for the simulation. The parasitic values were extracted as values per unit length and multiplied with the length of the PCB trace and integrated into

simulation as discrete R-, L- and C-values. As real capacitors are no ideal capacitors, the typical parasitic L- and R-values (ESL = 0.4 nH and ESR = 50 mΩ) of the capacitor (construction form: 0603) are also integrated into the simulation setup. Figure 16 illustrates the simulated robustness levels of TBM (dark red) and 100ns-model (purple) for Pin1-Pin2 (positive polarity) relative to the measured value (green bars). Again TBM is in a range of ±10% while the 100ns is 60% too high in the worst case (47nF).

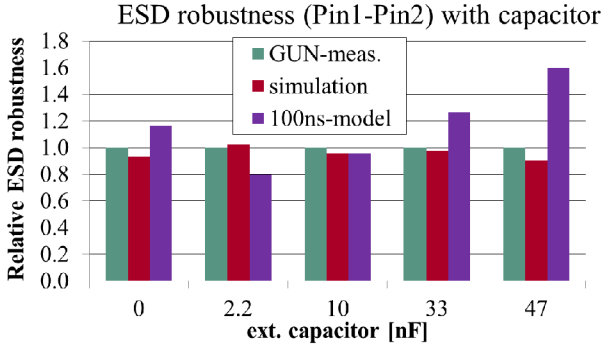

Figure 16: ESD robustness level of Pin1-Pin2 in positive polarity relative to measured value

As expected the external capacitor improves the ESD robustness of the ASIC. An increasing capacitance leads to higher withstand levels, although some kind of saturation effect occurs above 30 nF. An increasing capacitance is no longer leading to much higher robustness levels. This effect can be well reproduced with TBM while the 100 ns-model is not able to reproduce it, which shows clearly the advantage of TBM in predicting ESD robustness.

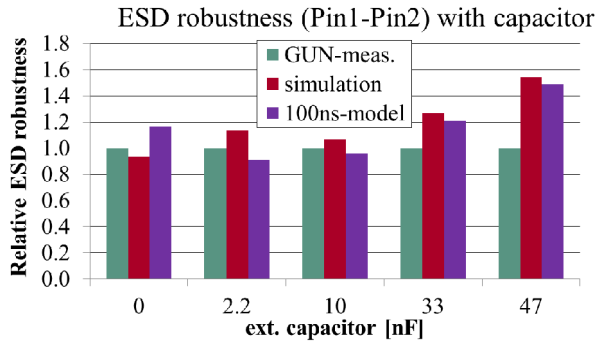

Figure 17: ESD robustness of Pin1-Pin2 in positive polarity relative to measured value without PCB parasitics

To investigate the influence of the PCB in simulation these parasitic elements were removed from the simulation setup and the robustness simulation was done again. With this setup the advantages of TBM disappear completely and both modeling methodologies, TBM and 100 ns-model, have an accuracy of only ±60%, see Figure 17.

This results shows that all elements should be considered in simulation which can have an influence on the transient behavior of the PCB. Accurate IC models alone are not sufficient to get an accurate simulation result. Every detail has to be taken into account.

C. GUN-Robustness on bare IC with 330pF/2kΩ network

The goal of this methodology is to provide accurate models for a time range of a few ns to a few tens of µs. ISO10605 permits different RC-discharge networks for the GUN. The RC-network of 150pF/330Ω has a time constant of $\tau_1 = R_{GUN} * C_{GUN} = 49.5\,ns$, while The RC-network of 330pF/2kΩ has a time constant of $\tau_2 = 660\,ns$. As τ_2 is significantly longer than 100ns this RC-network seems to be well suited to prove the quality of the modeling methodology. For simulation the discharge network (*150 pF/330 Ω*) of the GUN model [19] was simply changed to *330 pF* and *2 kΩ*. To validate the current waveform of the simulation model a short comparison of measured and simulated current for a short circuit discharge was made.

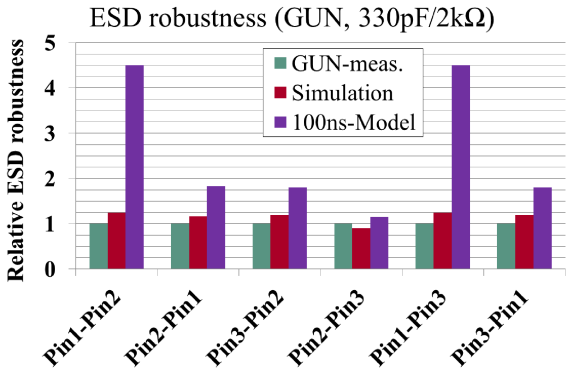

Figure 18: GUN-robustness with 330pF/2kΩ discharge network, comparison of measurement and simulation

Figure 18 shows the simulated GUN (330pF/2kΩ) robustness with the presented TBM methodology (red) and the 100ns-model (purple) relative to the measured values (green bars). The accuracy of the TBM model is within a range of ±25% while the 100ns-model shows deviations up to +350% in worst case, see Figure 18.

D. ISO7637-2 pulse 2a robustness

For automotive PCBs the car manufacturers often demand robustness tests against transient disturbances [10]. These test pulses are specified in [9]. Test pulse 2a has a width of 50 µs which is far away from the ESD time domain (tens to hundreds of ns). Therefore the presented modeling methodology is also validated with this test pulse. In measurement and simulation the pulse voltage U_S was raised in 5V-steps from 50V up to destruction. After each measurement a DC sweep was done to prove that no physical failure occurred during the pulse. The minimum pulse voltage that caused a physical failure was 95V in measurements what could be reproduced by simulation.

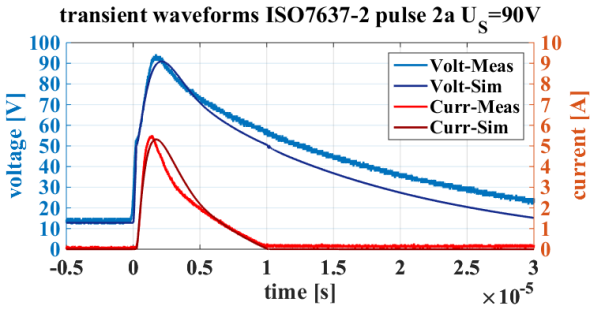

Figure 19: Voltage and current waveforms of the last passed ISO7637-2 pulse 2a with US=90V

The voltage and current waveforms show a good matching between simulation and measurement waveform especially for the peak values of current and voltage. The matching of the waveforms in Figure 19 also depends on the pulse generator model. The generator model was verified with measurements on different ohmic loads to ensure that the generator model does not distort the simulation.

VI. Conclusion

In this work a modular modeling methodology for complete ICs for system ESD and electrical stress simulation was presented. In contrast to prior works the basic approach is to use a generic module which can reproduce the transient behavior including the nominal destruction limit of a device depending on the set of parameters fed into it.

This generic module is able to reproduce the characteristic behavior of some typical ESD protection elements (e.g. diode in reverse and forward conduction or snapback-element) including transient effects like self-heating and conductivity modulation [13].

Reducing a complete IC down to the behavior in case of short pulses (e.g. ESD) brings two major advances. First of all is to say that such behavioral models strongly protect the IP of the IC vendor, the model shows only the behavior which can be measured as well. The second benefit is the compactness of the models which enables very quick simulation runs (in the range of a few seconds for a transient simulation). This enables a quick estimation of a systems robustness against transient disturbances.

The validity of this methodology was shown with the robustness against GUN and ISO7637-2 pulse 2a tests on IC- and PCB-level of an automotive ASIC.

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