vfTLP Characteristics of ESD Diodes in Bulk Si Gate-All-Around Vertically Stacked Horizontal Nanowire Technology

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Abstract - For sub-7nm bulk Si CMOS, a gate-all-around (GAA) nanowire (NW) device is a promising candidate. The new device architecture will have impact on the transient performance of an ESD protection diode. vfTLP measurement results and TCAD simulations prove that the performance in bulk GAA NW based diodes is maintained in comparison to bulk FinFET diodes.

I. Introduction

Bulk FinFET technology has been the mainstream in advanced CMOS technology nodes. ESD reliability has been investigated in SOI and bulk FinFET technologies [1, 2]. It is strongly impacted by the different process options and the specific device architecture [1-3]. Figure 1 shows the intrinsic ESD diode performance impacted by the technology options. A gate-structure-defined diode (gated diode) and a STI-defined diode (STI diode) have been proposed as ESD protection devices in sub-20nm bulk FinFET technologies [2]. The STI diode, has been proven its advantage on ESD protection design [2], because of an excellent ratio of failure current (*It2*) to parasitic capacitance. In sub-7nm CMOS nodes, bulk gate-all-around (GAA) vertically stacked horizontal nanowire (NW) technology is a promising candidate because of improved channel electrostatic and leakage control [4-8]. The stacked nanowires maximize the driving current per layout footprint [8, 9].

Recently, ESD diodes in bulk Si GAA vertically stacked horizontal NW technology have been reported [10]. However, only 100ns TLP results are disclosed in this prior work [10]. The purpose of this work is to study the influence of the GAA stacked NW device architecture on 2ns vfTLP characteristics in comparison with the bulk FinFET architecture. 3D TCAD simulations bring an in-depth physical understanding of the vfTLP current conduction and failure mechanism in these ESD protection diodes.

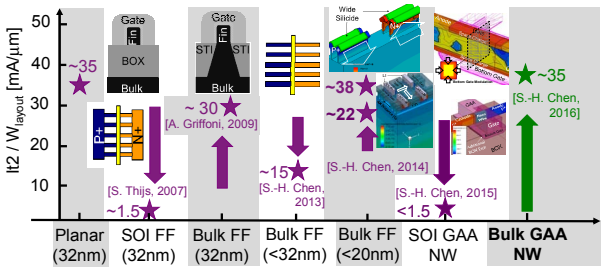


Figure 1: Normalized 100ns TLP failure current ($It2/W_{layout}$) of a ESD protection gated diode in different technology platforms.

II. Technology and ESD Diodes

Figure 2 shows a brief process flow for the fabrication of GAA Si NWFETs [9]. After well and ground plane (GP) implantations and SiGe/Si epitaxial growth, SiGe/Si fins were patterned by a self-aligned double patterning (SADP) process with a fin pitch of 45nm. The GP implant in this technology is used to prevent the parasitic channel formed at the bottom parasitic Si fins by the bottom gated structure, as shown in the TEM images of Figure 2. Dummy gates and spacers were defined and afterward SiGe/Si fins were

replaced by embedded Si epi in the source/drain (S/D) regions. The Si NWs were subsequently released in the RMG module by etching off the SiGe sacrificial layers. This etch process was followed by high-k/metal gate (HK/MG) deposition.

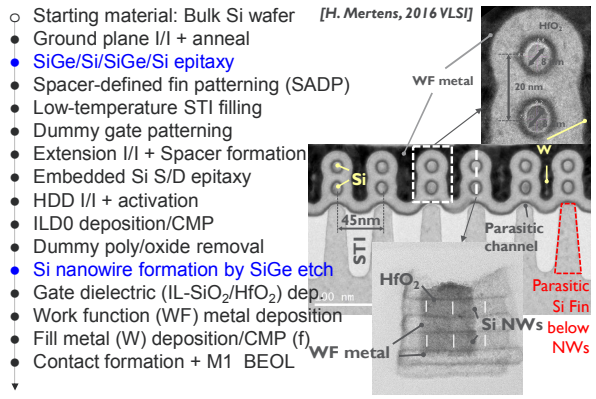


Figure 2: Schematic process flow for manufacturing gate-all-around (GAA) vertically stacked horizontal nanowires (NW) from a bulk FinFET (FF) baseline technology platform. HR-TEM cross section views of the two vertically stacked horizontal GAA NW (right) are also shown.

In Figure 2 [9], the TEM images show a GAA FET with two vertically stacked and densely spaced Si NWs with a diameter of 8nm. The local interconnect (LI) process with a pitch of 110nm is used to contact the S/D regions and the electrical metal gate. Before LI metallization is performed, a Ti-based direct contact [11] is formed at the bottom of LI trench. Two types of diodes are investigated as ESD protection devices: a gated diode and a STI diode, see Figure 3.

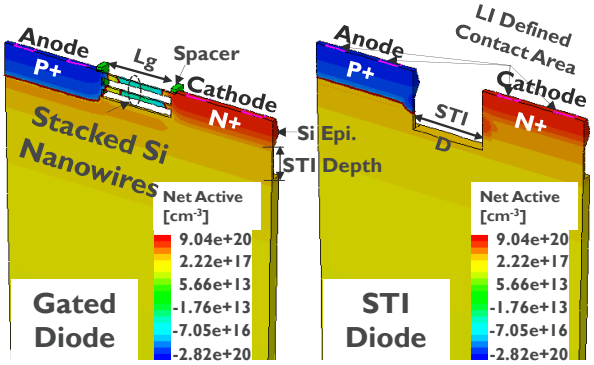


Figure 3: 3D TCAD simulation structures of the gated diode (left) and the STI diode (right). Both diodes have two local interconnect (LI) defined contacts on the anode and cathode sides. A half fin architecture is used for the 3D TCAD device simulations. The gate length (L_G) in the gated and the anode to cathode spacing (D) in the STI diodes are 140nm.

The layout parameters of the ESD diodes are: anode and cathode spacing (D) for the STI diode, and the gate length (L_G) for the gated diode. Both are fixed at 140nm in this work. The fin numbers (N_{fin}) for the STI diode (fins covered by S/D Si epi-layers) are 880 and nanowire numbers (N_{NW}= 2*N_{fin}) for the gated diode are 1760. Both have a 45nm fixed pitch. Symmetric numbers of the LI strips (N_{LI}) are 4 on the anode and cathode sides. The TCAD simulation structures used in this work are simplified with the N_{LI} of only 2 on the anode and cathode and with a half fin architecture in Figure 3.

III. Measurement Results and Discussion

The diodes are measured in forward conduction mode by using a 2ns vfTLP stress with a 200ps rise time in a 4-point Kelvin setup with RF needles. The device DC leakage current in reverse mode (at -1V) is monitored after each stress. A 10x increase in leakage current has been considered as the device failure.

A. Gated vs. STI Diodes

Figure 4 shows the vfTLP *IV* characteristics of the gated and the STI diodes. The STI diode shows slight advantage of *It2* compared with the gated diode. However, the STI diode does have a higher vfTLP on resistance (*Ron*).

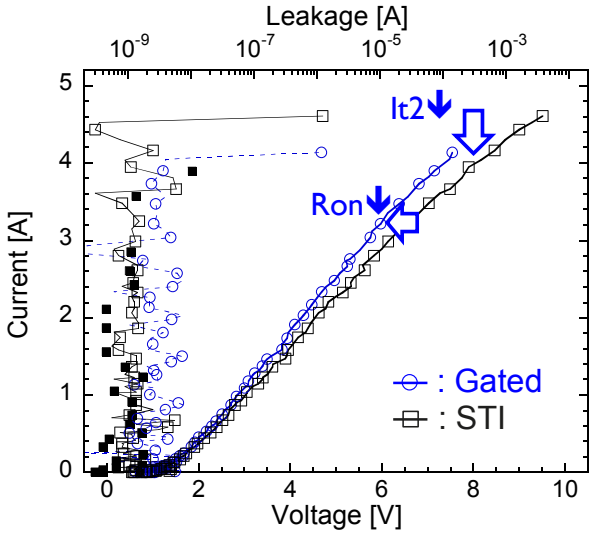


Figure 4: Measured vfTLP IV curves of the gated and the STI diodes. The two diodes have same layout parameters: the N_{fin} of 880 and N_{NW} of 1760, N_{LI} of 4, and the L_G or D of 140nm.

The differences of the *It2* and *Ron* are related to the different current distribution in these two diodes. The gated diode has a shallower and shorter anode to cathode current path through the parasitic Si fin below the NWs, compared to the STI diode with its current path fully under STI, as shown in Figure 5. This shorter current path results in a lower *Ron*. The highest current density for the gated diode is located at the top of the parasitic Si fin below the NWs. This can prevent the current crowding inside the NWs. Current crowding inside the NWs would otherwise result in an early thermal failure of the gated diode.

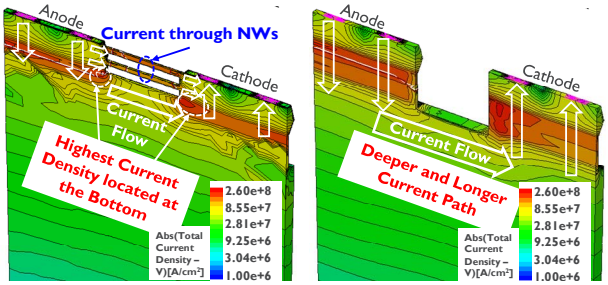


Figure 5: 3D TCAD simulated results of current density for the gated (left) and for the STI (right) diodes under the same vfTLP stress level.

Compared with the simulation results of the GAA gated diode in 100ns TLP [10], the ratio of current density inside NWs seems to be higher in the vfTLP simulated results in Figure 5. The current ratio inside the NWs strongly depends on the stress time, as illustrated in Figure 6. At the beginning of the vfTLP stress of 50ps, most current discharged through the top NW, as shown in Figure 6(a). Then, the current was discharged deeply through the bottom parasitic path as the stress time increasing in Figure 6(b) to (d). The slight current crowding under the fast- transient stress can be a reason for the slightly lower *It2* of the gated diodes under 2ns vfTLP stress. Without the NW structures, the STI diodes has no such concern of the current crowding effect. But, the overshoot voltage might be an issue for the STI diode.

In the bulk FinFET technology [12], the STI diode has been proven its excellent turn-on efficiency without a significant overshoot voltage. Figure 7 shows the current and voltage waveforms of the gated and the STI diodes under 2ns vfTLP stresses with two different stressed current levels of ~1.5A and ~3.5A. A very little overshoot voltage in Figure 7(b) and (d) was observed in both diode cases in these two stressed current levels. The STI diode has higher clamping voltage, compared with the gated one. But, in general, both diodes have very good turn-on efficiency and have <1V overshoot voltage under the high stressed current of 3.5A, as shown in Figure 7(d). Table 1 shows the parasitic capacitance ($C_{parasitic}$) [10] of these two ESD diodes and the TLP and vfTLP *It2* normalized by $C_{parasitic}$.

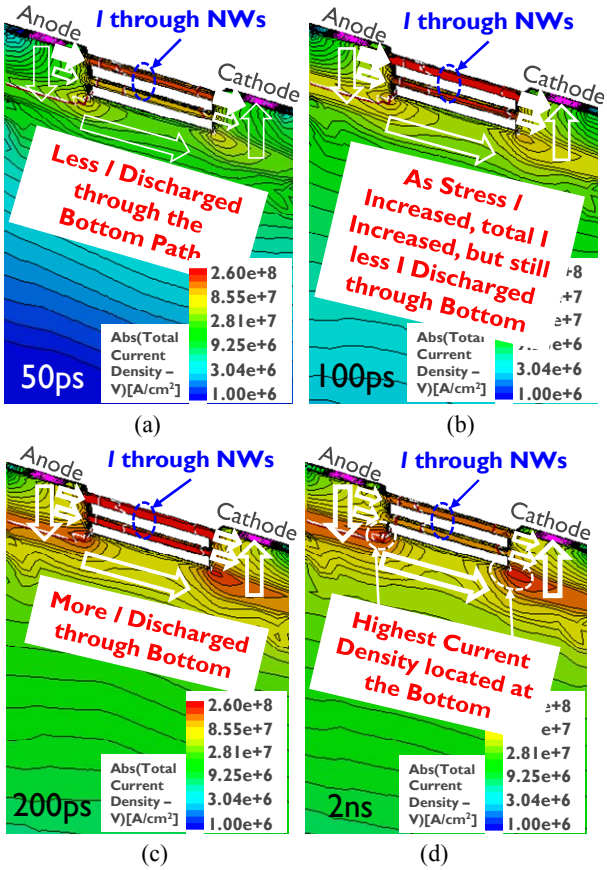
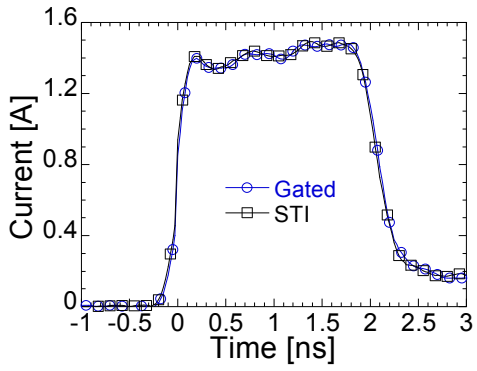


Figure 6: 3D TCAD simulated results of current density for the GAA NW gated diode under the same vfTLP stress level but with different stress time of (a) 50ps, (b) 100ps, (c) 200ps, and (d) 2ns.



(a)

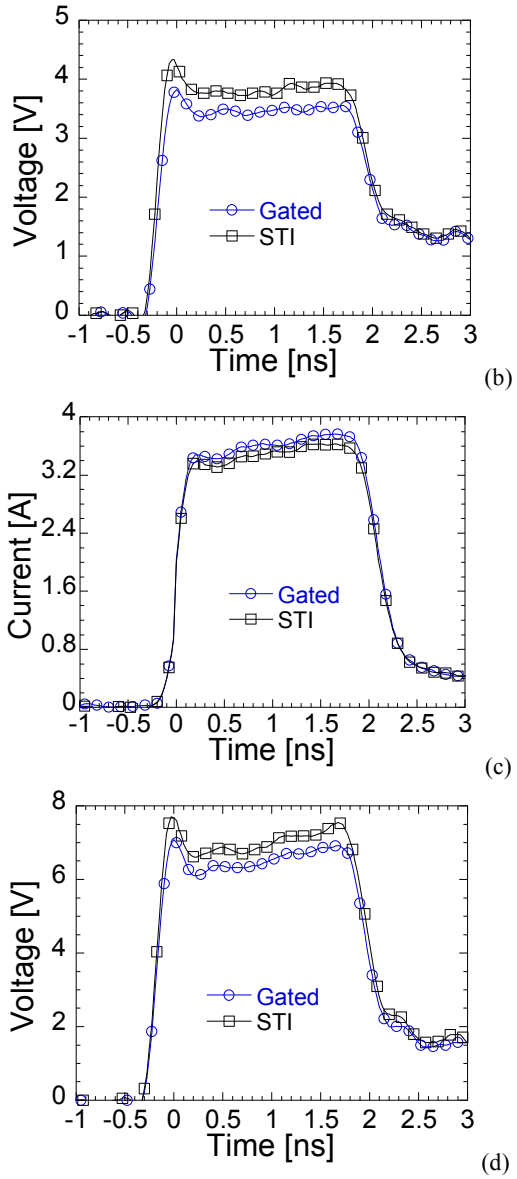


Figure 7 (a) and (c) Measured 2ns vfTLP current waveforms of the gated and the STI diodes under same pre-charge levels. The stressed current levels are (a) ~1.5A and (c) 3.5A. (b) and (d) the corresponding voltage waveforms captured with a 4-point Kelvin setup with RF needles in these two diode structures.

Table 1: Extracted total parasitic capacitance ($C_{parasitic}$) and the 100ns TLP and 2ns vfTLP *It2* normalized by $C_{parasitic}$ in the gated diodes and the STI diodes.

Parameters	**Gated**	**STI**
$C_{parasitic}$ [fF] at 10GHz	44	33
100ns *It2* / $C_{parasitic}$ [mA/fF]	32	42
2ns *It2* / $C_{parasitic}$ [mA/fF]	92	137

B. FinFET vs. GAA NW

Bulk Si FinFET (FF) processed diodes with the same layout parameters are available to access the impact of the GAA NW architecture on the vfTLP *IV* characteristics, see Figure 8. The FF diodes show slightly lower *It2* but a higher *Ron*, especially in the high current region (>1.5A). The *It2* and *Ron* difference in the gated diodes can be related to the different current path in these two device architectures.

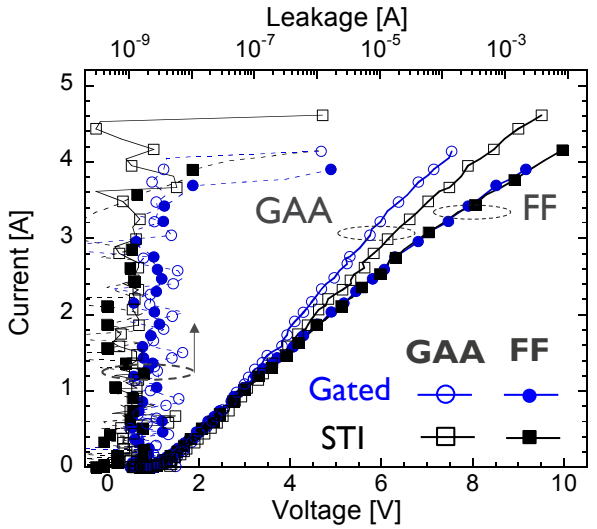


Figure 8: Measured vfTLP *IV* characteristics of the gated and STI diodes in the different processed wafers of FinFET and GAA NW.

Figure 9 shows the simulated results of the current density in the FF gated diodes under the vfTLP stress with different stressed times. At the beginning of the vfTLP stress, the current crowding location is at the surface next to the anode and cathode in Figure 9. The highest current density is always located at the surface during the entire vfTLP stress. Figure 10 shows that from ~25% to ~13% of the total current is conducted through the fin in the FF gated diodes under the vfTLP stress, but only less than 5% current finally is conducted through NWs in the GAA gated diodes. This can explain its slightly lower *It2* in the FF gated diode compared with the GAA gated diode. However, a shorter surface current path in the FF gate diode did not bring a lower *Ron*, compared with the GAA gated diode. This can be also attributed to the current crowding effect which can generate some local heat. The *Ron* difference between the FF and GAA gated diodes is more

pronounced in the high current region, as shown in Figure 8.

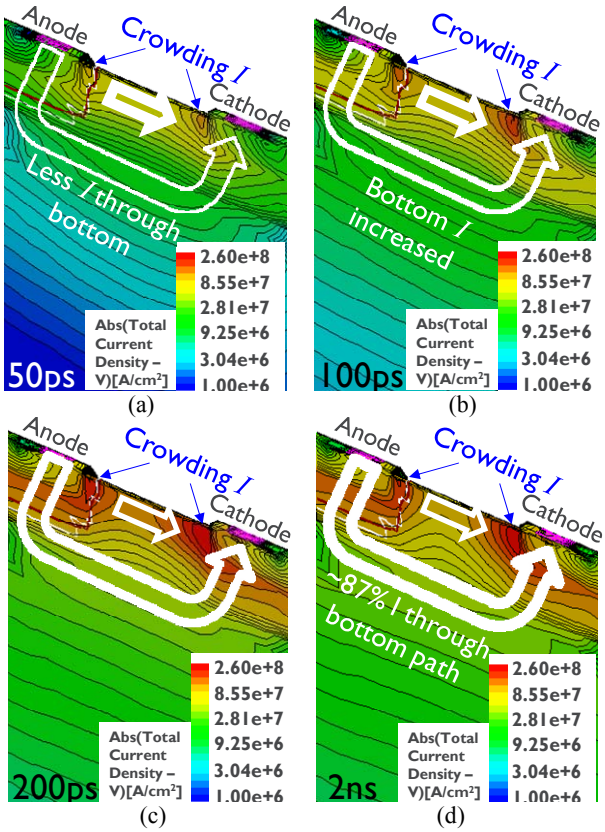


Figure 9: 3D TCAD simulated results of current density for the FinFET gated diode under the same vfTLP stress level with different vfTLP stress time from 50ps to 2ns.

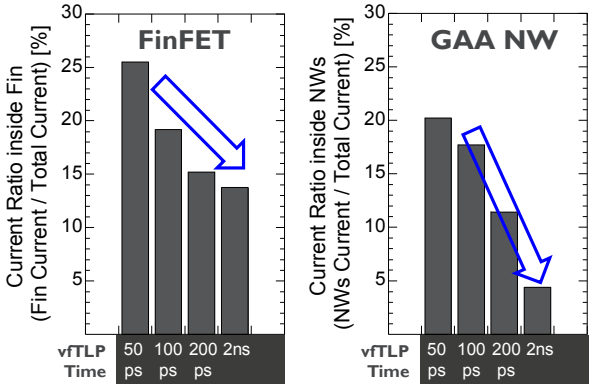
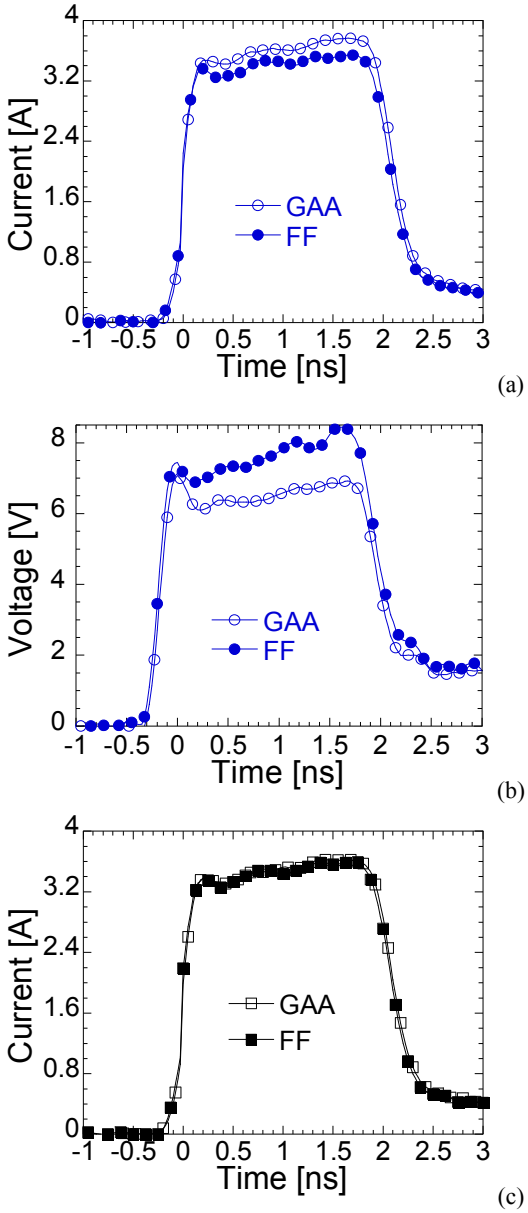
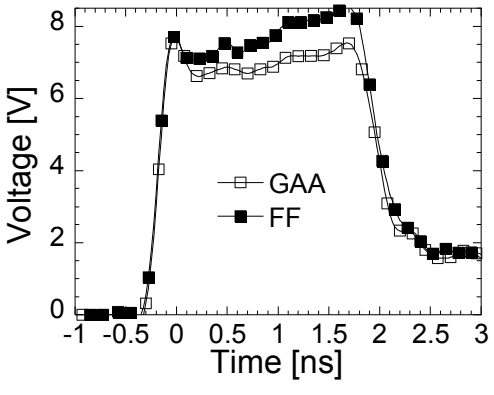


Figure 10: Simulated results of the integrated current ratio in the fin or the nanowires in the gated diodes for these two device architectures of the fin and the nanowires under the same vfTLP stress level with different vfTLP stress time from 50ps to 2ns.

In addition, the *V* waveforms in Figure 11(b) further indicate a significant voltage increase in the FF gated diode. These two observations can be the two evidences of the self-heating issue in the gated diodes. Similar results are shown in the FF STI diodes in Figure 11(d). Compared with the GAA STI diode, the FF STI diode also has a higher *Ron*, especially in the high current region, as shown in Figure 8. However, without the two stacked NWs in the STI-defined diode, the STI diodes should be identical in the FF and the GAA technologies. The difference of the self-heating behavior in the STI diodes can be related to the different options of the S/D epitaxial process [10] and is more pronounced in high current stress (~3.5A), as shown in Figure 11(d).

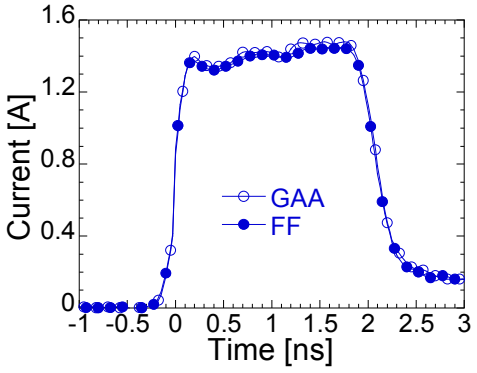




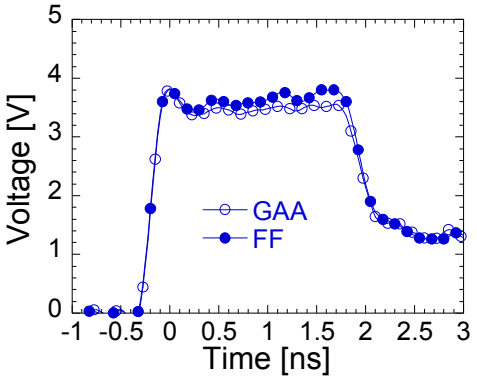
(d)

Figure 11: (a) and (c) measured 2ns vfTLP current waveforms of the gated and the STI diodes in the FF and GAA NW technologies. The stressed current levels are ~3.5A. (b) and (d) the corresponding voltage waveforms of these two diodes in the two different technologies, respectively.

Figure 12(a) to (d) shows the vfTLP transient waveforms with ~1.5A stress current. The voltage waveforms in either the gated diodes or the STI diodes are similar, especially in Figure 12(d). These results further prove the *Ron* difference between the FF and GAA STI diodes is mainly related to self-heating effect and only observed in a high current stress (>1.5A for 2ns vfTLP stress and >0.7A for 100ns TLP stress [10]).



(a)



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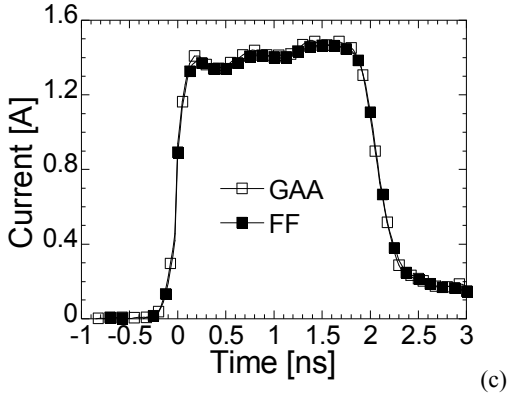

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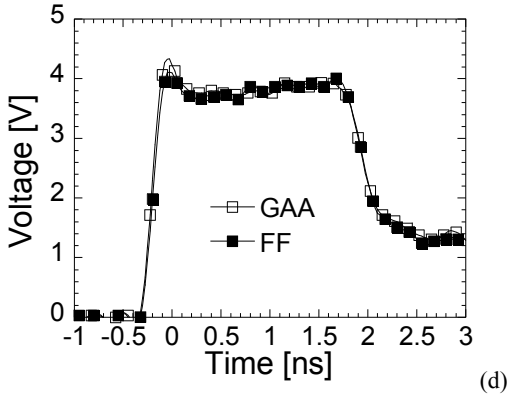

(d)

Figure 12: (a) and (c) measured 2ns vfTLP current waveforms of the gated and the STI diodes in the FF and GAA NW technologies. The stressed current levels are ~1.5A. (b) and (d) the corresponding voltage waveforms of these two diodes in the two different technologies, respectively.

Because of the requirement of two stacked NWs, the original fin height is higher in the GAA NW technology, but the STI depth under the fin was intentionally fixed in these two technologies. The anode and cathode fin height in the GAA STI diode is higher than that in the FF STI diodes. A 20nm fin height difference does not have a significant impact on the *It2* of the STI diodes in Figure 8. In fact, this taller fin with the same STI depth can create an even longer conduction path in the GAA STI diodes. However, this STI diode does not bring any real disadvantage of the *Ron* in the low current region (<1.5A), see Figure 8. In opposite, this STI diode shows a lower *Ron* under high current region (>1.5A). This can be attributed to the fact that a taller fin structure usually accompanies a large epitaxial volume on the S/D (or anode/cathode) regions. It is beneficial to the contacts of the diodes and further improves the thermal dispassion under high current stress which results in less self-heating.

IV. Conclusion

The vfTLP characteristics of two different ESD diodes, a gated diode and an STI diode, are presented in a bulk gate-all-around nanowire technology. The STI diode is the better ESD protection device in the bulk GAA NW technology due to the excellent *It2/C* ratio, compared to the gated diode. In addition, the GAA NW ESD diodes also show no disadvantage in comparison to the bulk FinFET ESD diodes.

Acknowledgements

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