Proper Human Body Model Testing of High Voltage and "No Connect" Pins

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Abstract – "No Connect" pins were exempted from HBM testing due to tester delivery path parasitics producing an unintended CDM-like overstress. A modified two-pin HBM tester has been build that reduces overstressing to a level were valid testing of No Connect pins and high voltage pins with snapback protection is possible.

I. Introduction

Over 10 years ago several large IC manufacturers traced their Human Body Model (HBM) failures to the testing of "No Connect" pins and concluded these were "false failures." They determined that their HBM testers were producing large, fast current pulses to some neighboring pins of the No Connects. The problems of testing No Connect pins have been studied and reported.[1] When this information was presented to the working groups at the Electrostatic Discharge Association (ESDA) and JEDEC this problem was discussed and analyzed. The conclusion of this work was that all HBM testers used at that time could produce large overstress when applying the HBM pulse to No Connects. The overstress was more like a Charged Device Model (CDM) event in timing rather than an HBM pulse, and the current levels were much higher than prescribed by the HBM standards. Both JEDEC and the ESDA standards organizations subsequently modified their HBM standard test methods [4,5] to allow device testing and classifications without applying stress to the No Connect pins "until the testers can be improved so as to not produce this extra stress". Their more recent joint HBM standard [6] also prescribes testing that avoids applying stress to No Connects. The Automotive Electronics Council [7] followed this change and now allow skipping the stressing of No Connects. This testing allowance does not provide an impetus to address the tester issues that caused this extra stress. However, looking toward future testing requirements there are additional benefits of testing all pins including No Connects.

Packages with smaller terminal dimensions, increasing the interaction of non-connected pins and sensitive pins may produce more testing problems. Additionally, it would be desirable to test devices without the detailed design information needed to determine the pin combinations required by JS-001-2014. Toward that end, testing using random sampling of pin combinations is being proposed [8] and stressing of all pins, including No Connects, would be desirable to conduct a fully black box HBM test. As will be described below, high voltage device pins can see overstressing similar to No Connect pins. For example, a opto-isolator, or photocoupler, can have 2 kV or more isolation between circuit sections making some pin combinations effectively not connected.

Therefore, to allow stressing of all pins without producing false failures a modified 2-pin HBM tester, that meets the latest JEDEC and ESDA HBM test method JS 001-2014 and other standards, has been developed.

II. Tester Problem Analysis

The HBM schematic in Fig. 1 is similar to diagrams appearing in HBM Standards [4,5,6,7]. As described in those documents, this schematic is over simplified and is not sufficient to describe and understand the problem being reported on herein. The parasitic inductance, resistance and capacitance in the wiring of HBM testers have significant effects on the HBM stressing current delivered to the devices under test (DUTs). An analysis of these unwanted parasites can explain the observed issues testing of No Connects and high voltage input/output pins.

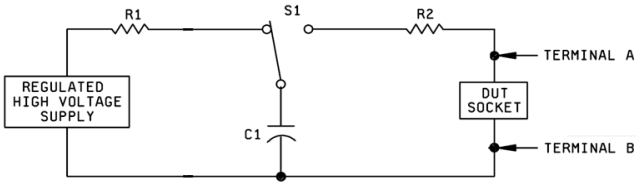

Figure 1: Basic HBM pulser generator

Since HBM testers provide a 1500-ohm series resistance the wiring parasitic resistances are normally insignificant. However, the wiring inductances and capacitances do effect the high frequency ESD simulated pulses. The focus on parasitic wiring capacitance is not new; the 500-ohm load test limits the parasitic wiring capacitance as will be explained. There has been a new focus on wiring capacitance as the technology drives device sizes smaller and small capacitances become more important to high frequency operation. The term *parasitics* has been applied to different HBM tester non-ideal operations, so a differentiation should be made between the effects of wiring capacitance on 1) stress to DUT pins that should be stressed, and 2) crosstalk among and loading of pins that should be floating.

HBM tester parasitic capacitance has been shown to significantly change the DUT stress when the DUT connects tester channels together.[9] The HBM standards do not detail the wiring nor directly describe the use of relay switching matrices that connect pulse generator(s) to DUT pins, but simply state the unconnected pins "shall be floated" so a description of how pins are "floated" is needed. In the typical relay matrix switched HBM tester, "floating" is accomplished by disconnecting the wires from the DUT test fixture board parasitics by internal relays. However, about two-thirds of a meter of tester wiring connects each "floating" DUT pin to its open relay. The capacitance of tester wiring, being comprised of the socket, test fixture board, relays and multiple printed wiring boards and their connectors internal to the tester, provides loading to the floated pins. The parasitics of this wiring can be termed *Floating Pin Parasitic Loading*, and is problematic to the testing of high frequency and/or small geometry technologies. The use of a two-pin, socketless tester can eliminate this wiring by contacting only two DUT pins and having all other pins truly float. However, the parasitic capacitance of the wiring from pulse generator to DUT remains. We can term this parasitic capacitance loading as *Delivery Path Parasitics*, and it can be significant in any HBM tester.

The Delivery Path Parasitic wiring capacitance, comprised of the internal relay matrix and PCB printed wiring plus the test fixture board and socket, can be modelled with a single capacitor shown in Fig. 2. The capacitor $C_{PARASITIC}$ can be identified as the root cause of the No Connect problem. The maximum capacitance of $C_{PARASITIC}$ is limited by the 500-ohm load test of the HBM Standard, and that also limits the number of tester channels. This limitation is overcome in common relay matrix tester designs by providing an additional pulse generator for every 96 pins.

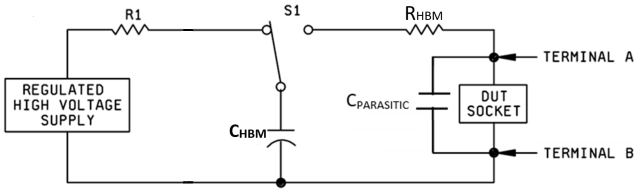

Figure 2: HBM pulser generator showing the parasitic capacitance of wiring to the DUT

II.A. Modelling

Determination of the limit of delivery path parasitic capacitance can be done with SPICE modelling. The HBM current waveform has been defined as a double exponential; a rising exponential with a few nanosecond time constant, and a decaying exponential with 150 ns time constant into a short. The circuit model in Fig. 3 uses a 1 Ω DUT rather than a short because the HBM waveform verification uses a Tektronix CT-1 or CT-2 inductive current probe which has a 1 Ω impedance in the frequencies of interest. The rising current edge speed is limited by tester wiring parasitic inductance and while not specified directly by the HBM Standards, the rise time is constrained to be between 2 to 10 ns, and most automatic testers have rise times between 8 and 9 ns. The inductance needed for 8.2 ns rise time is empirically found to be 7 μH in our SPICE model. Changing the DUT to 500 ohms, the maximum value of $C_{PARASITIC}$ can be determined to be 45.5 pF to limit the 500-ohm load rise time to 25 ns. The current waveforms with 1-ohm and 500-ohm DUTs is shown in Fig. 4 for a 1 kV HBM pulse simulation.

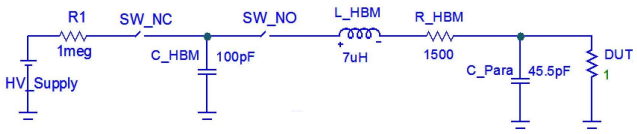

Figure 3: SPICE model schematic of the HBM circuit to determine the parasitic inductance and capacitance of the pulse delivery path based on the HBM waveform parameter limits.

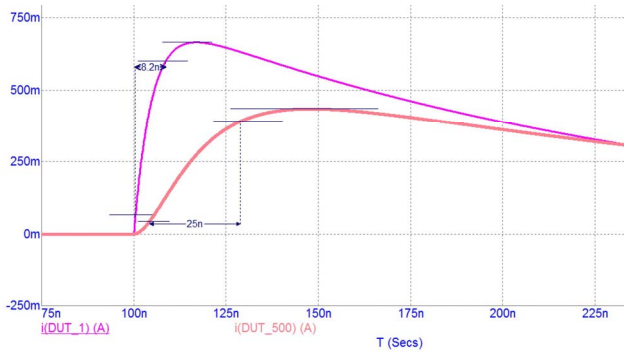

Figure 4: HBM current waveforms with parasitics of 7 µH series inductance and 45.5 pF shunt capacitance and DUTs of 1 and 500 ohms to meet 8.2 ns and 25 ns rise times.

The SPICE model can be improved as the parasitic capacitance is actually distributed along the entire pulse delivery path and is not completely located in parallel with the DUT. To improve the model the approximate impedance of the delivery path needs to be known. While there are many discontinuities and different impedances along the pulse delivery path components from tester internal printed wiring boards to DUT socket, and details on the connectors, pogo pins and DUT test fixture boards is not known in detail, we can estimate the path impedance. The Thermo Fisher Scientific MK.2 relay matrix switching tester uses a 75-ohm resistive termination on wires that conduct the current pulses to ground. This termination is prevent reflections from the ground back to the DUT pin and is effective to remove pulse ringing only when the termination is close to the wiring impedance. Having 75 ohm resistors on all HBM ground connections indicates that the typical wiring impedance is close to 75 ohms. Fig. 5 shows the improved model as 75 ohm cables are added to the DUT connections. To maintain the required 1500-ohm series resistance, the pulser resistance is reduced to 1425 ohms to accommodate the 75-ohm path and termination. The parasitic capacitance is then distributed along the cable delivering the pulse in this model. The capacitance of the cable from DUT to ground will have almost no effect on the current pulse as long its impedance does not significantly change along its length and it is terminated by a matching impedance. The Fig. 5 SPICE model parameters of the CABLE75 are Zo=75 ohms impedance and a length which can be adjusted to achieve the 25 ns rise time. When the electrical length is 3.25 ns the 500-ohm response agrees with the 45.5 pF lumped capacitor model as shown in Fig. 6. There are reflections due to the small cable impedance mismatch at both of its ends, preventing a smooth current pulse rise time, but the ripples are small and the fit is good. 3.25 ns of a typical RG59/U polyethylene dielectric cable with 20.5 pF/ft and propagation velocity of 66% of the speed of light in a vacuum (1.54 ns/ft) has a 66 cm cable length which has 43.3 pF total capacitance. This is close to the 45.5 pF from the simpler model. While an actual HBM tester is a blend of these two models, we can conclude that a practical upper limit of delivery path parasitic capacitance is slightly over 40 pF.

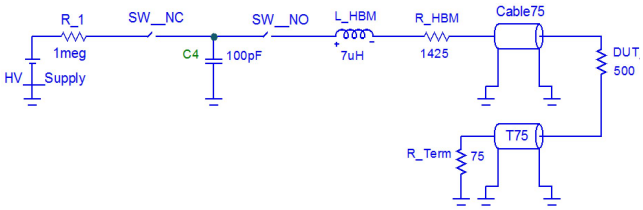

Figure 5: HBM pulser generator showing the parasitic capacitance of wiring to the DUT

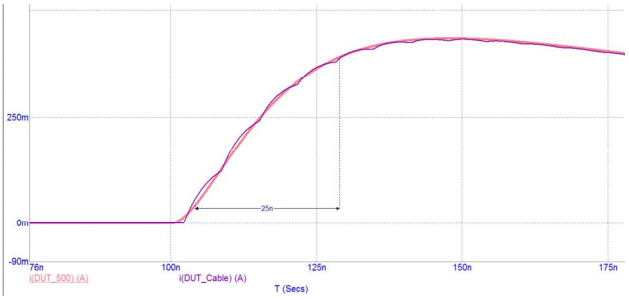

Figure 6: HBM pulser generator showing the parasitic capacitance of wiring to the DUT

It is common in modern HBM testers to have a 10 kΩ resistor in parallel with the DUT to prevent a pre-pulse voltage ramp on a high input impedance pin as described in JS-001-2014 Annex B.2. This resistor, if present, will be in parallel with capacitor $C_{PARASITIC}$ and that will provide a discharge path, but with relatively low conductance. With an assumed parasitic lumped capacitance of 40 pF, the time constant with a 10 kΩ resistor is 400 ns. In a span of 40 ns, a time that would charge the parasitics to half

the HBM voltage through the 1500 Ω HBM resistor, the charged capacitance will only decay less than 10% through the discharging 10 kΩ resistor. Therefore, the 10 kΩ resistor, while helpful, is not effective in protecting the DUT. All testing reported herein used a 10 kΩ discharge resistor permanently connected from the stressed DUT terminal to ground.

II.B. Applying Model to No Connects

When applying the HBM pulse to a No Connect pin of the DUT, the delivery path parasitic capacitance is charged by the HBM pulser current. The parasitic capacitance distributed along the pulse delivery path rises in voltage along with the No Connect pin. The rising voltage of the No Connect with capacitance dominated by the parasitic capacitance will exponentially approach $V_{HBM}\frac{C_{HBM}}{C_{HBM}+C_{PARASITIC}} \approx V_{HBM} \bullet 100/(100+40) = 0.714\ V_{HBM}$, where V_{HBM} is the HBM precharged voltage, increasing with a time constant of $R_{HBM}\frac{C_{HBM}C_{PARASITIC}}{C_{HBM}+C_{PARASITIC}} \approx 40$ ns. For example, a 2 kV HBM pulse will ramp the No Connect pin to over 1.4 kV. According to Paschen's Law, an arc will occur in the space between BGA balls with a pitch of 1 mm or less at this voltage. The arc will discharge the parasitic capacitance, and that discharging current is not limited by any significant current limiting resistance. The arc current will be mainly determined by the distributed parasitic delivery path capacitance because this is not actually a lumped capacitor at the No Connect pin but a combination of lumped and distributed capacitances. The discharge current can be delivered in about 5 ns and can be 2 to 3 times greater than the expected HBM peak current.

High voltage ICs, for example those with SCR power rail clamping protection, also allow charging of the parasitic capacitance before significant current flows through the stressed pin. High voltage (HV) pins will see excessive stress, but to a lessor degree than a No Connect. HV pins can allow charging the parasitic delivery path capacitance to the voltage where the ESD protection triggers and device conduction begins. For example, a snapback protection that has a trigger voltage in excess of 50 V ($V_{t1} \geq 50$ V, as would be measured with TLP) will have the delivery path capacitance charged to over 50 V before the turn-on voltage is reached and then upon turn-on a discharge current will flow through the DUT without the benefit of a series current-limiting resistor.

III. New HBM tester Design

Two techniques were used to reduce the extra discharge current from the charged parasitic delivery path capacitance: 1) introduction of a current limiting resistance between the parasitic wiring capacitance and the DUT, and 2) increased impedance of the delivery path. A modified 2-pin tester design was constructed where 350 ohms of the 1500-ohm series resistance was relocated from the vicinity of the HBM discharge switch S1 to very close to the DUT. In addition, the discharge path was made short, less than 5 cm, and the majority of it is two wires with a mainly constant 7.5 mm spacing, which results in an air dielectric twin lead of 300 to 350 ohms impedance. These changes reduce the parasitic path capacitance parasitics as shown in a schematic of Fig. 7.

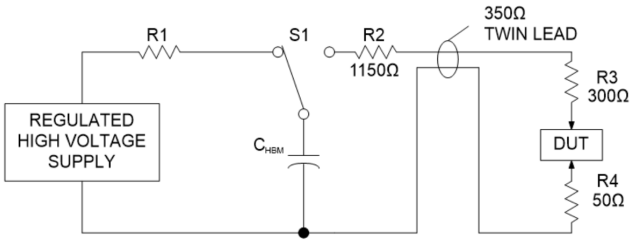

Figure 7: HBM tester concept with current limiting at the DUT

The combination of 350-ohm impedance wiring (TWIN LEAD in Fig. 7) and relocation of a 350 ohms of the 1500 Ω resistance close to the DUT (R3 and R4 in Fig. 7) totals an effective current limiting impedance close to the DUT of 700 Ω. The HBM waveform is maintained by having the total series pulse path resistance, R2+R3+R4 = R_{HBM} = 1500 Ω. The increase in delivery path impedance helps in two ways: the overall delivery path capacitance is reduced, hence the discharge current and total energy is reduced, and the instantaneous current that the wiring can support is lowered, thus the peak current is reduced.

IV. New HBM Tester Results

A short-circuit test showed the current pulse rise time, decay time, peak currents and ringing were within the required parameters of JS-001. The 500-ohm rise time was easily less than 20 ns. Thus, the new testing circuit was verified to meet all the normal HBM characteristics.

Two test structures were used. A device that is high impedance until it triggers at about 90 V, changing from high to low impedance, was used for high voltage pin testing. A No Connect pin with respect to a grounded Vss neighboring pin was produced by

using a probe card with needles having a pitch of 0.4 mm and allowing sparking between the needles. This simulates a package with the metal separation of 1 mm pitched 0.6 mm balls. Both test structures were tested with 6 discharges each at 8 voltages ranging from 100 to 2000 V.

Fig. 8 shows the peak voltages measured between the stressed pin pair. The HV pins (blue) had peak voltages ranging from 90 to 200 V which is effectively their clamping action at the various HBM voltages. At the higher HBM voltages the fast-rising pulse edge caused higher peak pin voltages to be reached before DUT protection clamping.

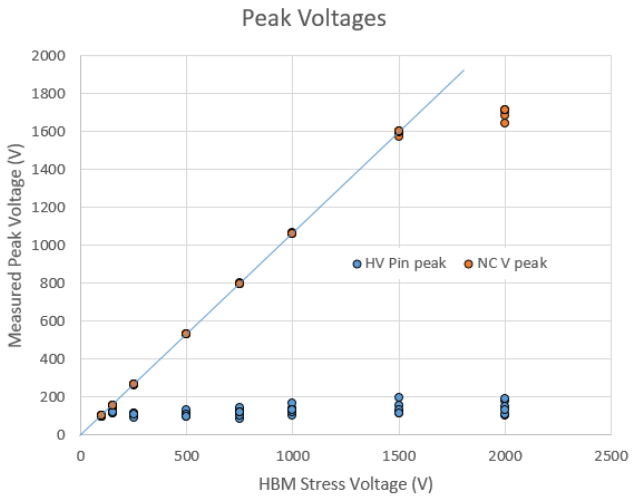

Figure 8: Measured peak voltages for a 90 V snapback DUT pin and a No Connect pin

The No Connect pins (orange in Fig. 8) followed the HBM voltages with a small amount of overshoot until arcing occurred. According to Paschen's Law for one atmosphere of air, arcing at small gaps should began when the breakdown voltage of 1.35 kV is reached. Arcing was observed beginning at 1.5 kV. At 2 kV HBM the arcing occurred with every pulse and prevented the full HBM precharge voltage from being reached at the simulated DUT pin.

Fig. 9 shows the peak currents, the critical parameter for the damage expected. Peak currents roughly followed the expected HBM short circuit current of 2/3 A/kV HBM (blue line). Operation at 500 V and below, with peak currents diagrammed in Fig. 10, showed overshoots from initial current spikes as the parasitic capacitance is discharged (blue points) to be almost as big as "steady state" current measured immediately after the overshoot, at the beginning of the decay (orange points). The initial spike almost doubled the HV pin peak current, but this overshoot didn't cause any device failures as total current levels were still quite low. As the HBM voltages approached 500 V, the overshoots became smaller as a percentage of the current after the overshoot. From 750 V upward, the overshoots were not significant. It is suspected that at low HBM voltages, the DUT voltage increases and close to the maximum pulse voltage is reached before triggering occurs, and the current spike discharging the parasitic capacitance is significant. But, at higher voltages the device turn-on occurs during the rising edge and clamping happens at lower voltage relatively to the maximum and therefore a relatively smaller overshoot occurs.

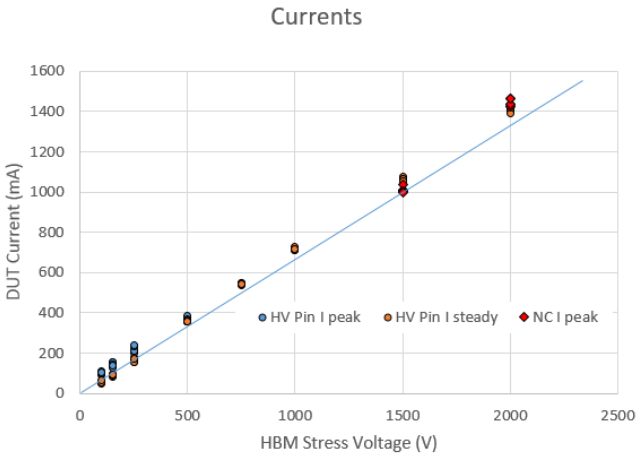

Figure 9: Measured peak currents for a 90 V snapback pin and a No Connect pin compared to the ideal HBM short circuit current line

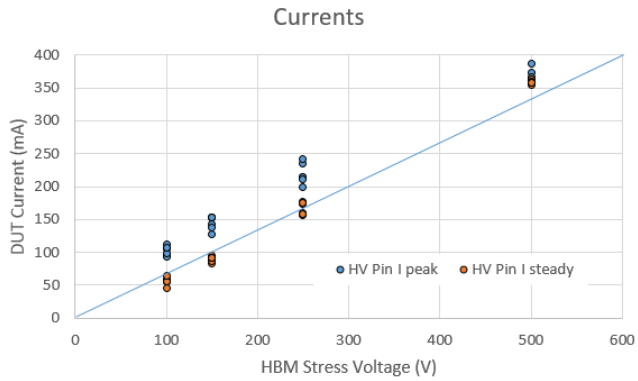

Figure 10: Measured currents of transient overshoot peak and steady state beginning of the normal decay for a HV snapback DUT pin compared to the ideal HBM short circuit current line

Overshoot current spikes are largest when the HBM voltage exceeds the turn-on voltage by small amounts. Examples of HBM pulse current waveforms from a HV pin are shown in Figure 11. With a 150 V HBM pulse, the DUT trigger voltage of approximately 90 V is exceeded with some delay as the DUT parasitic capacitances charge. The current starts about 25 ns after the HBM pulse begins and spikes to 150 mA which exceeds the expected short circuit current of 100 (the peak current of from 0.15 kV HBM pulse

should be 667 mA/kV, or 100 mA and the current axis is normalized to that short circuit current). At 750 V that initial current spike occurs earlier and is less than 10% overshoot. Since the current spike is large only at small currents, it would not be expected to cause a failure for a device that otherwise can withstand 500 V HBM. At HBM voltages exceeding several times the DUT trigger voltage, the initial spike is relatively small, an overshoot less than 10 %, typically staying within the allowed range of HBM short circuit currents. Therefore, at the HBM failure voltage the peak HBM current didn't exceed the standard short circuit peak current specification.

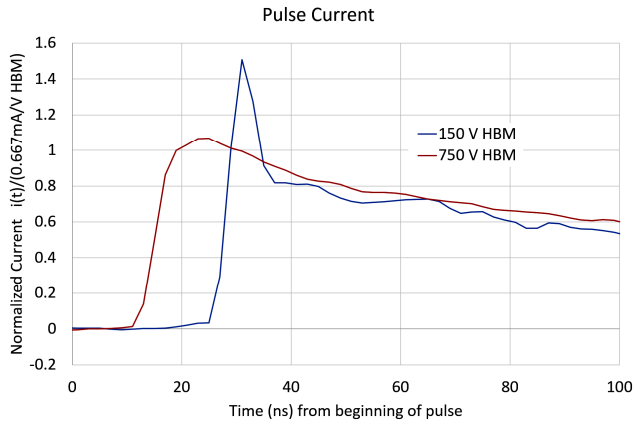

Figure 11: Overshoot current waveforms for a high voltage pin that triggers at about 90 V

Fig. 12 shows the peak current through both the high voltage pin and the No Connect pin at voltages that will cause arcing from the No Connect pin to a neighboring pin. In this region the initial current spikes are relatively small. However, we did observe slightly higher currents for the high voltage pins than the not connected pins at 1.5 kV HBM, but at 2 kV HBM the opposite was measured. This can be explained from the small overshoots and the relative timing of onset of current flow as seen in Figs. 13 and 14.

Figs. 13 and 14 show the current waveforms at high HBM voltages where arcing will occur between pins. As can be seen in the relative timing of these two cases, the HV pin conducts sooner than a No Connect pin as the trigger voltage of the HV pin is reached before the break down voltage between pins is reached. When the HBM voltage is increased to 2 kV, the time difference between the two cases is less as the voltage reaches the breakdown level sooner for the No Connect pin. Some overshoot and ring is observed from the no connect pin so a slightly higher peak current is obtained. Even taking into account the No Connect pin's overshoot and ring, a current waveform is obtained that meets the HBM short-circuit pulse current requirements.

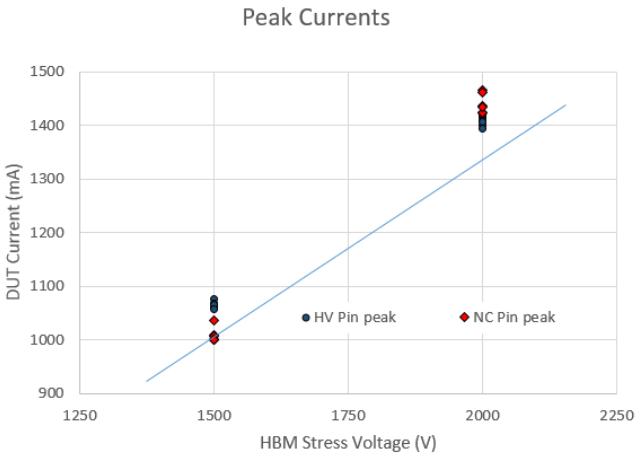

Figure 12: Measured peak currents at 1.5 and 2 kV HBM for a 90 V DUT pin and a No Connect pin compared to the ideal HBM short circuit current (blue line)

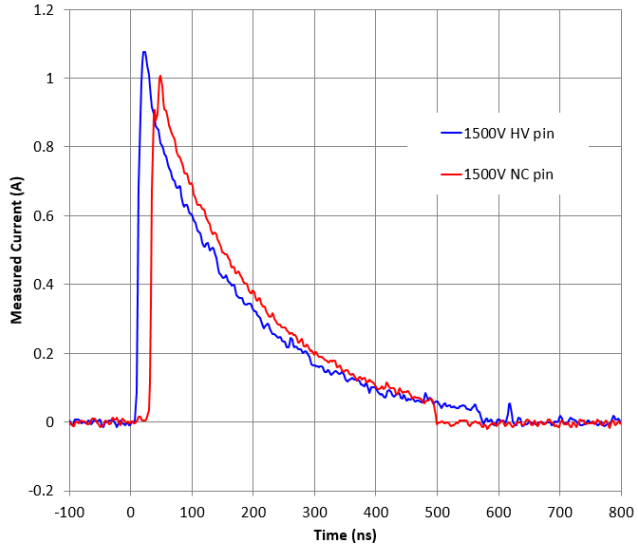

Figure 13: Measured 1.5 kV HBM current waveforms for a 90 V DUT pin (blue) and a No Connect pin (red)

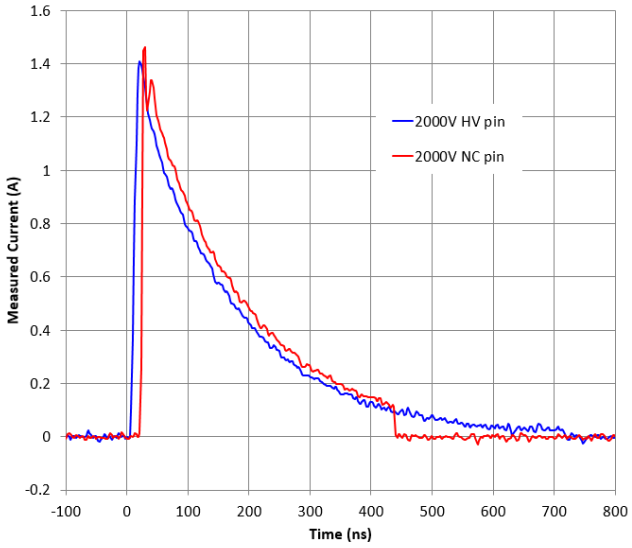

Figure 14: Measured 2 kV current waveforms for a 90 V DUT pin (blue) and a No Connect pin (red)

V. Conclusions

Arcing between a No Connect pin and one of its neighbors is expected to occur when stressing above 1 to 1.5 kV HBM. The arc current is supported in a typical HBM tester by charge stored in 30 to 40 picofarads of delivery path parasitic wiring capacitance. This parasitic capacitance can be charged to a voltage as much as 70% of the HBM stress voltage. When this voltage is large enough that a discharge occurs between an unconnected pin under test and one of its neighbors, the stored charge in the parasitic wiring is quickly discharged into the neighboring pin. The resulting current spike can exceed the normal peak current for this HBM voltage by factors of three or more depending on the distribution of the parasitic capacitance. High voltage devices with snapback protection designs, parts with high voltage isolation between sections, or any device that quickly transitions from high resistance to low resistance at significantly high voltages, can also suffer current spikes but to a lessor level. These high voltage devices trigger after the parasitic delivery path capacitance has been changed to the device's triggering voltage and wiring capacitance stored charge is quickly discharged before the pulse generator's 1500-ohm resistance limits the current.

A modified two-pin HBM tester solution presented here redistributed the 1500-ohms series resistances prescribed for an HBM tester, so there is adequate current limiting resistance between the parasitic wiring capacitance and the DUT pins. Additionally, an increase the wiring impedance will both reduce the parasitic capacitance and limit the discharging current. A reduction of the overstressing has been demonstrated by current pulse measurements. An effective impedance of up to 700 ohms can be placed in series with the DUT pins so the maximum current spike is limited to about twice the normal HBM peak current.

Data from the testing of HV pins showed the maximum peak current measured exceeded the normal HBM peak current by 100% when the HBM voltages exceeded the trigger voltages by just a small amount, and for HBM voltages exceeding trigger voltages by several times, only 10 to 15% above normal current was observed.

Proper peak current testing of No Connects and high voltage pins of devices with 500 V HBM protection can be made by a tester meeting all the requirements of various HBM test method standards if it has the proper current limiting features.

Acknowledgment

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