The main parameters affecting charged device discharge waveforms in a CDM qualification and manufacturing

Pasi Tamminen[1], Jeremy Smallwood[2], Wolfgang Stadler[3]

(1) EDR&Medeso Oy, Kalevantie 2, Tampere, Finland
tel.: +358505262479, e-mail: pasi.tamminen@edrmedeso.com

[2]Electrostatics Solutions Ltd, 13 Redhill Crescent, Southampton, SO16 7BQ, UK

[3]Intel Deutschland GmbH, Am Campeon 10-12, 85579 Neubiberg, Germany

Abstract – Charged device model (CDM) discharges in a CDM qualification and charged device discharges in electronics manufacturing are compared to evaluate the main discharge parameters. Accurate charged device ESD risk assessments would require to use discharge current waveform information and tailored measurement methods.

I. Introduction

ESD sensitivity of electrical components is characterized with standardized human body model (HBM) and field induced charged device model (FICDM) test methods [1]. The main purpose of these test methods is to compare ESD sensitivity information between different protection designs and between similar IC components from different suppliers. Both test methods currently report ESD sensitivity with a maximum withstand voltage the device I/Os and supply pins survive under test conditions. These voltage values are sometimes given in component datasheets and are typically the only source of ESD sensitivity information for system designers building on-board protections and ESD coordinators defining the protection methods for electrostatic protected areas (EPA).

Correlation of damage with CDM type discharges in a CDM tester have been extensively studied and it is known that CDM withstand voltage alone can only partially define ESD susceptibility of ICs [1]–[15]. In contrast, there is evidence that charged device damages correlate well with the peak currents in the CDM test waveforms despite package differences. The CDM test waveform rise time is a second parameter correlating with CDM damages, and the charge transferred in the first main pulse can correlate with damages with energy sensitive devices.

FICDM discharges in a qualification tester can reproduce component electrical failures similar to those observed in the field. However, there is less information available about the charged device discharge waveforms found in a real manufacturing environment. Here the charged device electrostatic discharges have additional uncontrolled environmental parameters that considerably affect the discharge waveform, and thus may change the failure threshold of the component. In practice, voltages considerably higher than the CDM withstand voltage may be sustained in a discharge without damage [20].

In common practice, charged device ESD occurring in the manufacturing is often referred to as “CDM”. In fact, the CDM waveform only occurs in the CDM tester. In this paper, we recognize this difference and restrict our use of the description “CDM” to CDM test situation in a qualification test system. For ESD occurring in other real-world situations, we refer to charged device ESD.

Controlling charged device discharges in an EPA can require more advanced control methods and understanding of the dynamics of the events. In parallel, industry is moving to use electrical components with lower CDM ESD withstand voltages [23][26][29]. Therefore, the purpose of this study is to collect information of the main parameters affecting the CDM current waveforms in a qualification, and the main parameters of charged device discharges in real processes. The focus is with charged device events with less than 250 V initial potential difference of the device-under-test to the contacting (typically grounded) metal object. The collected information can be further used to select efficient control methods and parameters to assess charged device type risks in manufacturing based on CDM qualification data and practical measurement methods in EPAs.

II. Research methods

A. CDM qualification analysis

Component CDM qualification based on the standard ANSI/ESDA/JEDEC JS-002 is extensively studied and these results are used to evaluate main parameters affecting discharge current [5][8]–[11][13]–[18].

Charged device discharges were analyzed primarily with current and charge measurement methods. Discharge events can also be detected with indirect methods by using electromagnetic interference (EMI) sensors and antennas [19]. EMI measurements are out of scope of this paper.

B. Laboratory analysis

CDM and charged device discharges type of events and the main waveform parameters were analyzed in a laboratory environment with manual and semi-automatized test methods. Different current probes were used to capture the discharges [29].

More than 20 different IC package types from 01005 discrete to 45 mm × 45 mm size µBGA are used in the study. A few of the ICs are presented in Figure 1. In addition, mobile phone printed circuit boards (PCB) were used with charged board analysis.

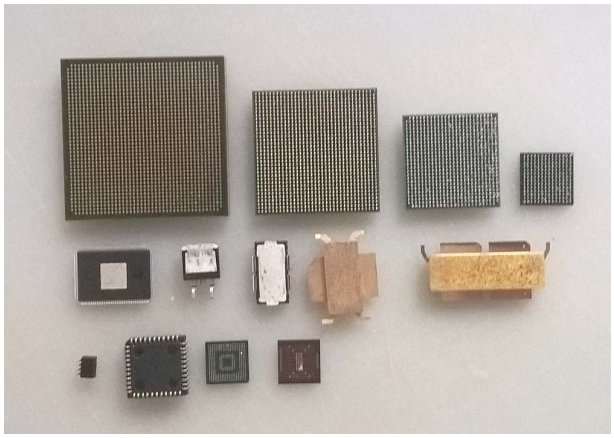

Figure 1: Example ICs used in the study.

C. Simulations

SPICE equivalent circuit simulations are the main method to simulate charged device ESD events in this study. SPICE is used to evaluate how circuit parameters can affect the stress level. This provides information to compare with control measurement methods in EPA.

The SPICE equivalent circuit in Figure 2 is a modified version of the CDM simulation model presented by Goëau [10] and Ashton [11]. Here the limited dynamic capacitance of the field plate $C_{\text{fieldplate}}$ is an additional part of the model.

Both the FICDM event and charged board event (CBE) are simulated with this circuit. Based on Maloney [8], the *RLC* parameters to reproduce the CDM waveform with a FICDM tester are for example R_{spark} = 28.6 ohms, C_{DUT} = 16.3 pF, and L_{pogo} = 11.7 nH. With these parameters, the 500 V stress level had a match with the peak current I_{max} and the charge of the first positive pulse Q_{fp} in a CDM tester.

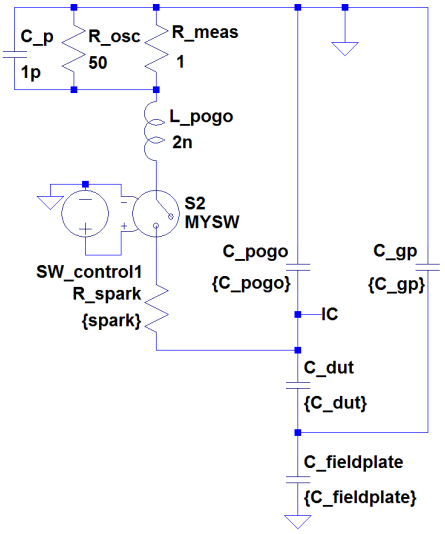

Figure 2: SPICE simulation model for the FICDM tester and for CBE discharges.

III. Results of the charged device discharge event analysis

A. The main discharge stress parameters

In both the CDM test and factory charged device ESD the peak current, pulse rise time, transferred charge, energy, and power are the main parameters to study. Generally, the peak current and charge transfer increases when the capacitance of the device under test (DUT) increases. The peak current and rise time are the dominant parameter defining the damage threshold with CDM discharges [13][16]–[18].

The peak current is in first order independent of the pulse width, and the width of the pulse has impact on the failure rate only if the failure requires a certain total energy [25]. In addition, the initial stored charge has no direct correlation with the peak current. Instead, CDM damage is caused by a thermal process driven by the electric power of the discharge current. In addition, a fast current rise time can induce excess voltage differences across power busses and ESD protection devices based on the equation $V = -L\frac{di}{dt}$. This induced voltage typically causes an oxide breakdown damage.

When the damage is related to the energy of the pulse, the total transferred charge is an additional parameter to study. Energy failures can occur for example with CBE and cable discharges where the source capacitance and series inductance are

typically higher than in a tester CDM event. The charge can be integrated from the discharge current waveform and the potential energy can be calculated in a time domain when the resistance of the sensitive circuit is known. The total energy can be calculated based on the known source capacitance and initial discharge voltage from the equation $E = \frac{1}{2}CV^2 = \frac{1}{2}QV$ [20][21].

CBE discharge waveforms have typically higher peak currents, charge transfer and a slower rise time than found with discharges from small size single ICs. In a CBE, the discharge current spreads and flows multiple parallel paths through PCB traces and components [20]. Therefore, the exact stress level ICs will see depends on the discharge contact point, the PCB layout, and the system mechanic designs. The current peak with the same charging voltage can also be smaller and the rise time slower due to the PCB serial inductances, resistance and parallel capacitances. There can, however, also be secondary discharges on the system board where the secondary pulse rise time can be about 4–5 times faster than the main discharge [22].

B. Parameter sensitivity tests

The following five parameters are selected for charged device ESD event sensitivity analysis and these are simulated with a SPICE equivalent circuit.

- Capacitance of the field plate; $C_{\text{fieldplate}}$
- Capacitance of the pogo pin; C_{pogo}
- Inductance of the pogo pin; L_{pogo}
- Air spark resistance; R_{spark}
- Ground plate capacitance; C_{gp}

There are additional parameters affecting charged device type discharges, such as the relative humidity, physical shape of the surfaces where the sparking occurs, and the speed of contact. These are typically not under control outside a CDM qualification tester and are out of scope of this study.

a) Air spark resistance

The air spark has been reported to be the main source of uncertainties with FICDM testing. The air spark is also affected by the physical location of the pogo contacting the pin on the DUT [15]–[16][17]. Here the spark length and resistance of the plasma channel have natural variation [13][18].

Figure 3 shows simulation result where the discharge spark resistance R_{spark} is varied between 10 Ω and 100 Ω when the C_{DUT} is kept constant 10 pF and the stress voltage is 250 V.

In most studies the air spark resistance in a CDM event has been assumed to be around 25 Ω [8][10][11][19]. When the stress level in a FICDM method is less than 250 V or more than 1500 V, the air spark channel can have a wide resistance variation from 5 Ω to 80 Ω [24]. This has a major effect on the peak current as seen in Figure 3, where the peak current decreases from 8.4 A (10 Ω) to 2.1 A (100 Ω). At the same time the pulse rise time gets faster as the pulse amplitude decreases.

In a CDM tester, the air spark is partially controlled as the temperature, humidity, and the speed of pogo pin movement can be controlled. In manufacturing these parameters can vary in a charged device discharge, thus, the spark resistance can be different between consecutive pulses. The same is observed when trying to repeat discharges with manual current measurement methods [29].

Based on Figure 3 and measurement trials, the difference of the peak current can vary three to four times, and the rise time about two times depending on the spark channel properties.

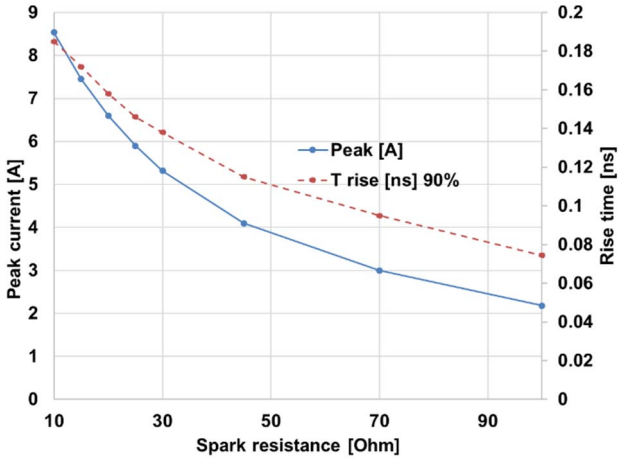

Figure 3: The CDM peak current and rise time with a varying spark resistance.

b) Inductance of the pogo pin

A series inductance between the discharge contact point and the ground reference plane depends on the shape of the object touching the charged device. In a CDM tester the contacting object is a pogo pin with a varying length of few millimetres, and the inductance value can be from a few up to over ten nanohenries.

A package internal inductance can be scaled with the square root of package area [19]. Typically, the maximum peak current is found in the middle and minimum at the outer edge of the package and when the pogo pin touches the middle of the ball or lead [9].

In manufacturing the contacting object can vary between a solid metal block to a tester pogo pin with tens of centimetres cable length.

To analyse fast ESD events, the main interest in charged device ESD is a serial inductance below 20 nH, in which case the pulse rise time is typically

shorter than 1 ns and the peak current the highest. Therefore, the inductance L_{pogo} in Figure 2 is varied between 4 nH and 16 nH, when the capacitance C_{DUT} is varied between 2 pF and 60 pF. The simulated peak current and rise time values are shown in Figure 4 with 250 V charging voltage and with 25 Ω spark resistance. The increasing inductance L_{pogo} decreases the peak current and slows down the pulse rise time, as expected.

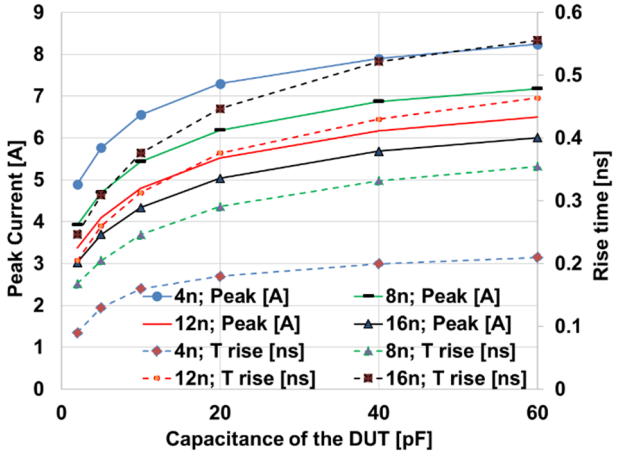

Figure 4: The CDM peak current and rise time with a four pogo pin inductances.

c) Capacitance of the pogo pin and capacitive coupling of product parts

Electrical circuit, spacing and dimensions of conductive and dielectric layers defines the ESD source capacitance of the DUT in a charged device event [13][21]. In a CDM tester, the reported CDM withstand voltage varies up to a factor of three with the same silicon chip when the capacitance of the package is changed. According to Jahanzeb [17], the peak current increases monotonically for small packages and then saturates for sizes larger than 1000 mm^2. Figure 4 and 5 presents the typical simulated peak current and rise time curves when the capacitance of the DUT increases in a FICDM tester. This is a similar result as reported in other publications [1][5][9][16][21][26].

In a FICDM tester, the IC is charged by induction and the induced voltage follows closely the potential of the field plate. The ground reference plane is kept at several millimetres distance from the IC, thus, the capacitive coupling between the ground plane, field plate, pogo pin, and the IC is limited by the tester construction [21]. The capacitance of the pogo pin C_{pogo} increases when the ground plane and pogo pin approaches the DUT.

The C_{pogo} is typically a small value around a few picofarads and is simulated here with two values; 2 pF and 4 pF. The simulated peak current and rise time are shown in Figure 5. Here the peak current and rise time changes less than 10 % when the C_{DUT} increases from 2 pF up to 4 pF.

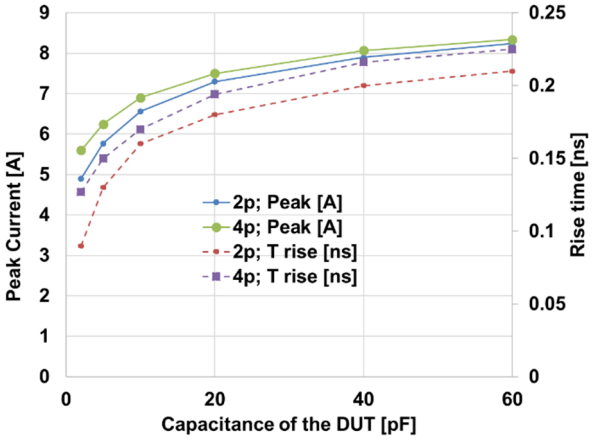

Figure 5: The CDM peak current and rise time with two IC to pogo pin capacitances.

When the contacting object is not a sharp pogo pin, but a parallel conductive surface, the charged device event can change significantly [7][26]. In that case the capacitance increases between the isolated charged object and the approaching surface, thus, decreasing the voltage difference between the objects according to the equation $V = \frac{Q}{C}$, with the charge Q constant. There can be a discharge when the objects move close to each other and an electrostatic field strength exceeds the electrostatic field breakdown limit, typically around 3 MV/m. Before discharge, the voltage difference can decrease to hundreds or tens of volts depending on the shape and capacitance of the objects, even for an initial voltage in kilovolt range.

Figure 6 shows an example simulated discharge scenario with a land grid array (LGA) package as it approaches a surface of a PCB in a placement equipment. The voltage V_{CDM} is the voltage difference between the IC and PCB, V_{ESDS} is the potential of the IC, V_{PCB} is the potential of the electrically floating circuit board, and the *Field* is the electrostatic field between the IC and the PCB. The example and calculation bases on equations presented in the reference [7]. Here the initial capacitance of the PCB is 30 pF, the capacitance of the IC is 4 pF, and the initial charge of the IC is 6.5 nC.

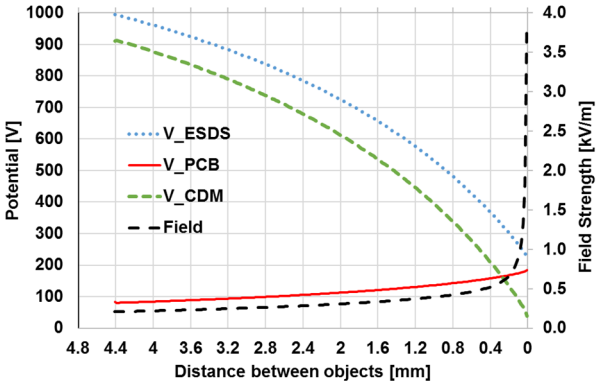

Figure 6: LGA package assembled on a grounded PCB.

In the calculated example case, the discharge is not destructive due to a low voltage and energy content at the moment of the discharge event. Therefore, the initial voltage or charge of a charged electrostatic discharge sensitive device (ESDS) cannot specify the level of ESD risks without information how the ESDS is contacted in the process and how device capacitance affects the potential difference at the time of contact.

d) Capacitance of the field and ground plates

In a charged device ESD event, the ground or field plate represents one reference voltage plane and the optional ground plate above the DUT, such as in a FICDM tester or in a component placement equipment, is the second ground reference.

In a CDM tester the field plate is connected to a high voltage source via a serial resistor. This resistor is typically 1 GΩ and electrically isolates the field plate during a fast ESD event [10]. When the DUT is grounded by the pogo pin, it increases the capacitance of the field plate and momentary pulls down the potential of the plate. This voltage drop can be calculated when the capacitance of the DUT and field plate are known [7][20][21][26]. The field plate charges back up to the set voltage level in a few tens of milliseconds after the discharge event according to the RC time constant. During a short CDM event the changing voltage attenuates the ESD stress level. The level of this attenuation is simulated with two capacitance $C_{\text{fieldplate}}$ values in Figure 7.

35 pF ± 10 pF is a typical measured field plate capacitance in CDM testers [18]. 108 pF capacitance simulates a scenario where DUT is close to a large capacitance ground reference in manufacturing.

As predicted, with a larger capacitance $C_{\text{fieldplate}}$, the peak current increases and the rise time decreases. The difference of the peak current can be 10 % and the rise time can vary 20 % with large size DUTs.

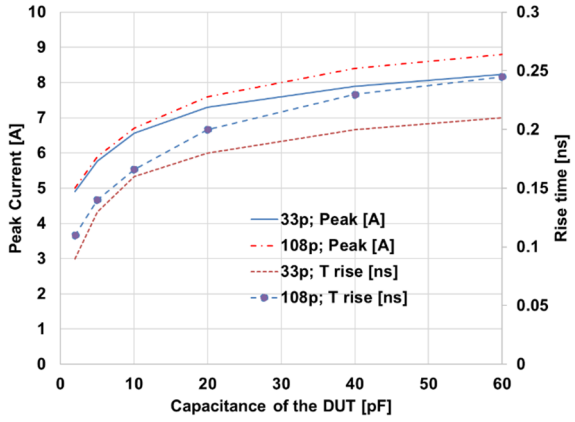

Figure 7: The CDM peak current and rise time with two field plate capacitances.

Similarly, as presented by Goëau et.al [10] the ground plate capacitance C_{GP} affects the peak current and rise time. The ground plane can be from 4 mm to 10 mm distance from the dielectric of the field plate; FICDM standards do not specify this dimension as the pogo pin length is compensated in a tester calibration phase [1]. Based on simulations and measurements, the peak current increases with higher ground plane capacitances. A C_{GP} variation from 13 pF to 33 pF is responsible of a variation of +11 % of the peak current for the 4 pF module. For the 30 pF module, the variation is +17 %.

The size of the ground plane affects also the initial part of the transferred charge. This is shown in Figure 8 where two CDM test heads with 60 mm × 60 mm (A) and 60 mm × 80 mm (B) size ground planes are used to discharge a charged mobile phone PCB on a 108 pF field plate. The peak current is closely the same in both events as PCB parasitics limits current flow. The pulse rise time is in both discharges 0.5 ns due to the same source capacitances and inductances. Here the initial charge transfer increases with the larger size discharge head and increases risks of energy based failures. However, the total transferred charge is the same after 50 ns in both cases.

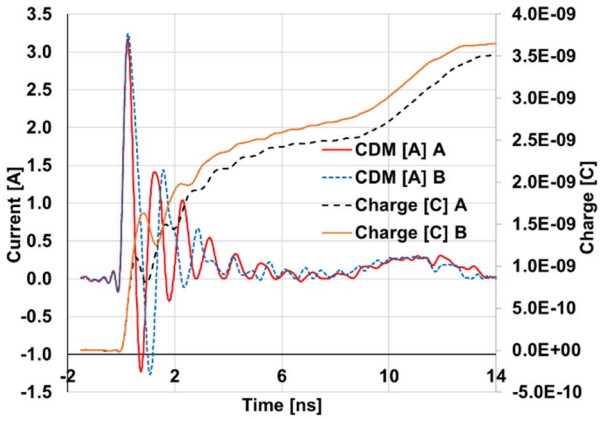

Figure 8: Charged board discharges measured with two different size CDM test heads from a PCB ground plane.

The ground plate capacitance C_{GP} can be a small value in real world charged device ESD events. For example, placing a charged DUT on a PCB with a dissipative nozzle may limit the capacitance C_{GP} below one picofarad. In this case the capacitance of the field plate $C_{\text{fieldplate}}$ defines the capacitive environment before a physical contact.

e) Summary of the parameter study

Table 1 presents a summary of the five parameters used with charged device ESD event sensitivity analysis. Here the peak current is the reference value to follow. The values in the table represents typical observed parameter values and may change based on the discharge setup. In addition, parameter variations can be in most cases both positive and negative, thus increase or decrease the ESD stress level.

The analysis shows the biggest change in peak current occurs due to the capacitance change between the DUT and the ground. A series inductance along the discharge path is the second most influential parameter affecting the peak current, and is the most influential parameter on pulse rise time changes. When increasing inductance up to a 100 nH can slow down the rise time from 200 ps to a few nanoseconds. In addition, varying air spark resistances can significantly change both the peak current and rise time.

Table 1. Summary of the observed CDM peak current variations with varying discharge parameters.

		Estimated values in a CDM tester	Values in process Min	Values in process Max	Observed peak current variation
Air spark resistance	[Ω]	25	10	100	1.5x
Capacitively Coupling	[pF]	3	1	>100	100x
DUT capacitance	[pF]	10	2	30	2.5x
Serial inductance	[nH]	6	4	>200	5x
Field plate capacitance	[pF]	33	5	>1000	1.2x
Ground plate capacitance	[pF]	17	5	>1000	1.2x

C. Discharges from DUTs with multiple conductive elements

Electrical components can have a metallic heat sink on the top or bottom of the package. This conductor can be directly grounded via some of the I/O connections or it can be electrically floating. However, there can be a resistive connection or a capacitive coupling from the conductor via the die during a high voltage CDM event. In that case, the CDM current waveform consists of several pulses summed together as shown in Figure 9. Here the CDM event is measured from a 35 mm × 35 mm processor component with a heat sink by using 500 V initial voltage with a total 20 nC charge transfer. During the initial part of the discharge, the charge of the I/O conductor, wire bond, and the die discharges and forms a pulse with 11.5 A peak current. From three nanoseconds forward there is a residual pulse with less than one ampere current slowly decaying down to zero within around 30 ns.

The measured current waveform is simulated with three parallel *RLC* circuits with the parameters shown in Table 2. The purpose of the simulation is to get more detailed information of the energy and power in each phase of the discharge. Here the first underdamped circuit forms the CDM main current pulse, and the second circuit forms ringing during the initial part of the event. The third overdamped circuit models the residual pulse from the heat sink with a decaying current waveform.

Table 2. RLC parameter values for the discharge simulations used in Figures 9 and 10.

Underdamped1			Underdamped2			Overdamped		
R_1	C_1	L_1	R_1	C_2	L_2	R_3	C_3	L_3
25	6	5.8	50	0.5	50	310	34	200
Ω	pF	nH	Ω	pF	nH	Ω	pF	nH

The model predicts well the initial peak current and has a reasonable approximation with the residual pulse. Here the varying spark resistance and reflections with the measurement setup add uncertainties. Based on the simulated values, the source of the initial CDM peak is a 6 pF capacitance with a typical air spark serial resistance of 25 Ω. The residual pulse has more charge due to the 34 pF source capacitance and has a higher serial resistance 310 Ω, and 200 nH inductance.

Figure 10 presents the calculated total power and energy plots of the *RLC* circuits. The CDM peak current gives about 2500 W peak power within the first nanosecond and can damage the die due to the thermal power. In addition, the 190 ps pulse rise time can induce an excess voltage over the sensitive parts of the die. However, about 60 % of the total energy of the pulse is released after the first three nanoseconds. Therefore, energy sensitive ICs can fail due to the excess energy released during the residual pulse.

There are uncertainties related to the calculation of the discharge power and energy. The power depends on the serial resistance R and current I as $P(t) = I(t)^2 R$, and the energy is a time integral of the power $E = \int_a^b P(t)dt$. However, when the source circuit consists of several parallel *RLC* source circuits the energy transfers into heat in different parts of the discharge path.

During the initial fast ESD pulse, most of the energy transfers into heat in the air spark, thus, only part of the energy heats the die structures. However, the voltage over the IC is related to the internal inductance L of the die structures and the rise time of the current. This voltage is not directly related to the total discharge power or energy, but the severity of the voltage breakdown damage on the die depends on the available total power and energy. Therefore, high power and energy discharges can produce more severe damages, such as oxide breakdown failures, when the total available charge increases. Respectively, discharges with a low transferred charge, peak power, and energy content may not damage the die event the current rise time would be fast [27].

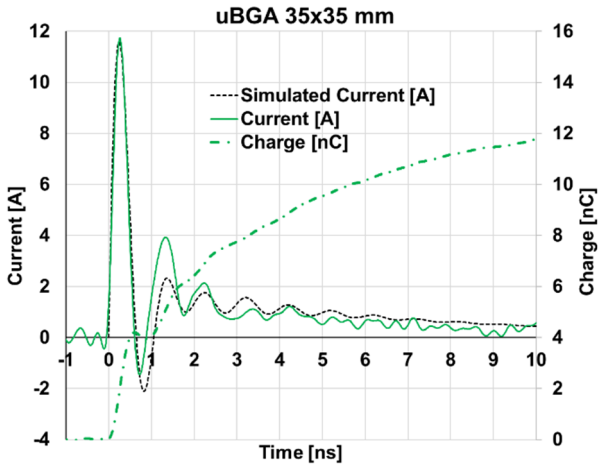

Figure 9: The measured and simulated current waveforms and an initial part of the integrated transferred charge.

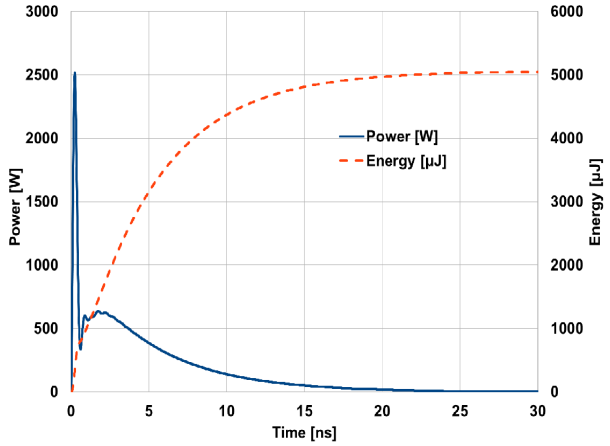

Figure 10: The calculated total power and energy based on the simulated discharge waveform in Figure 9.

During the residual pulse, the series resistance is higher, but the exact location of the resistance may not be known. The energy may not heat the die itself if the resistance is along the heat sink and die connection. In that case, the energy content of the pulse has less effect on ESD damage risks. This can make it challenging to estimate real ESD risks in electronics handling even if discharge source parameters, such as the initial potential difference and stored charge are known.

D. Orientation of the DUT on the ground reference plane

The total capacitance of the IC in a CDM event depends on the package type, design, and size [9]. Large size packages have typically the highest capacitance and a higher peak current in a CDM tester, but if the IC has a large metal layer close to the top or bottom surface of the package, the capacitance can vary depending the way the IC has been set on a ground reference plane. This apply also to other charged device ESD events with varying conductive elements around the device.

In a CDM tester, the IC is always placed with electrical contacts upwards. However, in a backend and assembly environment ICs can be handled also leads up or downwards, and the device can be surrounded by conductive elements. This will affect the charged device ESD event as shown in Figure 11, where the package has a solid 25 mm × 25 mm size conductive plane on top of the package. Here the measured discharge waveforms are from an RF power amplifier IC with a heat sink. From the integrated charge we can see that the device capacitance is about 2.5 times higher when the device is positioned leads down on the field plate in comparison to a CDM qualification. With the tested 20 different ICs the CDM peak current varies maximum 2.5 times higher or lower when the IC is placed in different positions on the field plate.

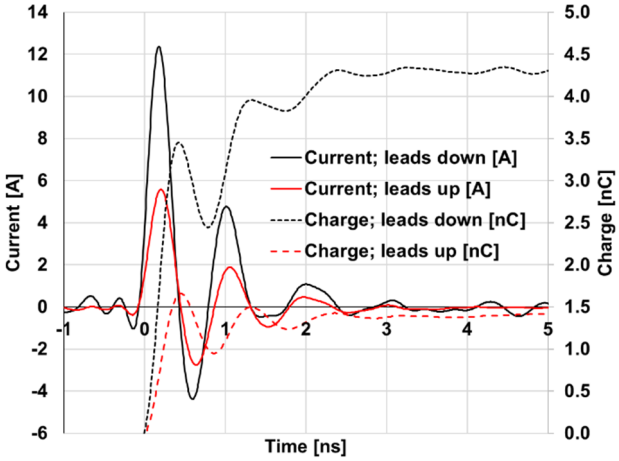

Figure 11: The measured current and integrated charge waveforms whem the IC is leads downwards and upwards on a CDM test bench.

E. Discharges from charged metal objects

It is known that large size charged metal objects contacting PCBs or ICs can initiate discharges with a high initial peak current and energy content [3][4][6][20][26]. In addition, small charged metal objects, such as a few millimetres long metallic wires with less than 1 pF capacitance, can initiate severe ESD events [28]. These small conductive objects can get static charges during handling and discharge on other electronic parts, such as on a PCB board, during electronics assembly phase. The discharge current waveform can have less than 50 ps rise time and several amperes peak current.

The rise time of the pulse can be faster than any on-chip or on-board ESD protection device has been characterized for when the characterization is made with the component package. In this case, the measured voltages in the process area should not be compared to CDM withstand voltages of ICs.

IV. Discussion

Charged device ESD events are complicated to measure and control. To help with the ESD control, component qualification should produce useful information for both system designers and ESD control teams in manufacturing to design and build up optimal ESD protection. Currently, the standardized CDM qualification methods does not fulfill this target.

Previously, there has been proposals to use for example 50 % extra safety margin when assessing charged device type ESD risks in electronics handling based on the measured DUT voltages. However, the CDM qualification is not always the worst case charged device ESD scenario.

In electronics manufacturing DUTs can have both higher or lower stored charges with the same voltage, thus, the peak current and pulse rise time can be several times higher or lower. Similarly, the total transferred charge may flow through one I/O or group of I/Os, thus, the amount of charge may not explain ESD risks in details. Therefore, any quasi-static measurement method, such as static voltage or charge measurement, cannot predict the shape and stress level of the realized ESD event in varying environments.

The main challenge with CDM qualification is that it defines ESD stress levels by using a single voltage parameter when the DUT is in a specific test environment. In addition, real world charged device events have so much variation that it is challenging to try to repeat discharge events in detail by using one fixed test setup. Instead, it would be more beneficial to report the most critical discharge parameters leading to failures.

One option to improve the current situation with CDM qualification would be to focus more on the stress parameters. Here the real component failure parameters; discharge peak current and pulse rise time with a specific voltage, would be the reported ESD sensitivity values for each tested I/O. In parallel, the total transferred charge information would be useful for ESD risk analysis in manufacturing.

In addition, there could be alternative methods to qualify and measure the maximum peak current and rise time values. One option would be to use test methods based on transmission line pulse (TLP). The rise time, peak amplitude, and total charge of the current waveform could be extracted from the TLP waveforms. In a TLP test the component package or air spark have less effect on the test results, thus, the results would be more accurate than obtained with current CDM testers.

The maximum allowed peak current and rise time data would be also useful information for system designers as maximum absolute rating data (AMR) [27]. The system level protection could be designed by using co-design concepts where the on-board parasitics, on-board protection devices, and the DUT sensitivity would be matched to each other.

To evaluate more accurately charged device ESD risks in manufacturing, the type of discharge contact, level of charges, capacitive coupling, and discharge path *RLC* parameters need to be analyzed in details. Here the discharge current measurement with different current probes and tailored measurement setups could produce more information for the risk estimation. Still the measured current waveform may not be the same as found in the real ESD event or the same as used in the CDM qualification. The used current measurement method affects the shape of the waveform and manual discharge tests have extra uncertainties. Discharge measurements would also require trained personnel with RF measurement skills and fast oscilloscopes, something not commonly available in manufacturing environment.

V. Conclusion

The objective of this study is to clarify what parameters in a CDM qualification affects the ESD stress level and could be used to evaluate charged device ESD type of risks in electronics handling and manufacturing.

Currently, the CDM withstand voltage is used to report the component ESD sensitivity. However, the peak current and pulse rise time are the dominant parameters defining damage thresholds with CDM discharges in a qualification tester. With CBE type of discharges the transferred energy can be an additional damage parameter.

To link to charged device ESD control, CDM qualification methods should record the charge transferred in the discharge, peak current and rise time as well as the ESD withstand voltage data. In addition, ESD control programs need have more focus on discharge current, DUT voltage, and charge control when ICs with low ESD immunity are handled. Here additional discharge current measurement methods and discharge event simulations are needed.

Acknowledgements

This research has been conducted under the ESD Research Council (ERC) project “Practical current and charge measurements of CDM type discharges in Electrostatic Discharge Protected Areas (EPAs)”, funded by Electrostatic Discharge Association (ESDA), Cisco, and Global Foundries.

References

[1] For Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Device Level, ANSI/ESDA/JEDEC JS-002-2014, 2014.

[2] Steinman A., Maloney T., "Measuring Handler CDM Stress Provides Guidance for Factory Static Controls", Proc. EOS/ESD Symposium 2014, 62–67.

[3] Gärtner R, Stadler W., Niemesheim J., Hilbricht O., "Do Devices on PCBs Really See a Higher CDM-like ESD Risk?", Proc. EOS/ESD Symposium 2014, 231–238.

[4] Steinman A., "Equipment ESD Capability Measure-ments", Proc. EOS/ESD Symposium 2014, 64–71.

[5] Sarro J., Reynolds B., Gauthier R., "Influence of Package Parasitic Elements on CDM Stress", Proc. EOS/ESD Symposium 2013, 407–415.

[6] Steinman A., "Process ESD Capability Measurements", Proc. EOS/ESD Symposium 2012, 111–119.

[7] Tamminen, P.,Viheriakoski T., "Characterization of ESD risks in an assembly process by using component-level CDM withstand voltage", Proc. EOS/ESD Symposium 2007, 202–211.

[8] Maloney T., "CDM Tester Properties as Deduced from Waveforms", IEEE Transactions, 2014, (Volume:14 , Issue: 3) TDMR-2014-01-0010-SS.

[9] T. Brodbeck, A. Kagerer, "Influence of the Device Package on the Results of CDM Tests – Consequen-ces for Tester Characterization and Test Procedure," Proc. EOS/ESD Symposium 1998, 320–327.

[10] Goëau C., Richier C., Salomé P., Chante J-P., Jaouen H., "Impact of the CDM tester ground plane capacitance on the DUT stress level", Proc. EOS/ESD Symposium 2005, 170–177.

[11] Ashton R., "Simulating Small Device CDM Using Spice", InCompliance Magazine, 2010, August 10th, Web page accessed 8/2016; http://incompliancemag.com/article/simulating-small-device-cdm-using-spice/

[12] Steinman A., et al., "Measurements to Establish Process ESD Compatibility", Proc. EOS/ESD Symposium 2010, 225–232.

[13] Carey R. E., "An Experimental and Theoretical Consideration of Physical Design Parameters in Field-Induced Charged Device Model ESD Simulators and Their Impact Upon Measured Withstand Voltages", proc. EOS/ESD Symposium 1998, 40–53.

[14] Esmark K., Gäertner R., Seidl S., Nieden F., "Using CC-TLP to get a CDM Robustness value", Proc. EOS/ESD Symposium 2015, Paper 4B.3.

[15] Nathan J., Maloney T., "Low Impedance Contact CDM", Proc. EOS/ESD Symposium 2015, Paper 8A.2.

[16] Nathan J., "Charged device model electrostatic discharge protection and test methods for integrated circuits," Dissertation, University of Illinois at Urbana-Champaign, 2012.

[17] Jahanzeb A., Lin, Y-Y., Marum, S., Schichl, J., Duvvury, C., "CDM peak current variations and impact upon CDM performance thresholds", Proc. EOS/ESD Symposium 2007, 83–88.

[18] Given R., Hernandez M., Meuse T., "CDM2 – A New CDM Test Method for Improved Test Repeatability and Reproducibility", Proc. EOS/ESD Symposium 2010, 359–368.

[19] Maloney T., "Easy Access to Pulsed Hertzian Dipole Fields Through Pole-Zero Treatment", EMC Society Newsletter, Issue no 230, IEEE, 2011.

[20] ESD Association Technical Report For Electrostatic Discharge Sensitivity Testing – Charged Board Event (CBE) ESD, TR25.0-01-16, 2016

[21] Industry Council on ESD Target Levels. (2009, Mar.). White Paper 2: A case for lowering component level CDM ESD specifications and requirements. https://www.esda.org/assets/Uploads/documents/White-Paper-2-A-Case-for-Lowering-Component-Level-CDM-ESD-Specifications.pdf, accessed last time Feb. 2017.

[22] Jiang Xiao, et al., "Model of Secondary ESD for a Portable Electronic Product", IEEE Transactions on Electromagnetic Compatibility, vol. 54, no. 3, June 2012.

[23] ESD Technology Roadmap, EOS/ESD Association, https://www.esda.org/assets/Uploads/docs/2016ESDATechnologyRoadmap.pdf, accessed last time Feb. 2017.

[24] Satoshi Isofuku, "Voltage Dependence of Spark Resistance at Low Voltage ESD in Air and Reed Switch", Proc. EOS/ESD Symposium 2006, 266–273.

[25] Nathan J., Rosembaum E., "Comparing FICDM and Wafer-Level CDM Test Methods: Apples to Oran-ges?", Proc. EOS/ESD Symposium 2012, 231–239.

[26] Tamminen P., "Optimization of ESD protection methods in electronics assembly based on process and product specific risks", Dissertation, Publication 1439, ISBN 978-952-15-3858-2, Tampere University of Technology, 2016.

[27] Industry Council on ESD Target Levels. (2016, Apr.) White Paper 4 - Understanding Electrical Overstress – EOS, accessed last time Feb. 2017. http://www.esdindustrycouncil.org/ic/en/documents/40-white-paper-4-elecrical-overstress

[28] Tamminen P., Fung R., Wong R., "Charged device ESD threads with high speed RF interfaces", Proc. EOS/ESD Symposium 2017, Paper 3A.2.

[29] Tamminen P., Smallwood J., Stadler W., "Charged device discharge measurement methods in electronics manufacturing", Proc. EOS/ESD Symposium 2017, Paper 1B.4.