DNW-Controllable Triggered Voltage of the Integrated Diode Triggered SCR (IDT-SCR) ESD Protection Device

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Abstract – A novel Integrated Diode Triggered SCR (IDT-SCR), with low capacitance (<200fF), and a controllable V_{T1} is proposed for 1.8V application. The triggering is determined by the DNW biasing plus one integrated diode. The fail-current density is 16 times higher, and leakage 20 times lower, compared to a traditional capacitive-triggered bigFET.

I. Introduction

Low capacitance, low leakage and robustness ESD/Surge requirements are getting more and more important for USB3-like high speed products in low voltage power domain. Silicon Controlled Rectifiers (SCRs) are one of the most efficient candidates compared to other solutions [1-5]. However, SCRs usually have some drawbacks, such as higher trigger voltage (V_{T1}), poor reaction speed (longer turn-on time and voltage overshoot) under transient events (1ns VF-TLP) and potential latch-up concern. The diode-triggered SCR (DTSCR) offers design flexibility for a range of different I/O voltage requirements due to its tunable trigger/holding voltages [6-10]. In addition, [11] proposed a controllable V_{T1} back-biased SCR device. However, this concept can only be used in SOI processes, not in bulk CMOS. This paper introduces a novel V_{T1} controllable integrated diode triggered SCR (IDT-SCR) [12]. Its V_{T1} is controlled by DNW-biasing and combines adequate condition against unpowered (HBM/CDM events) and powered (System-level ESD/Surge events) with false trigger immunity. There is only one diode integrated for a various I/O range (1.8V-5V) requirements than the traditional DTSCR. Section II shows the ESD fundamental ESD challenges for protecting low voltage transistors with SCR-based solutions especially for low capacitance, low leakage and robustness ESD/Surge requirements. Section III presents the device topology, the TCAD results and the silicon characterization results to demonstrate the current conduction mechanism of the new IDT-SCR. Multiple applications with the novel IDT-SCR will be presented in section IV. Further device optimization with TLP characteristics will be presented in section V. The paper finishes with a discussion and conclusions in section VI.

II. ESD Challenges for Protecting Low Voltage (1.8V) Transistors

A 1.8V low voltage ESD strategy with a 50µm wide Lateral Silicon Controlled Rectifiers (LSCR) ESD device for a low capacitance, low leakage and robust ESD/Surge requirement is shown in Figure 1: . To estimate ESD robustness in output mode, the Safe Operation Area of a 1.8V NMOS (Mn1) needs to be characterized [13]. On the other side, the gate-oxide failure voltage of a 1.8V Mn2 is a critical target in the input mode. 100ns (10ns rise time) TLP characteristic of the 1.8V ESD strategy with a LSCR ESD device combined with the failure voltage of the Mn1 and Mn2 is sown in Figure 2. The last data point is the point right before hard failure for a 50µm wide LSCR ESD device. It is clear that the trigger voltage (V_{T1}) of the LSCR ESD device is too high to protect the transistors Mn1 and Mn2 in both output and input modes, respectively. Besides, latch-up problem due to the holding voltage (V_H) is lower than 1.8V.

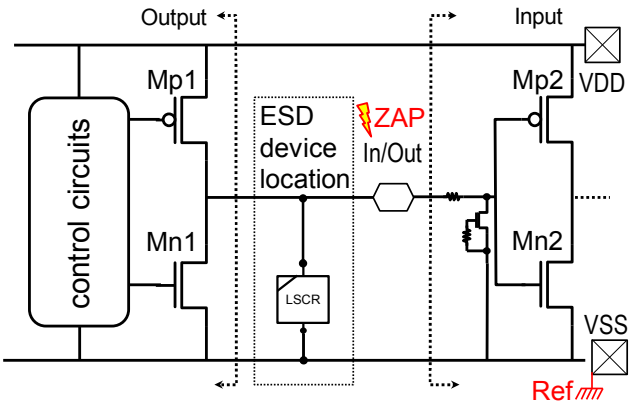

Figure 1: A 1.8V low voltage ESD strategy with a 50µm wide LSCR ESD protection device.

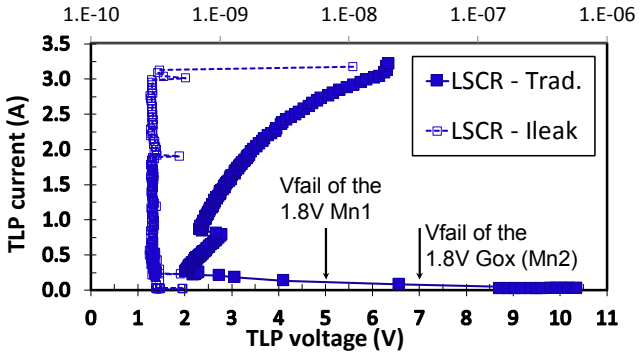

Figure 2: A corresponding 100ns (10ns rise tine) TLP characteristic of the 1.8V ESD strategy with a LSCR ESD device.

Stacking SCR-based ESD devices is a common way to increase V_H for latch-up safety. As a result, the trade-off is the V_{T1} will be also increased.

III. IDT-SCR ESD Device

This section presents the device topology, the TCAD and silicon characterization results to demonstrate the current conduction mechanism of the new IDT-SCR.

A. Topology

By adding an extra DNW layer underneath the traditional LVTSCR which is shown in Figure 3(a), the novel IDT-SCR is created, as shown Figure 3Figure 3: (b). The corresponding cross-sectional views from X-X' are shown in the Figure 3(c) and Figure 3Figure 3: (d) respectively. A 5V floating-base gg-NMOS [14] was used to reduce the leakage, capacitance and V_{T1}. Active P+ segment layout style [15] was used to increase V_H. Asymmetric PN space (d2 is twice larger than d1) was used in this case. The advantages of the DNW layer are:

- Enhanced latch-up immunity by proper DNW biasing conditions with nearby circuitry (e.g. a 1.8V/3.3V dual power domains chip).
- Creation of a dedicated integrated forward diode from P_PN_{NDRIFT}/N_{DNW} which, combined with a proper biased DNW, presents a new controllable triggering mechanism.
- Low capacitance for the signal pin: The largest part of the capacitance from the DNW to the substrate is connected to the power supply instead of the signal pins with a biased DNW.
- Multiple applications for different ESD/Latch-up specifications can be achieved with different DNW biasing which will be shown in Figure 14(a) and Figure 14(b) respectively.

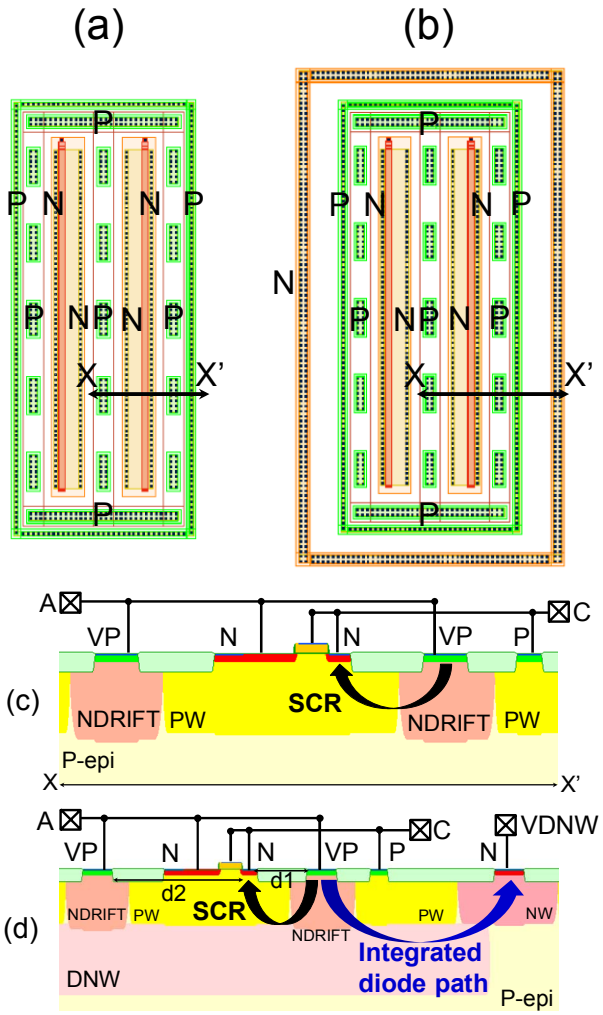

Figure 3: (a) The layout view of the traditional LVTSCR and (b) IDT-SCR, the corresponding X-section in (c) and (d) respectively.

B. TCAD analysis

2D-TCAD simulation was used to demonstrate the ESD conduction mechanisms of the new IDT-SCR The set-up is similar to the X-section in Figure 3(d). Figure 4 shows the overall current distribution of the device after triggering, for three different biases of the DNW-terminal. The currents I_A and I_C are nearly symmetric, implying that the DNW-terminal carries very little current. In fact, at 10mA/μm the DNW terminal current is only a few percent of the total current for all three bias cases. This is in spite of the fact that the DNW terminal bias is defined as a fixed, ideal voltage source. Furthermore, the device current is similar for all three DNW-biases after the device has triggered. Both observations are consistent with SCR action.

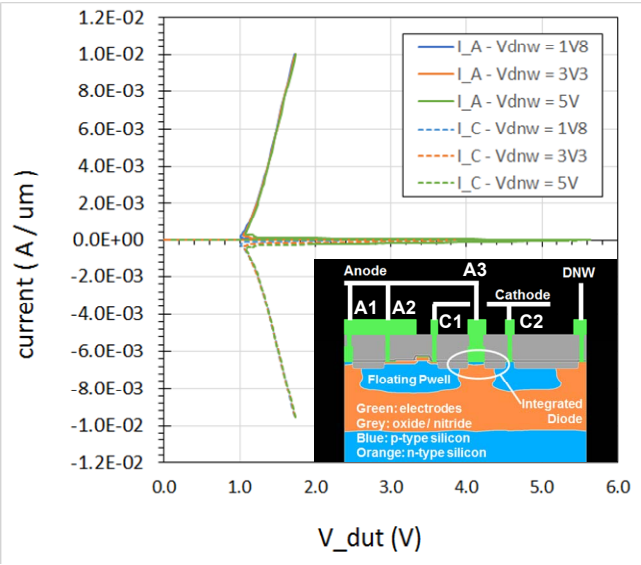

Figure 4: Simulated device current (A/µm) for 3 different biases (1.8 V, 3.3 V, 5.0 V) of the isolating deep nwell. Inset: Simulation structure. The A-terminal consists of three contacts (A1, A2, A3), the C-terminal consists of two (C1 and C2) and the DNW-terminal consists of just one contact (DNW).

Figure 5 shows the triggering behavior in more detail. From Figure 5(a) it is evident that the device triggers when the potential on the A-terminal exceeds that of the DNW-terminal by one diode voltage drop. When the bias potential of Anode terminal is lower than this threshold no significant currents flow in the device. When the device is triggering (point A), the internal NPN formed by the anode, floating pwell, and cathode is active as is indicated by the current flowlines between one of the cathode contacts and the DNW contact shown in Figure 5(b). This current, however, is not yet sufficient to put the internal SCR in a self-baised state. At higher current (point B) the SCR does trigger as indicated by the flowlines between one of the Anode contacts and one of the Cathode contacts shown in Figure 5(c), as well as by the very low operating voltage (1.3 V).

It is very common for SCR's to have an embedded gg-NMOS as trigger device. The SCR discussed in this paper has one, too. However, the fact that the pwell serving as body of this gg-NMOS has no explicit terminal, and is therefore electrically floating, means that the NPN between the Cathode, the floating pwell, and the DNW diffusion triggers before the gg-NMOS goes into breakdown via impact ionization at its drain. The embedded gg-NMOS is therefore redundant in this device. It is, however, kept in the simulation structure to preserve consistency with the silicon test structures that have the same embedded gg-NMOS.

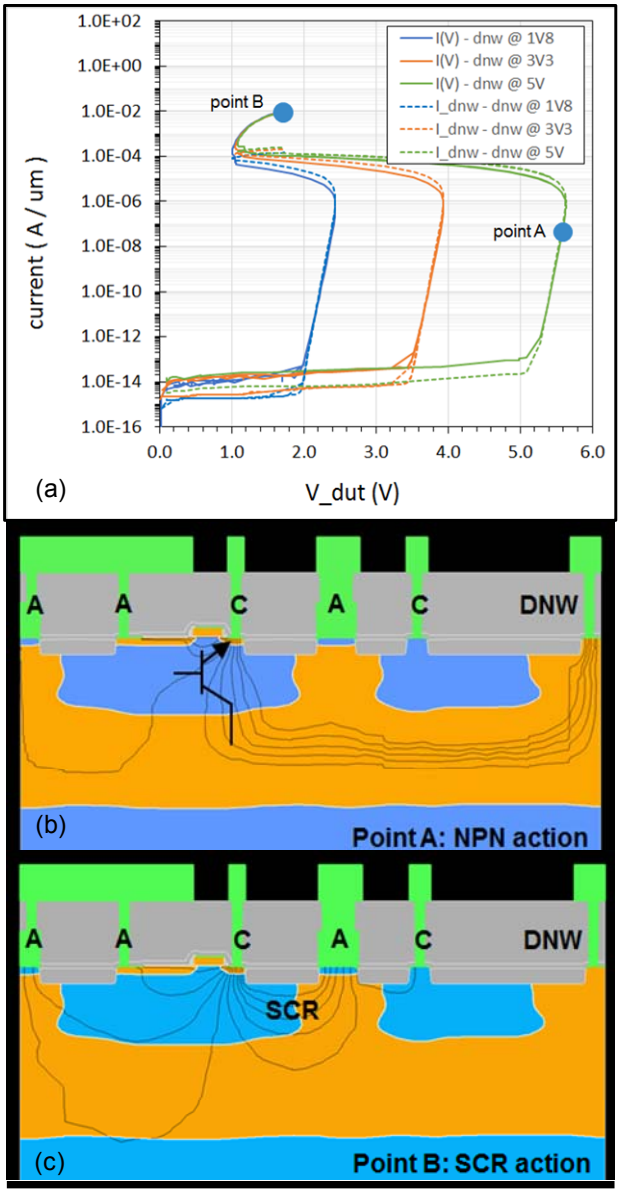

Figure 5: (a) Simulated device current on logarithmic scale showing triggering behavior. The triggering voltage is equal to the DNW bias voltage plus one forward diode voltage drop. (b) Internal current flowlines when the device is in breakdown that precedes triggering (Point A). The dominant current path is NPN current from the DNW-terminal to one of the Cathode terminals. (c) Internal current flowlines when the device is fully triggered (Point B). The dominant current path is SCR current from one of the Anode terminals to one of the Cathode terminals.

As confirmation that the embedded gg-NMOS is not essential for device triggering in this device, Figure 6 shows the I-V characteristic of the IDT-SCR device with the gg-NMOS (MOS-based) and without the gg-NMOS (STI-based). Both curves are taken with 1.8 V biasing condition on the DNW terminal. Although the curves show a difference in R-on, the triggering behavior is identical in both devices. This confirms that the gg-NMOS does not determine device triggering. Removing the gg-NMOS from the device

may be attractive in several ways: it would allow further capacitance reduction as well as further area reduction, and it could potentially improve device reliability as there is no longer a gate oxide presented.

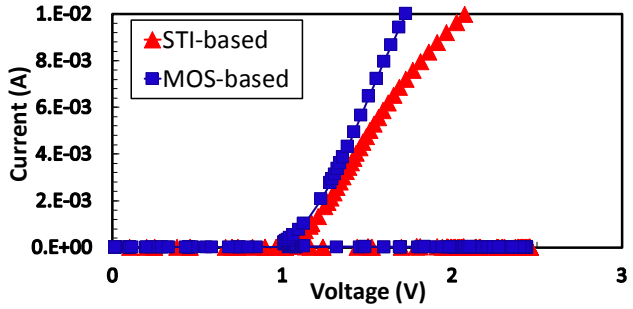

Figure 6: A TCAD I-V characteristic of the IDT-SCR with the gg-NMOS and without gg-NMOS in a 1.8V DNW biasing.

The effect of the floating PW on device triggering is shown in Figure 7. The cross-sectional views of the TCAD simulation setup files are shown in Figure 7(a) (floating PW) and 7(b) (non-floating PW). The PW region in Figure 7(a) was made floating by connecting its terminal to the reference node (0V) through a 1 Mohm resistor. For this comparison, the IDT-SCR without embedded gg-NMOS was used (STI-based device). In the I-V curves shown in Figure 7(c) it is evident that the V_{T1} of the non-floating PW variant is much higher. Close inspection of Figure 7(c) reveals that also the trigger current is much larger in the non-floating PW device. The explanation for these differences is that in the non-floating PW device, the NPN formed by Cathode/PW/Ndrift, which forms one half of the SCR, needs a much larger base current to bias itself. This base current is supplied by the PNP formed by Anode/Ndrift/PW.

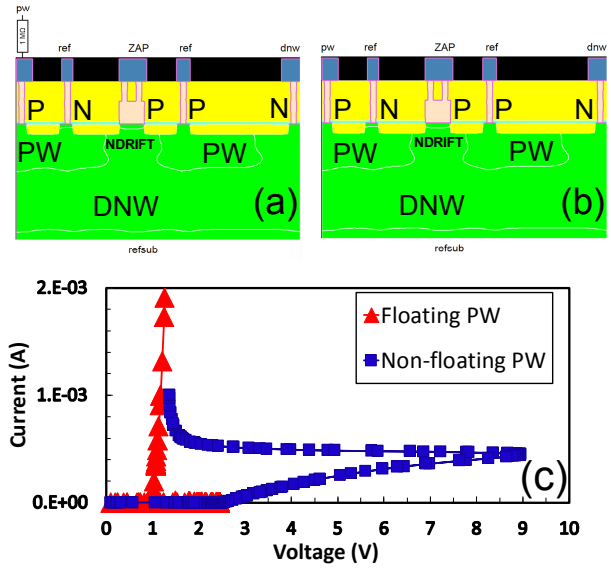

Figure 7: X-section of the (a) floating PW, (b) non-floating PW and (c) TCAD I-V characterization result at 1.8V DNW biasing.

As the current injected by the PNP increases, so does the voltage drop inside the device as the PNP has a finite internal resistance.

C. Characterization

Figure 8 compares the 100ns TLP characteristics for a traditional LVTSCR in Figure 3(c) and an IDT-SCR with 1.8V DNW biasing and 60µm wide in Figure 3(d), respectively. The V_{T1} of an IDT-SCR ESD protection device is lower than the traditional LVTSCR ESD device with the avalanche breakdown of the of gg-NMOS. The V_H of the IDT-SCR is also lower than 1.8V, for the version shown in Figure 8 which leads to a latch-up concern.

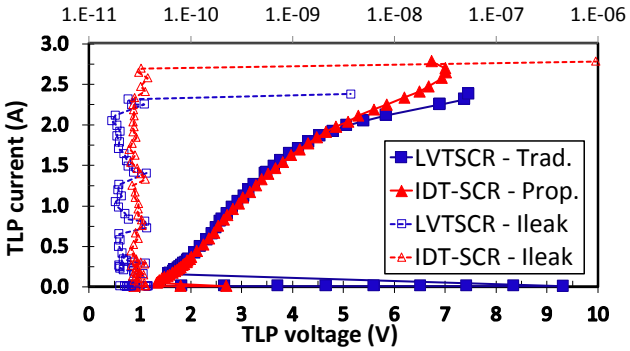

Figure 8: A 100ns (10ns rise time) TLP comparison data of a traditional LVTSCR and an IDTSCR with a 1.8V DNW biasing.

A PN space (d1=d2 with large dimension) was used to increase holding voltage (V_H) of the IDT-SCR ESD protection device for a 1.8V application. A DNW-controllable V_{T1} is demonstrated in DC and 100ns TLP characteristics in Figure 9 and Figure 10, respectively. The last data point is the point right before hard failure for a 60µm wide IDT-SCR ESD protection device.

The summary of V_{T1} and breakdown voltage (V_{BD}) regarding to different DNW biasing is shown in

Table 1. The V_{T1} and V_{BD} ~= 1Diode + DNW biasing. The final choice is application dependent.

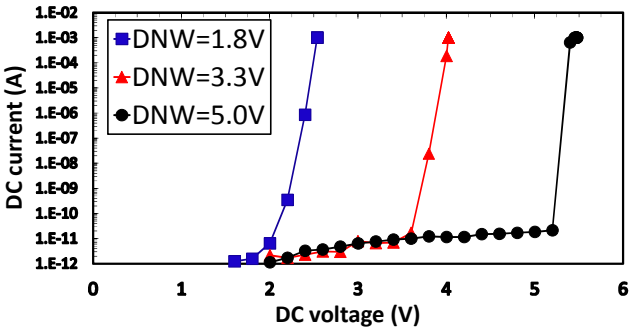

Figure 9: DC sweep of an IDT-SCR with different DNW biasing.

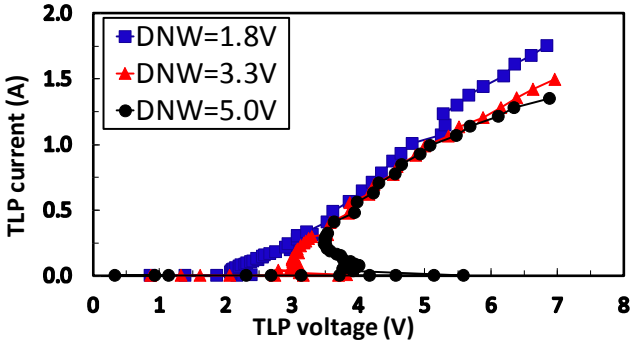

Figure 10: 100ns (10ns rise time) TLP comparison data of an IDTSCR with different DNW biasing.

Table 1: Effect of DNW biasing on V_{BD} and V_{T1} of an IDT-SCR.

DNW(V)	VBD(V)	VT1(V)
1.8	2.4	2.4
3.3	4.0	4.0
5.0	5.5	5.6

IV. Applications of IDT-SCR

This section presents multiple applications with a novel IDT-SCR ESD device in a 1.8V domain.

A. 1.8V Input/Output Pin

A simple 1.8V input/output ESD protection strategy with an IDT-SCR ESD protection device is shown in Figure 11. For the output circuitry, the worst-case failure voltage (Vfail) of a 1.8V silicided NMOS (Mn1) device is 5V under V_G=0V/1.8V. In addition, the ESD stress may happen in both powered and unpowered modes in a real world. 100ns TLP characterization data of a 1.8V output ESD strategy with the IDT-SCR ESD protection device in powered (DNW=1.8V) and unpowered (DNW=Floating) mode is shown in Figure 12. It is clear that the IDT-SCR ESD protection device can protect the transistor Mn1 up to ~1.2A for both cases before V_{fail}_Mn1=5V. DC characteristics of an IDT-SCR ESD device in different temperatures with DNW=1.8V is shown in Figure 13 to illustrate the device in latch-up testing mode. The V_H is lower than 1.8V from 50ºC to 150ºC. Stacked IDT-SCRs is one option to achieve a 1.8V latch-up safe and it will be discussed in section V. Alternative is to biased DNW to increase both the V_{T1} and V_H to achieve a latch-up immunity. Figure 14 shows the DC characteristics of (a) the V_{T1} and (b) the V_H of an IDT-SCR ESD device in different temperatures and DNW biasing variants. It is clear that both V_{T1} and V_H are higher than 1.8V with 3.3V DNW up to the 85ºC which is a requirement for most of the mobile products. The final choice is application dependent. Test structure and the corresponding capacitance characteristic of the IDT-SCR ESD protection device at 100KHz with 1.8V DNW is shown in Figure 15. A maximum capacitance included metal connection from Out pin to VSS is around 45fF at 100KHz with 1.8V DNW respectively which is compatible to a typical RF 2.4-5 GHz within 200fF [16]. The maximum capacitance from Out pin to VDD is around 27fF. Besides, the largest capacitance contribution from DNW-Psub is between VDD-VSS which is around 200fF. In this case, the critical low capacitance requirement is from Input/Output pin to VSS.

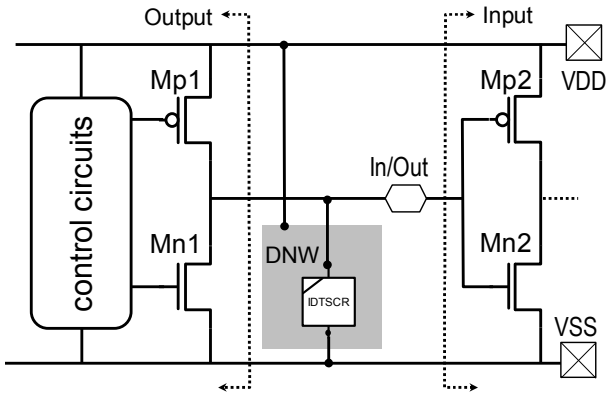

Figure 11: A 1.8V input/output pin ESD strategy with an IDT-SCR ESD protection device.

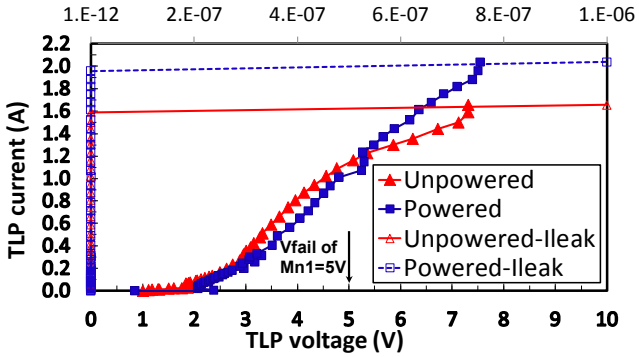

Figure 12: 100ns TLP data of a 1.8V output ESD strategy with a new IDT-SCR in powered and unpowered mode.

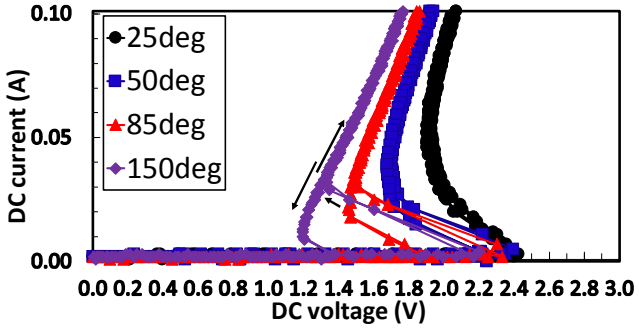

Figure 13: DC characterization data of an IDT-SCR ESD protection device in different temperatures with DNW=1.8V.

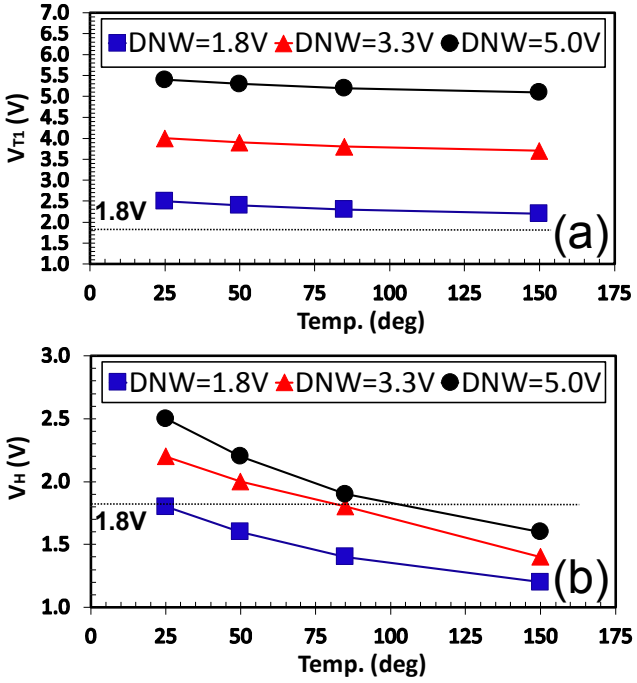

Figure 14: DC characteristic of (a) the V_{T1} and (b) the V_H of an IDT-SCR in different temperatures and DNW biasing.

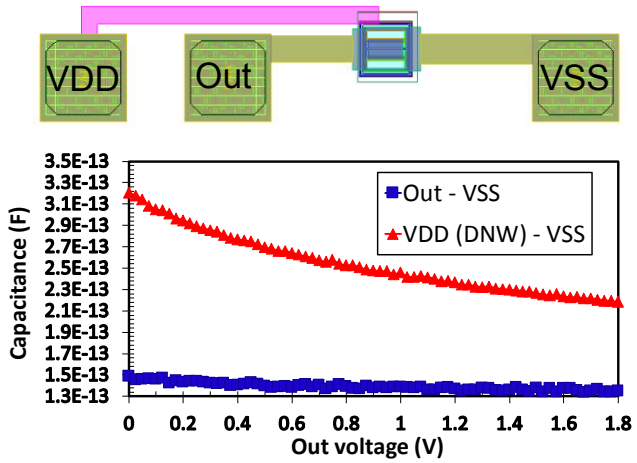

Figure 15: Test structure and the corresponding capacitance characteristic of the IDT-SCR at 100KHz with 1.8V DNW.

For the input circuitry, the target is to protect a 1.8V gate-oxide from CDM stress. 1ns VF-TLP (100ps rise-time) characteristics of an input ESD strategy with an IDT-SCR at 1.8V DNW biasing and floating DNW is shown in Figure 16. Usually the overshoot voltage during the fast transient with 100ps rise-time may kill the gate-oxide so it is better to check the voltage waveform. The corresponding voltage waveforms of the IDT-SCR ESD protection device at 0.5A, right before SCR triggered for both floating DNW and biased DNW, is shown in Figure 17. The trigger mechanism of the IDT-SCR ESD device with floating DNW (CDM event) totally depends on the intrinsic of the SCR itself. Therefore, the turn-on speed is slower and shows too much overshoot. As a result, there is a need for secondary protection.

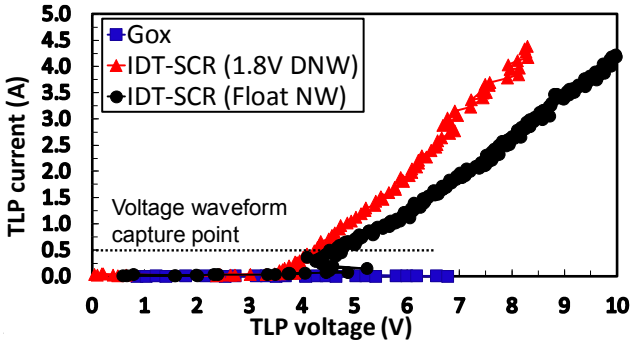

Figure 16: 1ns VF-TLP characteristic of a 1.8V input ESD strategy with a new IDT-SCR in different DNW biasing.

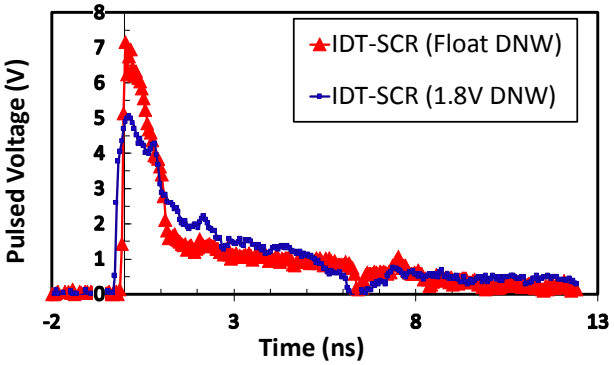

Figure 17: 1ns voltage waveform characteristic of the IDT-SCR after SCR triggered in different DNW biasing conditions.

B. 1.8V IDT-SCR ESD Supply Clamp

A capacitive-triggered IDT-SCR ESD supply clamp can be implemented by pulling down the DNW potential to VSS during a positive ESD zapping from VDD pin to VSS pin. An extra measurement is needed to prove the concept. The cross-sectional views of the two test structures are shown in Figure 18(a) DNW=0V biasing, (b) DNW through a 220Ω resistor to ground.

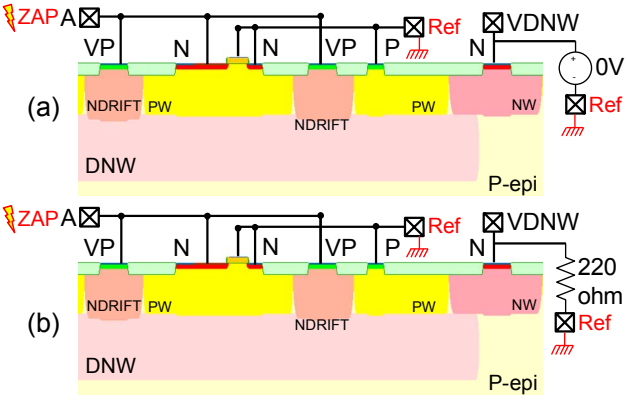

Figure 18: Test structure view of (a) DNW=0V biasing, (b) DNW through 220Ω resistor to GND.

The 100ns TLP characteristic of a positive stress from Pin A to GND (Ref) is shown in Figure 19. The compatible Ron values for both configurations show that the capacitive-triggered IDT-SCR with grounded DNW can be achieved during ESD event. The ESD current capability (I_{T2}) gap for both conditions mean that some ESD current still flows into DNW node. Further performance optimization is needed.

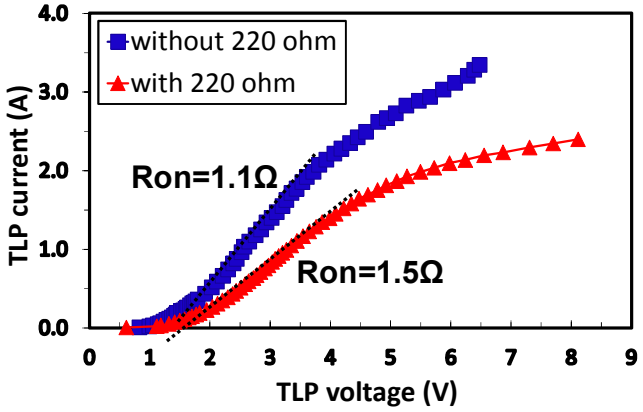

Figure 19: 100ns TLP characteristic of the IDT-SCR with (a) DNW=0V biasing, (b) DNW through 220Ω resistor to GND.

The schematic view of the traditional capacitive-triggered ESD supply-clamp and the capacitive-triggered IDT-SCR ESD supply-clamp are shown in Figure 20(a) and Figure 20(b), respectively. A PN space (d1=d2) with large dimension was used in implementing a 60µm wide capacitive-triggered IDT-SCR ESD supply-clamp. SCR does not need the holding state so the hold circuits can be removed to reduce area. A 2400µm wide 3.3V transistor, MESD, was used for a 1.8V ESD supply-clamp to achieve low leakage and better gate-oxide reliability. The corresponding 100ns TLP and leakage current at 1.8V characterization results are shown in Figure 21(a) and Figure 21(b), respectively. The failure current density of the capacitive-triggered IDT-SCR ESD supply-clamp is 16 times higher than a traditional capacitive-triggered ESD supply-clamp. Besides, the leakage current at 1.8V of the capacitive-triggered IDT-SCR ESD supply clamp is 20 times lower than a traditional capacitive-triggered ESD supply clamp. There are no any expectations such as false triggering during start-up or noise disturbance if the V_H is always larger than VDD. For instance, Figure 14(b) shows that V_H > 1.8V with 3.3V DNW until 85ºC however the power-on sequence needs to be specified clearly to avoid leakage during start-up. Alternative, Figure 24 demonstrates a cascaded IDT-SCR ESD protection device can be used as supply clamp for a 1.8V application without power-on sequence concern.

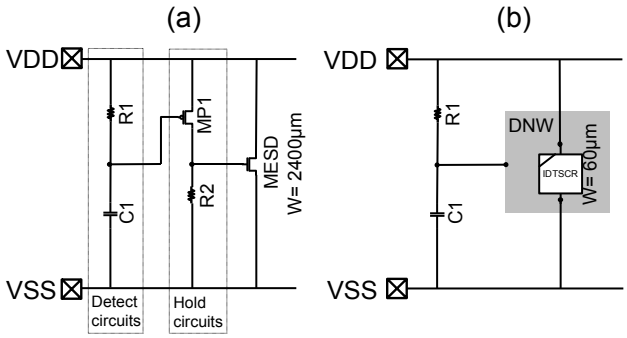

Figure 20: The schematic views of (a) traditional capacitive-triggered rail-clamp, (b) IDT-SCR supply clamp.

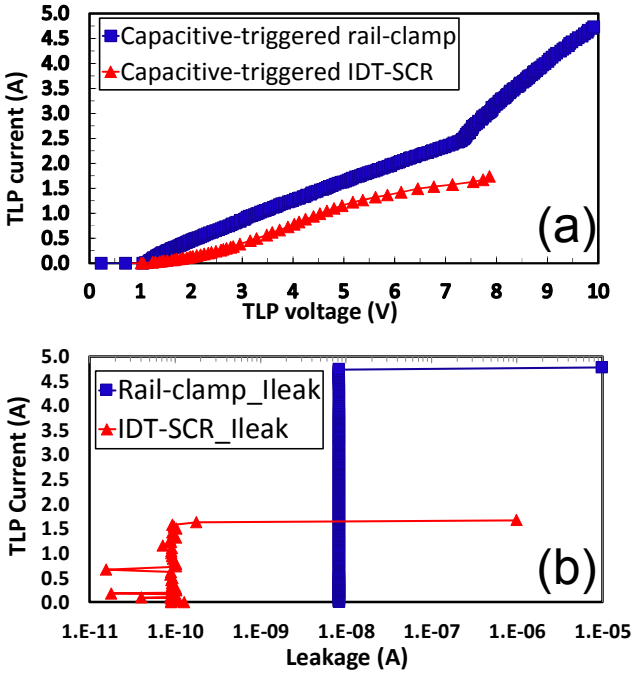

Figure 21: (a) 100ns TLP characteristic, (b) leakage current characteristic of a supply rail-clamp vs. IDT-SCR supply clamp.

V. IDT-SCR Optimization

Based on the TCAD simulation of section III.B, the trigger mechanism for both STI-based and MOS-based IDT-SCR ESD devices are compatible. 100ns TLP characteristics of the STI-based and MOS-based IDT-SCRs at 1.8V DNW biasing are shown in Figure 22. 60µm wide and non-segment active P+ stripe for I_{T2} enhancement was used for both STI-based and MOS-based IDT-SCR ESD devices. A PN space (d1=d2 with small dimension) was used for both variants. It is clear that the V_{T1} is comparable for both variants. The failure current density of the MOS-based is 70% higher than STI-based IDT-SCR. It is

due to there is another small amount SCR conduction path for the MOS-based device shown in Figure 3(c) at high current region than STI-based device. Stacking IDT-SCR ESD protection devices is a good approach to achieve latch-up immunity [17-19], further reduced capacitance, and maintain the same ESD current capability (I_{T2}). 100ns TLP characteristics of different stacked STI-based IDT-SCR ESD devices with 1.8V DNW biasing is shown in Figure 23. It is clear that the V_H increases with stacking STI-based IDT-SCR ESD devices. Besides, the ESD current capability (I_{T2}) maintains the same. Figure 24 shows DC characteristics of the V_H for different stacked STI-based IDT-SCR ESD devices in different temperatures with DNW=1.8V to illustrate the device in latch-up mode. It's clear that a 1.8V latch-up immunity application can be achieved with two stacked (2x) STI-based IDT-SCR ESD device up to 85ºC which is a requirement for most of the mobile products. For automotive products with higher specification at 150ºC, three stacked (3x) STI-based IDT-SCR ESD device is needed to achieve a 1.8V latch-up free application. I_{T2} is lower than 1A before reaching the 5V, the transistor failure voltage. Further investigation on design window and scaling is needed.

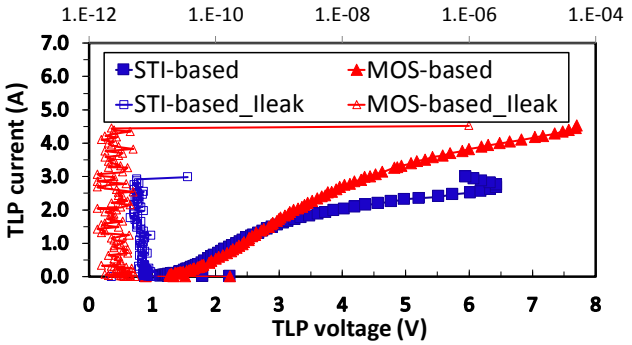

Figure 22: 100ns TLP characteristic of STI-based and MOS-based IDT-SCR with 1.8V DNW biasing.

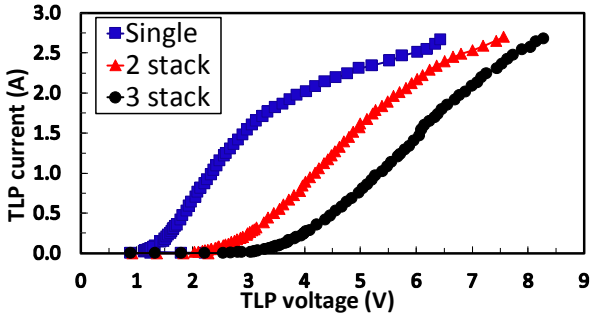

Figure 23: 100ns TLP characteristic of different stacked STI-based IDT-SCR ESD devices with 1.8V DNW biasing.

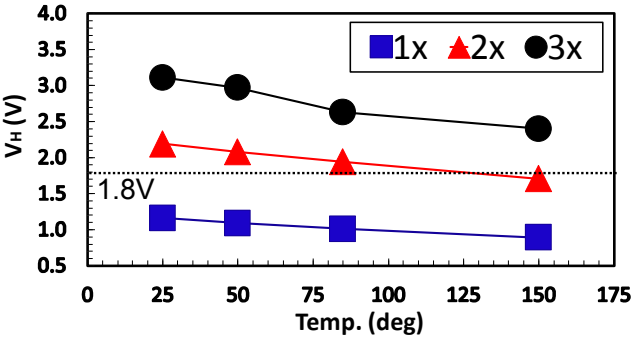

Figure 24: DC characteristics of the V_H for different stacked STI-based IDT-SCRs in different temperatures with DNW=1.8V.

Since surge robustness with power-on requirements become more relevant, it is interesting to see the ESD device behavior under long pulse width. A TLP characteristic of the two stacked STI-based IDT-SCR ESD protection device in 100ns and 1600ns pulse-width with 10ns rise-time at 1.8V DNW biasing condition is shown in Figure 25. It is clear that the STI-based IDT-SCR ESD device still demonstrates good performance under 1600ns (10ns rise-time) long pulse event.

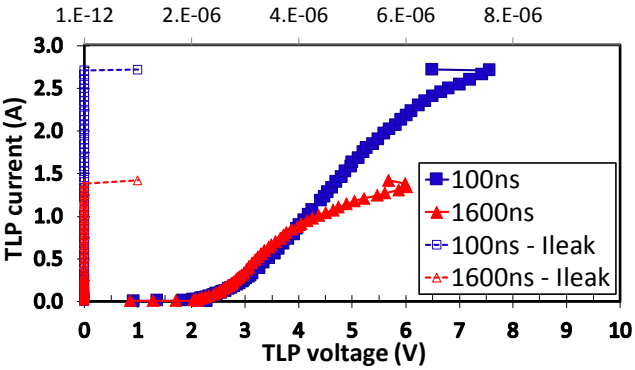

Figure 25: TLP characteristic of the two stacked STI-based IDT-SCR in different pulse-width at 1.8V DNW biasing.

VI. Conclusions

We presented a novel Integrated-Diode-Triggered SCR (IDT-SCR) ESD protection device with the following features:

- Base-line masks in CMOS process.
- Controllable-trigger voltage by DNW biasing.
- Trigger mechanism was determined by an integrated diode and main ESD current conduction by SCR action.
- Low capacitance (< 200 fF) for 1.8V IO pins.
- Suits for both power-off (floating DNW) and power-on (biased DNW) ESD/Surge conditions.

- As a 1.8V capacitive-triggered ESD supply-clamp, the failure current density is 16 times higher and the leakage is 20 times lower than a traditional capacitive-triggered ESD supply-clamp respectively.
- Stacked IDT-SCR to extend applications.
- Better reliability with STI-based IDT-SCR.

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