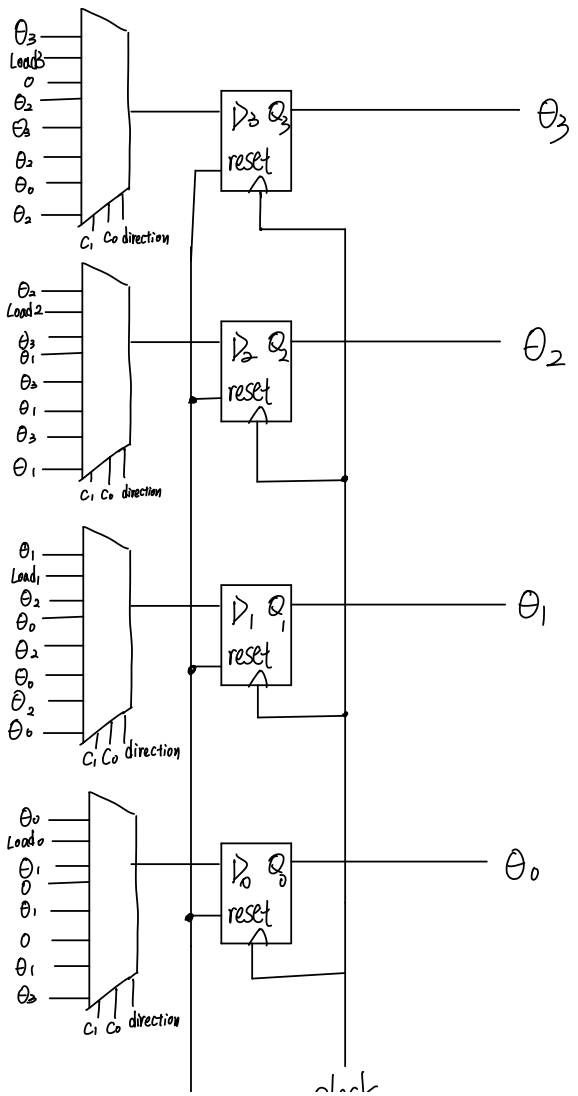
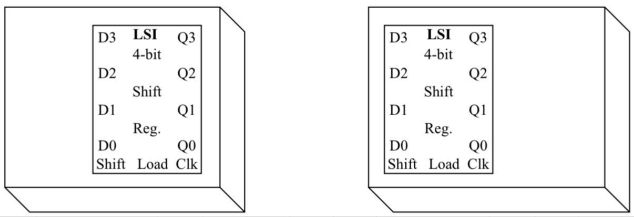
			Next state				
C_1	C_0	direction	θ_3^+	θ_2^+	θ_1^+	θ_0^+	
0	0	0	θ_3	θ_2	θ_1	θ_0	Hold
0	0	1	$Load_3$	$Load_2$	$Load_1$	$Load_0$	Parallel load
0	1	0	0	θ_3	θ_2	θ_1	Logical left
0	1	1	θ_2	θ_1	θ_0	0	Logical right
1	0	0	θ_3	θ_3	θ_2	θ_1	Arithmetic right
1	0	1	θ_2	θ_1	θ_0	0	Arithmetic left
1	1	0	θ_0	θ_3	θ_2	θ_1	Circular right
1	1	1	θ_2	θ_1	θ_0	θ_3	Circular left



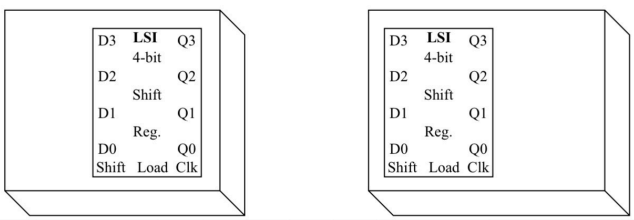
reset clock

2. a)



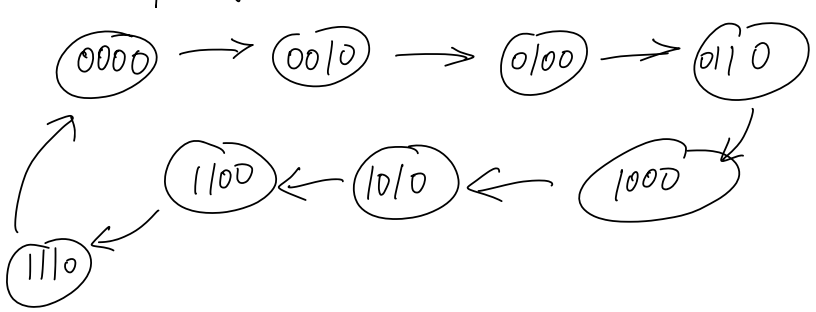
Cycle	Op - Sender	Q0	Q1	Q2	Q3		Op - Recvr	Q0	Q1	Q2	Q3
0	Load	x	x	x	x		shift	x	x	x	x
1	shift	D_0	D_1	D_2	D_3		shift	x	x	x	x
2	shift	x	D_0	D_1	D_2		shift	D_3	x	x	x
3	Load	x	x	D_0	D_1		shift	D_3	D_3	x	x
4	shift	D_0'	D_1'	D_2'	D_3'		shift	D_1	D_2	D_3	x
5	shift	x	D_0	D_1'	D_2'		shift	D_3	D_1	D_2	D_3
6											
7											
8											
9											
10											

b)



Cycle	Op - Sender	Q0	Q1	Q2	Q3		Op - Recvr	Q0	Q1	Q2	Q3
0	Load	x	x	x	x		shift	x	x	x	x
1	shift	D_0	D_1	D_2	D_3		shift	x	x	x	x
2	shift	x	D_0	D_1	D_2		shift	D_3	x	x	x
3	shift	x	x	D_0	D_1		shift	D_3	D_3	x	x
4	shift	x	x	x	D_0		shift	D_1	D_2	D_3	x
5	Load	x,	x,	x,	x,		shift	D_0	D_1	D_2	D_3
6	shift	D_0	D_1'	D_2'	D_3'		shift	x	D_0	D_1	D_2
7	shift	x	D_0'	D_1'	D_2'		shift	D_3'	x	D_0	D_1
8											
9											
10											

3. up by 2.



PS_3	PS_2	PS_1	PS_0	N_3	N_2	N_1	N_0
0	0	0	0	0	0	1	0
0	0	1	0	0	1	0	0
0	1	1	0	1	0	0	0

up by 4