```
1   // Alan Li
2   // 01/15/2022
3   // EE 371
4   // Lab #1
5
6   // userInput take 1-bit D as user input and return Q as output
7   // This module utilize two DFF to reduce the possibility of
    metastability by adding latency
8
9   module userInput(clk, D, Q);
10     input clk, D;
11     output logic Q;
12     logic temp;
13
14     always_ff @(posedge clk) begin
15        temp <= D;
16        Q <= temp;
17     end
18
19  endmodule
```