```
// Alan Li
 2
     // 01/15/2022
 3
     // EE 371
 4
     // Lab #1
 5
 6
     // hexDisplay takes 5-bit inputCount as inputs and return 7-bits HEX5,
     HEX4, HEX3, HEX2, HEX1, HEX0 as output.
 7
     // Upon start, the HEX display will display "clear0", when enter signal
     is given, the HEX display the counter on HEX1 and HEX0. The counter
     will keep adding up until reach 25.
     // Then the hex display will diaplay "FULL25".
 8
 9
     // If the counter reach 0, the hex display will display "clear0" as
     there is no car in the parking lot
10
11
     module hexDisplay(clk, inputCount, HEX5, HEX4, HEX3, HEX2, HEX1, HEX0);
12
        input clk;
13
        input logic [4:0] inputCount;
14
        output logic [6:0] HEX5, HEX4, HEX3, HEX2, HEX1, HEX0;
15
16
        // 7-bit parameter for the display to display different numbers or
     characters
17
                                       6543210
        //
18
        parameter [6:0]
                                    7'b1000000.
                           zero =
19
                                    7'b1111001,
                           one =
20
                                    7'b0100100,
                           two =
21
                                    7'b0110000.
                           three =
22
                                    7'b0011001,
                           four =
                                    7'b0010010,
23
                           five =
24
                           six =
                                    7'b0000010,
25
                                    7'b1111000.
                           seven =
                                    7'b0000000,
26
                           eight =
27
                                    7'b0011000,
                           nine =
                                    7'b0001110, //FULL
28
                           F =
29
                           U =
                                    7'b1000001,
30
                                    7'b1000111,
                           L =
31
                                    7'b1000110, //CLEAR
32
                           C =
33
                                    7'b0000110,
                           E =
34
                                    7'b0001000,
                                    7'b1001100,
35
                           R =
36
                           b1k =
                                    7'b1111111;
37
38
39
        // The hex are driven off upon start.
        // The hex will display counters when enter or exit signal is given
40
        // When the counter is 0, it will display "clear0". When full it
41
     will display "full25"
42
        always_comb begin
43
           HEX5 = b1k;
44
           HEX4 = b1k;
45
           HEX3 = b1k;
46
           HEX2 = b1k;
47
           HEX1 = blk;
48
           HEX0 = b1k;
49
           case(inputCount)
50
              0: begin HEX5 = C; HEX4 = L; HEX3 = E; HEX2 = A; HEX1 = R; HEX0
      = zero; end
51
              1: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 =
```

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b1k; HEXO = one; end
52
              2: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 = blk
      b1k; HEX0 = two; end
53
              3: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 = blk
      blk; HEXO = three; end
54
              4: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 =
      blk;HEX0 = four; end
55
              5: begin HEX5 = F; HEX4 = U; HEX3 = L; HEX2 = L; HEX1 = blk;
     HEXO = five; end // for demo purpose
56
57
              //5: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk;
     HEX1 = b1k; HEX0 = five; end
58
              6: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 =
      b1k;HEX0 = six; end
              7: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 = blk
59
      blk;HEX0 = seven; end
60
              8: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 =
      blk;HEX0 = eight; end
61
              9: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 = blk
      blk;HEX0 = nine; end
              10: begin HEX5 = blk; HEX4 = blk; HEX3 = blk; HEX2 = blk; HEX1 =
62
      one; HEXO = zero; end
63
              11: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      one; HEXO = one; end
64
              12: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      one; HEXO = two; end
65
              13: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      one; HEXO = three; end
66
              14: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      one; HEXO = four; end
67
              15: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      one; HEXO = five; end
68
              16: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      one; HEXO = six; end
69
              17: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      one; HEXO = seven; end
70
              18: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      one; HEXO = eight; end
              19: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
71
      one; HEXO = nine; end
72
              20: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      two; HEXO = zero; end
73
              21: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      two; HEXO = one; end
74
              22: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      two; HEXO = two; end
75
              23: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
      two; HEXO = three; end
              24: begin HEX5 = b1k; HEX4 = b1k; HEX3 = b1k; HEX2 = b1k; HEX1 =
76
      two; HEXO = four; end
77
              25: begin HEX5 = F; HEX4 = U; HEX3 = L; HEX2 = L; HEX1 = two;
     HEXO = five; end
78
           endcase
79
        end
80
     endmodule
81
82
```

// counter_testbench tests all expected behavior that the parking lot

83

Project: DE1_SoC

```
occupancy counter system in the lab may encounter
      module hexDisplay_testbench();
 84
 85
         logic clk;
         logic [4:0] inputCount;
 86
 87
         logic [6:0] HEX5, HEX4, HEX3, HEX2, HEX1, HEX0;
 88
 89
         hexDisplay dut (.clk(clk), .inputCount(inputCount), .HEX5(HEX5), .
      HEX4(HEX4), .HEX3(HEX3), .HEX2(HEX2), .HEX1(HEX1), .HEX0(HEX0));
 90
 91
         parameter CLOCK_PERIOD = 100;
 92
 93
         initial begin
 94
            c1k \ll 0;
            forever #(CLOCK_PERIOD/2) clk <= ~clk;</pre>
 95
 96
         end
 97
 98
         initial begin
 99
             inputCount <= 0;
                               @(posedge clk);
            inputCount <= 10; @(posedge clk);
100
            inputCount <= 20; @(posedge clk);</pre>
101
            inputCount <= 25; @(posedge clk);</pre>
102
103
             $stop;
104
         end
105
      endmodule
106
```