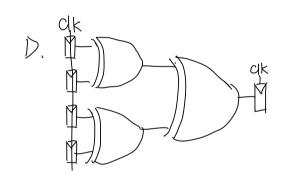
1.a tp1 = 100 ps 
$$t_{ccg} = 50 PS$$
  $t_{ccg} = 50 PS$   $t_{cd} = 55 PS$   $t_{pcg} = 70 PS$   $t_{cd} = 55 PS$   $t_{pcg} = 70 PS$   $t_{cd} = 70 + 30 0 + 60 = 430$   $t_{setup} = 60 PS$   $t_{nold} = 20 PS$   $t_{nold} = 20 PS$ 

b. 
$$T_c = \frac{1}{2GHz} = 50PS$$
  $T_c \ge t_{PC}g + 3t_{P}d + t_{Setup} + t_{Skew}$   
 $500 \ge 70 + 300 + b0 + t_{Skew}$   
 $t_{Skew} \le 70PS$  it can tolerate  $70PS$ 

it com tolerate 85PS



tc> tpcgt 2tpd+ tsetup  
= 
$$70+200+60=330$$
 ps  
max  $frequency = 330ps=3.03$  GHz

2. Q. 
$$T_c = \frac{1}{1GHz} = 1$$
 ns  $T = 100$  ps  $T_0 = 110$  ps  $T_0 = 70$  ps

MTBF = 
$$\frac{1}{P(follne/sec)} = 50 \text{ years} = 1.6 \times 10^9$$
  
P(failure/sec) =  $6.25 \times 10^{-10}$   
P(failure) =  $\frac{Pc(fai|ure/second)}{N} = \frac{6.25 \times 10^{-10}}{0.5} = 12.5 \times 10^{-10}$ 

b. Waiting time for one clock cycle 
$$P(failwe/sec) = 0.5 \times \frac{10.75}{1000} = 5.03 \times 10^{-6}$$

uaiting time for two clock cycle 
$$P(failure/sec) = 0.5 \times \frac{10^{95}}{1000}(e^{-\frac{930}{1000}})^2 = \pm 6 \times 10^{-10}$$
you need to vait 2 clock cycle before reading the sampled input

$$30.e^{-\frac{t}{50}} = 0.0|$$
 $-\frac{t}{50} = |y| 0.99$ 
 $t = 92 \text{ Seconds}$ 

b- 
$$t = 180$$
 seconds  
 $e^{-180} = 1.23 \times 10^{-2}$   
probability = 0.0123%

A. Ben is wrong if there is a normal transition on D. Dz will also have transition and enter the forbidden zone. Then it will be reset to zero.

also since the reset is async, if rest at the clock edge, it will cause second FF goes into metastability