Lab5

18) What element adds the most delay? How can we change the timing constraint such that setup slack does meet timing requirements?

Mult0~5747|chainout[0], slow down the clock speed

19) Repeat the Report Timing… steps to investigate the hold slack results. Do you expect the same element to add the most delay for hold slack?

No, in this case Mult0~8|clk[0] adds the most delay

22) Double-click Update Timing Netlist to view the new reports from your design with the updated clock. You can see the updated clock in the Report Clock summary page now. Double-click on Report Setup Summary to see if timing is met with these new conditions. What is the fastest frequency you can set the clock to for this to pass setup timing?

47.01MHz with period 21.27ns

23) Generate another timing report exactly as you did in Step 14 by selecting Custom Reports > Report Timing… in the Tasks pane. The design now passes timing. Investigate how it's different.

Data arrival path remain the same, but data required path has increased.

27) The Unconstrained Paths Summary should now have a yellow background with "OUT OF DATE" watermarks across the page. Double-click Report Unconstrained Paths in the Tasks pane to update it with your recent actions. Repeat the steps above for min and max set_output_delay using -0.5 ns for the min out delay and 5.6 ns as the max output delay, but add only the outputs of the design instead of A, B, and C. Are all the paths constrained?

Yes, both the input ports path and the output ports path are constrained.

32) Temperature and voltage have known effects on the speed of a circuit. Quartus by default will assume "Slow 1200mV 85C Model". We can change this by clicking the Set Operating Conditions tab. You will see the three options below.
Which of the three options will have the most setup slack? Why?
Fast 1100mV 0C model will have the most setup slack because the circuit has faster speed with lower temperature and high voltage. This means that the circuit will have a shorter delay and increase the setup slack.

How does increasing voltage change the speed of a circuit?
Raising the voltage decreases the prop delay through the circuit, thus increasing the speed.

How does increasing temperature change the speed of a circuit?
Increase temperature will increase the circuit resistance, thus lower the speed. Likewise, resistance is decreased with decreasing temperatures.

35) How will changing the operating conditions affect the hold slack? Why? Confirm your answer by changing the operating conditions in Timing Analyzer and trying all three operating condition

models.
Increase the circuit speed will shorten the hold slack. In other words, decreasing the temperature and increase voltage will decrease hold slack. As the circuit speed increase, data arrival time is decreased, and result in a shorter hold slack.