Problem 1.

a) Pipelining : clock is determined by the slowest operation.

cycle time = Instruction Decode = 350ps

Non-pipelining : cycle time is determined by all the stages combined

cycle time = 250+350+150+300+200 = 1250 ps

b) load instruction use all 5 stages

Pipeline. latency = cycle × clock cycle time

= 5 × 350 = 1750ps

Non-pipeline :

latency = 250+350+150+300+200 = 1250ps

c) we will split the longest stage

old cycle time = 350 ps

new cycle time is latency of memory = 300 ps

d) utilization = 20% (LDUR) + 15% (STUR) = 35%

e) utilization = 20% (LDUR) + 45% (ALU) = 65%

Problem 2

(a) read and write hazzard

ORR X_1, X_2, X_3

NOP

NOP

ORR X_2, X_1, X_4

NOP

NOP

ORR X_1, X_1, X_2

NOP

NOP

OR X_1, X_1, X_2

(b) there is no hazzard

(c) clock cycle time: 250ps

half forward 300ps

full forward 350ps

without forwarding

cycles: $(5-1+1-2)+6 = 14$

Time: $14 \cdot 250 = 3500$ ps

with full forwarding

Time: $8 \cdot 350 = 2800$ ps

speedup = 1.25

(d) no hazzard with ALU->ALU forwarding

(e) Time: $8 \cdot 300 = 2400$

Speed up = 1.46

Problem 3

(a) ADD X5, X2, X1

NOP

NOP

```
LDUR  X3, [X5, #8]
LDUR  X2, [X2, #0]
NOP
ORR   X3, X5, X3
STUR  X3, [X5, #0]
```

(b)
```
ADD   X5, X2, X1
LDUR  X2, [X2, #0]
NOP
LDUR  X3 [X5, #8]
NOP
NOP
ORR   X3, X5, X3
STUR  X3, [X5, #0]
```

(c)
```
ADD   X5, X2, X1
LDUR  X3 [X5, #8]
NOP
LDUR  X2, [X2, #0]
NOP
NOP
ORR   X3, X5, X3
NOP
NOP
STUR  X3, [X5, #0]
```

(d) the instruction get old data or junk data when initiate the register

Problem 4.

(a) first 3 cycle: IF, ID, EX
3 stall cycles
Accuray of the predicted Alway-taken = 45%
Accuracy of the non-predicated Aways-take = 55%
CPI = 3·0.55·0.25 = 0.4125

(b) CPI = 3·0.45·0.25 = 0.3375

(c) Accuracy of the non-predicated 2bit = 1-0.85 = 0.15
CPI = 3×0.15×0.25 = 0.1125

(d) CPI for ALU instruction = 1
CPI before conversion = 1+3·0.15·0.25 = 1.113
CPI after conversion = 1+ 3·15·0.25·0.5 = 1.054

(e) CPI before conversion = 1+3·0.15 0.25 = 1.113
CPI after conversion = 1+ (1+3·0.15)·0.25·0.5 = 1.181