Problem 1.

(a) only LDUR and STUR use date memory

25% + 10% = 35%

(b) every instruction needs to fetch from instruction memory

100%

(c) load a value from memory less than 32 bits require sign extension

CBZ . 0 are filled with 0 bits

for I type instruction, 16 bit immediate needs to get extended to 32 bits

for B the offset needs to get sign extension

1 − 24% = 76%

Problem 2.

(a) regWrite = 1

ALUSrc = 0

ALU operation = 10

MemWrite = 0

MemtoReg = 0

MemRead = 0

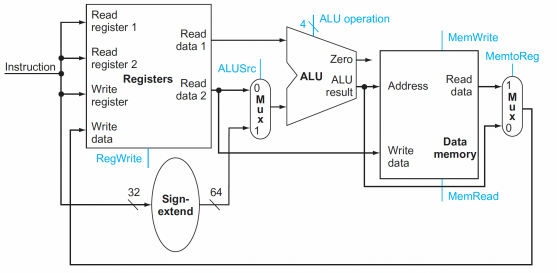


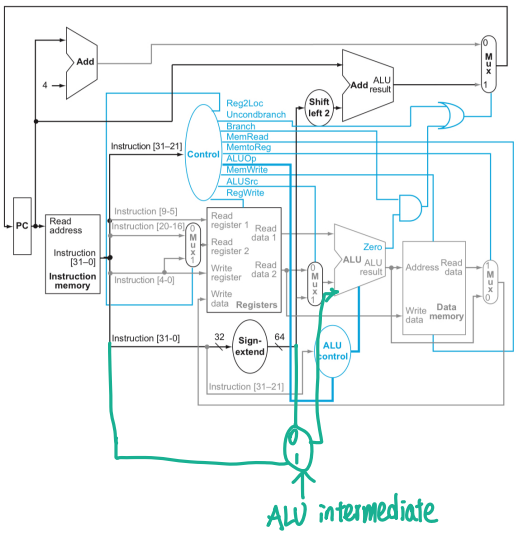
FIGURE 4.10 The datapath for the memory instructions and the R-type instructions. This example shows how a single datapath can be assembled from the pieces in Figures 4.7 and 4.8 by adding multiplexors. Two multiplexors are needed, as described in the example.

(b) registers, MUX, ALU

(c) sign-extend , data memory

Problem 3.

a. for i instruction, [21:10] is for immediate, we need to extend this to 32 bit to match the register size



b. Reg2Loc: don't care since there is no Rm

Uncondbranch = 0

Branch = 0

MemRead: don't care since we are not reading data from memory

Mem to Reg: 0

ALUOp = Addi

MemWrite = 0

ALUSrc: 1

Reg Write = 1

Problem 4

$(1EF00F00)_{16} = (0001\,1110\,1111\,0000\,0000\,1111\,0000\,0000)$

exponent $(0011\,1101)_2 = (61)_{10}$ $\quad 61-127 = -66$

fraction $\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{2^{12}} + \frac{1}{2^{13}} + \frac{1}{2^{14}} + \frac{1}{2^{15}}$

mantissa 1.875458

decimal $1.875458 \cdot 2^{-66}$

Problem 5

Sign bit 0

$16 < 31.7 < 32$ $4 + 127 = 131$

Exponent 10000011

Mantissa

$0.7 \times 2 = 1.4$ ✓

$0.4 \times 2 = 0.8$ ✗

$0.8 \times 2 = 1.6$ ✓

$0.6 \times 2 = 1.2$ ✓

$0.2 \times 2 = 0.4$ ✗

$0.4 \times 2 = 0.8$ ✗

$0.8 \times 2 = 1.6$ ✓

Mantissa 1111 0110 0110 0110 0110 0

binary representation 0 10000011 11110110011001100110011