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Thin Film Transistor Technologies: Implementing Research Results in Higher Education to prepare the emerging Multidisciplinary Connected Objects

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Thin-film technologies have been the backbone of large-scale electronics for decades. The electrical performances of the devices result from the improvement of the architectural and material properties. In new systems-on-chip, these technologies are increasingly involved. In order to develop new objects, such as connected objects, the skills and know-how of engineers and researchers have evolved into new architectures and new materials with multidisciplinary applications. An effort must be made for training and more particularly for the acquisition of know-how. The paper deals with: -the evolution of thin film technologies through research activities, - the societal issues for applications including the development of connected objects, - the need of training in higher education. This training is provided in France through a national network that has oriented the practice towards future digital and connected society. This transfer of research activities to higher education is the main mission of the academic world.

Introduction

Thin-film technologies have been the backbone of large-scale electronics for decades. The electrical performances of the devices result from the improvement of the architectural and material properties thanks to more than 25 years of research activities. In new systems-on-chip, these technologies are increasingly involved. In order to develop new objects, such as connected objects, the skills and know-how of engineers and researchers have evolved into new architectures and new materials with multidisciplinary applications. An effort must be made for training and more particularly for the acquisition of know-how.

After a presentation of the evolution of the thin film technologies thanks to the research activities, and of the societal issues for applications that include the development of connected objects, the presentation highlights the set-up of training covering the different aspects of the thin film technologies in order to train the graduate students for

the future digital and connected society. This transfer from the research activities towards the Higher Education is the main mission of the University world.

Origin of thin film transistor technology

Thin film technologies, particularly thin-film transistors, have been the backbone of large-area electronics for decades, primarily for display applications such as flat panel displays. In order to decrease the cost of the substrate and to give access to very large area possibilities, these devices were mainly manufactured on glass substrate. The deposition techniques were thus compatible with glass thermal limitation and the processes have therefore been considered as a low temperature technology compared to bulk silicon CMOS technology processes. The main drawback was the possibility to obtain a semiconductor deposited that keeps good electrical properties, and mainly a good Ion/Ioff current ratio with a not too high threshold voltage. The first operational transistors were based on deposited amorphous silicon. This material very well minimized the off current but had a too low doping efficiency in comparison with its monocrystalline counterpart. Because it was not possible to process an epitaxial layer on glass, the objective was to deposit polycrystalline silicon.

Many researches were performed in order to reach good thin film of silicon layers able to produce a good CMOS like-transistor. They involved several deposition and doping techniques such as CVD or plasma, several crystallization techniques by thermal annealing, rapid thermal annealing (RTA), laser crystallizations; different gate insulator materials, other semiconductors materials, semiconductor oxides (for example IGZO), large bandgap oxides, and organic semiconductors (1).

Figure 1 shows the main technological approaches that are involved in order to reach suitable electrical properties (2). The process temperatures were thus continuously decreasing to reach almost room temperatures. In this condition, the substrates can be less restrictive than glass. The new technologies are now compatible with plastics and organic film substrates. This evolution opened a large spectrum of applications much wider than flat panel displays, more especially in the development of sensors and actuators (3), but also in new three-dimension architectures leading to heterogeneous systems (4). Indeed, the vertical conduction becomes possible in thin film technology (5). The thin film technology is compatible with the use of nanowire-based devices (6) and allows the fabrication of biosensors (7).

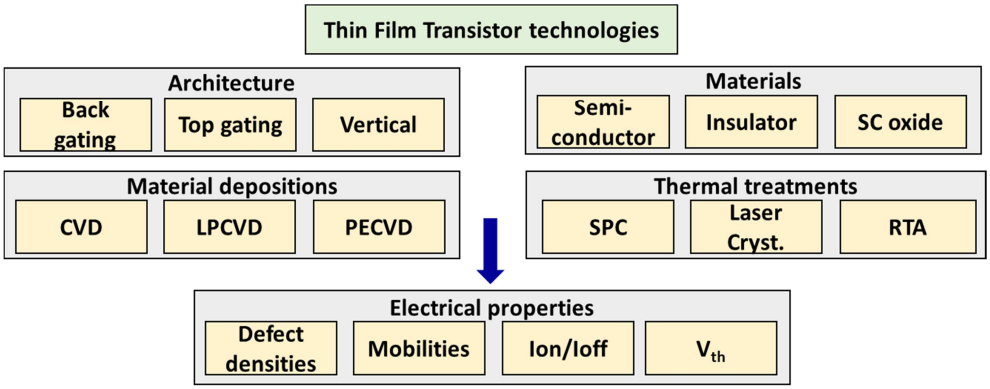

Figure 1. Main approaches of thin film transistors technologies. The main goal is to reach high electrical properties of the final devices or circuits.

Convergence of ULSI and TFT technologies

Due to the huge development of integrated electronics that is driven by a steady size reduction to cope with Moore's law, the CMOS thermal budget has been drastically lowered. The Ultra large Scale Integration (ULSI) leads to lateral dimensions that are controlled in the range of one nanometer. This evolution means a negligible lateral diffusion of doping. The process steps must have a maximum temperature lower than 700°C. The layers must have a nanometric thickness. The consequence is the involvement of new techniques such as atomic layer deposition (ALD) that corresponds to a relatively low temperature process step (8). These new techniques in-fine brought both technologies (TFTT and ULSI) to comparable processing temperatures. Figure 2 summarizes the main steps that govern the electrical properties of the final devices.

Today, flexible plastics is used as a substrate. In addition, as the physical limitation of dimensions becomes close to the size of one monolayer, integration has shifted to the third dimension by stacking circuit substrates and other physical or electrical functions (more than Moore(9)). As a result, electrical circuits become three-dimensional and increasingly involve thin-film technologies in new systems-on-a-chip (SOC) or systems-in-package (SiP).

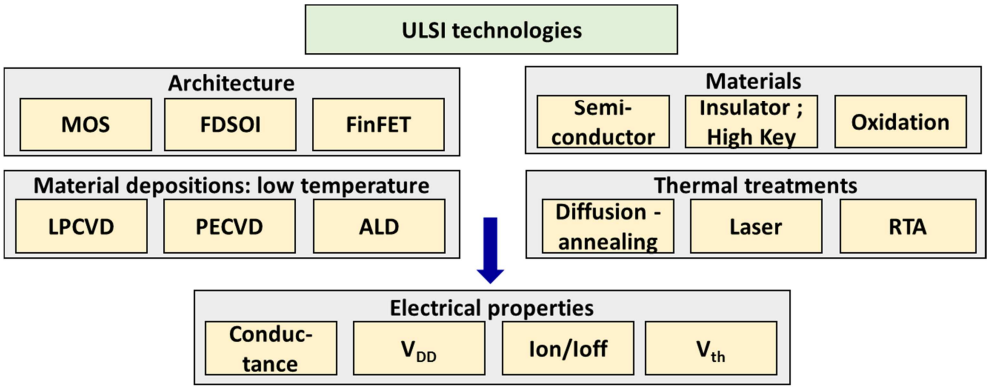

Figure 2. Main approaches of Ultra Low Scale Integration technologies. The main goal is to reach high electrical properties of the final devices or circuits. With the decrease of dimensions, the process temperatures are lower and lower.

Technology combinations towards connected objects

This trend allows creating new objects that are gathering several functions with communication capabilities, i.e. connected smart objects (10). The connected objects can contain sensors, actuators, signal processing circuits but also displays, and energy harvesting device. In other words, they combine large area electronics and CMOS ones. The main advantage of the thin film technologies is offering the possibilities to process multidisciplinary objects such as MEMS (micro-electrical-mechanical systems), BioMEMS for biological application, Optoelectronic systems, for example. The spectrum of combination is increasingly wider and hence addresses a large field of applications to many societal issues such as health, environment, security, transport, energy,

communications, new generation of production lines (4.0 approach), etc. As shown in figure 3, the connected objects are thus composed of several electronic functions that comprise:

- physical, chemical and biological sensors and actuators,
- equipment for energy harvesting suitable for remote or mobile objects,
- analog and digital electronic circuits for signal processing; these circuits can contain microprocessors, DSP, memories, embedded electronics,
- visualization panels, alarms, and control systems,
- receiving and transmitting modules adapted for the protocols of communications.

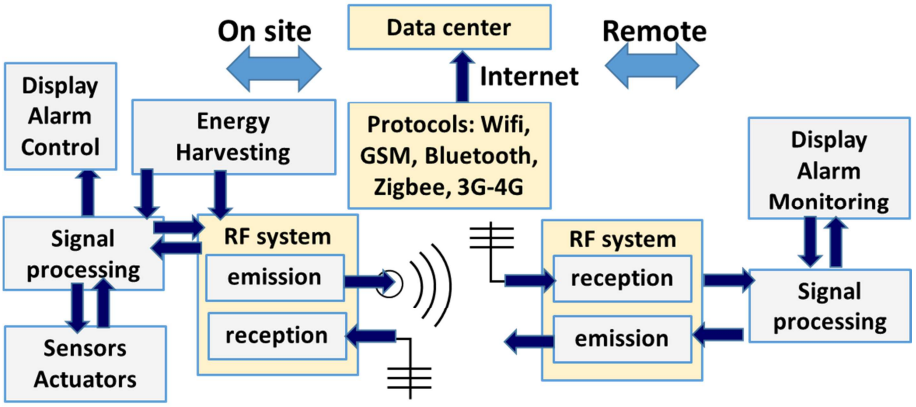

Figure 3. Structure of the future technologies adapted for connected objects. The part on site of the connected or smart objects can be fully integrated by combining ULSI and TFT technologies. The new packaging techniques allow this new approach.

It is clear that the development of such new objects supposes a wide spectrum of research activities and an advanced know-how for the future engineers and doctors. If they are not specialist in each technological step, they must have a specialty and a capability to work in team with other specialists.

Research activities and related skills

The research activities for the development of thin film transistors technologies is mature (11) even if further progress could be made to reduce the power consumption and/or to improve the electrical characteristics, the sensitivity and the reliability (12). Important research efforts were devoted to improve the quality of the semiconductor materials, to adapt the thin layer deposition techniques to the nature of the substrate, to improve the interfaces at the border of the active zones, to minimize the density of defects despite a low temperature budget by involving several techniques of crystallization and/or depositions, by and also changing the architecture of the elementary device, and the design of the circuits, ….

A large variety of skills has to be made available in order to keep the pace of this technology development. This means the training of skilled technicians, engineers, and researchers bearing PhD degrees. In a context of digital society, developing the skills of the graduate students is strongly linked to the knowledge and the associated know-how. The initial education of engineers and researchers must contain several practical training based on the outcome of research activity allowing an awareness of the students to the new challenge.

Need of Higher Education adapted to these technologies

Practical training to develop advanced know-how skills may be hampered by the cost of equipment and associated operating expenses. To meet this challenge, the strategy of the French network CNFM (National Coordination of Education in Microelectronics and Nanotechnology (13)) is to share manufacturing facilities such as the clean room and to share the design tools. In this strategy, twelve microelectronics centers were created in the early 1980s, seven of which have clean rooms open to initial education and lifelong learning. Today, these joint centers are organized in a network, recognized by the Ministry of Higher Education, which financially supports, at least partially, the joint activities. In this network, two important industrial partners, ACSIEL (14) and FIEEC (15) are members of the GIP-CNFM. These partners are industrial organizations representing the majority of companies working in France in the field of microelectronics and electronic systems. Through their presence, they can advise the network on new trends and priority innovative activities.

Practical training and know-how in the French Higher Education centers

Several CNFM centers have activities in the thin film technologies, mainly Rennes, Grenoble, Lille, Toulouse and Bordeaux centers. They have developed practical training for students; which comprises amorphous and polycrystalline silicon thin film transistors technologies, and more recently organic semiconductors for photovoltaic and optoelectronics applications, graphene thin film devices, or insulator ultrathin films for memories (such as Metal-Insulator-Metal or MIM structure), but also, sensors and actuators, which both involve suspended gate thin film transistors, suspended membranes, nanowires, cantilevers, piezoelectric films, etc. All these results come from research activities developed in the scientific and industrial environment of these centers. Below, several examples highlight this strong link between research and higher education with a spectrum of activities adapted to new objects and therefore to the needs of the industry.

Figure 4 describes through three images a suspended gate polycrystalline silicon TFT transistor, referred to as ionization sensitive thin film transistors (ISFET) or airgap TFT (16). This structure was patented in 2005 (17). Figure 4 shows: a) a cross section of the structure that gives the principle, b) a top view of a manufactured device, c) a scanning electron microscope image of a device manufactured by the students in initial training at the masters level.

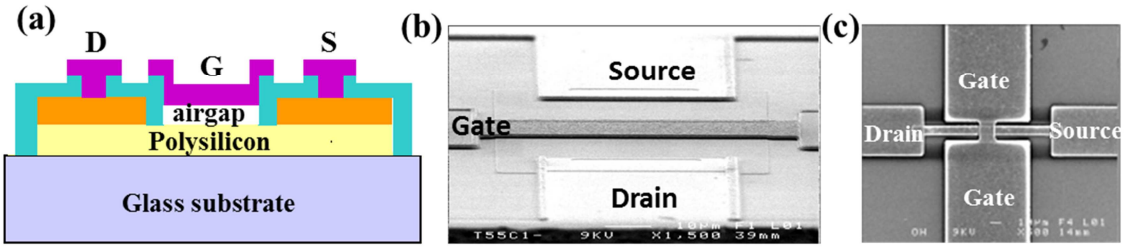

Figure 4. a) schematic cross-section of an airgap transistor; b) top view of the fabricated device for patent deposition; c) realization in cleanroom by student in initial education of microelectronic engineering.

Figure 5 shows a silicon nanowire transistor for which the nanowires can be used as sensing elements (18). On the left, the schematic architecture, in the center the nanowire positioned on a contact, on the right, scanning electron micro combined with a nano-robot manipulator of the nanowire. This equipment is accessible to master-level students for practice on innovative devices. This structure can be carried out on a low temperature substrate involving conventional thin film technology as well as on an existing integrated circuit (principle of "above-IC" technology).

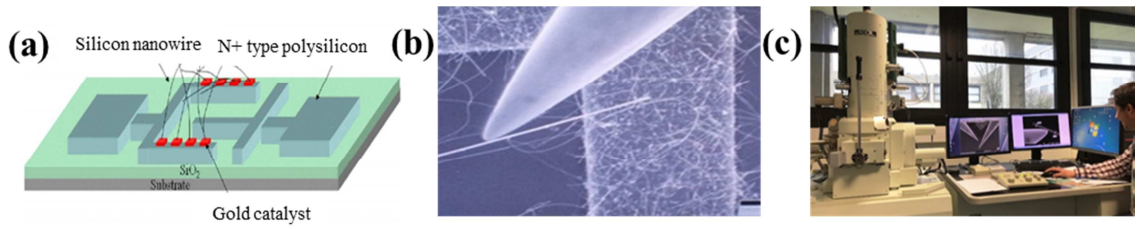

Figure 5. Silicon nanowire-based device: a) structure, b) device, c) test with TEM

Figure 6 shows a Metal-Insulator-Metal structure (Ru/RuO2/ATO/Pt) issued from research activities (19). In this case, the MIM stacked structure is realized in a three-dimension architecture in order to increase the capacitance area for the same substrate area (see Figure 6a). The trenches are processed by deep reactive ion etching process. The films are deposited by atomic layer deposition (ALD), a low temperature process step compatible with the Ultra Large Scale Integration (ULSI). Figure 6b) show a TEM image of a planar structure fabricated by students in cleanroom. Figure 6c, shows a picture of the ALD reactor in the cleanroom of the Grenoble center. The process is simplified for students. However, they have the know-how of ALD process step and must prepare the sample for TEM analysis. Finally, the sample is electrically analyzed, mainly from capacitance measurements. At the master level, this practice enriches the skills of students.

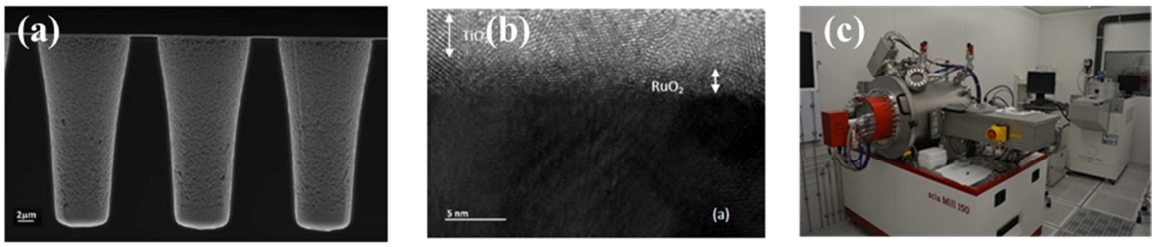

Figure 6. Metal-Insulator-Metal structure: a) three-dimensional structure from research studies (19), b) planar structure fabricated in cleanroom by students, c) ALD equipment opened to education and research activities at the Microelectronics center of Grenoble.

In the frame of the French network, we may have many other examples of transfer of research activities to Higher Education with the goal to give know-how to the students in the innovative technologies. We can mention:

- the realization of flexible electronics including microcrystalline silicon film based transistors at the center of Rennes (20),
- the realization of RF antennas involving printed electronics on flexible substrate (Kapton) at the center of Bordeaux (21)

- the realization of sensors by printed electronics on flexible substrate such as plastics and papers at center of Rennes (22),
- the realization of light emitting diodes and flat panel displays based on organic materials at the center of Bordeaux (23),
- the fabrication of graphene-based transistors at the center of Lille (24); in this practical training, the graphene film is used as channel material of a MOS transistor for high frequency applications,
- the design and the fabrication nanodots-based MOSFET for memory application (25) by the center of Toulouse.

Taking into account the diversity of the circuits in a connected object as mentioned above, all these examples can constitute an elementary piece of the final heterogeneous circuits.

Discussion and conclusion

This paper has highlighted the importance of the know-how for the future engineers and doctors more especially in the new digital environment. In microelectronics, this know-how must involve very complex and big software and very expensive equipment more especially in cleanroom. The organization in network that promotes that sharing of these tools appears as a judicious approach for two main reasons: economical one, by sharing the functioning expenses and the equipment cost that are very high, but also pedagogical one by increasing the efficiency of teachers that build new practice.

The expected needs in formation must cover the basic pieces that constitute the electronic functions of the connected objects. In this way, several partners of the French network have set-up practical trainings that cover the different aspects of the thin film technologies in order to train the graduate students for the future digital and connected society. This training is issued of research activities of the research laboratories in the close environment of the Higher Education Microelectronics centers. Several given examples may show the diversity of the proposed subjects and their more and more multidisciplinary aspects. This trend seems adapted to the development of Internet of Things (IoT) and Internet of Everything (IoE). To conclude, let us notice that this transfer from the research activities towards the Higher Education of specialists is certainly the main mission that the academic faculties must accomplish.

Acknowledgments

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