Numbers in parenthesis denote pin numbers for F package (Case 650).

FUNCTIONS AND CHARACTERISTICS (continued)

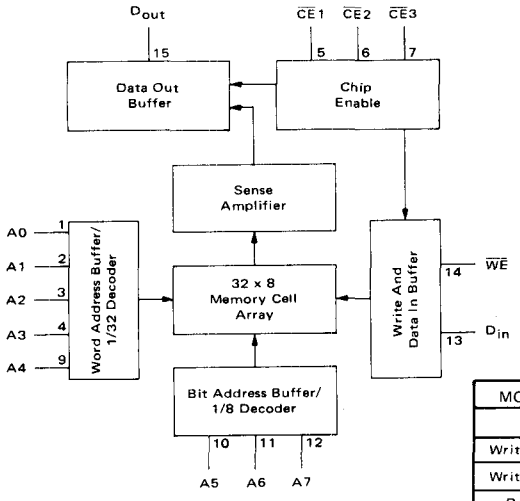
Function	Type ①		Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
	-30 to +85°C	-55 to +125°C			
Universal Decade Counter	MC10137	MC10537	f = 150 MHz	625	620,650
Bi-Quinary Counter	MC10138	–	f = 150 MHz	370	620
64-Bit Random Access Memory (90 Ω)	MCM10140	–	t_{Access} = 15 (max)	420	620,690
Four-Bit Universal Shift Register	MC10141	MC10541	f = 200 MHz	425	620,648,650
64-Bit Random Access Memory (50 Ω)	MCM10142	–	t_{Access} = 10 (max)	420	620
8 x 2 Multiport Register File (RAM)	MCM10143	–	t_{Access} = 10	610	623
256-Bit Random Access Memory	MCM10144	–	t_{Access} = 30 (max)	420	620,690
64-Bit Register File (RAM)	MCM10145	–	t_{Access} = 10	625	620
128-Bit Random Access Memory	MCM10147	–	t_{Access} = 12 (max)	420	620
64-Bit Random Access Memory (50 Ω)	MCM10148	–	t_{Access} = 15 (max)	420	620
1024-Bit Programmable Read Only Memory	MCM10150	–	t_{Access} = 20	–	690
Quad Latch	MC10153	–	4.0	310	620
12-Bit Parity Generator-Checker	MC10160	MC10560	5.0	320	620,648,650
Binary to 1-8 Decoder (Low)	MC10161	MC10561	4.0	315	620,648,650
Binary to 1-8 Decoder (High)	MC10162	MC10562	4.0	315	620,648,650
Error Detection-Correction Circuit	MC10163	–	5.0	520	620
8-Line Multiplexer	MC10164	MC10564	3.0	310	620,648,650
8-Input Priority Encoder	MC10165	–	7.0	545	620,648
5-Bit Magnitude Comparator	MC10166	–	6.0	440	620
Quad Latch	MC10168	–	3.0	310	620
Dual Binary To 1-4 Decoder (Low)	MC10171	MC10571	4.0	325	620,648,650
Dual Binary To 1-4 Decoder (High)	MC10172	MC10572	4.0	325	620,648,650
Quad 2-Input Multiplexer/Latch	MC10173	–	2.5	275	620,648
Dual 4 To 1 Multiplexer	MC10174	MC10574	3.5	305	620,650
Quint Latch	MC10175	MC10575	2.5	400	620
Hex "D" Master-Slave Flip-Flop	MC10176	–	f = 250 MHz	460	620
Triple MECL to NMOS Translator	MC10177	–	–	1.0 W	620
Binary Counter	MC10178	–	f = 150 MHz	370	620
Look-Ahead Carry Block	MC10179	MC10579	3.0 (Cn,P) 4.0 (G)	300	620,648,650
Dual High Speed Adder/Subtractor	MC10180	MC10580	4.5	360	620,648,650
4-Bit Arithmetic Logic Unit/Function Generator	MC10181	MC10581	See Logic Diag.	600	623,649,652
2-Bit Arithmetic Logic Unit/Function Generator	MC10182	–	See Logic Diag.	575	620
Error Detection-Correction Circuit	MC10193	–	7.5	520	620
Hex Inverter/Buffer	MC10195	–	2.0	200	620
Hex "AND" Gate	MC10197	–	2.8	200	620
High Speed Dual 3-Input 3-Output OR Gate	MC10210	–	1.5	160	620
High Speed Dual 3-Input 3-Output NOR Gate	MC10211	–	1.5	160	620
High Speed Dual 3-Input 3-Output OR/NOR Gate	MC10212	–	1.5	160	620
High Speed Triple Line Receiver	MC10216	MC10616	1.8	100	620,648,650
High Speed Dual Type D Master-Slave Flip-Flop	MC10231	MC10631	f = 225 MHz	270	620,648,650
High Speed 2 x 1 Bit Array Multiplier Block	MC10287	–	–	400	620

① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*Load Power not included

MEMORIES (continued)

MCM10144
256 Bit Random Access Memory



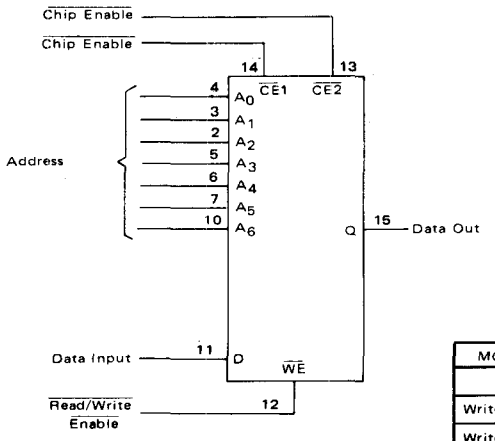
V_{CC} = Pin 16
V_{EE} = Pin 8
t_{Access} = 30 ns (max) (Address Inputs)

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care

MCM10147
128 Bit Random Access Memory



P_D = 415 mW typ/pkg (No Load)
t_{Access} = 10 ns typ (Address Inputs)

TRUTH TABLE

MODE	INPUT				OUTPUT
	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	D	Q
Write "0"	L	L	L	L	L
Write "1"	L	L	L	H	L
Read	L	L	H	ϕ	Q
Disabled	H	L	ϕ	ϕ	L
	L	H	ϕ	ϕ	L

ϕ = Don't Care

128-1 BIT RANDOM ACCESS MEMORY

MCM10147

128 x 1 BIT RANDOM ACCESS MEMORY

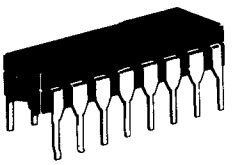
The MCM10147 is a 128-bit RAM organized as a 128-word by 1-bit array. This organization and the high speed of this MECL 10,000 device make the MCM10147 particularly useful in fast scratch pad, register file, and buffer memory applications. Full address decoding, and two Chip Enables ($\overline{CE}$) are included in this device to permit simple memory expansion.

For writing Data (D) into this memory, both Chip Enables $\overline{CE1}$ and $\overline{CE2}$ are brought low, the address is presented at A0-A6, and the Read/Write Enable ($\overline{WE}$) is taken low while Data is valid. To read a particular address, both Chip Enable inputs must again be low, but the Read/Write input is high (Data input disabled) while the location is addressed.

The two Chip Enables are provided for row or column selection of device packages in an expanded memory system. Either input can be used to select a particular row or column of stored data bits.

Open emitter outputs permit full wire-ORing to data buses, with the output being held low when either Chip Enable is high.

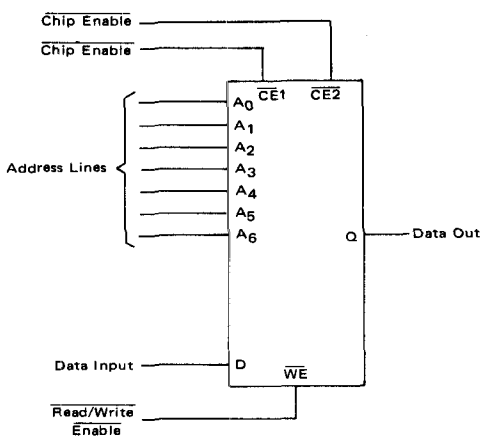
Internal input pulldown resistors are not used on this device. Unused inputs should be tied to V_{EE}.



L SUFFIX
CERAMIC PACKAGE
CASE 620

3

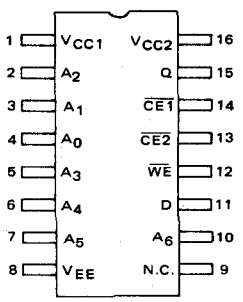
BLOCK DIAGRAM



$V_{CC1} = V_{CC2} = Gnd$
$V_{EE} = -5.2\ V$

$P_D = 415$ mW typ/pkg (No Load)
$t_{Access} = 10$ ns typ (Address Inputs)

PIN ASSIGNMENT



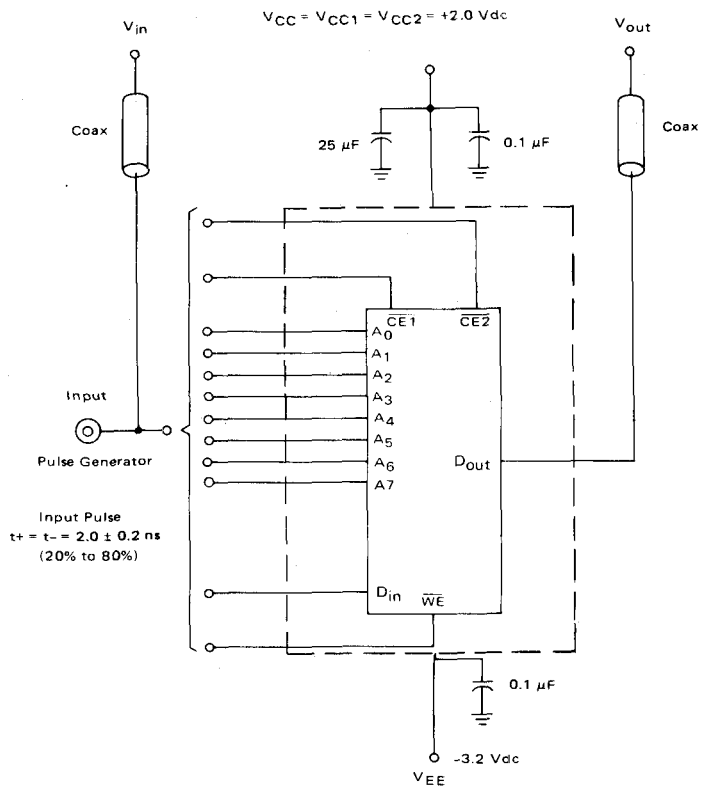
TRUTH TABLE

MODE	INPUT				OUTPUT
	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L	L
Write "1"	L	L	L	H	L
Read	L	L	H	ϕ	Q
Disabled	H	L	ϕ	ϕ	L
	L	H	ϕ	ϕ	L

ϕ = don't care

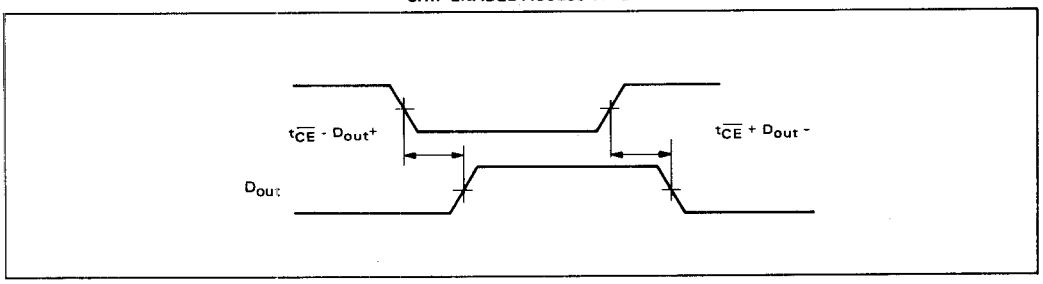
This is advance information and specifications are subject to change without notice.

SWITCHING TIME TEST CIRCUIT @ 25°C



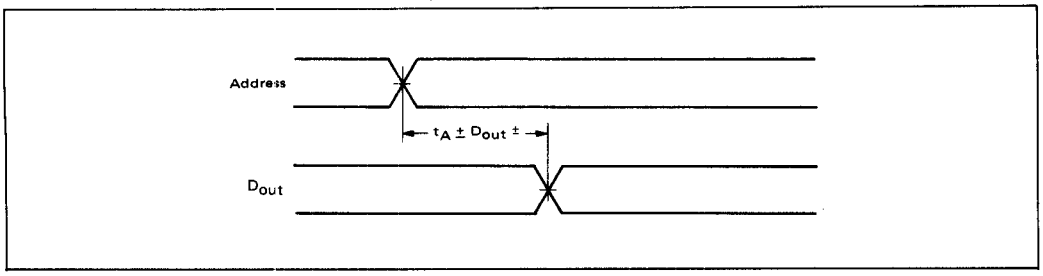
50-ohm termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

CHIP ENABLE ACCESS TIME



3

ADDRESS ACCESS TIME



WRITE STROBE MODE