F10181 • F10581

4-BIT ALU/FUNCTION GENERATOR

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10181 and F10581 are high-speed arithmetic logic units capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple through operation.

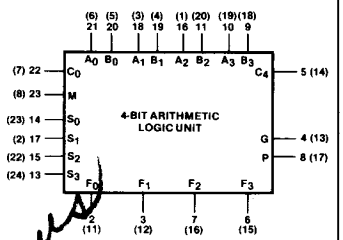
Arithmetic/logic operations are selected by applying the appropriate binary word to the select inputs (S_0 through S_3) as indicated in the tables of arithmetic/logic functions.

Group carry propagate (P) and carry generate (G) are provided to allow fast operations on very long words using a second order lookahead. The internal carry is enabled by applying a LOW level voltage to the Mode Control input (M).

When used with the F10179, full carry lookahead, as a second order lookahead block, the F10181 provides high speed arithmetic operations on very long words.

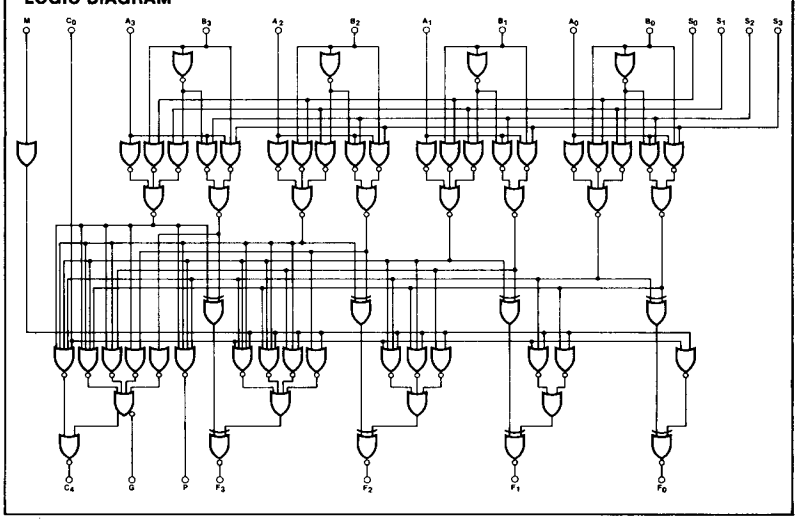
- VOLTAGE COMPENSATED—INSENSITIVE TO POWER SUPPLY VARIATIONS AND GRADIENTS
- OPEN EMITTER-FOLLOWER OUTPUTS
- SEPARATE V_{CC} PINS TO ELIMINATE NOISE COUPLING
- INTERNAL 50 kΩ (NOMINAL) INPUT PULL-DOWN RESISTORS—UNUSED INPUTS MAY BE LEFT OPEN

LOGIC SYMBOL

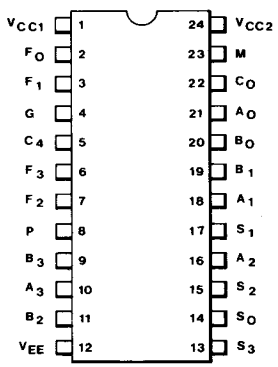


V_{CC1} = Pin 1 (10)
V_{CC2} = Pin 24 (9)
V_{EE} = Pin 12 (21)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



PIN NAMES

A_n, B_n	Operand Inputs	M	Mode Control
F_n	Function Outputs	C_4	Carry Out
S_n	Select Inputs	G	Carry Generate
C_0	Carry In	P	Carry Propagate

LOGIC FUNCTIONS

				OUTPUT FUNCTION F		
FUNCTION SELECT				M = HIGH (Logic Mode)	M = LOW (Arithmetic Mode)	
S_3	S_2	S_1	S_0	C_0 = H or L	C_0 = LOW	C_0 = HIGH
L	L	L	L	$\overline{A}$	A	A plus 1
L	L	L	H	$\overline{A}+\overline{B}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
L	L	H	L	$\overline{A}+B$	A plus AB	A plus AB plus 1
L	L	H	H	HIGH	A plus A (2 times A)	A plus A plus 1
L	H	L	L	$\overline{A}\overline{B}$	A + B	(A + B) plus 1
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$	(A + B) plus $A\overline{B}$ plus 1
L	H	H	L	$\overline{A \oplus B}$	A plus B	A plus B plus 1
L	H	H	H	$A+\overline{B}$	(A + B) plus A	(A + B) plus A plus 1
H	L	L	L	$\overline{A}B$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
H	L	L	H	$A \oplus B$	A minus B minus 1	A minus B
H	L	H	L	B	$(A+\overline{B})$ plus AB	$(A+\overline{B})$ plus AB plus 1
H	L	H	H	A + B	$(A+\overline{B})$ plus A	$(A+\overline{B})$ plus A plus 1
H	H	L	L	LOW	minus 1 (2's complement)	Zero
H	H	L	H	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
H	H	H	L	AB	AB minus 1	AB
H	H	H	H	A	A minus 1	A

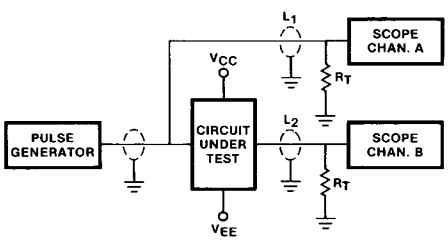
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	Pin M			200			
	Pins A3, A2, A1, A0			220			
	Pins B3, B2, B1, B0			245			
	Pins S3, S2, S1, S0			265			
	Pin C0			290			
I_{EE}	Power Supply Current	−145	−110		mA	25°C	Inputs Open

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	CHARACTERISTIC	OUTPUT	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS See Figure 1
t_{PHL},t_{PLH}	Propagation Delay, C – C_4	1	1.1	3.1	5.0	ns	A_0, A_1, A_2, A_3 = +1.11 V
t_{THL},t_{TLH}	Transition Time, C_4	1	1.0	2.0	3.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, C – F_1	1	2.0	4.5	7.0	ns	A_0, = +1.11 V
t_{THL},t_{TLH}	Transition Time, F_1	1	1.5	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, A_1 – F_1	1	3.0	6.5	10.0	ns	All Inputs = +0.31 V
t_{THL},t_{TLH}	Transition Time, F_1	1	1.5	3.0	5.0	ns	
t_{PHL},t_{PLH}	Propagation Delay, A_1 – P	1	2.0	5.0	6.5	ns	S_0, S_3, = +1.11 V
t_{THL},t_{TLH}	Transition Time, P	1	1.1	2.0	3.5	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, A_1 – G	1	2.0	4.5	7.0	ns	A_0, A_2, A_3, C = +1.11 V
t_{THL},t_{TLH}	Transition Time, G	1	1.5	4.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, A_1 – C_4	1	2.0	5.0	7.0	ns	A_0, A_2, A_3, C +1.11 V
t_{THL},t_{TLH}	Transition Time, C_4	1	1.0	2.0	3.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, B_1 – F_1	1	3.0	8.0	11.0	ns	S_3, C = +1.11 V
t_{THL},t_{TLH}	Transition Time, F_1	1	1.5	3.5	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, B_1 – P	1	2.0	6.0	7.5	ns	S_1, A_1, = +1.11 V
t_{THL},t_{TLH}	Transition Time, P	1	1.1	2.0	3.5	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, B_1 – G	2	2.0	6.0	8.0	ns	S_3, C = +1.11 V
t_{THL},t_{TLH}	Transition Time, G	2	1.5	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, B_1 – C_4	2	2.0	6.0	8.0	ns	S_3, C = +1.11 V
t_{THL},t_{TLH}	Transition Time, C_4	2	1.0	2.0	3.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, M – F_1	1	3.0	6.5	10.0	ns	All Inputs = +0.31 V
t_{THL},t_{TLH}	Transition Time, F_1	1	1.5	4.0	5.0	ns	
t_{PHL},t_{PLH}	Propagation Delay, S_1 – F_1	2	3.0	6.5	10.0	ns	A_1, B_1, = +1.11 V
t_{THL},t_{TLH}	Transition Time, F_1	2	1.5	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, S_1 – P	1	2.0	6.0	8.0	ns	A_3, B_3, = +1.11 V
t_{THL},t_{TLH}	Transition Time, P	1	1.1	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, S_1 – C_4	1	2.0	6.0	9.0	ns	A_3, B_3, = +1.11 V
t_{THL},t_{TLH}	Transition Time, C_4	1	1.1	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, S_1 – G	1	2.0	6.0	9.0	ns	A_3, B_3, = +1.11 V
t_{THL},t_{TLH}	Transition Time, G	1	0.8	3.0	6.0	ns	Other Inputs = +0.31 V

AC TEST CIRCUIT AND WAVEFORMS



V_{CC} = +2 V, V_{EE} – 3.2 V
R_T = 50 Ω termination of scope
L_1 = L_2 = 50 Ω transmission lines
Decoupling 0.1 μF from V_{CC} and V_{EE} to gnd

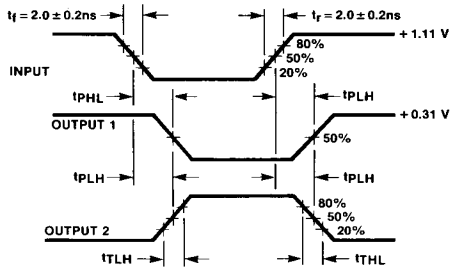


Fig. 1