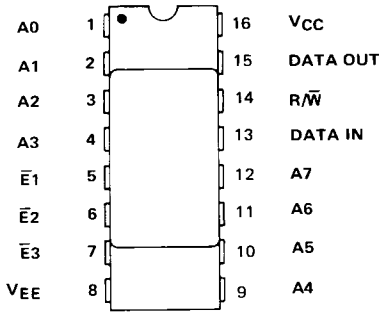
- Fast Access Time . . . 18 ns Typical
- 256-Word-by-One-Bit Organization
- Drives 50-Ohm Loads
- Full On-Chip Address Decoding and Output-Sense Amplification
- Capability for Wired-OR Connections
- Low Sensitivity to Supply Voltage Variation

J OR JE
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

This 256-bit active-element memory is a monolithic high-speed, emitter-coupled-logic (ECL) array of 256 storage cells organized to provide 256 words of one bit each. Full address decoding and output sense amplification are included on the chip. An additional level of decoding is provided for memory systems by the three enable inputs. Each of the 256 words is addressed by the binary address inputs A0 through A7. The output can be connected to other emitter-follower outputs to achieve wired-OR word expansion.

Information at the data input is written into the memory by addressing the desired word with the address lines and taking the read/write input low while all enable inputs are held low. The output is forced low while the memory is in the write mode.

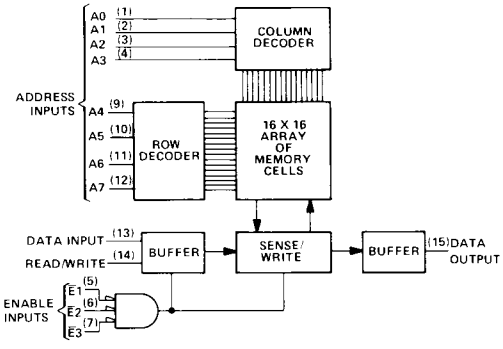
Information stored in the memory is read out by holding the read/write line high, selecting the desired address, and taking all enable inputs low.

FUNCTION TABLE

READ/ WRITE	ENABLE $\overline{E}1$	ENABLE $\overline{E}2$	ENABLE $\overline{E}3$	OPERATION
L	L	L	L	Write (output low)
H	L	L	L	Read
X	H	X	X	Chip disabled (output low)
X	X	H	X	Chip disabled (output low)
X	X	X	H	Chip disabled (output low)

H = high level, L = low level, X = irrelevant

functional block diagram



5

recommended operating conditions

		B	NOM	A (SEE NOTE 3)	UNIT
Supply voltage, V_{EE}		−5.72	−5.2	−4.68	V
Width of write pulse, $t_{w(wr)}$ (see Figure 9)		25			ns
Setup time, t_{su} (see Figure 9)	Address before write pulse	8			ns
	Enable before write pulse	2			
	Data before end of write pulse	27†			
Hold time, t_h (see Figure 9)	Address after write pulse	2			ns
	Enable after write pulse	2			
	Data after write pulse	2			
Operating ambient temperature, T_A		0		85	C

†Note that this setup time is referenced to the end of the write pulse. With a minimum-width (25-ns) write pulse, this limit is equivalent to a 2-ns setup time referenced to the start of the write pulse. The setup-time requirement is thus made independent of write pulse width.

electrical characteristics at specified ambient temperature‡

PARAMETER		TEST CONDITIONS (SEE NOTES 1 AND 2)		B	TYP	A (SEE NOTE 3)	UNIT
V_{IH} High-level input voltage			0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{IH'}$ High-level input voltage			0°C	−1145			mV
			25°C	−1105			
			85°C	−1035			
V_{IL} Low-level input voltage			0°C	V_{EE}		−1645	mV
			25°C	V_{EE}		−1630	
			85°C	V_{EE}		−1595	
$V_{IL'}$ Low-level input voltage			0°C			−1490	mV
			25°C			−1475	
			85°C			−1440	
V_{OH} High-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1000		−840	mV
			25°C	−960		−810	
			85°C	−890		−700	
V_{OL} Low-level output voltage		$V_{IH} = V_{IHB}$, $V_{IL} = V_{ILA}$	0°C	−1870		−1665	mV
			25°C	−1850		−1650	
			85°C	−1825		−1615	
$V_{OH'}$ High-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1020		−840	mV
			25°C	−980		−810	
			85°C	−910		−700	
$V_{OL'}$ Low-level output voltage		$V_{IH} = V_{IH'B}$, $V_{IL} = V_{IL'A}$	0°C	−1870		−1645	mV
			25°C	−1850		−1630	
			85°C	−1825		−1595	
I_{IH} High-level input current	$\overline{E}$ inputs	V_I = −810 mV, Other inputs open	25°C			265	μA
	Other inputs					50	
I_{IL} Low-level input current	$\overline{E}$ inputs	V_I = −1850 mV, Other inputs open	25°C	0.5			μA
	Other inputs			−50			
I_{EE} Supply current		All inputs and the output open	25°C	−125		−90	mA

NOTES: 1. All parameters are measured with V_{EE} = −5.200 V, V_{CC} = 0 V, and (unless otherwise noted) the output is connected to −2.000 V through 50 Ω.

2. Test conditions stating $V_{IH} = V_{IHB}$ (or $V_{IH'B}$) and/or $V_{IL} = V_{ILA}$ (or $V_{IL'A}$) mean that the high-level input voltages are equal to the B limit of V_{IH} (or $V_{IH'}$) specified for the particular temperature (see note 3) and/or the low-level input voltages are equal to the appropriate A limit of V_{IL} (or $V_{IL'}$). The output voltage limits are guaranteed for any appropriate combination of input conditions specified by the function table for the desired output.

3. This data sheet uses the algebraic-limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

‡The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 500 feet per minute with the device under test soldered to a 4 x 6 x 0.062-inch double-sided 2-oz copper-clad circuit board.

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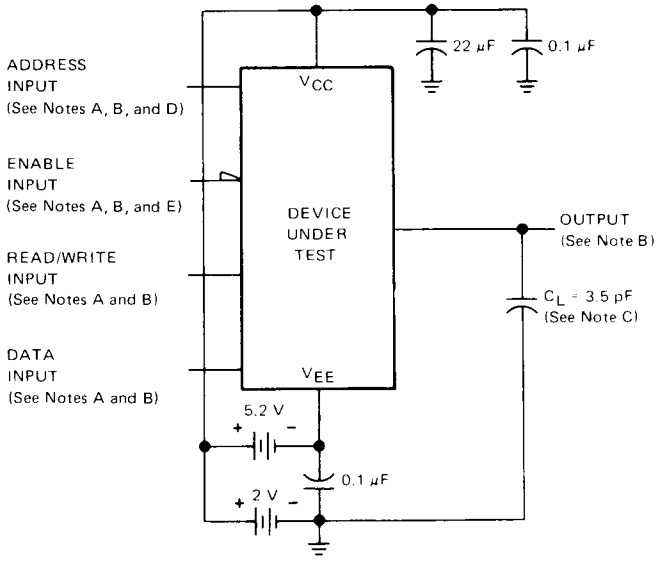
switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	B TYP A (SEE NOTE 3)		UNIT
$t_{a(ad)}$	Access time from address		C_L = 3.5 pF, R_L = 50 Ω, See Figures 6 and 9 and Note 4	18	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{E}$ (enable time)			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{E}$ (disable time)			8	12	
t_{PHL}	Propagation delay time, high-to-low-level output from read/write			8	17	ns
t_{TLH}	Transition time, low-to-high-level output (20% to 80%)			2.5		ns
t_{THL}	Transition time, high-to-low-level output (80% to 20%)			2.5		
t_{SR}	Sense recovery time			8	17	ns
$t_{w(wr,min)}$	Minimum width of write pulse			15	25	ns
$t_{su(min)}$	Minimum setup time	Address before write pulse		−15	8	ns
		Enable before write pulse		−8	2	
		Data before end of write pulse		8	27	
$t_{h(min)}$	Minimum hold time	Address after write pulse		−3	2	ns
		Enable after write pulse		−8	2	
		Data after write pulse		−7	2	

NOTES: 3. This data sheet uses the algebraic limit system that has been adopted by the International Electrotechnical Commission. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.
4. Actual values for the minimum width of write pulse, the three minimum setup times, and the three minimum hold times can each be determined separately by setting the other six intervals at their A-limit values.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveforms are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 2 MHz. Transition times of input waveforms are 2 ± 0.1 ns between the 20% and 80% levels and are determined with no device in the socket.
B. The waveforms are monitored on an oscilloscope having the following characteristics: $t_r \leq 0.35$ ns, R_{in} = 50 Ω. Input and output cables are equal lengths of 50 Ω coaxial cable.
C. C_L includes jig capacitance.
D. All address lines not under test must be biased to select a memory cell.
E. Enable lines not under test must be at a low logic level.

FIGURE 6—TEST CIRCUIT