

1. Description

1.1. Project

Project Name	usb-ssb-exciter
Board Name	custom
Generated with:	STM32CubeMX 6.14.0
Date	03/11/2025

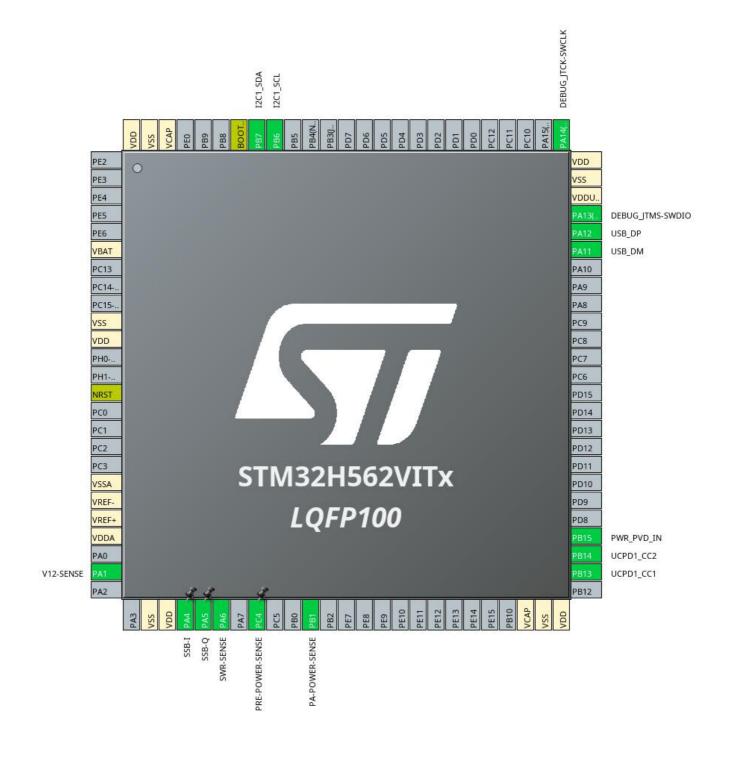
1.2. MCU

MCU Series	STM32H5
MCU Line	STM32H562
MCU name	STM32H562VITx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	ARM Cortex-M33

2. Pinout Configuration

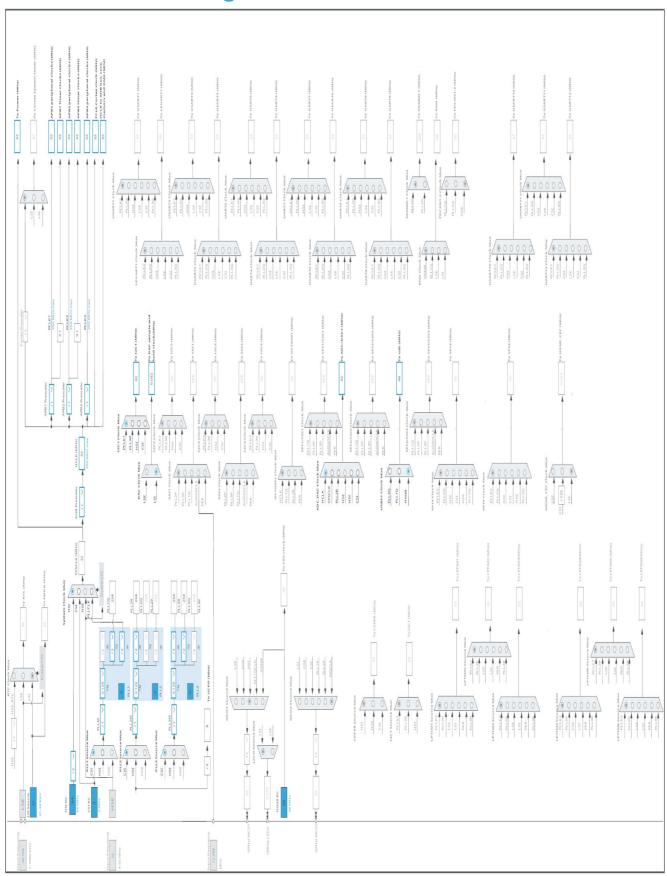


3. Pins Configuration

Company	Pin Number	Pin Name	Pin Type		Label
6	LQFP100			Function(s)	
10		reset)			
11	6	VBAT	Power		
14	10	VSS	Power		
19	11	VDD	Power		
20	14	NRST	Reset		
21	19	VSSA	Power		
22	20	VREF-	Power		
24 PA1 I/O ADC1_INP1 V12-SENSE 27 VSS Power Power 28 VDD Power Power 29 PA4 I/O ADC1_INP18, DAC1_OUT1, ADC2_INP18 SSB-I 30 PA5 I/O DAC1_OUT2, ADC1_INP19, ADC2_INP19 SSB-Q 31 PA6 I/O ADC1_INP3 SWR-SENSE 33 PC4 I/O ADC1_INP4 PRE-POWER-SENSE 36 PB1 I/O ADC1_INP5 PA-POWER-SENSE 48 VCAP Power Power PA-POWER-SENSE 49 VSS Power Power PA-POWER-SENSE 50 VDD Power Power POWER-SENSE 51 VDD Power POWER-SENSE POWER-SENSE 52 PB13 I/O UCPD1_CC1 POWER-SENSE POWER-SENSE 54 PB15 I/O PWR_PVD_IN POWER-SENSE POWER-SENSE 54 PB15 I/O <td< td=""><td>21</td><td>VREF+</td><td>Power</td><td></td><td></td></td<>	21	VREF+	Power		
27	22	VDDA	Power		
28	24	PA1	I/O	ADC1_INP1	V12-SENSE
PA4	27	VSS	Power		
ADC2_INP18 30 PA5 I/O DAC1_OUT2, ADC1_INP19, SSB-Q ADC2_INP19 31 PA6 I/O ADC1_INP3 SWR-SENSE 33 PC4 I/O ADC1_INP4 PRE-POWER-SENSE 36 PB1 I/O ADC1_INP5 PA-POWER-SENSE 48 VCAP Power 49 VSS Power 50 VDD Power 52 PB13 I/O UCPD1_CC1 53 PB14 I/O UCPD1_CC2 54 PB15 I/O PWR_PVD_IN 70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	28	VDD	Power		
ADC2_INP19	29	PA4	I/O		SSB-I
33	30	PA5	I/O		SSB-Q
36 PB1 I/O ADC1_INP5 PA-POWER-SENSE 48 VCAP Power 49 VSS Power 50 VDD Power 52 PB13 I/O UCPD1_CC1 53 PB14 I/O UCPD1_CC2 54 PB15 I/O PWR_PVD_IN 70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	31	PA6	I/O	ADC1_INP3	SWR-SENSE
48 VCAP Power 49 VSS Power 50 VDD Power 52 PB13 I/O UCPD1_CC1 53 PB14 I/O UCPD1_CC2 54 PB15 I/O PWR_PVD_IN 70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	33	PC4	I/O	ADC1_INP4	PRE-POWER-SENSE
49 VSS Power 50 VDD Power 52 PB13 I/O UCPD1_CC1 53 PB14 I/O UCPD1_CC2 54 PB15 I/O PWR_PVD_IN 70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	36	PB1	I/O	ADC1_INP5	PA-POWER-SENSE
50 VDD Power 52 PB13 I/O UCPD1_CC1 53 PB14 I/O UCPD1_CC2 54 PB15 I/O PWR_PVD_IN 70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	48	VCAP	Power		
52 PB13 I/O UCPD1_CC1 53 PB14 I/O UCPD1_CC2 54 PB15 I/O PWR_PVD_IN 70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	49	VSS	Power		
53 PB14 I/O UCPD1_CC2 54 PB15 I/O PWR_PVD_IN 70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	50	VDD	Power		
54 PB15 I/O PWR_PVD_IN 70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	52	PB13	I/O	UCPD1_CC1	
70 PA11 I/O USB_DM 71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	53	PB14	I/O	UCPD1_CC2	
71 PA12 I/O USB_DP 72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	54	PB15	I/O	PWR_PVD_IN	
72 PA13(JTMS/SWDIO) I/O DEBUG_JTMS-SWDIO 73 VDDUSB Power 74 VSS Power 75 VDD Power	70	PA11	I/O	USB_DM	
73 VDDUSB Power 74 VSS Power 75 VDD Power	71	PA12	I/O	USB_DP	
74 VSS Power 75 VDD Power	72	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
74 VSS Power 75 VDD Power	73	·	Power		
75 VDD Power			Power		
	75				
				DEBUG_JTCK-SWCLK	
92 PB6 I/O I2C1_SCL					
93 PB7 I/O I2C1_SDA					
94 BOOTO Boot					
98 VCAP Power					
99 VSS Power					

	Pin Number	Pin Name	Pin Type	Alternate	Label
ı	LQFP100	(function after		Function(s)	
ı		reset)			
	100	VDD	Power		

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H5
Line	STM32H562
мси	STM32H562VITx
Datasheet	DS00000_Rev0

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

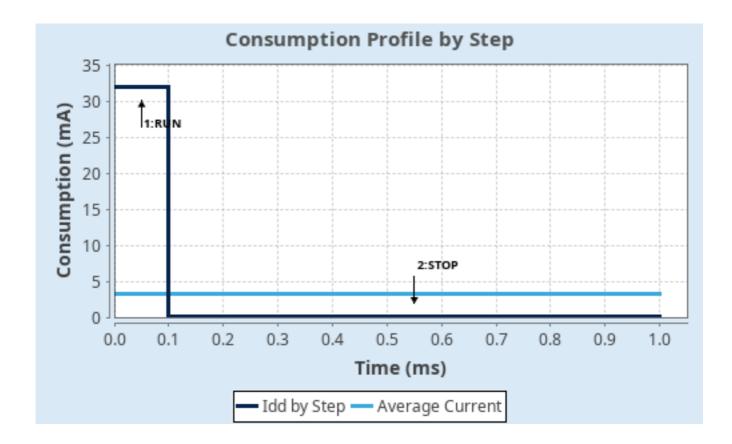
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-
		Scale5/SMPS
Fetch Type	FLASH_ON/Cache2Ways_A	Flash-
	LL_RAM_RETENTION	PwrDwn_PwrDwnStop_OFF
CPU Frequency	250 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	32 mA	51.5 μA
Duration	0.1 ms	0.9 ms
DMIPS	535.0	0.0
Ta Max	120.68	124.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	3.25 mA
Battery Life	1 month, 13 days,	Average DMIPS	535.0 DMIPS
	4 hours		

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	usb-ssb-exciter
Project Folder	/home/alan/softshack/usb-ssb-exciter
Toolchain / IDE	CMake
Firmware Package Name and Version	STM32Cube FW_H5 V1.5.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_ADC2_Init	ADC2
5	MX_CORDIC_Init	CORDIC
6	MX_DAC1_Init	DAC1
7	MX_DTS_Init	DTS
8	MX_FLASH_Init	FLASH
9	MX_FMAC_Init	FMAC
10	MX_I2C1_Init	I2C1
11	MX_UCPD1_Init	UCPD1

Rank	Function Name	Peripheral Instance Name
12	MX_USB_PCD_Init	USB
13	MX_GTZC_Init	GTZC

3. Peripherals and Middlewares Configuration

3.1. ADC1

IN1: IN1 Single-ended IN3: IN3 Single-ended IN4: IN4 Single-ended IN5: IN5 Single-ended

mode: IN19

3.1.1. Parameter Settings:

ADCs Common Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Scan Conversion Mode Disabled

Data Alignment Right alignment

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Conversion Data Management Mode Regular Conversion data stored in DR register only

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Sampling Mode Normal
Rank 1

Channel 19 *

Sampling Time 2.5 Cycles
Offset Number No offset
Monitored by None

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

3.2. ADC2

mode: IN19

3.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Scan Conversion Mode Disabled

Data Alignment Right alignment

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Conversion Data Management Mode Regular Conversion data stored in DR register only

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Sampling Mode Normal
Rank 1

ChannelChannel 19Sampling Time2.5 CyclesOffset NumberNo offsetMonitored byNone

 $ADC_Injected_ConversionMode:$

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

3.3. BOOTPATH

mode: Activated

3.4. CORDIC

mode: Activated

3.5. CORTEX_M33_NS

SysTick Source Selection: HCLK

3.5.1. Parameter Settings:

Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled

during hard fault, NMI and FAULTMASK handlers *

Cortex Memory Protection Unit Region 0 Settings:

Region Enabled *

Region Base Address

0x08000000 *

Region Limit Address

0x081FFFF *

Attributes Number

ATTRIBUTE 0

Access Permission READS Permissions *

Instruction Access Enable
Shareability Permission Disable

Cortex Memory Protection Unit Region 1 Settings:

Region Enabled *

Region Base Address 0x20000000 *
Region Limit Address 0x2009FFFF *

Attributes Number ATTRIBUTE 1 *

Access Permission READS\WRITES Permissions

Instruction Access Enable
Shareability Permission Disable

Cortex Memory Protection Unit Region 2 Settings:

Region Disabled

Cortex Memory Protection Unit Region 3 Settings:

Region Disabled

Cortex Memory Protection Unit Region 4 Settings:

Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

Region Disable

Cortex Memory Protection Unit Region 6 Settings:

Region Disable

Cortex Memory Protection Unit Region 7 Settings:

Region Disabled

3.5.2. Attributes Settings:

Cortex Memory Protection Unit Attributes 0 Settings:

Attributes Enabled *

Memory type Normal cacheable *

Cache policy WRITE THROUGH

Transient permission TRANSIENT

Allocate permission R ALLOCATE *

Cortex Memory Protection Unit Attributes 1 Settings:

Attributes Enabled *

Memory type Normal cacheable *

Cache policy WRITE BACK *

Transient permission TRANSIENT

Allocate permission RW ALLOCATE *

Cortex Memory Protection Unit Attributes 2 Settings:

Attributes Disabled

Cortex Memory Protection Unit Attributes 3 Settings:

Attributes Disabled

Cortex Memory Protection Unit Attributes 4 Settings:

Attributes Disabled

Cortex Memory Protection Unit Attributes 5 Settings:

Attributes Disabled

Cortex Memory Protection Unit Attributes 6 Settings:

Attributes Disabled

Cortex Memory Protection Unit Attributes 7 Settings:

Attributes Disabled

3.6. DAC1

OUT1 connected to: only external pin OUT2 connected to: only external pin

3.6.1. Parameter Settings:

Common DAC Settings:

DAC High Frequency Mode Disable

DAC Out1 Settings:

Mode selectedNormal ModeOutput BufferEnableDMA double data modeDisableSigned FormatDisableTriggerNone

User Trimming Factory trimming

DAC Out2 Settings:

Mode selectedNormal ModeOutput BufferEnableDMA double data modeDisableSigned FormatDisableTriggerNone

User Trimming Factory trimming

3.7. DEBUG

Debug: Serial Wire

3.8. DTS

mode: Activated

3.8.1. Parameter Settings:

Basic parameters:

Reference Clock Selection High speed reference clock (PCLK)

Quick Measurement Disable the Quick Measurement (Measure with calibration)

Input Trigger Selection

No Hardware trigger detection

Sampling Time

1 cycle for the sampling time

Divider 0

High Threshold 0x0 *

Low Threshold 0x0 *

3.9. FLASH

mode: Enable

3.9.1. HAL Option Bytes Settings:

Advanced settings:

Activate false

Product State:

Activate false

BOR Level:

Activate false

User Configuration:

Activate false

User Configuration 2:

Activate false

Boot Configuration:

Activate NS BOOT LOCK false

Write sector group Protection:

Activate Bank 1 WRP false
Activate Bank 2 WRP false

OTP write protection:

Activate false

Flash data sectors:

Activate Bank1 EDATA false
Activate Bank2 EDATA false

Flash HDP:

Activate Bank1 HDP false
Activate Bank2 HDP false

3.9.2. Block-based sector protection:

AREA1:

Activate AREA 1 true *

Bank FLASH BANK 1

Start page 0

End page 127 *

Attribute privilege Privileged
Attribute security Not secure

AREA2:

Activate AREA 2 true *

Bank FLASH BANK 2 *

Start page 0
End page 127 *
Attribute privilege Privileged
Attribute security Not secure

AREA3:

Activate AREA 3 false

AREA4:

Activate AREA 4 false

AREA5:

Activate AREA 5 false

AREA6:

Activate AREA 6 false

AREA7:

Activate AREA 7 false

AREA8:

Activate AREA 8 false

3.10. FMAC mode: Mode

3.11. GTZC

mode: Enable

3.11.1. TrustZone Security Controller - Privilegeable Peripherals:

Privilegeable Peripherals:

Configure Privilege IP by Individual Privileging from full Not Privileged

Privilegeable Peripheral Privilege Attribute

ADC1|2 not privileged

CORDIC not privileged

CRC not privileged

CRS not privileged

DAC1 not privileged

not privileged

not privileged

not privileged

not privileged

DCMI not privileged DTS not privileged FDCAN1 not privileged not privileged **FMAC FMC** not privileged HASH not privileged HDMI_CEC not privileged 12C1 not privileged 12C2 not privileged I2C3 not privileged I2C4 not privileged I3C1 not privileged **ICACHE** not privileged **IWDG** not privileged LPTIM1 not privileged LPTIM2 not privileged LPTIM3 not privileged LPTIM4 not privileged LPTIM5 not privileged LPTIM6 not privileged LPUART1 not privileged OCTOSPI1 not privileged PKA not privileged RAMCFG not privileged RNG not privileged SAI1 not privileged SAI2 not privileged not privileged SDMMC1 SPI1 not privileged SPI2 not privileged SPI3 not privileged SPI4 not privileged SPI6 not privileged TIM1 not privileged TIM2 not privileged TIM3 not privileged TIM4 not privileged TIM5 not privileged TIM6 not privileged TIM7 not privileged TIM8 not privileged TIM12 not privileged TIM13 not privileged

TIM14 not privileged TIM15 not privileged TIM16 not privileged TIM17 not privileged USART1 not privileged USART2 not privileged USART3 not privileged UART4 not privileged UART5 not privileged **USART6** not privileged UART7 not privileged **UART8** not privileged UART9 not privileged USART10 not privileged USART11 not privileged UART12 not privileged UCPD1 not privileged USB not privileged **VREFBUF** not privileged WWDG not privileged

3.11.2. Block-Based Memory Protection Controller:

MPCBB1 (SRAM1):

Memory Privilege Attributes Settings

Configure Memory from full Not Privileged

Area Start Offset 0x0 *

Area Size 0x00040000 *

Area 2 Start Offset

Ox0 *

Area 2 Size

Ox0 *

Area Attribute

privileged

MPCBB2 (SRAM2):

Memory Privilege Attributes Settings

Configure Memory from full Not Privileged

Area Start Offset 0x0 *

Area Size 0x00010000 *

Area 2 Start Offset

Area 2 Size

Ox0 *

Area Attribute

privileged

MPCBB3 (SRAM3):

Memory Privilege Attributes Settings

Configure Memory from full Not Privileged

Area Start Offset 0x0 *

Area Size 0x00050000 *

Area 2 Start offset

Ox0 *

Area 2 Size

Ox0 *

Area Attribute

privileged

3.12. I2C1 I2C: I2C

3.12.1. Parameter Settings:

Timing configuration:

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz)100Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Analog Filter Enabled

Timing **0x00707CBB** *

Slave Features:

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

3.13. MEMORYMAP

mode: Activated

3.14. PWR

mode: Analog voltage detector

Power Voltage Detector In: Power Voltage Detector In (External input analog voltage)

mode: Power saving mode mode: Privilege attributes

3.14.1. Parameter Settings:

Programmable_Voltage_Detector_Settings:

AVD detection Level PWR AVD LEVEL 0 (1.7 V)

PWR AVD Mode basic mode is used PWR PVD Mode basic mode is used

3.14.2. PWR Privilege:

Privilege PWR:

PWR Privilege Disable

3.15. RCC

3.15.1. RCC Privilege:

Privilege RCC:

Privilege of RCC Non-Secure Items Disable

3.15.2. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 1 WS (2 CPU cycle)

Flash Programming Delay 0

RCC Parameters:

HSI Calibration Value 64
CSI Calibration Value 32
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
TIM Prescaler Selection Disabled

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 3

3.16. SYS

Timebase Source: SysTick

3.17. UCPD1

UCPD Mode: Sink

3.17.1. Parameter Settings:

Version 1.0

3.18. USB

Mode: Device_Only

3.18.1. Parameter Settings:

Basic Parameters:

Speed Full Speed 12MBit/s

Physical interface Internal Phy
Signal start of frame Disabled

Power Parameters:

Low PowerDisabledLink Power ManagementDisabledBattery ChargingDisabled

EndPoint Parameters:

Bulk double buffer Disabled lso single buffer Disabled

3.19. VREFBUF

VREFBUF Mode: Internal voltage reference

3.19.1. Parameter Settings:

Voltage_Reference_Buffer_Settings:

Trimming Mode Factory Trimming
Internal Voltage reference scale SCALE 0: around 2.5 V

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_INP1	Analog mode	No pull-up and no pull-down	n/a	V12-SENSE
	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	SSB-I
	PA5	ADC1_INP19	Analog mode	No pull-up and no pull-down	n/a	SSB-Q
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	SWR-SENSE
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	PRE-POWER-SENSE
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	PA-POWER-SENSE
ADC2	PA4	ADC2_INP18	Analog mode	No pull-up and no pull-down	n/a	SSB-I
	PA5	ADC2_INP19	Analog mode	No pull-up and no pull-down	n/a	SSB-Q
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	SSB-I
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	SSB-Q
DEBUG	PA13(JTMS/ SWDIO)	DEBUG_JTMS- SWDIO	n/a	n/a	n/a	
	PA14(JTCK/ SWCLK)	DEBUG_JTCK- SWCLK	n/a	n/a	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
PWR	PB15	PWR_PVD_IN	Analog mode	No pull-up and no pull-down	n/a	
UCPD1	PB13	UCPD1_CC1	Analog mode	No pull-up and no pull-down	n/a	
	PB14	UCPD1_CC2	Analog mode	No pull-up and no pull-down	n/a	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	

4.2. GPDMA1

4.3. GPDMA2

4.4. LINKEDLIST

4.5. NVIC configuration

4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
PVD/AVD through EXTI Line detection Interrupt	unused			
Flash non-secure global interrupt	unused			
RCC non-secure global interrupt	unused			
ADC1 global interrupt	unused			
DAC1 interrupt	unused			
I2C1 Event interrupt	unused			
I2C1 Error interrupt	unused			
ADC2 global interrupt	unused			
USB FS global interrupt	unused			
UCPD1 global interrupt	unused			
FPU global interrupt	unused			
CORDIC global interrupt	unused			
FMAC global interrupt	unused			
DTS global interrupt		unused		

4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
Non modicable interrupt	false		false
Non maskable interrupt	laise	true	raise
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

usb-ssb-exciter	Project
Configuration	Report

* User modified value

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32h5-bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32h5-ibis.zip

System View https://www.st.com/resource/en/svd/stm32h5-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_eval-

tools_portfolio.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_software_development_tools.pdf

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers-

stm32h5-series-overview.pdf

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers-

stm32-family-overview.pdf

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers-

stm32-entry-level-graphics.pdf

Brochures https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-

and-smart-i-os.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32nucleo.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32h5.pdf

Security Bulletin https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-

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